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TRANSIENT SPECTROSCOPY OF II-VI SEMICONDUCTORS

by

M. Claybourn

Presented in cadidature for the degree of

Doctor of Philosophy

in the

University of Durham

September 1985

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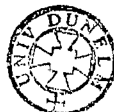

15. APR. 1986

for Ailsa

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Acknowledgements

I would like to thank my supervisors Dr.J.Woods and Dr.A.W.Brinkman for their patience and assistance during my research at Durham. I also owe a debt of gratitude to Norman Thompson, Trevor Harcourt and the technicians under the beady eye of Mr.F.Spence. Without their help and expertise, this thesis would not have been possible.

I am grateful to Dr.G.J.Russell for the use of his electron microscope and ...., and to Dr.J.E.Hails for proof reading this thesis thoroughly and setting it to rights.

Greatest thanks are owed to my parents and Ailsa for their encouragement throughout my 3 years at Durham.

Abstract

DLTS, ODLTS and DLOS have been used to characterise the main deep level trapping centres in some II-VI semiconductors; these were single crystal CdS, (ZnCd)S, CdSe, CdTe and ZnS, and polycrystalline CdS films.

Undoped, single crystal CdS contained four electron traps as detected by DLTS, at 0.29eV, 0.41eV, 0.61eV and 0.74eV below the conduction band (CB). The first two were observed in all samples and were due to native defects. The two states of highest energy were found only in material that had been annealed in S or Cd vapours. The 0.61eV level could be photoinduced by illumination at photon energies greater than about 1eV. It decayed in the dark with an activation energy of 0.25eV. The 0.61eV and 0.74eV centres were associated with electrically active extended defects (subgrain boundaries). Such samples had dislocation densities of about 10^{10} cm^{-2}.

Copper was found to be a residual impurity in CdS. It produced two deep hole traps resulting from a crystal field splitting of the Cu d^9 state. They were detected by ODLTS and DLOS and were found at 0.35eV and 1.1eV above the valence band (VB).

Introduction of the isoelectronic impurity tellurium into CdS induced a hole repulsive centre at 0.21eV above the VB. This is thought to be an important radiative recombination centre.

The main electron trap in CdS at 0.41eV was found to shift to higher energy with incorporation of Zn. Replacement of 20% of the Cd with Zn shifted the energy to 0.63eV. The level appeared fixed to the VB and had a similar functional dependence on composition as the band gap.

The activation energies of the copper centres observed in CdS remained unchanged with incorporation of Zn up to the composition $Zn_{0.45}Cd_{0.55}S$. This showed that the crystal field splitting was constant and that these levels were also pinned to the VB.

During the fabrication process of the (ZnCd)S/Cu_2S solar cell, a deep level was induced at about 1.2eV below the CB. This is thought to be a recombination centre and one of the contributory factors to the reduction observed in the current collection efficiency of these devices.

Polycrystalline CdS films were prepared by silk screen printing (SP) and evaporation. The SP films were annealed at various times and temperatures to improve the crystallinity of the layers. At 640C for 1hr, deep states at 0.16eV and 0.48eV were detected, The levels disappeared when annealed at 670C-700C and a new level was observed at 0.13eV. CdS/Cu_2S heterojunctions were prepared on the material sintered at 670C; this induced a further trapping level at 1.1eV and one that was poorly resolved. Copper diffused into the CdS during the fabrication of the device so the states associated with copper were detected at 0.35eV and 1.1eV.

The evaporated CdS layers showed that the defect signature was sensitive to the type of substrate. Using Ag instead of the usual SnO_x, deep states were induced at 0.48eV and 0.98eV below the CB. These Ag-associated impurity centres prevent the indiffusion of Cu during the optimising heat treatment of the CdS/Cu_2S heterojunction. This maintains the stoichiometry of the Cu_2S layer, thereby, preventing degradation of the devices.

CdSe and copper doped CdSe were found to contain several important defect centres: a native sensitising centre (0.64eV from the

VB), a class I recombination centre (0.9eV from the CB), a copper impurity centre (0.2eV from the VB) and two native defects (0.16eV and 0.45eV from the CB).

n-type CdTe grown by the Piper-Polich technique contained 6 electron traps at 0.15eV, 0.21eV, 0.40eV, 0.47eV, 0.53eV and 0.63eV. Their presence was shown to be dependent upon the method of growth of the crystal by comparing with material grown by other techniques. One or more of these states were thought to be due to extended defects or Te precipitates.

Low resistivity ZnS contained two deep electron traps at 0.25eV and 0.50eV as detected by DLTS. In addition DLOS showed the presence of four further states at 1.25eV, 1.37eV, 1.89eV and 2.19eV below the CB. The first two are thought to be the strong luminescence centres observed by other workers.

CHAPTER 1

INTRODUCTION TO II-VI SEMICONDUCTORS

1.1 Introduction

The II-VI semiconductors have received much attention over the past three or more decades since their earliest use as phosphors in CRT screens [1]. The diversity of the potential applications is reflected in the large number of publications on the properties of these compounds. However, there are many remaining unsolved problems. One of the most important of these, especially with respect to the application of this group of materials to electronic devices, is the control of crystalline imperfections. These may produce electronic states in the semiconductor which can affect its electronic and optical properties [2,3]. This thesis is concerned with the electronic states in some II-VI compounds that result from such crystal defects. Some of the general properties and applications of II-VI semiconductors and the aims of the project are summarised in this chapter.

1.2 Properties of II-VI Materials

II-VI semiconductors are composed of equal atomic proportions of a group IIb element (Zn, Cd, Hg) and a group VIb element (O, S, Se, Te). They all crystallise with the zinc blende (fcc) or wurzite (hexagonal) structure with the

exception of CdO which has the halite structure and will not be considered here. For both zinc blende and wurzite the metal atom is surrounded tetrahedrally by 4 chalcogen atoms and vice versa.

The zinc blende structure is similar to that of diamond. It is composed of two interpenetrating face-centred cubic lattices which are displaced from one another by 1/4 of the body diagonal of the unit cell (see fig. 1.1). The nearest neighbour distance is $\sqrt{3}/4a_o$, where a_o is the lattice parameter. The wurzite structure (see fig. 1.2) consists of two interpenetrating hexagonal lattices displaced by $3c_o/8$ along the c-axis (c_o is the unit cell lattice parameter along the c-axis). Fig. 1.3 summarises the crystallographic data on II-VI materials.

One of the important properties of these compounds is that they all have direct band gaps which means that they have a high radiative recombination efficiency. This has proved useful in device applications such as LED's and they compare favourably with other well established semiconductor technologies based on the elemental and III-V semiconductors. Some of the important optical and electrical properties of these materials are summarised in fig. 1.4.

One of the main problems with II-VI compounds is that they can either be made only n-type or p-type with the exception of CdTe. Consider ZnTe which is p-type. If impurities are added such as Al that create shallow donor states, the material compensates by creating shallow acceptor states so

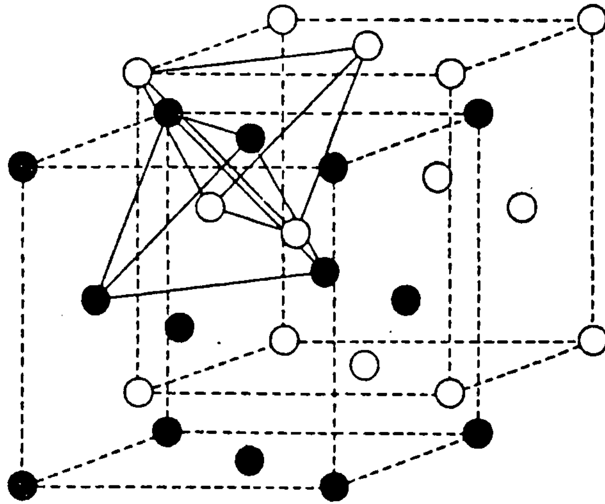

Figure 1.1 The zinc blende structure

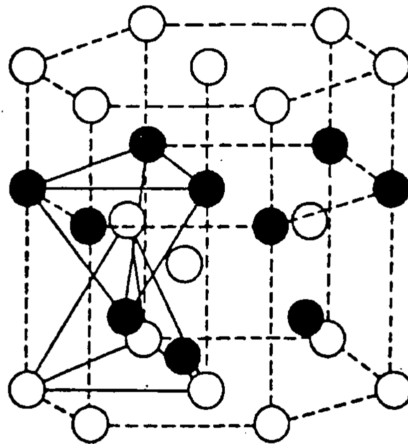

Figure 1.2 The wurzite structure

Compound	Stable structure (metastable)	Lattice constant (Å)	c_0/a_0	$d(M\text{-}X)$ (Å)	$d(M\text{-}M)$ (Å)	Ionicity f_i
CdO	Halite	$a_0 = 4.71$	–	2.305	4.71	0.785
CdS	Wurtzite	$a_0 = 4.1368$	1.624	2.53	4.1368	0.685
		$c_0 = 6.7163$				
	(Zincblende)	$a_0 = 5.8378$	–			
CdSe	Wurtzite	$a_0 = 4.298$	1.631	2.64	4.30	0.699
		$c_0 = 7.01$				
	(Zincblende)	$a_0 = 6.084$	–			
CdTe	Zincblende	$a_0 = 6.481$	–	2.80	4.58	0.717
	(Wurtzite)	$a_0 = 4.57$	1.635			
		$c_0 = 7.57$				
ZnO	Wurtzite	$a_0 = 3.25$	1.602	1.997	3.25	0.616
		$c_0 = 5.207$				
ZnS	Zincblende	$a_0 = 5.409$	–	2.34	3.82	0.623
	Wurtzite	$a_0 = 3.819$	1.638			
		$c_0 = 6.256$				
ZnSe	Zincblende	$a_0 = 5.669$	–	2.45	4.01	0.630
	(Wurtzite)	$a_0 = 4.01$	1.627			
		$c_0 = 6.54$				
ZnTe	Zincblende	$a_0 = 6.104$	–	2.64	4.32	0.609
	(Wurtzite)	$a_0 = 4.27$	1.579			
		$c_0 = 6.99$				

Figure 1.3 Crystallographic properties of the II-VI compounds

MATERIAL	E_g (eV)		dE_g/dT	DIELECTRIC CONSTANT		EFFECTIVE MASS (m_0)		ELECTRON AFFINITY	MOBILITY (cm^2/Vs)	
	4K	300K	(10^{-4} eV/K)	ε_s	ε_∞	m_e^*	m_h^*		e	h
CdS (W)	2.58	2.42	-5.2	8.6	5.26	0.17	0.7	4.5	350	10
CdSe (W)	1.84	1.73	-4.6	9.4	6.2	0.13	0.45	4.58	650	7.3
CdTe (ZB)	1.60	1.58	-2.3	10.9	7.2	0.1		4.28	1100	80
ZnS (W)	3.91	3.68	-8.5	8.6	5.2	0.21	0.51	3.9	140	5
ZnSe (ZB)	2.83	2.67	-4.6	8.1	6.0	0.13	0.7	4.09	530	28
ZnTe (ZB)	2.39	2.25	-5.0	9.3	6.9	0.17	1.0	3.53	73	100

Figure 1.4 Some of the electrical and optical properties of the II-VI compounds [1, 4, 5]

that n-type conductivity is never achieved [6]. This means that only CdTe p-n homojunctions can be fabricated and so to overcome this problem heterojunctions have been used. Care must be taken in devising a junction between two materials so that they are reasonably lattice matched to minimise strain at the junction, and have matched electron affinities to minimise band discontinuities. Examples of such II-VI heterojunctions are nCdS/pCdTe [7] and nZnSe/pZnTe [8]. Poor lattice and electron affinity matching may be improved by using ternary II-VI compounds such as $Zn_xCd_{1-x}S$, $CdSe_yS_{1-y}$, ZnS_yTe_{1-y}, etc whose compositions can be varied so that the lattice parameter and band gap can be tailor made to suit the requirements for matching. Most of the II-VI ternary compounds have been characterised. They exhibit band gaps which vary monotonically with composition with the exception of CdS_yTe_{1-y} and ZnS_yTe_{1-y}. These two compounds have a band gap minimum at a composition between that of the two binaries that constitute each of the ternaries. The degree of bowing for the band gap/composition relation is characterised by a bowing parameter which is specific to a particular ternary [1,9,10]. The band gap E(x) of the ternary A_xB_{1-x}, where A and B are the two binary compounds with one common element constituting the ternary, can be defined by:

$$E(x) = E(B) + [E(A)-E(B)-b]x + bx^2 \qquad 1.1$$

where E(A) and E(B) are the band gaps of A and B respectively, x is the composition of the ternary and b is the bowing parameter. The band gap range and bowing parameters for the wide band gap II-VI ternaries are given in

fig. 1.5.

1.3 Applications of II-VI Semiconductors

As a result of their optical properties the II-VI semiconductors have received much academic as well as commercial interest. The main applications are summarised in fig. 1.6. To discuss all of these is beyond the scope of this work so only a brief mention is given of those that are important here.

Fahrenbruch [11] has reviewed the uses of II-VI compounds in solar energy conversion. The principal advantages of these materials are low cost, direct band gap and ease of deposition of good quality films by a variety of methods. Typical deposition techniques are silk screen printing [12], evaporation [13], electrophoresis [14] and spray pyrolysis [15]. As already mentioned, suitable p-n homojunctions cannot be fabricated, therefore, emphasis has been placed on such heterojunction systems as CdS/Cu_2S, CdS/CdTe, $Zn_xCd_{1-x}S/Cu_2S$ etc. These have maximum reported operational efficiences of 9.1% [16], 12% [17], and 10.2% [18] respectively.

An important property of many of the II-VI compounds is that by doping with impurities, luminescence centres can be created. As such they can give unique properties to the material. Examples of these are manganese doped ZnS which is potentially useful as a blue LED [19] and $ZnS:TbF_3$ as an electroluminecent device [20]. Many others have been

TERNARY COMPOUND	BOWING PARAMETER	BAND GAP RANGE (eV)
$(ZnS)_x(CdS)_{1-x}$	0.61	2.42-3.66
$(ZnSe)_x(CdSe)_{1-x}$	0.75	1.73-2.67
$(ZnTe)_x(CdTe)_{1-x}$	0.20	1.58-2.25
$(ZnS)_x(ZnSe)_{1-x}$	0.41	2.67-3.66
$(ZnS)_x(ZnTe)_{1-x}$	3.00	2.25-3.66
$(ZnSe)_x(ZnTe)_{1-x}$	1.27	2.25-2.67
$(CdS)_x(CdSe)_{1-x}$	0.31	1.73-2.42
$(CdS)_x(CdTe)_{1-x}$	1.70	1.58-2.42
$(CdSe)_x(CdTe)_{1-x}$	0.85	1.58-1.73

Figure 1.5 Bowing parameter and band gap range for the wide gap II-VI compounds

Type of application	Homogeneous area wanted	Crystallographic properties wanted	Electrical properties wanted	Optical properties wanted	Suitable materials	Preparation methods
Photoresistors, photoconductive detectors	< 10 cm^2	Single crystalline layers or polycrystalline layers with as few grain boundaries as possible	Highly compensated material, high dark resistivity, high majority carrier $\mu\tau$ product	None special	CdS, CdSe, CdS_xSe_{1-x} ($Zn_xCd_{1-x}S$)	Vacuum evaporation, cathodic sputtering; spray deposition; sintering
Photovoltaic detectors	< 1 cm^2	Highly perfect single crystalline layers, layer thickness larger than average penetration depth of light	Low resistivity	Good optical transparency	p–n heterojunctions (e.g. p-InP/n-CdS, p-$CuInSe_2$/n-CdS, p-Si/n-CdS, p-GaAs/n-ZnSe, p-Si/n-ZnSe, n-CdSe/p-ZnTe, n-Si/p-ZnTe etc.)	Vacuum evaporation; vapour phase epitaxy VPE (sublimation, CVT, CSVT, CVD)
Absorber material for solar cells	10–100 cm^2	Thin polycrystalline layers usable (grain dimensions > 1 μm)	Low resistivity, doping level controllable, minority carrier diffusion length as large as possible	Energy gap between 1.0 and 1.7 eV	CdTe	Vacuum evaporation; VPE (CVT, CSVT, CVD); sintering
Window material for solar cells	10–100 cm^2	Thin polycrystalline layers usable, lattice constant and thermal expansion coefficient comparable with the absorber material	Resistivity as low as possible	Energy gap as large as possible, good optical transparency	CdS, $Zn_xCd_{1-x}S$	Vacuum evaporation, cathodic sputtering; VPE (CVT, CSVT, CVD); spray pyrolysis
Light emitting diodes	≤ 1 cm^2	Monocrystals or single crystalline layers	Low resistivity n- and/or p-type	Efficient room-temperature luminescence in the visible	ZnS, ZnSe, ZnS_xSe_{1-x}, ZnTe	All growth methods which provide single crystalline samples
ac, dc electroluminescent thin film displays	≥ 10 cm^2 ≤ 200 cm^2	Active layer: poly- or single crystalline layers	High resistivity	High concentration of luminescent centres, inner shell transition favoured	ZnS, ZnSe, ZnS_xSe_{1-x}	Vacuum evaporation, sputtering; VPE including atomic layer epitaxy (ALE)
ac, dc electroluminescent powder displays	≤ 100 cm^2	Active layer: ZnS powder-surface treated with Cu_xS	High resistivity	High concentration of luminescent centres	ZnS, $Zn_xCd_{1-x}S$	Settling processes
Nonlinear optical devices						
(1) Optical waveguides and modulators	≈ 1 cm^2	Highly perfect, pure single crystalline layers	High resistivity	Good optical transparency, low optical propagation loss	1. ZnO, ZnS	(1) Cathodic sputtering, vacuum evaporation; VPE (sublimation, CVT)
(2) Bulk-modulators and switches	> 1 cm^2	Highly perfect, pure single crystals	High resistivity	Good optical transparency, low optical propagation loss	2. ZnS, CdS, CdTe	(2) Melt growth; vapour growth (sublimation and chemical transport in closed and open systems)
Laser window material	> 1 cm^2	Highly perfect, pure single crystalls	None special	Good optical transparency, especially in the infrared	ZnSe, CdTe	Melt growth, vapour growth (seed methods)
Television						
(1) Cathode ray tube screens, 400–5000 cm^2		Luminescence grade grain sized powder		High concentration of luminescent centres	(1) ZnS, $Zn_xCd_{1-x}S$	(1) Settling processes
(2) Projection colour television		High perfect, pure single crystals	None special	Plane parallel high quality faces	(2) ZnS, ZnSe, ZnS_xSe_{1-x}	(2) Melt growth, vapour growth (seed methods)

Figure 1.8 Summary of the important uses of the II–VI compounds

characterised and are reviewed by Hartmann et al [1].

Most of the applications of II-VI semiconductors have not reached their full potential due, in the main, to the difficulty in the control of defects in the material. These defects can behave, for example, as recombination centres and thereby reduce the carrier lifetimes [2,3]. In the case of solar cells this would cause a reduction in the device efficiency.

1.4 Scope of the Present Study

Deep level defect states are known to affect the operation of a device [2]. This study is concerned with the investigation of electrically and optically active defect states in II-VI semiconductors. The principal techniques used were deep level transient spectroscopy (DLTS) [21], optical DLTS (ODLTS) [22] and deep level optical spectroscopy (DLOS) [23]. These are transient capacitance methods that for DLTS and ODLTS enable the activation energy, capture cross-section and density of a particular deep state to be determined; and for DLOS the spectral distribution of the capture cross-section for a defect state.

The theory of defect states in general, and with respect to the II-VI compounds in particular, is discussed in the next chapter. The subsequent chapter is concerned with the theory of the techniques mentioned and how they are applied. In Chapter 4 a discussion is given of the experimental side of this work - crystal growth, basic structural assessment

techniques, the design and operation of the DLTS system and how this was adapted to meet the operating needs of other experiments including ODLTS and DLOS.

The initial study was to characterise the main electron and hole trapping centres in single crystal CdS. The first part concerned the undoped material and the effect of various annealing treatments on the defects present. This is important since defect states are created according to the thermodynamic conditions. The next part involved doping of the CdS with Cu or Te and to monitor any changes that these impurities had on the defect signature. In the case of the CdS/Cu_2S solar cell, the device has to undergo an optimising heat treatment; this is known to cause copper migration from the Cu_2S into the CdS [24]. This has two important effects, firstly, it causes changes in the stoichiometry of the Cu_2S absorber layer and results in degradation of the device, and secondly, it creates trapping levels in CdS which can result in a lower current collection efficiency [24]. In the case of Te, the impurity behaves as an efficient radiative recombination centre in CdS [25] so it was interesting to deduce the position of these states in the band gap and, therefore, with which band edge they communicate to produce the luminescence.

CdS was used as a basis for the study of deep level defect states in the ternary system $Zn_xCd_{1-x}S$ and in polycrystalline CdS. The ternary crystal was investigated with two aims - firstly to study the effect of a composition change on deep levels seen in CdS and secondly to provide an

explanation for the reduction in short circuit current in the $Zn_xCd_{1-x}S/Cu_2S$ heterojunction compared to the CdS/Cu_2S heterojunction. The mixed crystal of composition $Zn_{0.2}Cd_{0.8}S$ has a better lattice and electron affinity match to Cu_2S than does CdS which should improve the current collection efficiency [26]; however, a poorer efficiency has been observed for both evaporated and single crystal CdS [eg 27]. So, the study was looking for any defect level that may contribute to the reduced current collection by behaving, for example, as a recombination centre.

One of the important properties of CdS is that it can be prepared relatively cheaply in the form of films. Therefore, for any device application it may be necessary to characterise any deep levels in the material that may worsen or improve its properties. To this end, polycrystalline CdS, prepared by vacuum evaporation and by silk screen printing, was studied. Schottky barrier and heterojunction devices on these materials were investigated in an effort to study the effect of annealing treaments on the defects present in silk screen printed films; and the effect of the type of substrate on the defect signature for evaporated layers of CdS.

The final chapter is concerned with some other II-VI materials that have received interest in relation to their potential application. These were nCdTe as substrate material for infrared detectors; low resistivity ZnS which gives rise to an efficient blue luminescence centre; and undoped and copper doped CdSe with reference to the native and copper states in the $CdSe/Cu_2Se$ heterojunction.

DLTS, ODLTS and DLOS proved useful techniques in this study, providing the basic properties of the dominant defect states in the semiconductors. The single drawback of these techniques for the study of deep defect states is that they are unable to directly identify the origin of these centres.

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CHAPTER 2

DEEP LEVELS IN II-VI SEMICONDUCTORS

2.1 Introduction

The study of defect levels in II-VI semiconductors using space charge techniques was the aim of this work. The techniques used are discussed in the next chapter; here the main concern is with the nature of defect states in the energy gap.

The suitability of semiconductor materials for device applications depends very much on crystal perfection and its control. In general, imperfections appear to be a major limiting factor with respect to device performance and reliability [1] and so they have become an important area of study. When a defect state is introduced into the band gap of a semiconductor it can behave in many ways, for example as an electron or hole trap, recombination centre, luminescent centre etc. Indeed, it is well known that deep level defects can affect the electrical and optical properties of a material. Some of the basic theory and work relevant to II-VI materials is reviewed in this chapter.

2.2 Defect States in Semiconductors

Defect levels are localised electronic states in the solid due to a variety of causes but all leading to a loss of translational symmetry of the crystal lattice. Examples of these are substitutional or interstitial impurities, native defects, dislocations, or termination of the lattice at the surface. Weakly bound (shallow) defect states can be predicted using a simple hydrogenic model [2] and applying the Schrödinger equation :

$$H \psi = E \psi \qquad 2.1$$

where H = H(0) + V, H(0) is the perfect crystal Hamiltonian, V is the effective impurity potential centred at the site of the defect, ψ defines the wavefunctions associated with the states of the impurity electron in the potential, and E gives the energies of these states. Reducing the Schrödinger equation to its hydrogenic form by assuming the amount of localised charge remaining in the region of the short range potential is small leads to the effective mass theory [3]. The energies E_v of defect levels near the band edges are given by [4] :

$$E_v = \frac{m^* Ry}{v^2 \epsilon^2} \qquad 2.2$$

where Ry is the Rydberg energy, m^* is the electron effective mass, ϵ is the host's dielectric constant and v is the principal quantum number of the state. This resembles the

solution for a hydrogen atom immersed in a uniform dielectric medium. The spatial extent of the defect is given by the Bohr radius which is related to the hydrogenic radius a(0) by

$$a = \frac{v^2 \epsilon}{m^*} a(0) \qquad 2.3$$

The hydrogenic model has been successful in calculating properties of shallow donors and acceptors [5,6,7] where the impurity potential is dominated by its long range coulomb term.

However, for deep levels, strong, short range interactions become increasingly important [8]. The resultant contraction of the defect wavefunction and the resulting deviation from the hydrogenic model make theoretical predictions more difficult; indeed it is still not possible to calculate the exact binding energy of a deep level defect in a semiconductor. The main significant differences in calculating the properties for deep levels are: unlike shallow defects it is crucial to know the precise atomic locations; one is often concerned with a change in the charge state such as photoionisation or carrier capture; or there may be a geometrical change in the defect. A change in the charge state of a deep level involves a redistribution of localised charge. So, defect calculations are based on self consistent methods [2].

There are two types of self consistent methods: (a) the molecular cluster method which uses standard molecular

techniques to examine cluster sizes of the order of 5-100 atoms. This has been used in the case of transition metal impurity calculations in II-VI semiconductors [9,10]. (b) Green's function method which defines an operator for the perfect crystal - $G(0) = 1/(E-H(0))$. The Schrödinger equation then becomes :

$$[1 - G(E)V]\, \phi = 0 \qquad 2.4$$

This can be solved by expressing the operators G(E) and V in a particular representation reducing to a simple set of algebraic expressions. Both techniques have been used successfully and rather than taking competing roles they have been complementary. Green's function methods avoid possible problems with cluster surfaces although these may be eliminated for the cluster method by choosing sufficiently large clusters [8]. Jaroś [2] has reviewed these techniques.

2.3 Properties of Shallow Levels

The terms 'shallow' and 'deep' applied to defect energy states refer to the energy position such a state has in the band gap. Shallow levels have ionisation energies comparable to kT and so are generally <0.1eV (eg in Si they are located at about $(E_C-0.07)$eV and $(E_V+0.07)$eV [11]). They can be classified as either donors (positively charged when ionised) or acceptors (negatively charged when ionised). Since shallow levels are ionised at room temperature they play the dominant role in the determination of the semiconductor conductivity type (n- or p-). As has been mentioned, the

hydrogenic model can be used to describe the shallow levels produced by a defect; therefore, such levels can be spectroscopically resolved. Low temperature luminescence has been a widely used experimental technique for the study of shallow levels - for example CdS [12,13]. The distinction between deep and shallow levels is somewhat arbitrary often corresponding to the experimental method used for their analysis. In the case of trapping effects they are referred to as deep.

2.4 Properties of Deep Levels

2.4.1 Introduction

Deep level defects can enhance the recombination of excess pairs of electrons and holes, in other words free carrier lifetimes can be drastically reduced by these centres [4]. Depending on the application this may or may not be useful :

(a) Long minority carrier lifetimes are required particularly in electro-optic devices in which photons are generated in, say, LEDs or in photovoltaic devices. In solar cells, deep level impurities will influence current collection in three ways : by reducing the minority carrier lifetime [4]; by recombination losses in the depletion region [4,14]; and by modification of the junction electric field under illumination [15]. In general all these effects may apply and so the deep levels will result in a poor solar cell efficiency.

(b) Fast switching Si devices require short but controlled minority carrier lifetimes. However, Si has long minority

carrier lifetimes due to its indirect band structure. To suppress carrier storage, in other words reduce carrier lifetime, impurities are introduced which give states in the band gap that are sufficiently deep not to contribute carriers in competition with shallow dopants but have large capture cross-sections to curtail the lifetime.

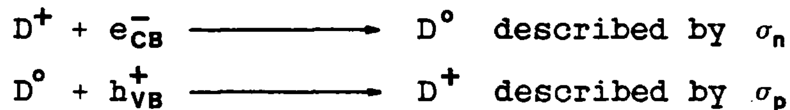
Defect states in semiconductors have many labels often depending on the experimental technique used to observe them: majority or minority carrier traps, electron or hole traps, recombination-generation centres, luminescence centres, photoconductive sensitising centres, shallow or deep levels, donor or acceptor levels etc. Energetically, shallow levels lie close to the band edges and may be described as hydrogenic as indicated above. The energy levels lying further into the energy gap that do not obey the hydrogenic model are classified as deep levels. The physical characteristics of a deep level defect may be defined in terms of 11 parameters: density, thermal and optical activation energies, thermal and optical capture cross-sections for electrons and holes, and thermal and optical emission rates for electrons and holes [16].

2.4.2 Capture Cross-Section

The capture cross-section is dominated by the potential energy variation in the region of the defect. Those exhibiting a large value will be charged centres having a coulombic attraction for free carriers. A neutral centre has a capture cross-section of the order of atomic dimensions -

10^{-15} cm^2. The third type of defect which displays a coulombic repulsion for free carriers will have a small capture cross-section. Fig.2.1 presents the potential distribution about these defect types [17].

All levels can trap either electrons or holes depending on their charge state. For example for a donor, D:



$D^+ + e^-_{CB} \longrightarrow D^o$ described by σ_n

$D^o + h^+_{VB} \longrightarrow D^+$ described by σ_p

where σ_n and σ_p are the capture cross-sections for electrons and holes respectively. One may consider such a level as an electron trap since σ_n is expected to be larger than σ_p because of coulombic attraction.

2.4.3 Thermal Emission Rate

At a fixed temperature, carrier capture is balanced by thermal emission of the same carrier type to maintain thermal equilibrium. For thermal equilibrium:

$$e_n n_t = c_n p_t \qquad 2.5$$

where e_n and c_n are the electron emission and capture rates, n_t is the density of occupied levels and p_t is the density of empty levels. The emission rate for electrons in n-type material is given by

$$e_n = \sigma_n V_{th} N_c \exp[-(E_C-E_T)/kT] \qquad 2.6$$

where V_{th} is the electron thermal velocity, N_c is the

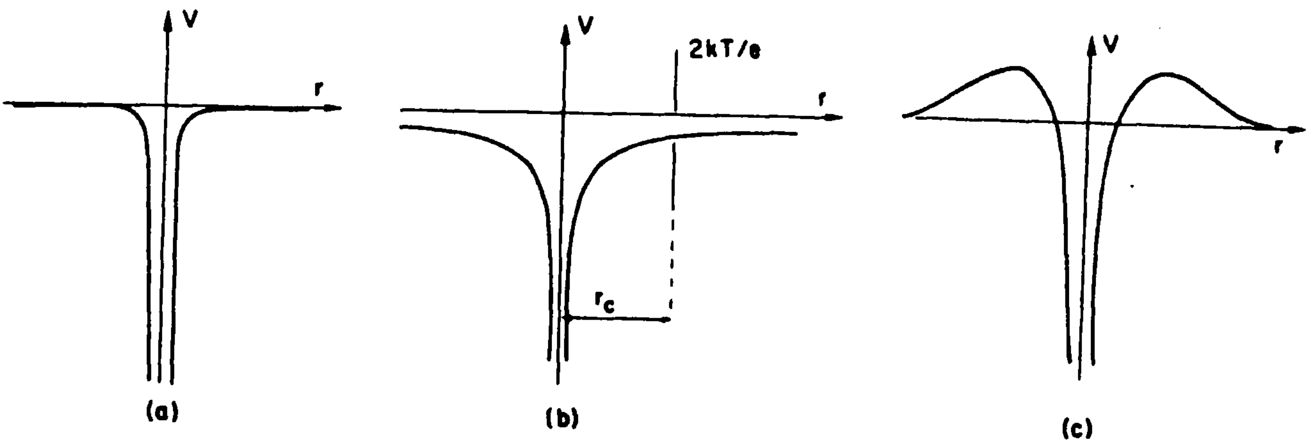


Figure 2.1 Schematic potential distributions of defect levels in semiconductors (a) neutral trap (b) coulomb-attractive trap (c) coulomb-repulsive trap. The effective radius r_c is the radius at which the coulomb potential in (b) has reached a value that is smaller by $2kT/e$ than the conduction band edge.

effective density of states in the conduction band and (E_C-E_T) is the energy of the level below the conduction band. The trap occupancy is

$$f_T = 1 - \frac{1}{1 + \exp[-(E_F-E_T)/kT]} \qquad 2.7$$

where (E_F-E_T) is the trap energy below the Fermi level. Traps will tend to emit electrons when $e_n \gg e_p$, and holes when $e_n \ll e_p$. These may be defined as electron and hole traps respectively since a defect can act as a trap only after emitting its carrier. Generally, electron traps exist in the upper half of the band gap and hole traps in the lower half. The optical emission rates for electrons and holes will depend upon the photon flux $\Phi(h\upsilon)$ and the trap density N_T:

$$e_n^o(h\upsilon) = \sigma_n^o(h\upsilon)\ \Phi(h\upsilon)\ N_T \qquad 2.8$$

$$e_p^o(h\upsilon) = \sigma_p^o(h\upsilon)\ \Phi(h\upsilon)\ N_T \qquad 2.9$$

The equilibrium conditions may be deduced from equations 2.5 and 2.6. For thermal emission/capture and optical emission, the trap occupancy is given by

$$f_T = \frac{e_p^t + e_p^o + c_n}{(e_p^t + e_p^o + c_n) + (e_n^t + e_n^o)} \qquad 2.10$$

where e_n^o and e_p^o are the optical electron and hole emission rates, e_n^t and e_p^t are the thermal electron and hole emission rates and c_n is the capture rate.

2.4.4 Lattice Relaxation Associated With Defects

As the localisation of a bound particle increases, so does the coupling to lattice phonons [2]. This has been used to explain the differences between optical absorption and emission lines, and between thermal and optical ionisation energies of deep level defects.

Consider a deep level, electron trap in the energy gap of a semiconductor. Lattice vibrations will cause the energy level to move up and down the energy gap. Sufficiently large vibrations will cause it to cross into the conduction band where it can capture an electron. The probability for electron capture is proportional to $\exp(-E_B/kT)$ [18] where E_B is the lattice energy required to shift the deep level to the conduction band. Immediately after electron capture, the lattice in the neighbourhood of the defect absorbs the available energy and vibrates violently around a new equilibrium position. These vibrations dampen rapidly as the energy propagates away from the defect site in the form of lattice phonons until the new equilibrium position of the deep level in the energy gap is attained. If a localised state becomes occupied with an electron, an additional polarisation of the lattice may take place and the defect finds a new equilibrium position. The capture cross-section is proportional to the product of the probability for 'crossing-induced' vibrations, the probability for electron capture during crossing and the probability that the electron will not be reemitted after capture [19]. This implies that the capture cross-section is temperature dependent according

to $\exp(-E_B/kT)$. Then E_B is the activation energy for non-radiative multiphonon capture.

Fig. 2.2 shows the electronic and lattice (elastic) energy as a function of the displacement coordinate Q, representing the lattice deformation. The potential energy is assumed to be a quadratic function of Q (harmonic oscillator). The position $Q=Q(0)$ corresponds to identical equilibrium positions when the electron is in the conduction band or in the valence band (this corresponds to the occupational state of the trap as empty). $Q=Q(t)$ corresponds to the position of the potential when the electron is trapped.

Consider the optical transitions E_V^o and E_C^o. Both of these are greater than the respective trap depths E_C-E_T and E_T-E_V by 2d where d results from the different equilibrium positions of the energy parabolas for empty and occupied states. This is known as the Stokes shift. The thermal activation energy for multiphonon capture is E_B. The activation energies for thermal emission of charge carriers are : $(E_C-E_T)+E_B$ and $(E_T-E_V)+E_B$. Consequently, the measured activation energies for thermal emission are not equal to the trap depths E_C-E_T and E_T-E_V whenever the capture process is thermally activated (ie $E_B^C \neq 0$ and $E_B^V \neq 0$).

The strong coupling of a deep level defect to the lattice increases the probability of a multiphonon capture process. Indeed, such systems exhibit a strong dependence on temperature, for example, resulting in broadening of

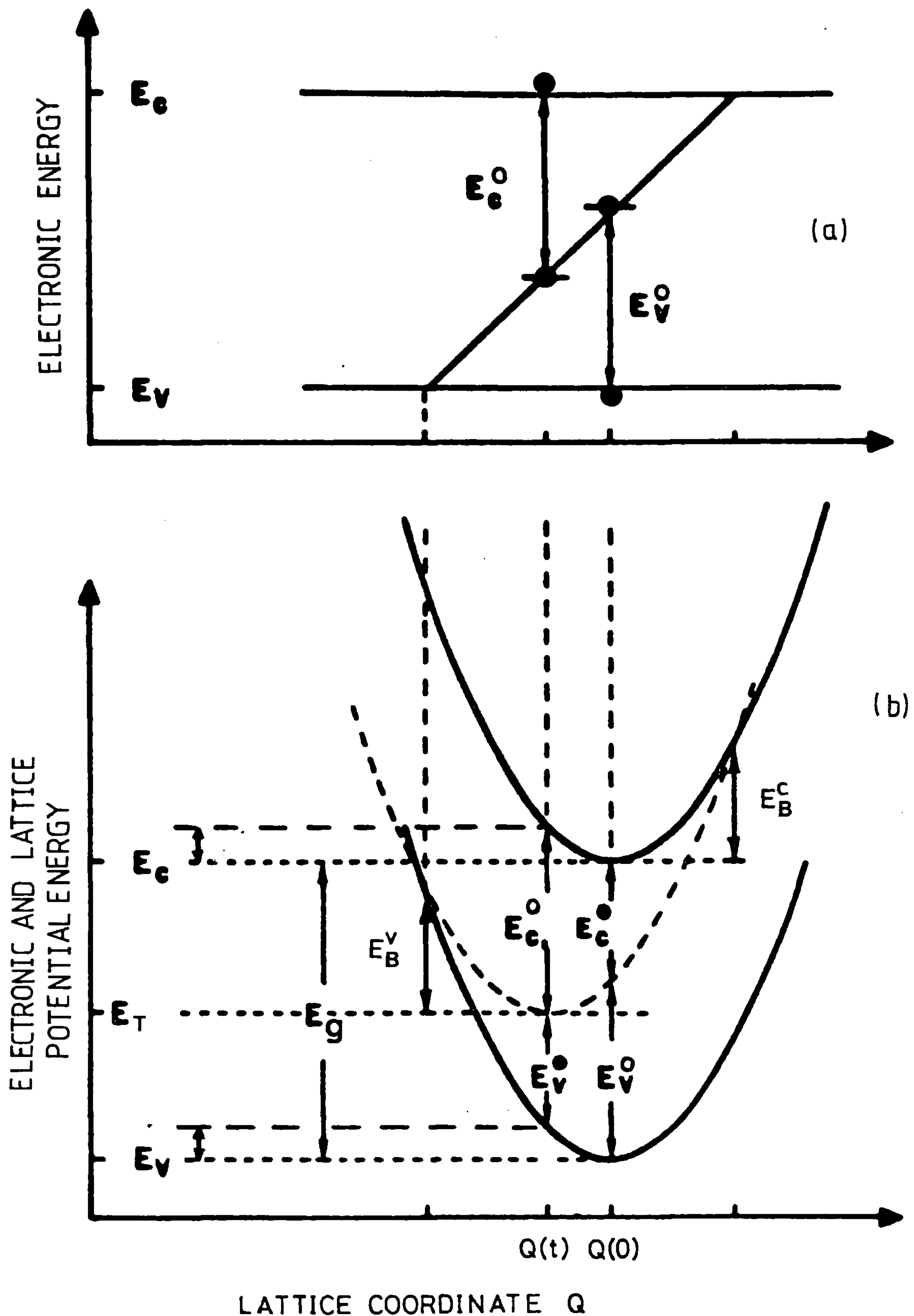


Figure 2.2 Schematic diagram of (a) the electronic energy and (b) the parabolic lattice potentials as a function of the lattice coordinate for trap levels with strong electron-lattice coupling

absorption or emission bands with increasing temperature [20]. It has also been shown and discussed by Henry and Lang [19] that the capture cross-section at high temperture may also be thermally activated

$$\sigma_n(T) = \sigma_n(\infty)\exp(-E_B/kT) \qquad 2.11$$

In fact they found for GaAs and GaP as $T \rightarrow \infty$ that $\sigma_n(\infty) \rightarrow 10^{-15}$ cm^2 and E_B varied between 0 and 0.56eV. Such large cross-sections which increase exponentially with temperature are often observed in semiconductors [21]. At low temperatures the capture cross-sections are weakly dependent on temperature and vary in the cases of attraction, neutrality and repulsion as $1/T$, $1/T^{1/2}$ and $T^{7/6}\exp[-3(\theta/T)^{1/3}]$ where θ depends on the magnitude of the charge [18].

As can be seen from fig. 2.2, optical and thermal ionisation energies are likely to be different. This derives from the Frank - Condon Principle which states that for an optical transition, the slowly moving atoms are effectively stationary and so the transition is vertical, as shown in the configuration coordinate diagram. For thermal processes this is not the case; the atoms attain a vibrational configuration making the transition thermally favourable. If the capture cross-section is not thermally activated, the difference in energy between the optical and thermal transitions is known as the Frank - Condon shift [22].

2.5 Deep Levels in II-VI Semiconductors

2.5.1 Introduction

Deep levels in II-VI semiconductors have been investigated for many years. Much of the early work was carried out using TSC and photoconductivity measurements, the interpretation of which was not always easy. In more recent years techniques such as photocapacitance, DLTS, EPR, and ODMR have been used to gain a better picture of the properties of these defect levels. However, to date, very little is known about their nature. In the following discussion of deep localised states in II-VI semiconductors much of the fundamental investigations carried out in recent years is reviewed.

2.5.2 Native Defects

In II-VI semiconductors the possible native point defects are anion vacancies, cation vacancies, antisite defects corresponding to a metal on a chalcogen site or vice versa, and interstitial defects where the metal or chalcogen occupies an interstitial site in the lattice.

EPR has been used to identify metal and chalcogen vacancies, for example, the metal vacancy V_{Zn}^{-} in ZnSe [20,23]. A hole trapped at the vacancy gives rise to the resonance; it was found that the hole was trapped at a single Se neighbour, largely in a p orbital. With 1.5MeV electron bombardment a Zn interstitial as well as the vacancy was found to occur [24]. In CdS, the metal vacancy centre, V_{Cd}^{-}

is similar to that found in ZnSe [25] with the hole localised on one of the four S neighbours.

Using the technique of ODMR it has been shown that V_{Zn}^{-} is a luminescent active defect in ZnSe [26] and gives rise to broad photoluminescence. These results have also shown that V_{Zn}^{2-} is a deep acceptor state. At room temperature there is very little evidence for single vacancies since there is a tendency for vacancies to form complexes with other defects [27,28]. This is suggested from the facts that these complexes are energetically favoured and that the activation energy for the migration of vacancies is likely to be low eg 1.26eV for V_{Zn} migration in ZnSe [27,29].

It is difficult to correlate the information obtained using magnetic resonance techniques with that obtained from deep level transient spectroscopy (DLTS) [30]. The results from DLTS enable the trap density, activation energy for electron emission and carrier capture cross-section for the defect state to be determined, but with no direct identification of the trap. Only the fact that the same trapping centres are reproducibly observed, perhaps by several researchers, suggests the probability that they are due to native defects. For example, two electron traps in CdS at 0.25eV and 0.4eV have been observed by a number of workers [31-38]. These have been tentatively ascribed to sulphur vacancies [31] or donor like associates formed between native defects and residual impurities [38].

2.5.3 Isoelectronic Impurities

Photoluminescence has been used to investigate the systems ZnTe:O [39], ZnS:Te [40] and CdS:Te [41]. In all these cases it is assumed that the isoelectronic impurity lies on an anion site and induces deep electron or hole trapping centres : O is an electron trap in ZnTe with a binding energy of 0.4eV; Te is a hole trap in CdS and ZnS with binding energies of 0.2eV and 0.4eV respectively. The luminescent spectra for ZnS:Te and CdS:Te suggest there is strong phonon coupling [40,41]. At high impurity concentrations ($>10^{19} cm^{-3}$) a second luminescent band is observed and is thought to be due to pairing of the substitutional Te atoms. There has been very little other experimental work on these types of isoelectronic impurities.

2.5.4 Copper Impurity

Copper is important in II-VI semiconductors as a residual impurity and as a dopant for the 'activation' of II-VI phosphors; it is recognised as forming deep acceptor states in II-VI semiconductors [42]. It has a high diffusion coefficient and consequently, in bulk crystals which are grown at high temperatures over long periods, it is almost unavoidable [43]. Due to its high mobility it is then likely to create complex centres with native defects or impurities [42].

The optical spectra and EPR [44], photocapacitance [45,46] and optical DLTS [36,47] results for II-VI crystals

have been interpreted in terms of crystal field theory. The symmetry groups for cubic and hexagonal crystals are T_d and C_{3v} respectively. Cu^{2+} has the d^9 configuration. The energy level diagram can be found by using the effective Hamiltonian invariant under the symmetry operations of the particular symmetry group. From Russell-Saunders coupling one can assign the term ^2D to the free ion. In a tetrahedral field this energy level loses some degeneracy and is split to give two levels $E_2$and $^2T_2$ (see fig.2.3). The fine stucture of these levels is determined by spin-orbit coupling and in the case of hexagonal crystals by an additional small crystal field with symmetry group C_{3v} (tetragonal distortion).

EPR measurements on Cu-doped II-VI materials [20] provide evidence for resonances related to Cu. As well as substitutional Cu^{2+}, evidence has been obtained to show that copper easily associates with other defects to form complexes. In CdS, 4 resonances have been observed [49], only one of which is thought to be due to isolated, substitutional Cu^{2+}. In ZnS, 8 have been reported [50].

2.5.5 Other Impurities

Several other impurities in II-VI materials that are thought to introduce deep levels into the band gap have been studied. These states may or may not have resulted from intentional doping. Here two specific examples are considered.

CdS/Cu_2S thin film solar cells have been prepared on a

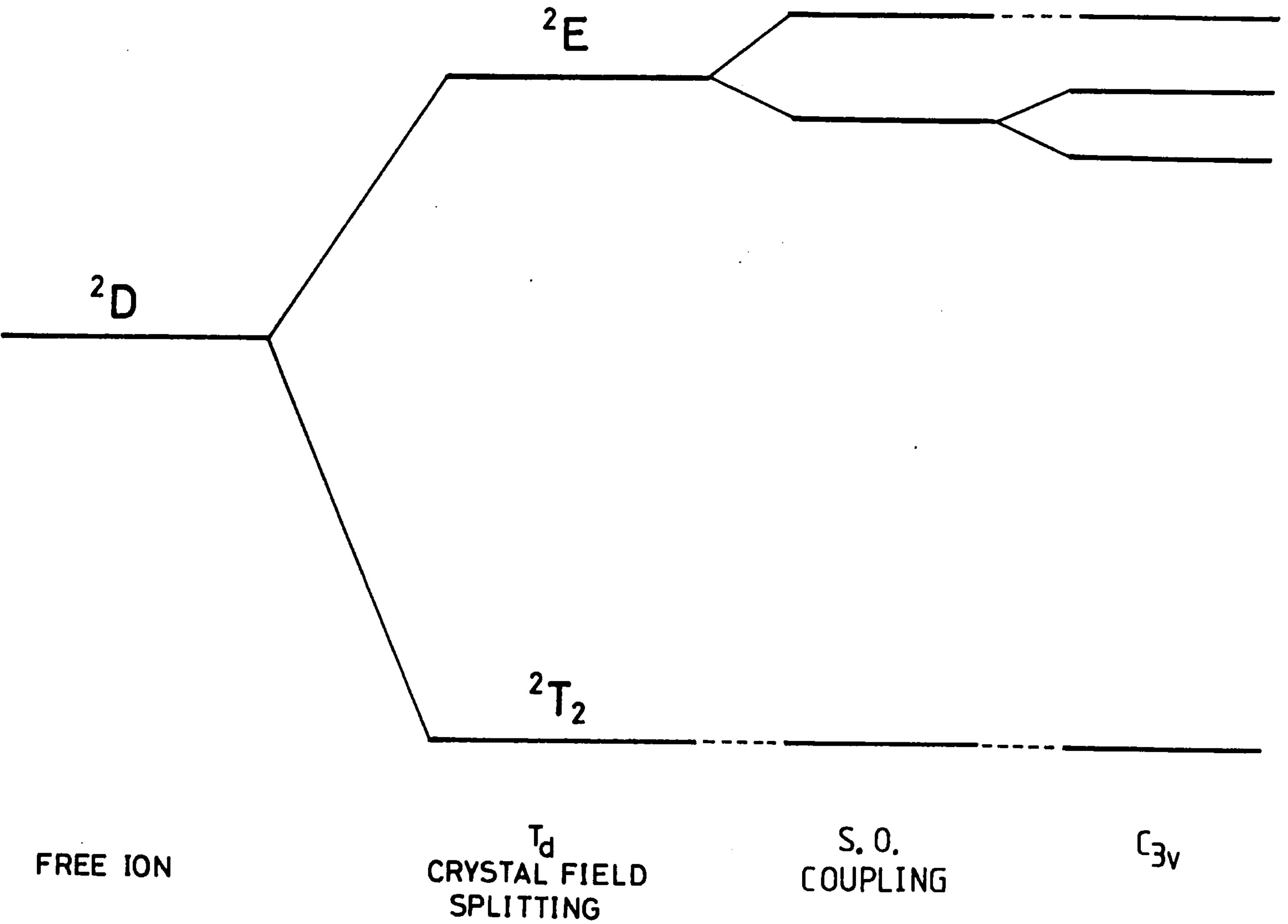


Figure 2.3 Crystal field splitting, spin-orbit coupling and tetragonal distortion of the ^2D free ion state of Cu^{2+} (d^9) [48]

variety of substrates such as tin oxide coated glass. One feature developed by Bloss and co-workers [51] was CdS evaporation onto a layer of silver. Using the technique of steady state photocapacitance on dry barrier [52] CdS/Cu_2S solar cells, Pande et al [53] found a deep donor level that was only present in films deposited onto silver substrates, implying the level was due to the silver. This silver level was found to inhibit the diffusion of copper into the CdS which is thought to cause degradation of the device. Consequently, this feature of the device processing has resulted in an improvement in the device stability.

The transition metal ions (Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu) and rare earth ions (Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm) have an open shell core configuration. Consequently, under the influence of a crystal field the 3d levels (transition metal) or 4f levels (rare earth) lose their degeneracy, leading to several electronic states any of which may lie deep within the semiconductor band gap [42]. The transition metals may be incorporated unintentionally as residual impurities during crystal growth as has been discussed for copper.

The manganese ion Mn^{2+}, which has the $3d^5$ configuration, is a substitutional impurity in CdS, ZnS and ZnSe [42]. The luminescence resulting from internal transitions has been investigated by Busse et al [54,55]; five emission bands were observed in ZnS:Mn. In general Mn doped II-VI compounds show efficient electroluminescence. The deep levels produced by Mn behave as luminescence centres communicating with shallow

states by optical transitions; this has been reviewed by Mach and Müller [56].

2.5.6 Deep Levels from Extended Defects

Very little is known about the influence of extended defects such as dislocations and grain boundaries upon the electrical and optical properties of II-VI semiconductors nor indeed whether they create localised states in the energy gap. They have been associated with a variety of phenomena such as enhanced carrier recombination at grain boundaries [57] and dislocations [58], poor electronic device characteristics [59], and degradation of semiconductor lasers [60]. Theoretical calculations of the band structure of dislocations have only recently been attempted [61,62]. Such calculations have shown that they can produce a range of defect states in the band gap including localised states; these have been discussed by Ourmazd [63] and by Labusch and Schröter [64]. If defect states can be assigned to dislocations it may not be clear whether the states are due to ruptured bonds at the dislocation core or due to particular sites along the core such as kink sites. Vyvenko and Schröter [33] have correlated DLTS measurements with EBIC observations in CdS. It was found that two deep levels were only observed in the presence of dislocations. They suggested that these states arose from point defect clouds surrounding the dislocations.

2.6 Summary

Deep levels are known to affect the electrical and optical properties of semiconductors. This is an important consideration for the device applications of a material. Deep levels can control carrier lifetimes in such a way that may be detrimental to the device operation (eg solar cells) or indeed improve its properties (eg Si switching device).

Unlike shallow levels, the deep states produced by a defect cannot be described by a simple hydrogenic model. Other theoretical approaches have been taken that have proved successful although further improvements are needed to correlate such information with experimental data. To an experimentalist a deep level in the band gap of a semiconductor can be completely defined by 11 parameters - density, thermal and optical activation energies, thermal and optical capture cross-sections for electrons and holes, and thermal and optical emission rates for electrons and holes. They may arise from native defects (vacancies, interstitials, antisite defects), impurities (substitutional, interstitial defects), complexes or extended defects (eg dislocations, grain boundaries). Very often they may be controlled by the crystal growth procedure and conditions, but they would be difficult to eradicate.

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CHAPTER 3

CAPACITANCE MEASUREMENTS FOR THE STUDY OF DEEP LEVELS

3.1 Introduction

The study of deep level defects in semiconductors using space charge techniques is well established and there are some excellent reviews [1-3]. The main techniques used in the present work were deep level transient spectroscopy (DLTS) [4] and optical DLTS (ODLTS) [5] to determine the thermal activation energies and capture cross-sections for deep trapping levels in semiconductors; and deep level optical spectroscopy (DLOS) [6] for determining the spectral distribution of the optical capture cross-sections for the deep states. Schottky barrier devices provide a convenient method for obtaining a space charge region in a semiconductor for the application of these techniques. The II-VI semiconductors studied were all n-type and so DLTS, which can only give information on majority carrier (electron) traps, was used to study the deep donor levels. However, in many applications such as LED's, minority carrier traps which can act as recombination centres, are important [7,8]. To study these traps ODLTS was used, enabling the parameters for a deep level near the valence band (n-type semiconductor) to be determined. The DLOS signature gives the energy distribution of the optical capture cross-section and so this technique was used to gain optical information about traps observed in

DLTS and ODLTS and those traps lying near midgap which are difficult to observe using thermal techniques.

This chapter contains a discussion of the relevant theory of Schottky barrier devices which has been reviewed by Rhoderick [9] showing the importance of space charge methods for monitoring deep level defects. This is followed by a description of the techniques mentioned above.

3.2 The Metal-Semiconductor Junction

Consider a metal and an n-type semiconductor that are electrically neutral and separated from each other; the semiconductor work function (Φ_s) is less than that of the metal (Φ_m). If the metal and the semiconductor are connected electrically by a wire, electrons flow from the semiconductor into the metal. This results in the Fermi levels becoming coincident; in effect the semiconductor Fermi level is lowered by an amount equal to the difference between the two work functions. As the distance between the metal and semiconductor decreases, an increasing negative charge is built up at the metal surface. There is an equal and opposite charge in the semiconductor provided by conduction electrons receding away from the surface. This leaves uncompensated positive donor ions in a region depleted of electrons. Since the donor concentration is many orders of magnitude less than the electron concentration in the metal, this depleted region of uncompensated donors occupies a layer of appreciable volume extending into the semiconductor. This is known as the space charge or depletion region. The

density of free carriers N_d is assumed to fall abruptly from a value equal to the density in the semiconductor bulk to a value which is negligible compared with the donor concentration; this is known as the depletion approximation. Outside the depletion region the semiconductor is neutral and within this region it has a charge density of qN_d where q is the fundamental electronic charge. The variation of the charge density with distance x from the metal is shown in fig. 3.1a. The electric field (ξ) is related to the charge density by Gauss's theorem such that it increases linearly as the metal is approached to a value $qN_d w/\epsilon_s$ at the interface (see fig. 3.1b) - w is the space charge region width, ϵ_s is the dielectric constant of the semiconductor. The electrostatic potential ($\psi(x)$) is given by

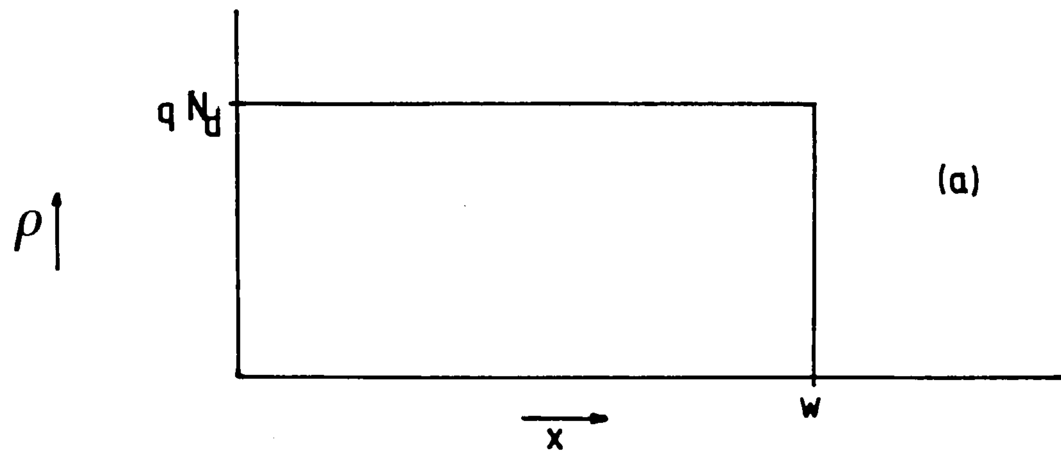
$$\psi(x) = \int_x^w \xi \, dx \qquad 3.1$$

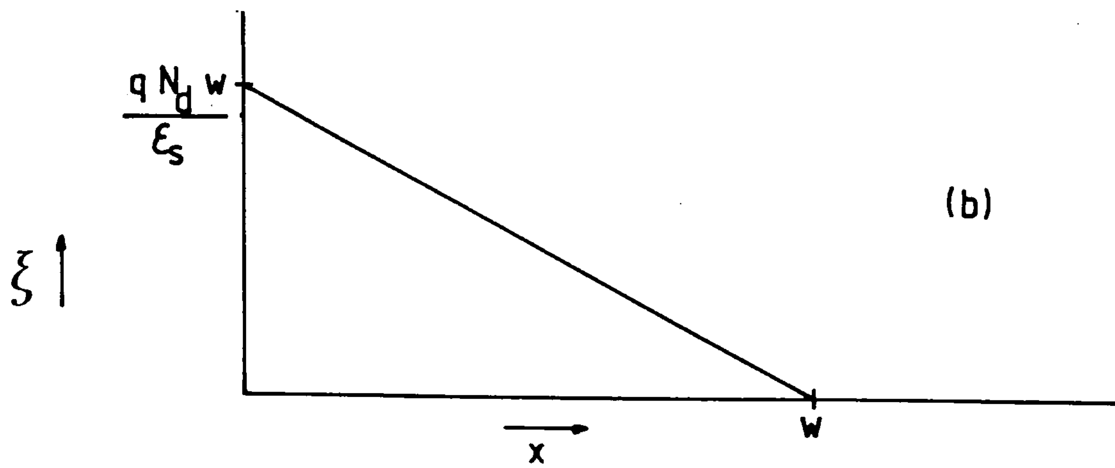
which reduces to the quadratic

$$\psi(x) = \frac{-qN_d}{2\epsilon_s}(w-x)^2 \qquad 3.2$$

The variation of $\psi(x)$ with x is shown in fig.3.1c. For the metal-semiconductor contact, the subsequent parabolic band bending is shown in fig. 3.2. This is known as a Schottky barrier.

The height of the potential barrier on the semiconductor





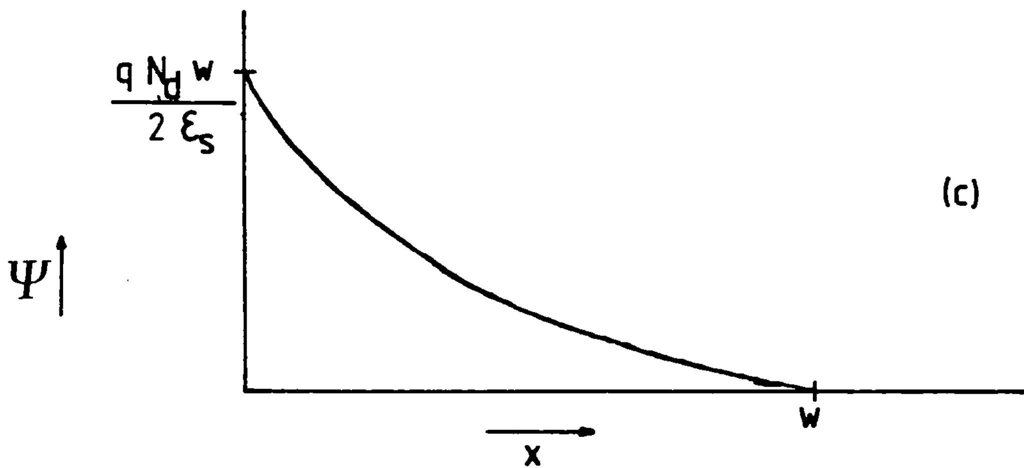


Figure 3.1 Variation of (a) charge density (b) electric field strength and (c) electrostatic potential with distance according to the depletion approximation

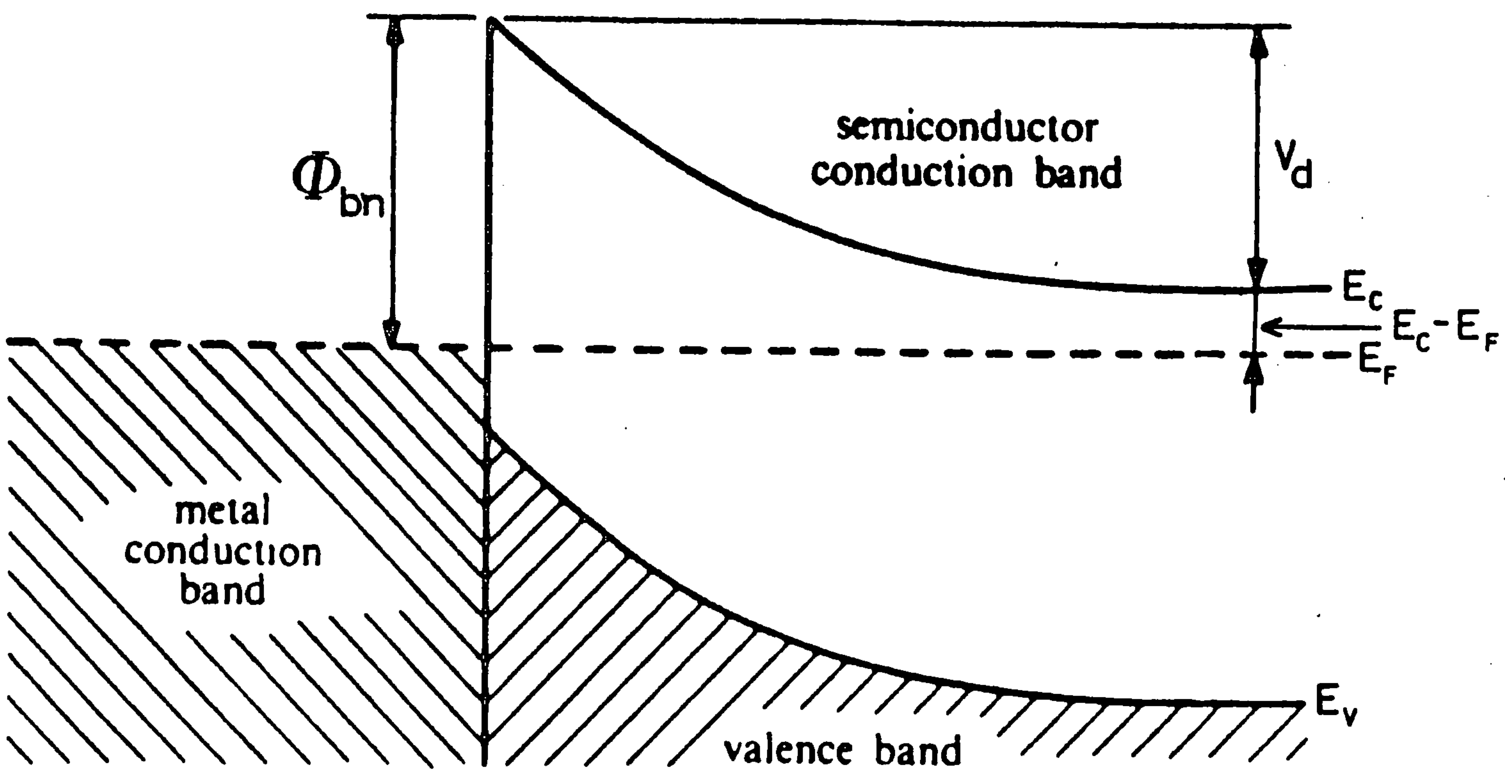


FIGURE 3.2 Energy band diagram of an ideal metal n-type semiconductor contact(Schottky barrier).

side is

$$qV_d = \Phi_m - \Phi_s \qquad 3.3$$

V_d is the diffusion potential in the interior of the semiconductor with respect to the metal surface. The height of the barrier on the metal side is given by

$$\Phi_{bn} = (\Phi_m - \Phi_s) + (\Phi_s - X_s) = \Phi_m - X_s \qquad 3.4$$

or

$$\Phi_{bn} = V_d + (E_c - E_f) \qquad 3.5$$

where X_s is the electron affinity of the semiconductor and $(E_c - E_f)$ the depth of the Fermi level below the conduction band.

In most cases the ideal Schottky barrier shown in fig 3.2 is never achieved due to a thin insulating layer on the surface of the semiconductor which is generally brought about during the processing of the semiconductor surface (polishing, etching) prior to applying a contact. This usually leaves a thin, oxide layer. The barrier presented by this interfacial layer may be sufficiently narrow to allow electron tunneling. The band diagram for a metal-insulator-semicondutor (MIS) structure is given in fig. 3.3.

The potential drop $q\Delta$ across the interfacial layer may

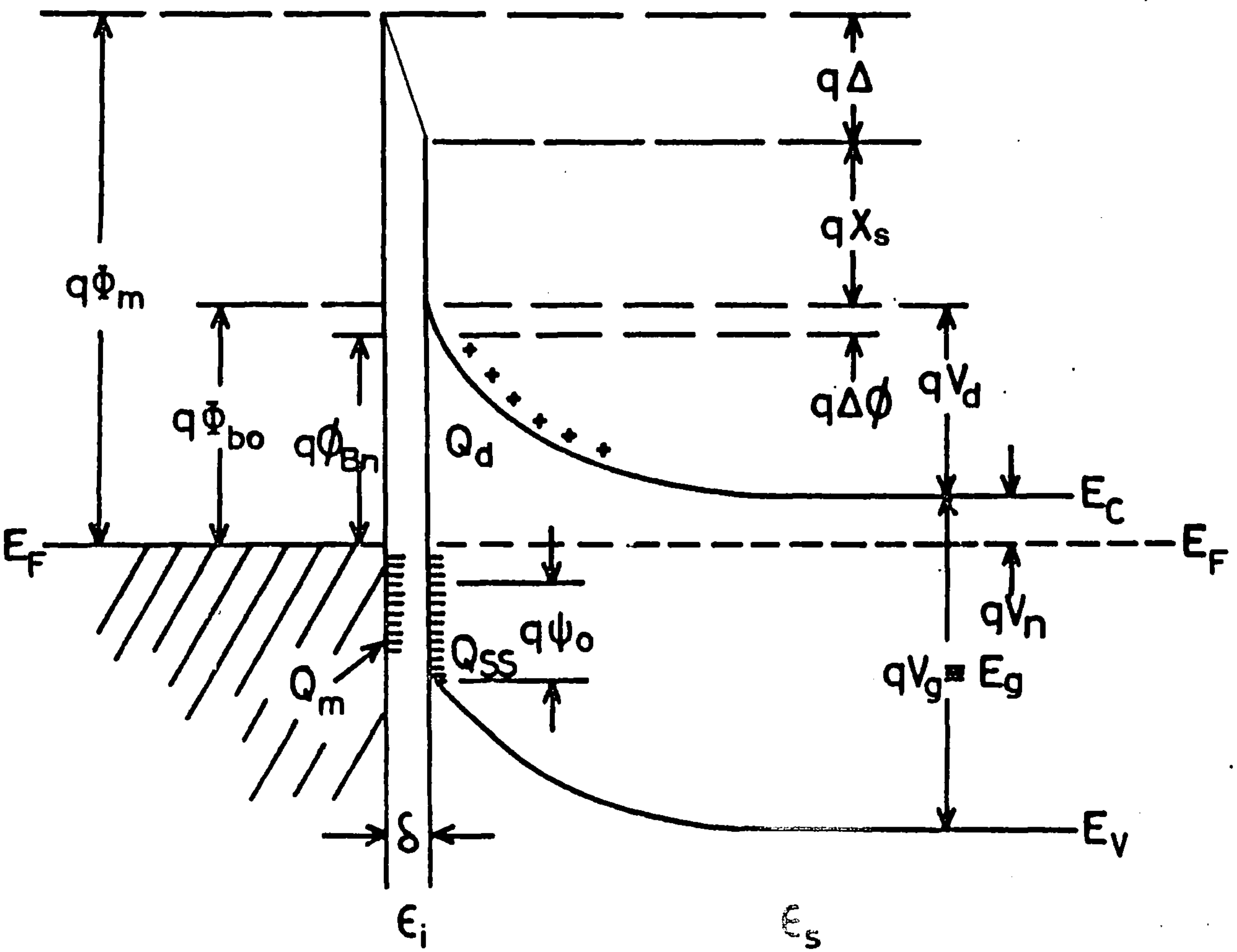


FIGURE 3.3 Detailed energy band diagram of a metal n-type semiconductor contact with a thin interfacial layer [13]

be small enough to render equation (3.3) a good approximation for the barrier height. However, it is often found that the barrier height is not very sensitive to the metal work function and may be almost independent of the choice of metal. Bardeen [10] proposed a model in which surface states located in the energy gap played the key role.

Dangling bonds at the pure semiconductor surface can strongly adsorb impurities. Such bonds give rise to discrete states at the surface boundary of the crystal. This was first shown by Tamm [11] and the theory expanded by Shockley [12]. The states associated with the dangling bonds are known as Tamm states and have a density of the order of surface atoms - $10^{14}\,cm^{-2}$. In addition to these intrinsic states there are extrinsic surface states arising from adsorption of impurities, such as oxygen, which can act as donors or acceptors. The surface then has a positive or negative charge which is compensated by an equal but opposite space charge near the surface. For n-type material at thermal equilibrium, the energy bands may bend downwards (donor-like surface states) or upwards (acceptor-like surface states). According to Bardeen, if these surface states have a sufficiently high density, the band bending may be dominated by the charge localised at the interface rather than by the metal work function.

In the absence of surface states the negative charge on the surface of the metal Q_m is equal and opposite to the space charge in the semiconductor Q_d. With the presence of surface states this condition of neutrality becomes

$$Q_m = -(Q_{ss} + Q_d) \qquad 3.6$$

Q_{ss} is the charge due to the surface states. In general, the barrier height is a function of both the charge in the interface states and the metal work function. Cowley and Sze [13] have demonstrated this and have obtained a general expression for the zero bias barrier height

$$\Phi_{bn} = z(\Phi_m - \chi_s) + (1 - z)(Eg - \psi_o) \qquad 3.7$$

where $z = \epsilon_i / (\epsilon_i + \delta q D_s)$, ϵ_i is the permittivity of the interface layer, δ is the thickness of the interface layer D_s is the density of interface states, and ψ_o, the neutrality level.

For a high density of surface states, the charge associated with the electric field across the interface can be accommodated by these states. The height of the barrier is then determined by the occupancy of the surface states rather than the metal work function. The Fermi level is pinned by the high density of surface states. This extreme is known as the Bardeen limit [10] and the barrier height is given by

$$\Phi_{bn} = Eg - \psi_o \qquad 3.8$$

3.3 The Capacitance of a Schottky Barrier

3.3.1 Bias Dependence of Capacitance

Consider a Schottky barrier at zero bias; the band diagram for an n-type semiconductor is shown in fig. 3.2. The electric field at the interface is only due to the uncompensated donors and is given by [9]

$$\xi_{max}^2 = \frac{2q}{\epsilon_s}\left\{N_d\left(V_d - \frac{kT}{q}\right) + \frac{kTN_d}{q}\exp\left(\frac{-qV_d}{kT}\right)\right\} \qquad 3.9$$

where V_d is the diffusion voltage associated with the reverse bias V_r. If $qV_d > 3kT$ then this becomes

$$\xi_{max}^2 = \frac{2qN_d}{\epsilon_s}\left(V_d - \frac{kT}{q}\right) \qquad 3.10$$

From Gauss's theorem, the charge due to uncompensated donors is given by

$$Q = \epsilon_s \xi_{max} = \left(2q\epsilon_s N_d\right)^{1/2}\left(V_d - \frac{kT}{q}\right)^{1/2} \qquad 3.11$$

The capacitance is given by

$$C = \frac{dQ_d}{dV_r} = \frac{dQ_d}{dV_d} \qquad 3.12$$

and so

$$C = \left(\frac{q\,\epsilon_s N_d}{2}\right)^{1/2} \left(V_d - \frac{kT}{q}\right)^{-1/2} \qquad 3.13$$

Using the depletion approximation [9] this becomes

$$C = \left(\frac{q\,\epsilon_s N_d}{2V_d}\right)^{1/2} \qquad 3.14$$

where

$$V_d = \frac{qN_d w^2}{2\epsilon_s} \qquad 3.15$$

and so $C = \epsilon_s/w$. This shows that the capacitance is analogous to that of the parallel plate capacitor with dielectric permittivity ϵ_s and width w. However, $V_d = V_{do} + V_r$, where V_{do} is the diffusion voltage at zero bias, therefore

$$C = \left(\frac{q\,\epsilon_s N_d}{2}\right)^{1/2} (V_{do} + V_r)^{-1/2} \qquad 3.16$$

When a reverse bias is applied, electrons in the conduction band recede from the metal and the depletion width increases. From equation (3.16)

$$\frac{1}{C^2} = \left(\frac{2}{q\,\epsilon_s N_d}\right) (V_d + V_{do}) \qquad 3.17$$

From a plot of $1/C^2$ against reverse bias V_r, the slope gives the uncompensated shallow donor concentration N_d

$$N_d = \frac{2}{q\epsilon_s}\left\{-\frac{d(C^{-2})}{dV}\right\}^{-1} \qquad 3.18$$

The barrier height can be obtained from the voltage intercept

$$\Phi_{bn} = V_i + (E_c - E_f) \qquad 3.19$$

where V_i is the voltage intercept and $(E_c - E_f)$, the depth of the Fermi level below the conduction band, obtained from [9]

$$\frac{N_d}{N_c} = \exp(-(E_c - E_f)/kT) \qquad 3.20$$

N_c is the effective density of states in the conduction band.

If the donor distribution is non-uniform then equation 3.17 is not linear for $f(1/C^2)=V$. The donor density $(N_d(w))$ can be determined at the edge of the depletion region w from the slope of the curve [9]

$$N_d(w) = \frac{2}{q\epsilon_s}\left\{-\frac{d(C^{-2})}{dV}\right\}^{-1} \qquad 3.21$$

From this equation it can be seen that by increasing the reverse bias, the depletion region width increases and so the donor density profile into the semicondutor bulk can be obtained.

Another consideration is the effect of an interfacial layer on the capacitance-voltage characteristics of a device. The capacitance of a thin insulating layer will be in series with the capacitance of the depletion region. Cowley [14] and Goodman [15] have shown that in the presence of an interfacial layer, the barrier height deduced from C-V measurements usually exceeds that obtained from current-voltage or photoelectric methods. More recently, Fonash [16] has given a rigorous analysis of the effects of an interfacial layer with a re-evaluation of Cowley's results. Fonash has shown that there is a non-linear dependence of $1/C^2$ on the reverse bias voltage. This is due to interface states which follow the metal and/or semiconductor Fermi level with reverse bias, and which may follow the oscillating voltage under most biassing conditions. This results in a shift in the voltage intercept giving, on the basis of the analysis for an ideal Scottky device, an erroneous result for the barrier height.

3.3.2 The Effect of Deep Traps

The capacitance of a Schottky barrier can be affected by the presence of deep energy levels in the semiconductor. The case of a single deep donor trap of uniform density N_T lying at a depth E_C-E_T below the conduction band is considered here and shown in fig. 3.4. At thermal equilibrium the traps lying below the Fermi level E_F will be full of electrons and those above, empty. The degree of band bending depends upon the reverse bias voltage. This means that by applying a reverse bias, the depletion region increases as does the

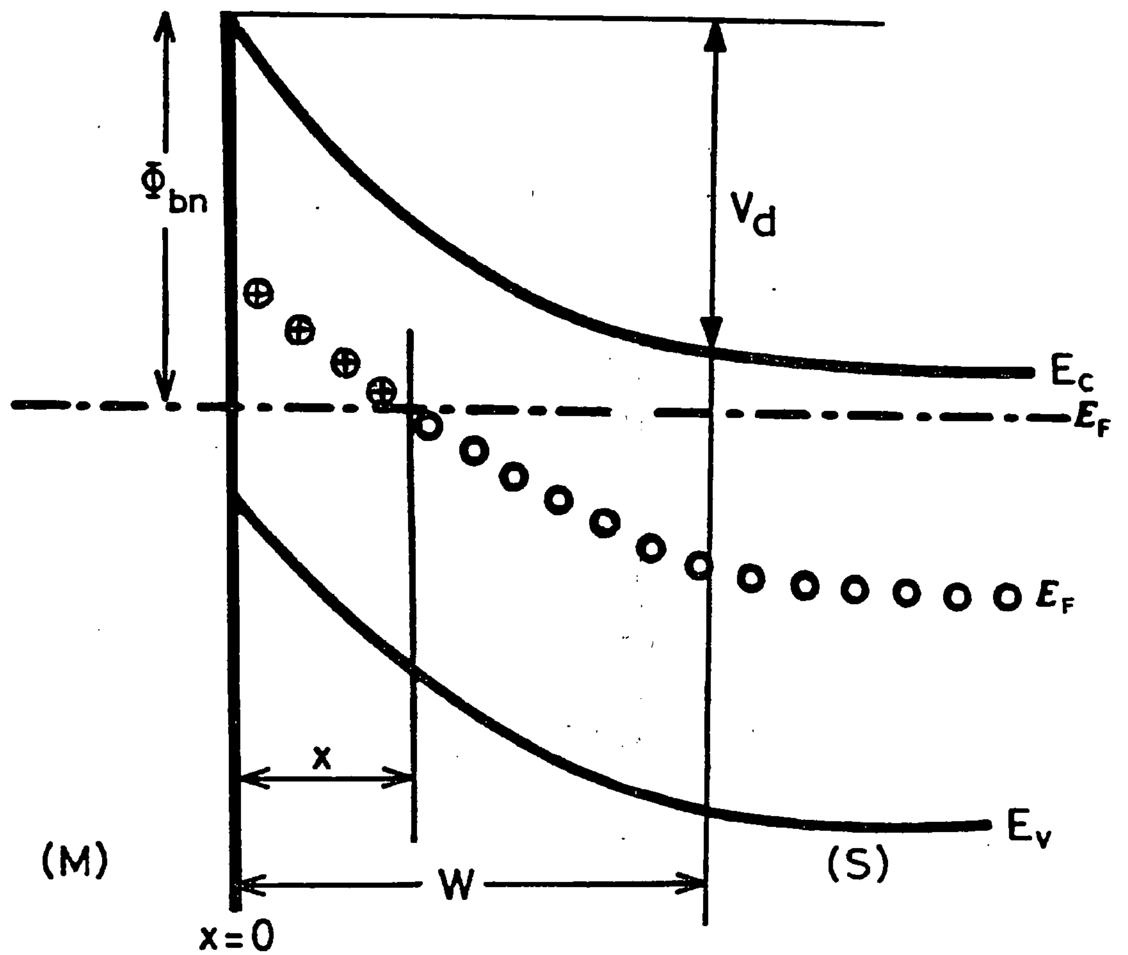


FIGURE 3.4 Energy band diagram of a Schottky barrier containing donor-like deep traps.

density of deep donor levels above the Fermi level. The thermal emission of electrons can be obtained by applying the principle of detailed balance which states that at thermal equilibrium the electron capture rate is equal to the electron emission rate [17]. Therefore the rate equation is given by

$$e_n = \sigma_n V_{th} N_c \exp(-(E_C-E_T)/kT) \qquad 3.22$$

where e_n is the electron emission rate from the trap, σ_n is the capture cross-section, V_{th} is the electron thermal velocity and N_c is the effective density of states in the conduction band.

The effect of a reverse bias on deep levels present in the depletion region is shown in fig 3.5. The donor traps are uncompensated within the depletion region width w so that the variation in charge density with x is shown by the solid line in fig. 3.5b. During a capacitance-voltage measurement, a small, oscillating voltage is superimposed on the bias voltage. This oscillating voltage uncovers charge at y - electrons are emitted by the trap into the conduction band. If the frequency of the oscillating voltage is less than the deep level electron emission rate then the traps at point y can follow the voltage variation by emission and capture processes. If the voltage is changed from V_r to $V_r + \Delta V_r$ and the traps can exactly follow this change, then the charge distribution increases by an amount $qN_d/\Delta w$ due to the uncompensated donors as shown by the dotted line in fig. 3.5b. The general expression for the capacitance of a

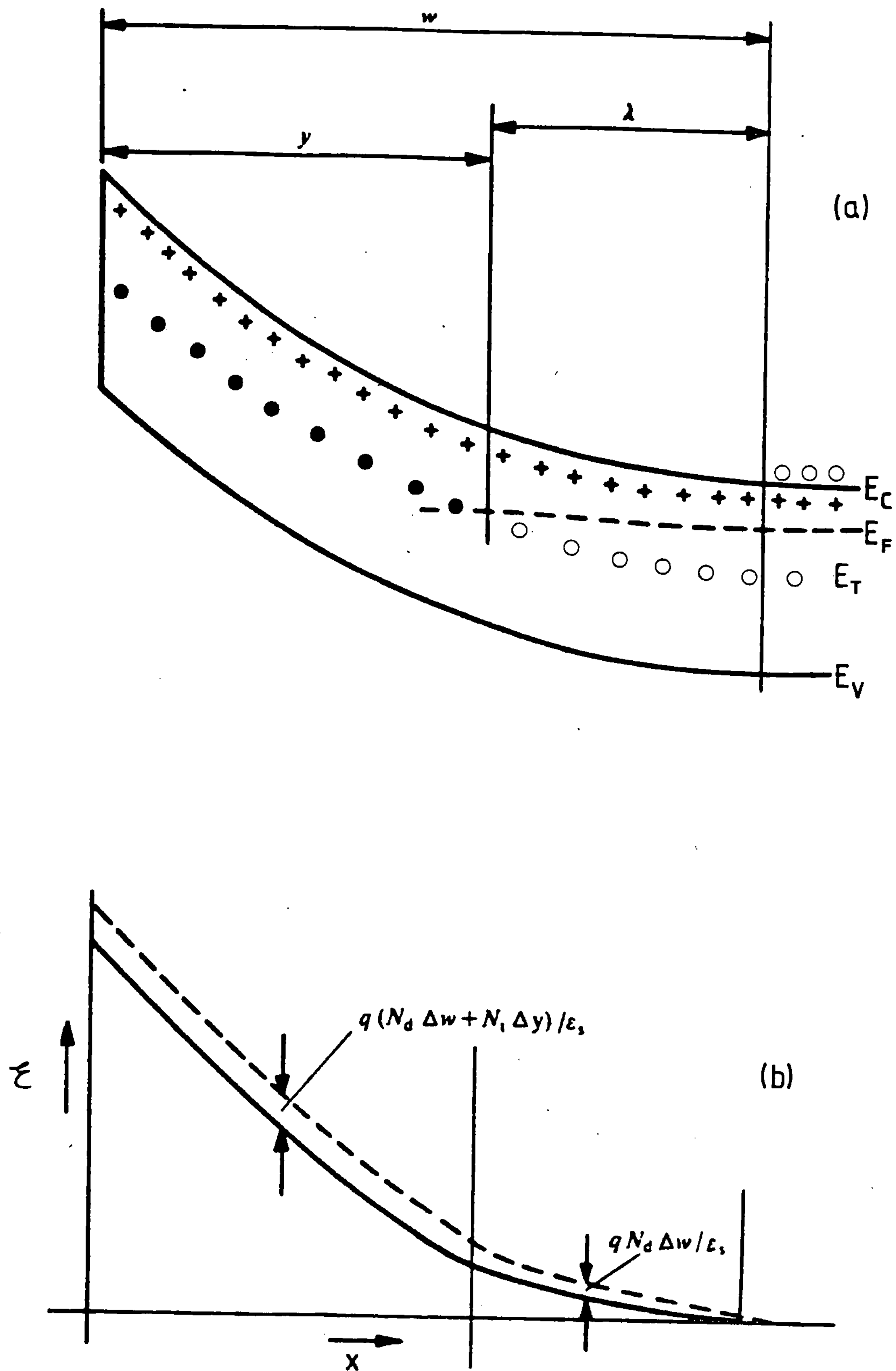


Figure 3.5 Effect of reverse bias on deep traps

(a) charge state, (b) field distribution
- reverse bias V_R ----- reverse bias $V_R + \Delta V_R$

Schottky barrier in the presence of deep traps is [18]

$$C = A\left\{\frac{qN_d\epsilon_s}{2(V_d + V_r)}\right\}^{1/2}\left\{1 + \frac{N_T}{N_d}\frac{e_n^2}{(e_n^2 + w_s^2)}\right\} \qquad 3.23$$

If the frequency w_s of the oscillating voltage is greater than the electron emission rate then the traps cannot follow the test signal; this condition is most often met in practice. Equation 3.23 then reduces to that of the ideal Schottky barrier capacitance (3.16). For a sample with a high density of deep levels the measurement of the capacitance must be made with care. Fig. 3.6 shows the capacitance response during a C-V measurement carried out by Lang and Logan [19] on AlGaAs for which $N_T/N_d = 8$. The capacitance decay is related to the electron emission rate for the deep traps by equation 3.22. Furukawa and Ishibashi [20] have shown that the initial capacitance state gives the usual linear $1/C^2$ vs V plot, whereas the steady-state capacitance does not. Therefore, care must be taken for a C-V measurement when the free carrier concentration and barrier height is to be calculated. Roberts and Crowell [21], Zohta [22], Kimerling [23] and Noras [24] have discussed the effects of deep traps on the junction capacitance; their frequency dependence; and the effect they have on the measurement of the free carrier distribution.

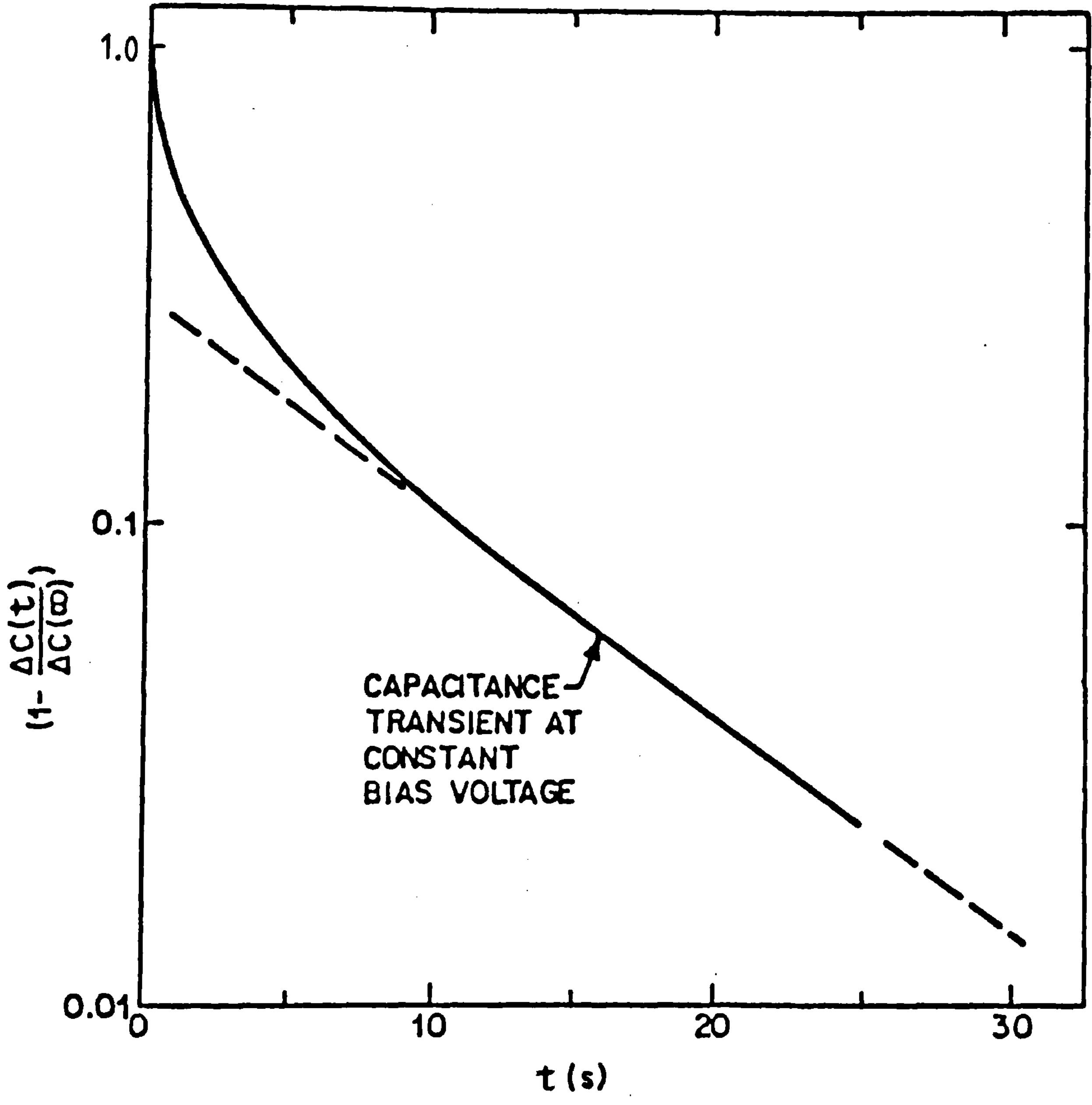


Figure 3.8 Effect of a large trap concentration on the constant-bias carrier emission transient

3.4 Space Charge Techniques

3.4.1 The Capacitance Transient

Consider a Schottky barrier on an n-type semiconductor containing a uniform density of deep donor traps N_T, lying at a depth E_C-E_T below the conduction band. The band diagram of such a system at zero bias is shown in fig. 3.7. Those traps up to a distance w_0^T from the interface lie above the Fermi level and will be empty of electrons; these traps will have a positive charge. At a distance greater than w_0^T from the metal, the level will be below the Fermi level, full of electrons and hence, neutral. If the bias is instantaneously changed to a reverse bias V_r, the depletion region width is changed from w_0 to w_r (see fig. 3.7). Since $C = \epsilon_s/w$ then the capacitance is reduced according to the voltage change. However, the deep traps at E_T between w_r^T and w_0^T cannot follow the change instantaneously, that is, compensating majority carrier charge remains trapped in the space charge region between w_r^T and w_0^T. Subsequently, these trapped electrons can be excited into the conduction band and swept away from the space charge region by the applied junction potential. These traps will empty into the conduction band at a rate governed by the temperature - see equation 3.22. The sequence of events for majority carrier traps is shown in fig 3.8. The general expression for the rate of change of trap occupancy between t=0 (the point when voltage is changed) and $t \to \infty$ is given by [3]:

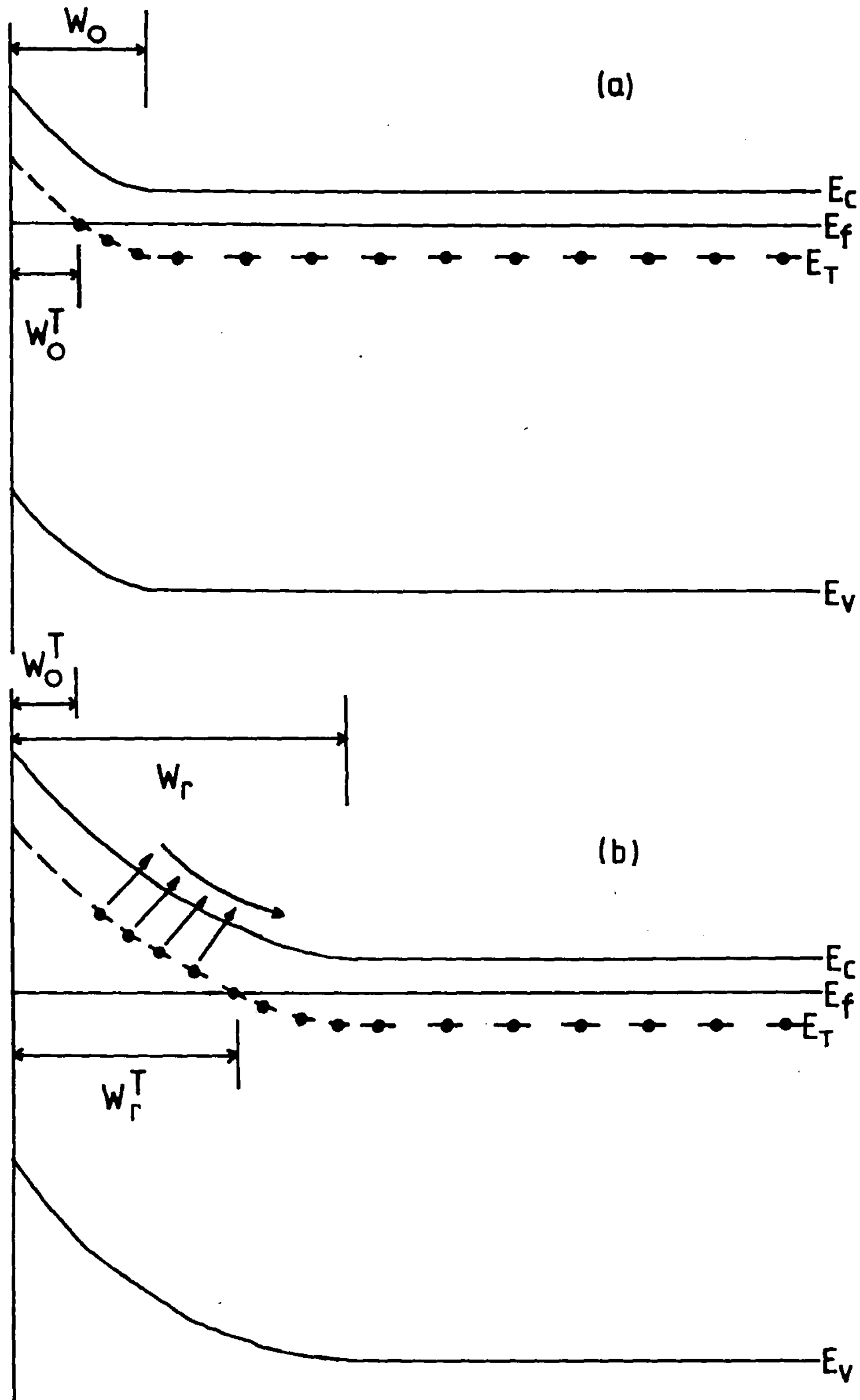


Figure 3.7 Schottky barrier depletion region at (a) zero bias and (b) immediately following a change to a reverse bias V_r

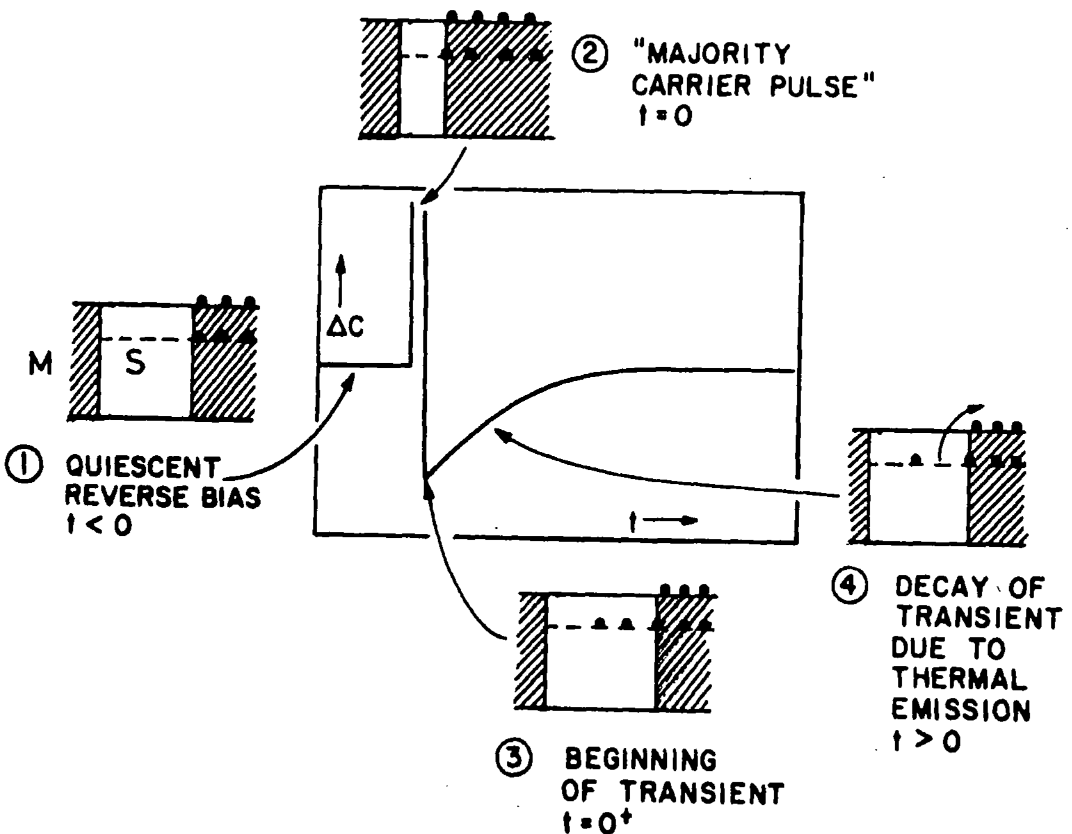


Figure 3.8 Isothermal capacitance transient for thermal emission from a majority carrier trap

$$\frac{dn_t}{dt} = (c_n + e_p^t + e_p^o)p_t - (c_p + e_n^t + e_n^o)n_t \qquad 3.24$$

which for thermal emission of electrons in the dark gives

$$\frac{dn_t}{dt} = - e_n n_t \qquad 3.25$$

As t increases the trap occupancy between w_r^T and w_O^T decreases according to equation (3.22) and the traps become positively charged. In other words, there is an increase in the positive space charge and so the capacitance will increase. The rate of change of the capacitance governed by the increase in the positive space charge density reflects the thermal emission rate of electrons into the conduction band. This is the isothermal capacitance transient shown in fig. 3.8.

In capacitance transient measurements such as DLTS, the sample under a steady state reverse bias undergoes an injection pulse to forward bias, that is, free carriers are injected into the depletion region thereby filling the traps in this region. After removal of the filling pulse the deep traps will empty at a rate dependent upon the temperature according to the rate equation 3.22. This can be monitored by the capacitance transient.

3.4.2 Deep Level Transient Spectroscopy

DLTS was devised by Lang [4] as a sensitive technique for studying deep level defects in semiconductors. It can display the spectrum of traps in a crystal as positive and negative peaks on a flat baseline as a function of temperature. The temperature position of the peak is uniquely defined by the thermal emission properties of the corresponding trap. The sign of the peak indicates whether it is associated with a majority or minority carrier trap. The height of the peak is related to the trap concentration. For a Schottky barrier device majority carriers only can be investigated since only majority carriers can be injected. For minority carriers other techniques are used which for this work were ODLTS and DLOS.

Consider a Schottky barrier on n-type material with a uniform deep donor trap density at E_C-E_T below the conduction band; the device is under a steady state reverse bias. At periodic intervals the device is pulsed to zero bias producing a periodic capacitance transient as discussed in the previous section and shown in fig. 3.8. The emission rate of the trapped electrons in the depletion region after the pulse, is given from detailed balance - see equation 3.22 - E_C-E_T is the thermal activation energy for electron emission into the conduction band. The trap time constant τ is:

$$\tau = 1/e_n \qquad 3.26$$

At low temperature the thermal emission rate from the trap is slow, giving a small capacitance transient and the trap has a long time constant. Conversely, at high temperature the emission rate is high (time constant short). Between, and including these two extremes, the emission rate has an exponential dependence on temperature as indicated in equation (3.22). The capacitance as a function of temperature is shown in fig. 3.9.

For DLTS one makes use of a 'rate window' which is fixed for the experiment. As the temperature is scanned there comes a point when the emission rate coincides with this rate window and one observes a maximum in the change in capacitance with temperature. If the rate window is changed for the scan, the corresponding emission rate will occur at a different temperature. By repeating the experiment for different rate windows, the dependence of the emission rate on temperature can be obtained. The original technique by Lang used a double boxcar for selecting the rate windows; this is shown in fig. 3.10 with the capacitance being monitored at time delays t_1, t_2 and t_1', t_2' after the injection pulse. The normalised DLTS signal S(T), is given by [4]

$$S(T) = (\Delta C(t_2) - \Delta C(t_1)) / \Delta C(0) \qquad 3.27$$

$\Delta C(0)$ is the capacitance change due to the pulse at t=0. For exponential transients

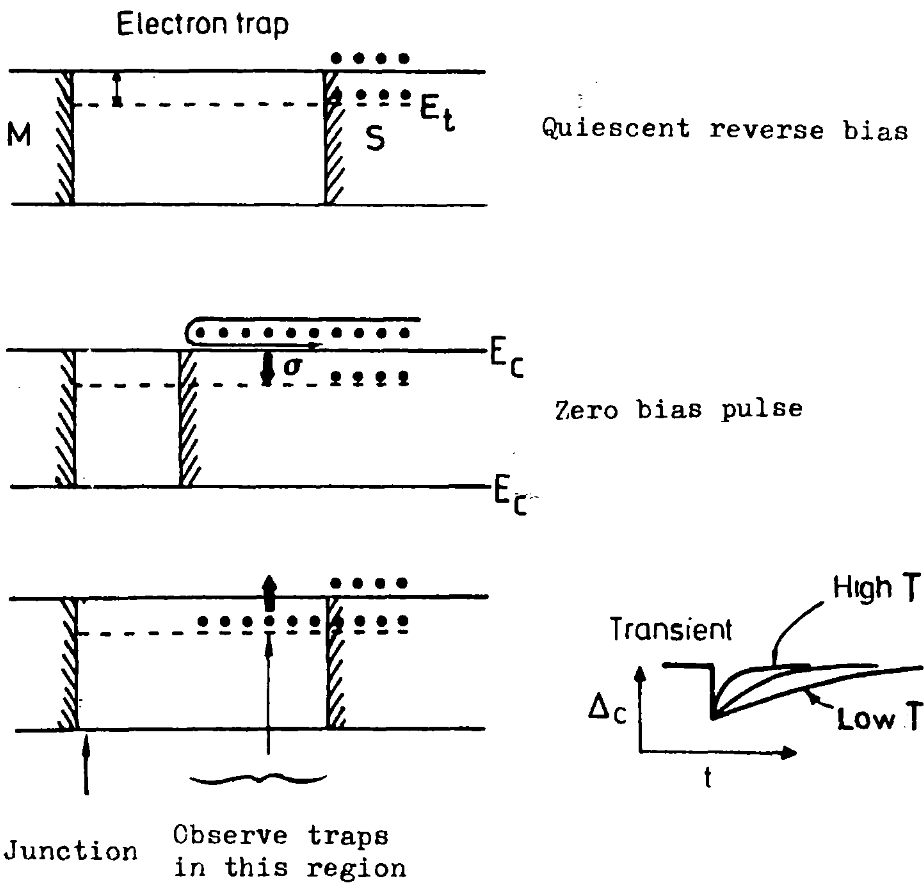


Figure 3.9 Thermal emission from a majority carrier trap showing the temperature dependence of the capacitance transient

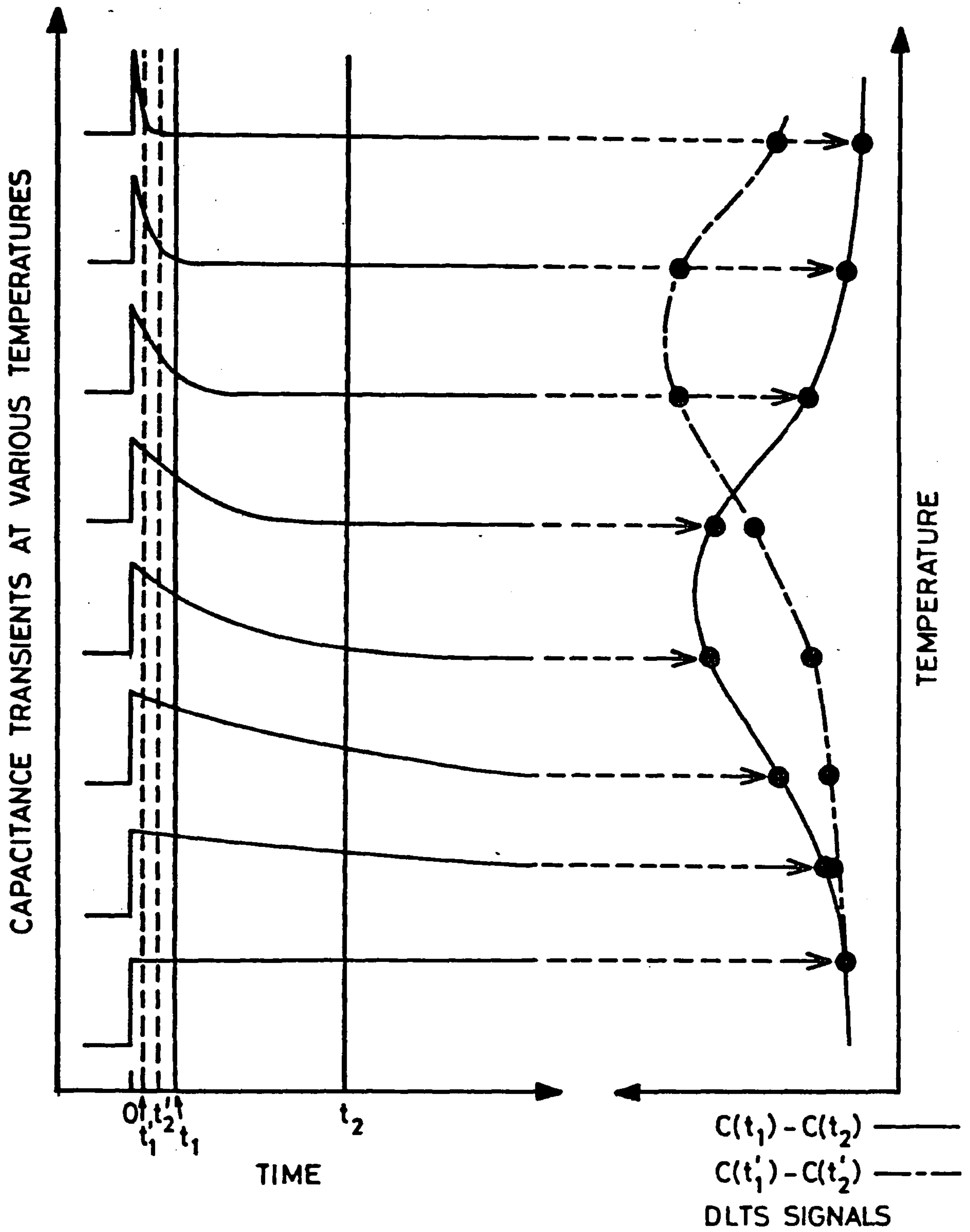


Figure 3.10 Implementation of a rate window by means of a double-boxcar integrator .

$$S(T) = \exp(-t_1/\tau) - \exp(-t_2/\tau) \qquad 3.28$$

The DLTS signal is a maximum when

$$\frac{dS(T)}{d\tau} = 0 \qquad 3.29$$

and so differentiating equation (3.28) and setting it to zero defines the experimentally set time constant

$$\tau = \frac{t_2 - t_1}{\ln(t_2/t_1)} \qquad 3.30$$

The temperature dependence of τ can be determined from equations (3.22) and (3.26), such that

$$\tau = \frac{1}{\sigma_n V_{th} N_c} \exp\left\{\frac{E_C - E_T}{kT}\right\} \qquad 3.31$$

where $v_{th} = (3kT/m^*)^{1/2}$ and $N_c = 2(2\pi m^* kT/h^2)^{3/2}$, so the pre-exponential term becomes $2.8\text{x}10^{-56}/m^* T^2 \sigma_n$. Then

$$\ln(\tau T^2) = \ln\left\{\frac{2.8\text{x}10^{-56}}{m^* \sigma_n}\right\} + \left\{\frac{E_C - E_T}{kT}\right\} \qquad 3.32$$

The first term on the right hand side is in SI units.

So, for each thermal scan at different rate windows one can define τ from equation (3.30), and the temperature position of the DLTS signal maximum from the DLTS spectrum. For the semilog plot $\ln(\tau T^2)$ vs $1/T$ the thermal activation energy can be obtained from the gradient and the capture cross-section

from the y-intercept (see equation 3.32).

As stated above, the height of the DLTS peak reflects the density of traps in the bulk. This may be obtained from the relation [25]

$$N_T = \frac{2\,C_o N_d}{C(V)}\left[1 - \frac{2\lambda}{w(V)}\left(1 - \frac{C(0)}{C(V)}\right) - \left(\frac{C(0)}{C(V)}\right)^2\right]^{-1} \qquad 3.33$$

where C_o is the change in the reverse bias, steady state capacitance after the zero bias filling pulse, C(0) is the zero bias capacitance, C(V) is the capacitance under the steady state bias, λ is the transition region width given by

$$\lambda = \left[\frac{2\,\epsilon_s\,(E_F - E_T)}{q^2 N_d}\right]^{1/2} \qquad 3.34$$

w(V) is the depletion region width under the steady state reverse bias and is given by

$$w(V) = \left[\frac{2\,\epsilon_s\,(V_{bi} - V_r)}{qN_d}\right]^{1/2} \qquad 3.35$$

3.4.3 Optical DLTS

The technique of optical DLTS (ODLTS) has been used for the study of minority carrier traps in semiconductors [5,26]. As with DLTS the capacitance transient is monitored with

temperature; but in this case the electrical pulse is replaced with an optical pulse. The sequence of the experiment is shown in fig. 3.11. With the light on, electrons from the deep traps are emitted into the conduction band. The population of carriers trapped at deep levels in the depletion region will change according to the optical and thermal, electron and hole capture cross-sections. This implies that the occupation function f_T given by

$$f_T = \frac{\sigma_n^o(h\nu)}{\sigma_n^o(h\nu) + \sigma_p^o(h\nu)} = \frac{e_p^o}{e_p^o + e_n^o} \qquad 3.36$$

will be neither 0 nor 1 since at equilibrium, with the light on, traps are being filled as well as emptied. This makes calculating the density of minority carrier traps difficult.

With the light off, hole emission into the valence band will occur with a time constant dependent on the hole emission rate. This will cause a decrease in the positive space charge and hence, produce a transient as shown in fig. 3.11. The analysis is the same as that for DLTS : scans for different time constants defined for the experiment by equation (3.30) will produce ODLTS signal maxima at temperatures where the hole emission rate corresponds to experimentally set time constants. From equation (3.32), following a similar analysis for DLTS, the thermal activation energy and capture cross-section for a hole trap can be obtained.

Using both techniques of DLTS and ODLTS, the majority

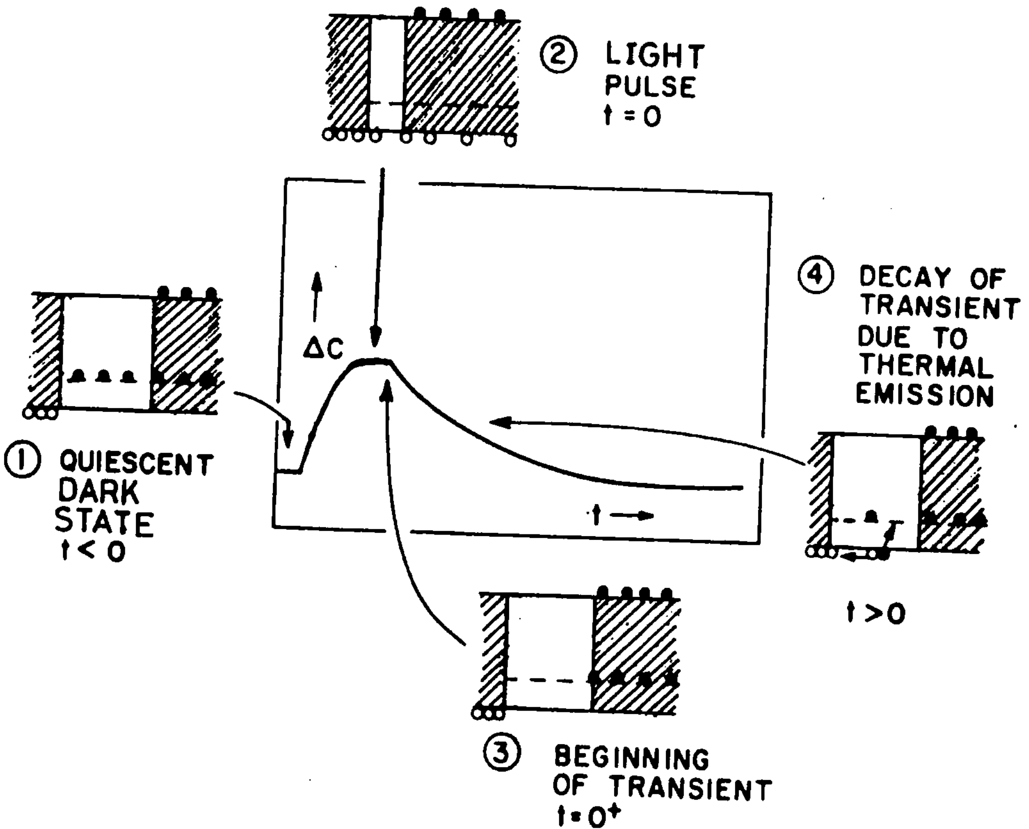


Figure 3.11 ODLTS capacitance transient for thermal emission from a minority carrier trap

and minority carrier traps can be characterised for a semiconductor.

3.4.4 Deep Level Optical Spectroscopy

Deep level optical spectroscopy (DLOS), devised by Chantre et al [6], has been used for the study of the spectral distribution of the electron and hole capture cross-sections for transitions between a deep level and the conduction and valence bands. It is based on photostimulated capacitance transients measured after electrical, thermal or optical excitation of the sample.

When photons are sent into the depletion region, the occupancy of the traps can be changed by optically induced emission of carriers. This will give a change in the capacitance of the junction. At low temperatures, for which thermal emission of trapped carriers can be neglected, the occupancy of a defect level under illumination, with time, is given by:

$$\frac{dn_t}{dt} = - \sigma_n^o \Phi\, n_t + \sigma_p^o \Phi\, p_t \qquad 3.37$$

where σ_n^o and σ_p^o are the optical capture cross-sections for electrons and holes respectively, Φ is the photon flux, n_t is the concentration of traps full of electrons and p_t, those that are empty. For steady state photocapacitance measurements the observed spectrum is a complex function of both electron and hole emission and capture rates. It is

also dependent upon the sweeping rate of the wavelength of the light since the trap time constant can be very large. Another complication may be the presence of several deep levels of widely differing concentrations so that the capacitance response of one may swamp out that of another. In photocapacitance transient measurements the problem again arises that the optical cross-sections cannot be separated.

At t=0 equation (3.37) can be simplified by choosing an initial condition such that only one of the two terms remains. This gives two possible conditions:
(a) If all the centres are filled with electrons then $n_t(0)=N_T$ where N_T is the total density of the traps, and $p_t(0)=0$ and so

$$\frac{dn_t}{dt} = -\sigma_n^o(h\nu)\ \Phi(h\nu)\ N_T \qquad 3.38$$

N_T is a constant, $\Phi(h\nu)$ is the photon flux which is known from a calibration of the monochromator output. The spectral distribution of the capture cross-section $\sigma_n^o(h\nu)$ can be obtained by measuring the initial derivative of the capacitance transient since [6]

$$\left(\frac{d\Delta C}{dt}\right)_{t=o} \propto \left(\frac{dn_t}{dt}\right)_{t=o} \qquad 3.39$$

just after the excitation pulse.
(b) If at t=0 all the levels are filled with holes then $p_t(0)=N_T$ and $n_t(0)=0$. This gives

$$\frac{dn_t}{dt} = \sigma_p^o(h\nu)\ \Phi(h\nu)\ N_T \qquad 3.40$$

With the same analysis as in (a) the spectral distribution for $\sigma_p^o(h\nu)$ can be determined.

The experimental procedure used in this work consisted of applying majority carrier pulses to a Schottky barrier on an n-type semiconductor while the wavelength of the light was slowly scanned. This was the situation in condition (a) above so that the centres fill with electrons during the excitation pulse. The subsequent plot of $(d\Delta C/dt)$ at $t=0$ corrected for photon flux against photon energy, gave the spectral distribution of the electron optical capture cross-section for each trap.

Chantre et al [6] have proposed a theoretical model for the energy dependence of the photoionisation cross-section. Unlike other models, such as those suggested by Lucovsky [27], and Kopylov and Pikhtin [28], it can predict the behaviour far from the threshold energy. Chantre et al gave the O level in GaAs as an example; this shows an initial increase followed by a sudden drop in the optical cross-section for holes, as shown in fig. 3.12. The Lucovsky and Kopylov models use a unique conduction band minimum which for this particular case is not applicable due to the complexity of the transitions involved. Other models have been proposed that have taken a similar approach to that of Chantre such as Banks et al [29] but these require experimental verification. Many functions could fit the

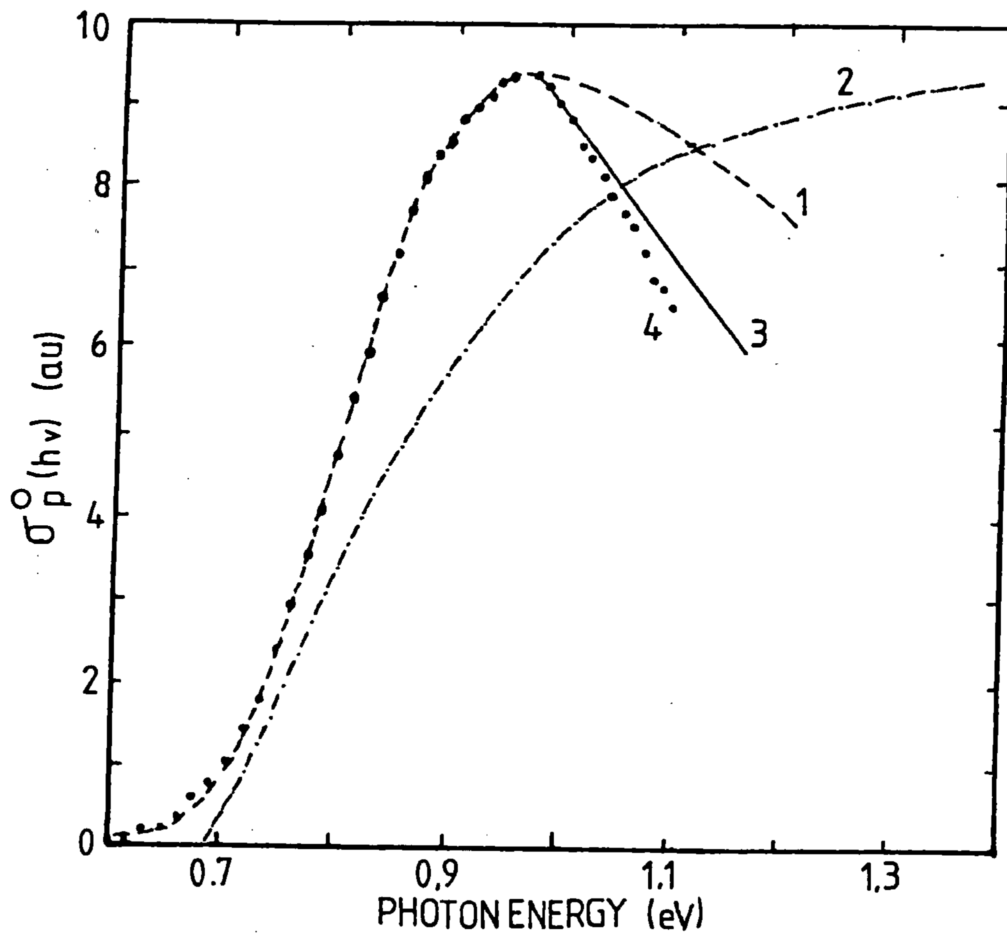


Figure 3.12 Theoretical fits to the DLOS data (4) for the O level in GaAs using (1) Kopylov model (2) Lucovsky model and (3) Chantre model [6]

capture cross-section data that stops at the maximum in the curve. So for a reliable test of the physics of the proposed model a fit to a wider spectral range must be considered as in that by Chantre et al. The expression used in the present work for fitting DLOS data is based on the Chantre function

$$\sigma \propto \frac{y - 1}{y(y - 1 + k)^2} \qquad 3.41$$

where $y = h\nu / E^o$ (E^o is the threshold energy), and $k = \hbar^2 \alpha^2 / 2m^* E^o$ (α is related to the extent of the defect state, m^* is the effective mass).

DLOS was used in conjunction with DLTS and ODLTS to give a more complete characterisation of the deep levels. The thermal techniques of DLTS and ODLTS enabled temperatures to be chosen so that thermal processes for a deep level under investigation by DLOS could be neglected.

3.4.5 Non-exponential Behaviour

3.4.5.1 Field Dependent Emission

There is a general assumption that the emission rate is not dependent upon the electric field in the depletion region. However, there is strong evidence that in some cases the rate does depend on the applied bias voltage [4,30,31]. The effect of the electrostatic field would be to lower the trapped carrier potential barrier, thereby enhancing the thermal emission rate. Several models have been proposed - Poole - Frenkel effect [32], tunnelling [33] and

phonon-assisted tunnelling [34] (see fig. 3.13). The strength of the field varies linearly through the depletion region. If the field is nonuniform then the emission rate will also be spatially nonuniform leading to a non-exponential capacitance transient.

3.4.5.2 Transition Region

The analysis of capacitance transients assumes that the free carrier tail in the neutral region decays abruptly to zero at the depletion region/neutral bulk interface. However, the free carrier tail does extend into the depletion region [35] and the effect of this on subsequent measurements has been examined [36-39]. Figure 3.7 shows a Schottky device with a uniform density of one deep trap under reverse bias. After applying a refilling pulse the traps lying in the region $w_0^T < x < w_r^T$ will thermally empty into the conduction band. The traps lying between w_r^T and w_r are full. They can also empty into the conduction band at a rate exponentially dependent upon the depth below the Fermi level [24]

$$e_n = \sigma_n V_{th} N_c \exp(-(E_F - E_T)/kT) \qquad 3.42$$

At thermal equilibrium the emission and capture rates are the same at w_r^T. As a result of the dynamical process in this region, the time constant for these traps will be much longer than those in the region $x < w_r^T$. The capacitance transient due to the fast exponential traps will have superimposed on it another transient with a longer time constant due to the

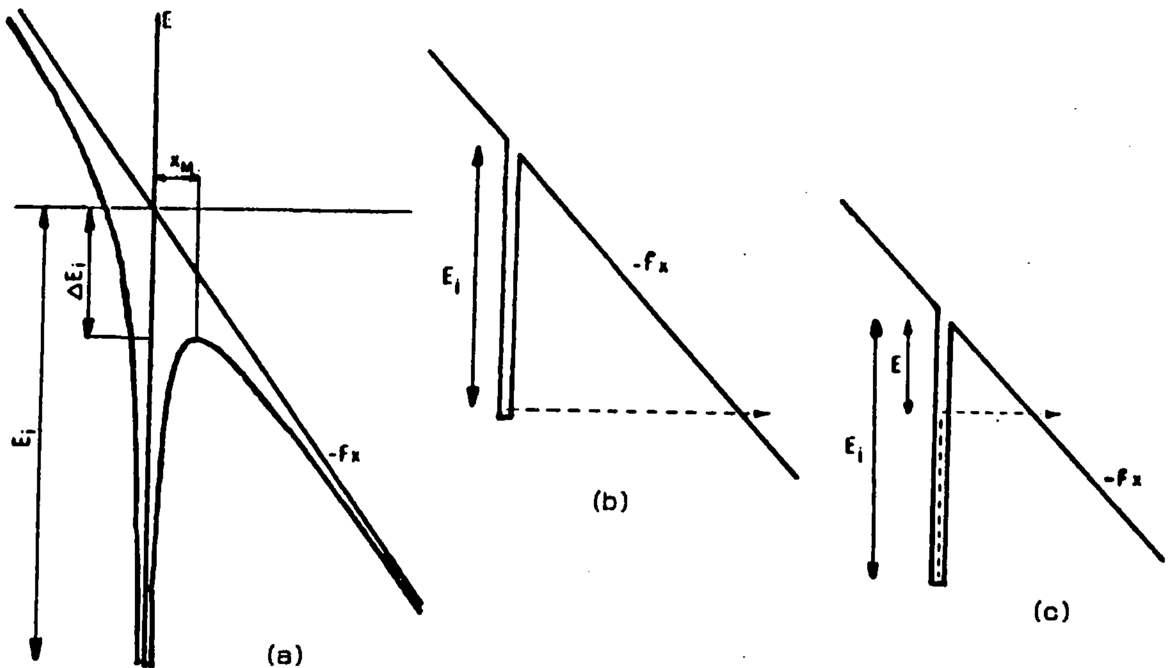


Figure 3.13 Possible mechanisms for electric field enhanced carrier emission (a) Poole-Frenkel effect (b) tunnelling (c) phonon assisted tunnelling

emission and capture processes between $w_r^T < x < w_r$. This effect has been used by Zilberstejn [36] to obtain trap activation energies and capture cross-sections from isothermal refilling experiments.

For DLTS a sufficiently large, steady state reverse bias is applied to minimise this effect in the transition region. For DLOS this is not important when all the centres are filled with electrons since $p(x,0) = 0$ for whatever value of x. However, when all the centres must be filled with holes, the free carrier tail extending into the depletion region makes this condition unattainable. Consequently, the energy spectrum of the hole electron capture will have a contribution from the electron capture cross-section.

3.4.5.3 Multi-level System

If the emission rates of two traps are close together then the resultant capacitance transient will consist of these superimposed. This may give a non-exponential transient. The effect for one trap will be dominant if the other trap is of a much lower density. For a broad distribution of states in the energy gap of the semiconductor a standard DLTS analysis may not be appropriate as a result of a nonuniform energy distribution of states [3].

3.4.5.4 Large Trap Concentrations

For deep level concentrations close to or greater than the free carrier concentrations the capacitance transient will be nonexponential [25]. Consider a Schottky diode under reverse bias with a uniform density of traps N_T, $(E_C - E_T)$ below the conduction band. If a refilling pulse is applied to the sample, the electron occupancy n_t of the traps in the depletion region has a time dependence [40]

$$n_t = N_T \left[1 - \exp(-t/_\tau)\right] \qquad 3.43$$

As n_t decreases from N_T to zero, the capacitance C(t) increases with time until an equilibrium value $C(\infty)$ is reached. The difference $\Delta C(t) = C(\infty) - C(t)$ may be expressed as [40]

$$\frac{\Delta C(t)}{C(0)} = \left\{\left(1 + \frac{N_T}{N_d}\right)^{1/2} - \left(1 + \frac{n_t}{N_d}\right)^{1/2}\right\} \qquad 3.44$$

Combining these two equations and assuming that $N_T \ll N_d$ then [41]

$$\frac{\Delta C(t)}{C(0)} = \frac{1}{2}\frac{N_T}{N_d}\exp(-t/_\tau) \qquad 3.45$$

This is the classical exponential dependence used by Lang [4] for the DLTS analysis. However, if the trap density is close to or greater than the free carrier concentration then the

capacitance transient will not follow the exponential relation - equation 3.43. Morante et al [42] have shown that for large deep to shallow trap ratios in GaAlAs the thermal emission rates from deep levels can vary with the applied electric field as described in section 3.4.5.1. This leads to a further possible condition for nonexponential behaviour.

3.5 Summary

Space charge capacitance techniques such as those described above provide important information about deep level defects in a semiconductor. The initial consideration is to obtain a space charge region. This is easily facilitated and most convenient by applying a Schottky barrier contact. In the case of an n-type semiconductor the barrier has a positive space charge and is depleted of free carriers (electrons). Assuming the depletion approximation the capacitance of the space charge region is analogous to that of a parallel plate capacitor and is given by $C = \epsilon_s/w$ where ϵ_s is the semiconductor dielectric constant and w the barrier depletion width. The depletion region width is voltage dependent and so, therefore, is the capacitance. Indeed from this relationship the free carrier concentration and the barrier height may be determined (see equation 3.17).

As has been discussed, the presence of deep levels may affect the measurement of the capacitance depending on whether the test signal frequency is greater or smaller than the emission rate from the traps. The usual condition is that where the traps cannot respond instantaneously to the

test signal.

A capacitance transient can be observed when the traps cannot follow a sudden change in the reverse bias to a Schottky device. It is the time dependent response by the traps that gives rise to the transient. For an isothermal transient the emission rate from the traps uncovered in the depletion region after an increase in reverse bias is given by equation 3.22 obtained from detailed balance. For DLTS and ODLTS which involve measuring the temperature dependence of the capacitance transient, the thermal activation energy and capture cross-section of a deep level can be obtained as discussed in section 3.4.2.

Nonexponential capacitance transients have been observed and various explanations have been proposed. Possible sources of this behaviour may be field dependent emission of carriers from the traps; the transition region may be large compared to the depletion region so that emission and capture processes within this region are superimposed on the normal emission process of the uncovered traps after a filling pulse; for a multilevel system the exponential transients from different trapping levels may be superimposed; and if $N_T/N_d \gg 1$ then the time dependence of the capacitance does not have a simple exponential form as required for the DLTS analysis.

DLTS, ODLTS and DLOS were the main techniques used in this study of deep level defects. The materials investigated were selected II-VI semiconductors with reference to the

possible effects deep levels may have on the characteristics of a device.

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CHAPTER 4

EXPERIMENTAL TECHNIQUES

4.1 Introduction

The aim of this work was to characterise the main electron and hole trapping centres in various II-VI materials using transient capacitance techniques. Deep level transient spectroscopy (DLTS) formed the basis of the work around which other experiments were designed - ODLTS, DLOS, capacitance-voltage and capacitance-temperature measurements. A description of how these techniques were implemented is given in this chapter. In addition to these measurements, other important considerations were crystal growth, compostion analysis for the ternary compound $Zn_xCd_{1-x}S$, structural analysis and electron microscopy in order to characterise the materials studied and perhaps to correlate these results with other observations. A brief discussion of these techniques is given.

4.2 Crystal Growth

4.2.1 The Clark-Woods Method

The technique used for the growth of single crystal CdS and (ZnCd)S was developed by Clark and Woods [1,2]. For CdS, a charge was initially prepared by passing a stream of argon over heated poly-crystalline material; this gave platelets

which were used for the growth of the single crystals. The charge was contained in an evacuated sealed tube which was held vertically in the growth furnace (see fig.4.1) and maintained at a temperature of 1150C. A reservoir of Cd or S, held in a long tail tube, was connected to the growth ampoule via a narrow orifice. This maintained a constant vapour pressure of one of the constituent elements over the evaporating charge. As the ampoule was pulled through the furnace and the growth gradient developed, the various vapour species diffused to the cooler regions resulting in supersaturation of the vapour and growth of the crystal. For CdS a boule 3cm long and 1cm in diameter took about one month to grow.

The crystal grew in an oriented manner although from boule to boule it was not necessarily along the same crystallographic axis. To eliminate any effects in measurements which may be due to devices made on different crystallographic planes all the crystals were oriented along the c-axis by X-ray back reflection. After this the boule was cut into dice typically with dimensions 1mmx3mmx3mm with the c-axis lying parallel with the short edge.

4.2.2 The Piper-Polich Method

The second method of crystal growth was based on a technique developed by Piper and Polich [3]. This method was used for the growth of $Zn_xCd_{1-x}S$, ZnS and CdTe. The arrangement of the system used is shown in fig. 4.2. An open silica tube was loaded into a tubular furnace so that

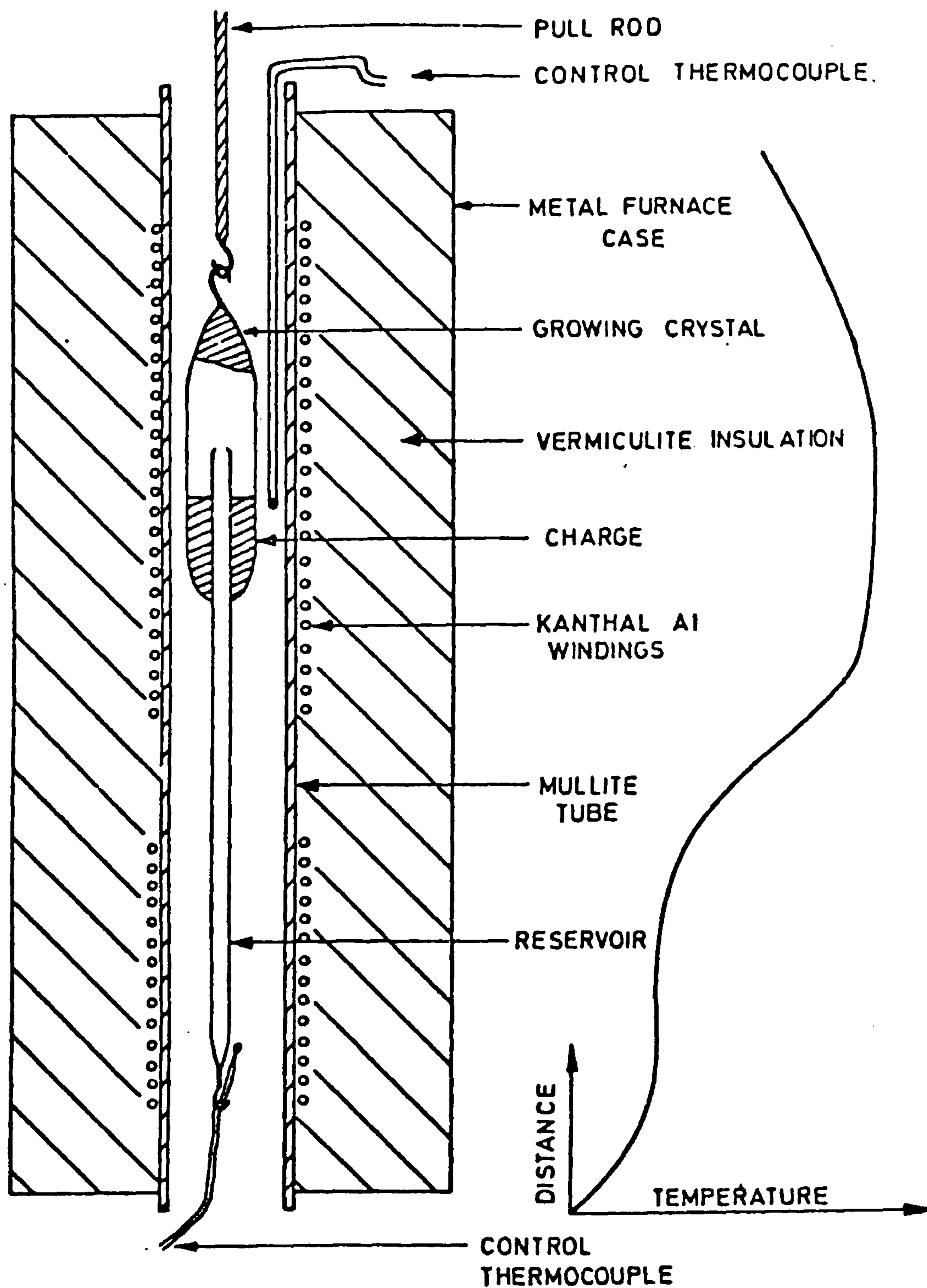

Figure 4.1 The Clark-Woods method [1, 2] for the growth of II-VI crystals

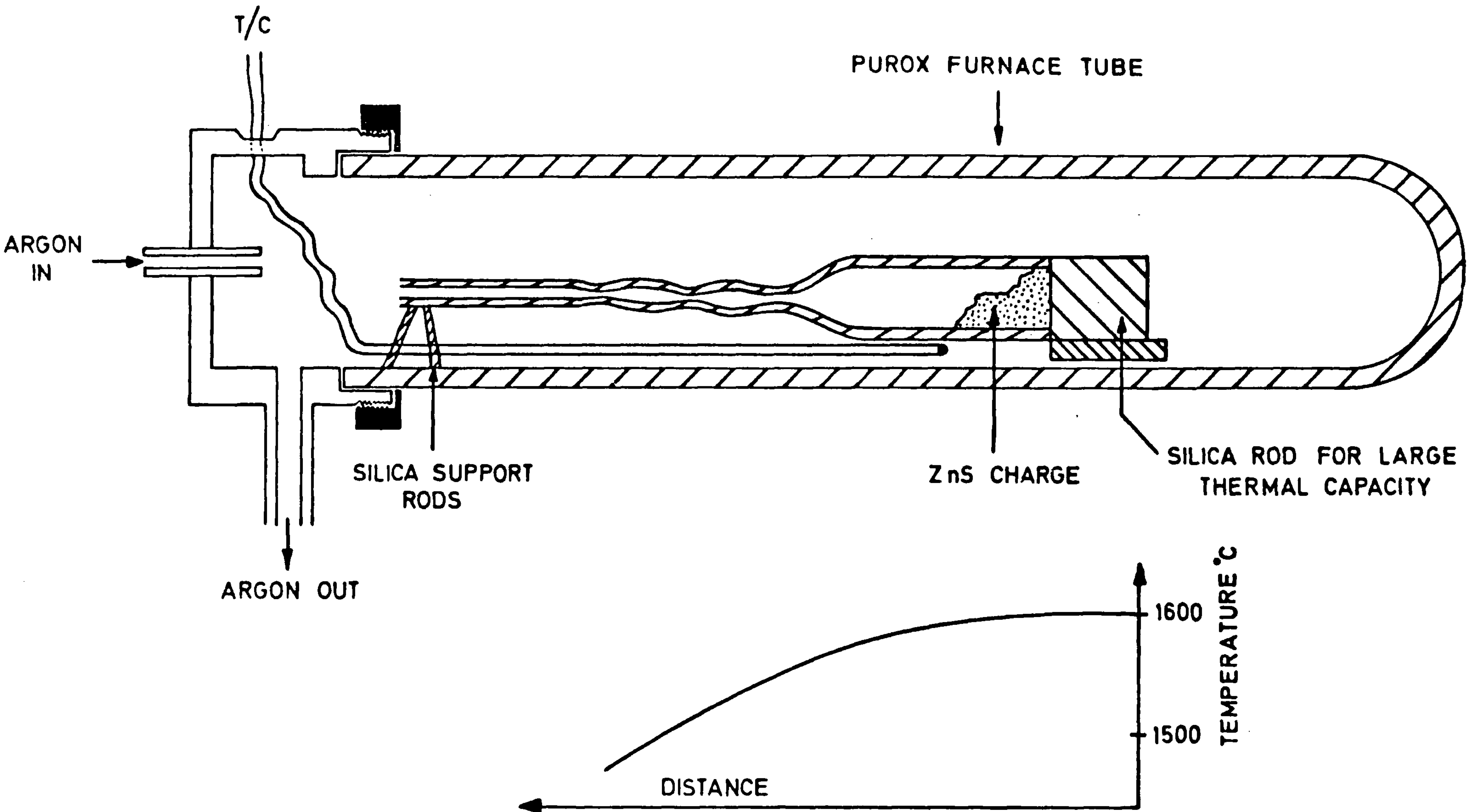

Figure 4.2 The Piper-Polich method [3] for the growth of II-VI crystals

the charge was near the flat region of the temperature profile. The temperature profile required depended upon the material to be grown - that for ZnS is given in fig. 4.2. Argon was admitted via a needle valve, passing through the system at a rate of 100ml/min. As the material was transported to the cooler end of the capsule, condensation occurred at progressively hotter constrictions with the result that the growth chamber was sealed off. This procedure allowed unwanted volatile impurities to escape prior to crystal growth. Generally a run lasted 2-3 days which included a cool down period of 24hrs. The boules were 2-4cm long and 1cm in diameter. Again the boules were cut into dice suitable for device fabrication.

4.3 Junction Formation

One of the main points about forming an electrical barrier on a semiconductor is surface preparation and cleanliness. In the case of CdS the dice were initially degreased in i-propanol vapour to remove any grease from the cutting procedure. They were polished with 5μ alumina to remove surface work damage, and then with 1μ alumina to give a scratch free surface. Concentrated HCl was used as the etchant [4,5]; this distinguished the S and Cd faces of the material. Ohmic contacts were formed by annealing In on one surface of a dice at 180-200C in an argon atmosphere [4]. A Schottky barrier was formed by evaporation of a Au dot on the opposite face. Device characteristics were obtained from current-voltage and capacitance-voltage measurements.

4.4 X-ray Diffraction

A Philips X-ray diffractometer with a Co source ($\lambda_{k\alpha}$ = 1.789Å) was used to determine the lattice parameter and hence composition of (CdZn)S. This showed reflections due to the (0001) planes since the crystals were oriented along the c-axis. This enabled easy measurement of the lattice parameter c_o since for hexagonal material [6]

$$\frac{1}{d^2_{hkl}} = \frac{4(h^2+hk+k^2)}{3a_o^2} + \left\{\frac{l}{c_o}\right\}^2 \qquad 4.1$$

which reduces to

$$c_o = ld \qquad 4.2$$

for (0001) reflections.

4.5 Electron Microscopy

The surface topographies of single crystal and polycrystalline films of CdS were investigated using a Cambridge Stereoscan 600 scanning electron microscope (SEM). The cross-section of some of the polycrystalline films was imaged to assess film thickness and degree of grain growth. For this type of study the SEM was operated in secondary emission mode. However, one of the investigations carried out, which will be discussed in the next chapter, was based on electron beam induced current (EBIC). This was used to image electrical activity around extended defects at a

barrier contact. Electron-hole pairs were generated by the electron beam and collected at contacts applied to the sample (Schottky barrier, Ohmic contact). At an electrically active extended defect, the current collection efficiency may differ from the bulk. If such is the case one can image an EBIC contrast. The SEM could provide a narrow beam (~500A) giving a good spatial resolving power of localised differences in collection efficiency. When compared with the secondary emission image, electrically active features could be identified.

For studying the crystallographic properties of polycrystalline materials a JEM120 transmission electron microscope was used in RHEED mode; the machine was operating at 100kV. The lattice planes of a crystal diffract the electrons according to the Bragg condition:

$$n\lambda = 2d_{hkl}\sin\theta \qquad 4.3$$

The wavelength λ is dependent upon the accelerating voltage, d_{hkl} is the interplanar spacing and θ is the Bragg angle between the incident beam and the atomic planes. RHEED was principally used to determine the phase and crystallinity of the thin film CdS.

4.6 The DLTS System

One of the main aims of this study was to design an automated DLTS system to capture, digitise, and store the capacitance transient for post scan analysis. This would

have the primary advantage over the original double boxcar DLTS rig based on Lang's system [7,8], of reducing the number of temperature scans on a sample from a minimum of 3 to 1, thereby eradicating the possibility of device deterioration during its analysis.

4.6.1 Design and Operation of the DLTS Rig

The central feature of an automated experiment is a computer which takes over the arduous, manual operation of data collection. In this case a Commodore PET 4032 was used, which had an IEEE interface to control such devices as printer, plotter, digital voltmeter and disc drive, and a user port for user designed interfaces. See fig. 4.3 for the schematic diagram of the system.

The sample under investigation was housed in an Oxford Instruments helium gas exchange cryostat. The sample was glued to a copper plate with Ag paste; the copper plate was bolted to the sample rod of the cryostat. This served as the back contact to the sample. The top connection was made with a phosphor-bronze spring contact.

The temperature was controlled with a DTC2 temperature controller. The capacitance was measured on a Boonton 72B differential capacitance meter. A bias was applied from a pulse generator and the subsequent capacitance transient was captured by a sampling DVM (Hewlett-Packard 3456A). The triggering for the measurement cycle was under computer control through the interface on the user port which gated

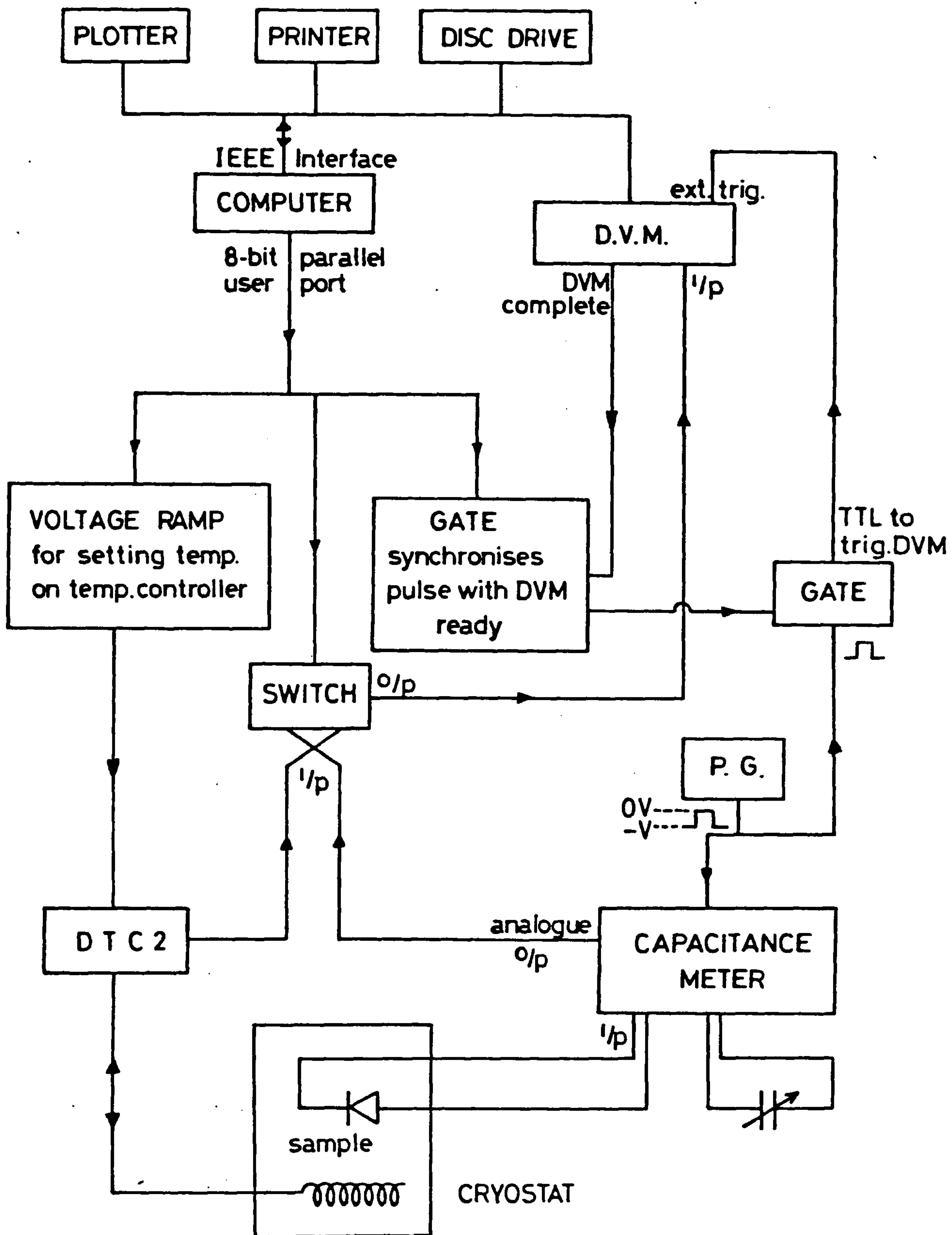

Figure 4.3 Schematic diagram of the DLTS system

the 'DVM start' with the pulse generator pulse.

Initially, the computer requested run details : sample name and number, boule number, date, initial and final temperatures, and heating rate. The axes for an on-line plot of a DLTS spectrum for a given time constant were plotted by the digital plotter (Hewlett-Packard 9872C). The DTC was set to the start temperature using the interfaced voltage ramp (see fig. 4.3). Timing and bias information were given to the computer (bias, pulse height, pulse width, pulse repetition period and time constant). On a start instruction the run commenced.

The gated triggering pulse to the DVM triggered the measurement as soon as the PG pulse was removed from the sample. The steady state bias to the sample was generally between -1 and -5V; the sample was pulsed to zero bias in order to fill deep traps near the junction. The pulse width was of the order of 20msec. One problem was that the DVM required a TTL pulse to start the measurement and so a unit had been inserted which gave a gated TTL pulse output to the DVM once triggered by the pulse generator (see fig. 4.3).

The DVM sampled 8 transients 16 times at each set temperature. The first 4 transients were sampled at 4msec intervals and the second 4 at 40msec intervals. The 128 data points were stored by the DVM as they were being taken and at the end of the measurement, the data was sent to the computer. The data for the 2 sets of 4 transients was averaged to remove some noise and stored on floppy disc.

Applying a digital filter to a set of data for a given time constant, again to reduce noise, a point in the DLTS spectrum was displayed on the digital plotter. The set temperature was incremented by 1K and the measured temperature was checked and ramped until it reached the set temperature. The measurement cycle was then repeated. The whole sequence took about 2mins, so a typical temperature scan of 80-380K would take about 9hrs. On completion of the run a print-out of the run details was obtained from the printer.

Although the system was automated care had to be taken when setting up the experiment; this especially concerned setting the triggering sequence and levels correctly and ensuring temperature stability before the start of the run.

4.6.2 Data Processing

The simplest method for data processing was to select various time constants and plot several DLTS spectra from the stored data. For a particular trap which gave a DLTS response, a temperature shift in the peak position was observed for different time constants. From this information an Arrhenius plot was drawn, and the trap activation energy and capture cross-section were calculated. The principles of the method of analysis are given in chapter 3.

To minimise the effect of noise in the system on the DLTS signal, the capacitance data was filtered using a simple digital filters

$$C''(t) = (1 - a)C'(t) + aC(t) \qquad 4.4$$

where $C'(t)$ is the filtered capacitance value for the previous transient at time t, $C(t)$ is the capacitance of the present transient at time t, $C''(t)$ is the filtered value to be determined for the capacitance at time t for the present transient, and a is the filter factor ($0<a<1$). To obtain some indication as to how well the trap was behaving with respect to the emission process - that is whether or not it was exponential - selected capacitance transients were curve-fitted to the function

$$C = P1 + P2\exp(-t/P3) \qquad 4.5$$

where C is the capacitance, t the time and P1, P2 and P3 the estimated parameters (P1 - offset, P2 - scaling parameter, P3 - time constant).

4.6.3 Optical DLTS

Data obtained from DLTS could only give information for majority carrier traps. Optical DLTS can overcome this problem where, say, for n-type material traps below the Fermi level and close to the valence band can be emptied by light of the appropriate wavelength. If then the light is removed the traps will thermally refill; this effect can be observed in the form of a capacitance transient [9] (see chapter 3).

In addition to the basic DLTS equipment, several light sources and a means of chopping the light to the sample were

required. Chopping was implemented using an acousto-optic modulator (Oriel AOM40); this has a response time of ~150nsecs, which is well within the capacitance meter response of 1msec. The drive electronics for the modulator was an IntraAction ME-40G AOM Signal Processor.

The modulator was used to chop laser light to the sample in the cryostat. Two lasers were available - an Argon ion laser (Spectra Physics 162A) operating at 489nm and a He-Ne laser (Griffin) at 633nm. The modulator diffracted the light beam and when the carrier signal from the drive electronics was pulsed using the pulse generator the diffracted beams were chopped. These diverging beams were spread using mirrors and the chopped light was focussed onto the end of an optic fibre. This was coupled to the cryostat and the light focussed onto the sample (see fig. 4.4).

Two other light sources were used: a high intensity LED with peak output at 650nm and a 'sweet spot' which peaks at 820nm; these were chopped by pulsing from the pulse generator. They had a response time of the order of ~100-200nsec again well within the response time of the capacitance meter. In addition, they could be coupled directly to the optic fibre and therefore, to the cryostat as was mentioned in the case of the laser operation of optical DLTS. Using the method of optical DLTS, information concerning minority carrier traps has been obtained.

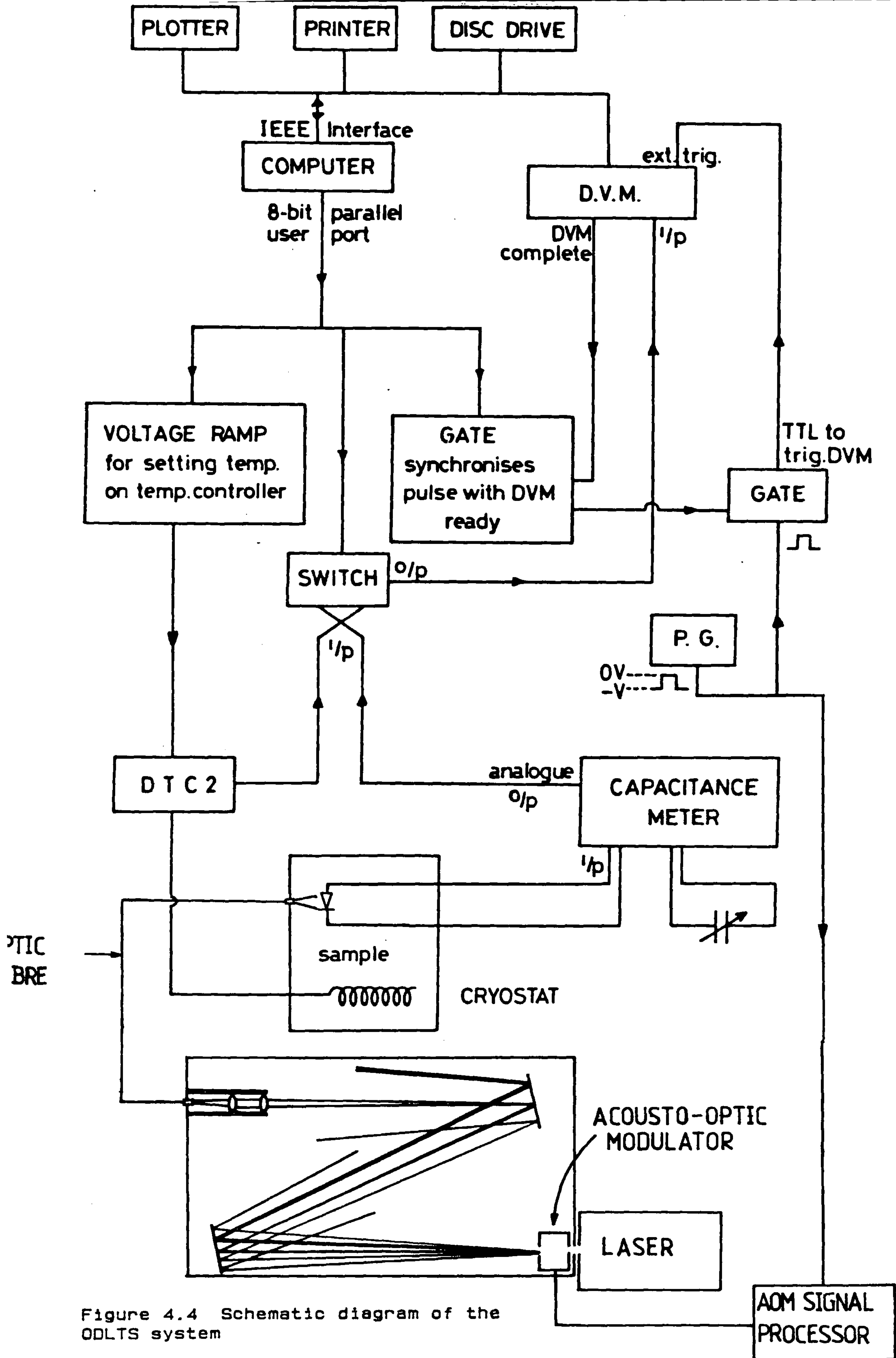

Figure 4.4 Schematic diagram of the ODLTS system

4.7 Deep Level Optical Spectroscopy

Electrical DLOS [10] was used to characterise the optical depth of traps below the conduction band by determining the spectral distribution of the optical capture cross-section for electrons. This gave information about traps that could be correlated with the thermal techniques of DLTS and ODLTS or traps that were near the middle of the band gap which were inaccessible to these other methods.

The experiment was based around the DLTS system but without the temperature control since this was an isothermal experiment. The sample was mounted in a cold finger cryostat which could be maintained at room or liquid nitrogen temperature depending upon the experimental requirements. A Barr & Stroud monochromator was used to give monochromatic light from a 250W quartz-halogen lamp. The experimental set-up is shown in fig. 4.5.

Initially run details were entered on the computer (date, sample name and number, initial optical energy, pulse height, width and repetition period). The monochromator was set to the initial optical energy and a capacitance transient was obtained in the manner described for DLTS. This information was stored on floppy disc. The monochromator was manually set to the next optical energy and a further transient taken and stored. This was repeated over the required energy range. The DLOS spectrum was plotted after the run - this was a plot of the capacitance difference on each transient for times t1 and t2 close to t=0, the time

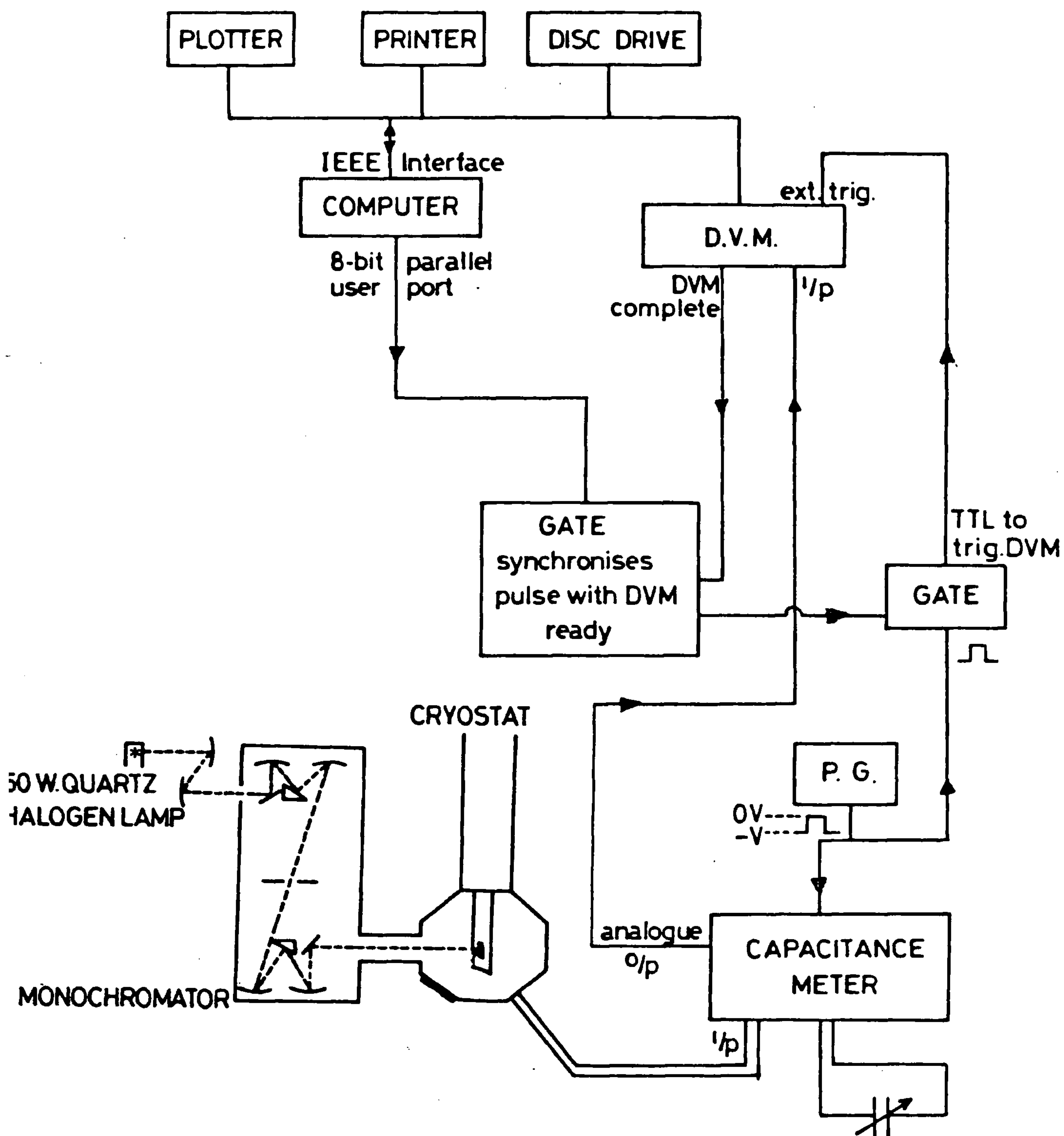

Figure 4.5 Schematic diagram of the DLOS system

when the refilling pulse was removed. This was corrected for the lamp response.

A theoretical function was defined by Chantre et al [10] that could be numerically fitted to the DLOS data. Equation 3.41 gives the simplified version of this function as applied to the experimental results here. Indeed, the function used for the numerical fit was

$$\sigma(h\upsilon) = \frac{P1\ (h\upsilon - P2)}{h\upsilon\ (h\upsilon + P3)^2} \qquad 4.6$$

where $\sigma(h\upsilon)$ is the optical capture cross-section, $h\upsilon$ the optical energy, P1 a scaling parameter, P2 the threshold energy and P3 a fitting parameter but dependent upon the spatial extent of the defect state. Using a nonlinear least squares fit for the DLOS data the optical threshold energies for electron emission from trapping levels could be determined.

4.8 Capacitance-Voltage

Capacitance-voltage measurements were carried out as a routine technique. The voltage supply was interfaced to the computer via the user port and could give an output between -10V and +10V. Temperature control was available so that C-V measurements could be carried out at any temperature within the limitations of the cryostat. The bias voltage was incremented or decremented as required in 5mV steps at a rate of about .2V/min. The controlling program firstly gave a C

vs V plot and, subsequently, $1/C^2$ vs V plot on the digital plotter. From equation 3.18, the free carrier concentration was calculated. Finally, run details and results were printed out.

4.9 Capacitance-Temperature

Capacitance as a function of temperature was measured for most samples routinely. The temperature was ramped under computer control as described in section 4.6 for DLTS and the absolute capacitance measured via the Boonton analogue output on the DVM. Five measurements were taken at each temperature sent to the computer, averaged to remove noise and a point plotted on the digital plotter. At the end of the run the data was stored on floppy disc and a print out of the run details was obtained.

4.10 Summary

The aim of this thesis was to characterise the main electron and hole trapping centres in CdS, (ZnCd)S, ZnS, CdTe and CdSe single crystals and polycrystalline CdS films. The techniques used for this study, and discussed above, were based on capacitance transient measurements - DLTS, ODLTS, DLOS. The first two techniques gave information about the thermal activation energy and capture cross-section for a particular trap. DLOS gave the energy distibution of the electron optical capture cross-section; this gave energy

thresholds which corresponded to optical depths of traps below the conduction band.

Various other techniques were used to characterise the materials studied and to correlate with and account for the DLTS, ODLTS and DLOS responses. These were X-ray diffraction, scanning electron microscopy (secondary and EBIC modes) and device capacitance as a function of voltage and temperature. The results based on these techniques are presented and discussed in the following chapters.

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CHAPTER 5

SINGLE CRYSTAL CdS

5.1 Introduction

Extensive work over the past two decades has been carried out on CdS in an effort to characterise the deep trapping centres and to identify their origin. Possible causes include intrinsic point defects (interstitial atoms, vacancies, antisite defects) as well as complexes formed by these defects. Techniques such as thermally stimulated current [eg. 1-6], admittance spectroscopy [7] and DLTS [8-16] have been used. In the case of thermally stimulated current there is much scatter in the reported results illustrating their questionable nature. Consequently, correlating the results from this technique with those from others is difficult. In more recent years, the use of DLTS for the study of CdS has proved more consistent and a catalogue of deep electron traps is being built up [8-16].

In this study, DLTS has been used to investigate the main electron trapping centres in single crystal CdS and the results presented here correlated well with those obtained by others. In addition the main hole traps were investigated using ODLTS and DLOS. There are few reported results using ODLTS [13,16] and none for DLOS. The results on the undoped material were also used as a basis for the investigation of

CdS doped with copper and tellurium.

It is well known that copper forms acceptor states in CdS [13,17-19]. They can only be eradicated with difficulty and usually their presence arises from residual copper impurity from the growth procedure [20]. In fact copper states were observed in almost all the samples studied including those that were 'undoped'. One important area concerning copper impurities is that they may also be created during the optimising heat treatment of the CdS/Cu_2S solar cell by diffusion of copper from the Cu_2S into the CdS [21,22]. In the present work the copper states were investigated using ODLTS and DLOS on Au/CdS:Cu Schottky devices and CdS/Cu_2S heterojunctions. These results have been correlated with those obtained by transient photocapacitance techniques [17-19].

Tellurium is an isoelectronic, substitutional impurity in CdS [23]. The interest in CdS:Te lies in the fact that it has a high luminescence efficiency for electron-hole recombination at Te traps [24,25]. In addition, there has been much recent interest in sintered, thin-film CdS/CdTe junctions as low cost solar cells [26,27]. During the sintering process Te may diffuse across the junction into the CdS thereby introducing deep level defect states that may reduce the device efficiency. DLTS, ODLTS and DLOS have been used here to study tellurium doped CdS in an effort to characterise the defect states that this isoelectronic impurity may introduce.

5.2 Electron Traps in Undoped Single Crystal CdS

5.2.1 Material Characteristics

The CdS used in this study was grown by the vertical transport growth technique described in section 4.2. The material obtained from different boules (519, 537, 647, 732, 759, 779, 808) displayed dark resistivities in the range 10Ωcm to 1MΩcm. Most of the samples studied had values in the 10Ωcm to 2kΩcm range although a photoconductive sample (ρ(dark) 1MΩcm) was investigated. To reduce the resistivities for device purposes CdS dice, previously degreased and etched, were annealed in cadmium vapour. For this process they were sealed in evacuated silica ampoules and heated at 600C (vapour pressure of cadmium was about 0.1atm) for two days; they were subsequently quenched to room temperature in water. Some low resistivity CdS samples were annealed in sulphur vapour at 400C for 24hrs for comparison with the Cd annealed material; again the samples were quenched. Schottky diodes were made on the dice as described in section 4.3. From the capacitance-voltage charateristics the free carrier concentrations were found to be in the range 10^{15} -10^{17} cm^{-3}. Fig. 5.1 summarises the properties of the samples studied.

5.2.2 DLTS Measurements

DLTS was used to investigate the thermal trapping parameters of deep donor levels in single crystal CdS. As-grown CdS in the temperature range 80-380K gave a typical DLTS spectrum as shown in fig. 5.2. There is clear

SAMPLE	$\rho/\Omega cm$	N_d/cm^{-3}	COMMENT
519	20	2.3×10^{17}	doped with Te during growth
537	100	3×10^{16}	
647	10^3	2×10^{16}	annealed in Cd vapour
732	$\sim10^6$	-	photoconductive, as grown
759	100	3×10^{16}	annealed in Cd vapour
799	8×10^3	4×10^{15}	annealed in S vapour
808(A)	50	4×10^{16}	as grown
808(B)	3×10^3	8×10^{15}	Cu doped

Figure 5.1 Summary of the types of CdS material investigated.

indication of two peaks at about 140K and 200K each of which corresponds to an electron trap; these have been denoted E1 and E2. Samples annealed in Cd or S vapour gave two further peaks corresponding to electron traps denoted E3 and E4, as well as E1 and E2 (see fig.5.2). The high temperature peaks associated with E3 and E4 will be discussed in the next section. Typical Arrhenius plots for E1 and E2 for all of the samples studied are shown in fig. 5.3. The activation energies and capture cross-sections for E1 and E2 were 0.29eV, $4x10^{-15}cm^2$ and 0.44eV, $1.5x10^{-14}cm^2$ respectively. The activation energies, capture cross-sections and trap densities are summarised in fig. 5.4. These summarised results came from repeated DLTS scans for each sample and there was found to be negligible deviation from these values indicating consistent thermal ramping over the temperature range used. The capacitance transients at temperatures in the range corresponding to E1 and E2 follow an exponential decay for trap emptying as predicted by DLTS theory [28]. Fig. 5.5 shows a curve fitted transient due to E1 at 140K. Fig. 5.6 shows a similar plot for E2 at various temperatures. Theoretical DLTS peaks were determined by combining equations 3.28 and 3.30. The activation energies from sample 799 were used and the capture cross-sections fitted to give the same position in temperature as the experimental peaks; these were $8x10^{-15}cm^2$ for E1 and $7x10^{-14}cm^2$ for E2. The experimental DLTS peaks for E1 and E2 with the theoretical results are shown in figs 5.7 and 5.8 ; the sampling times were t1=120msec and t2=480msec.

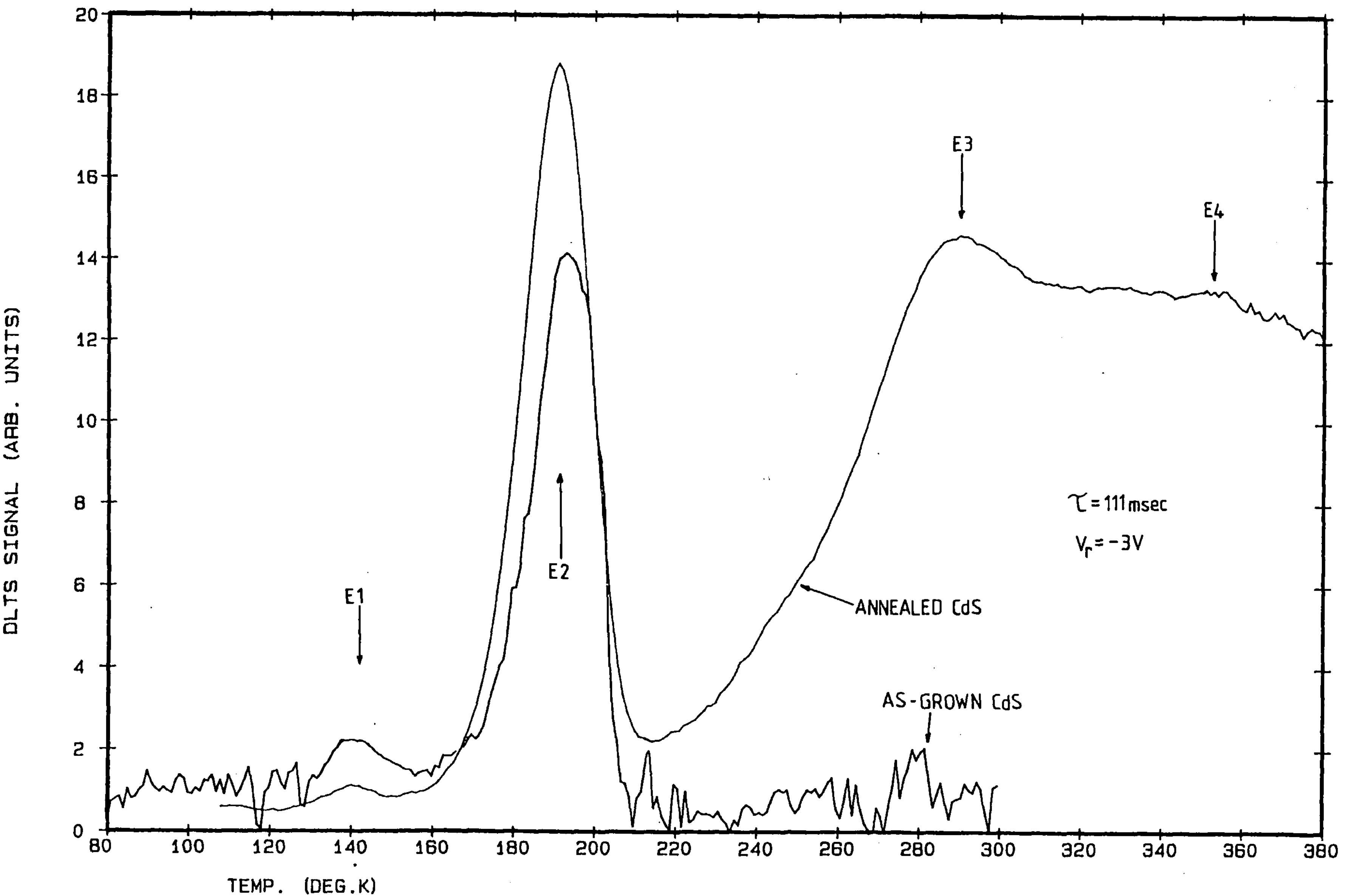


Figure 5.2 DLTS of as-grown and annealed single crystal CdS

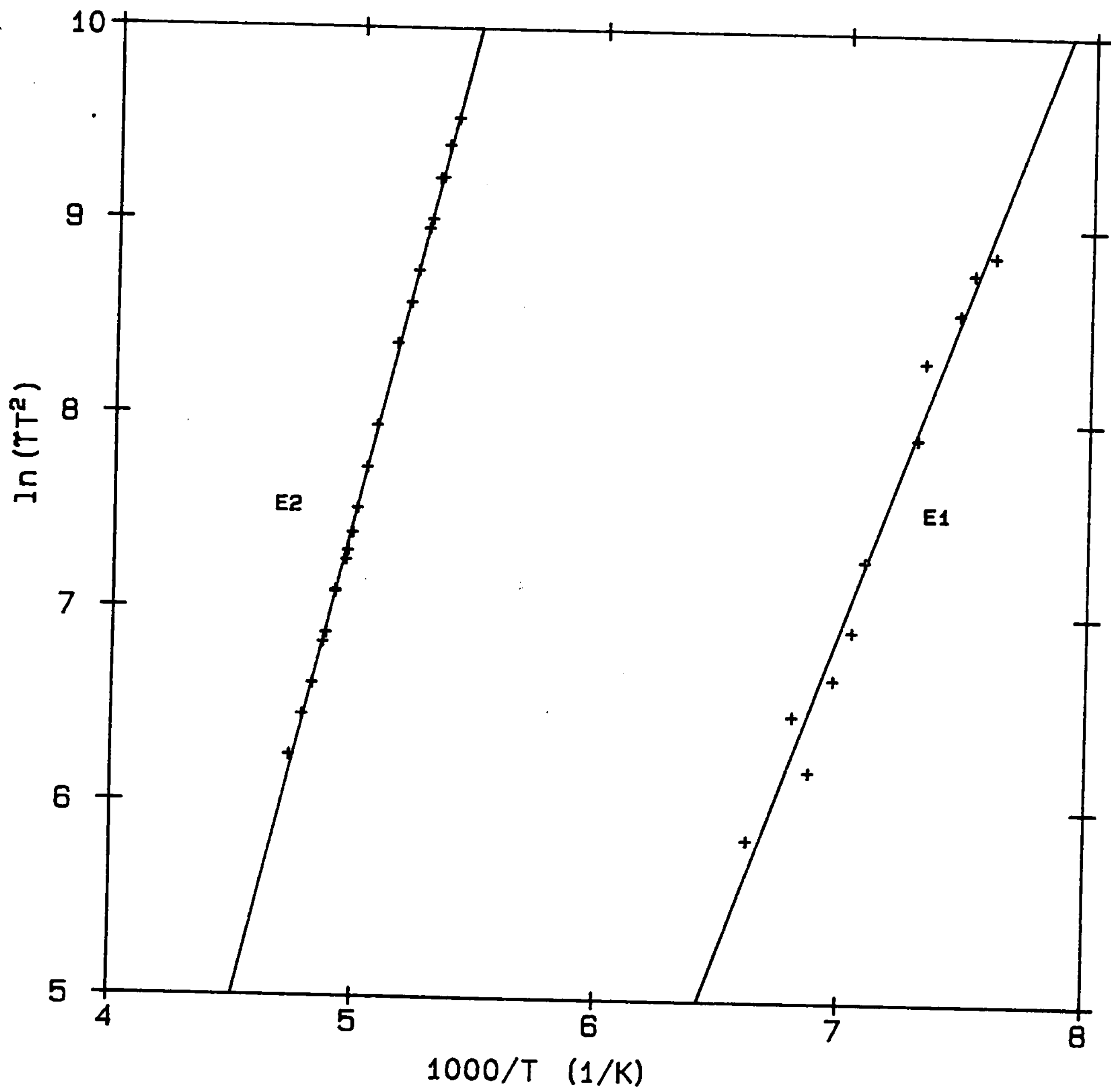
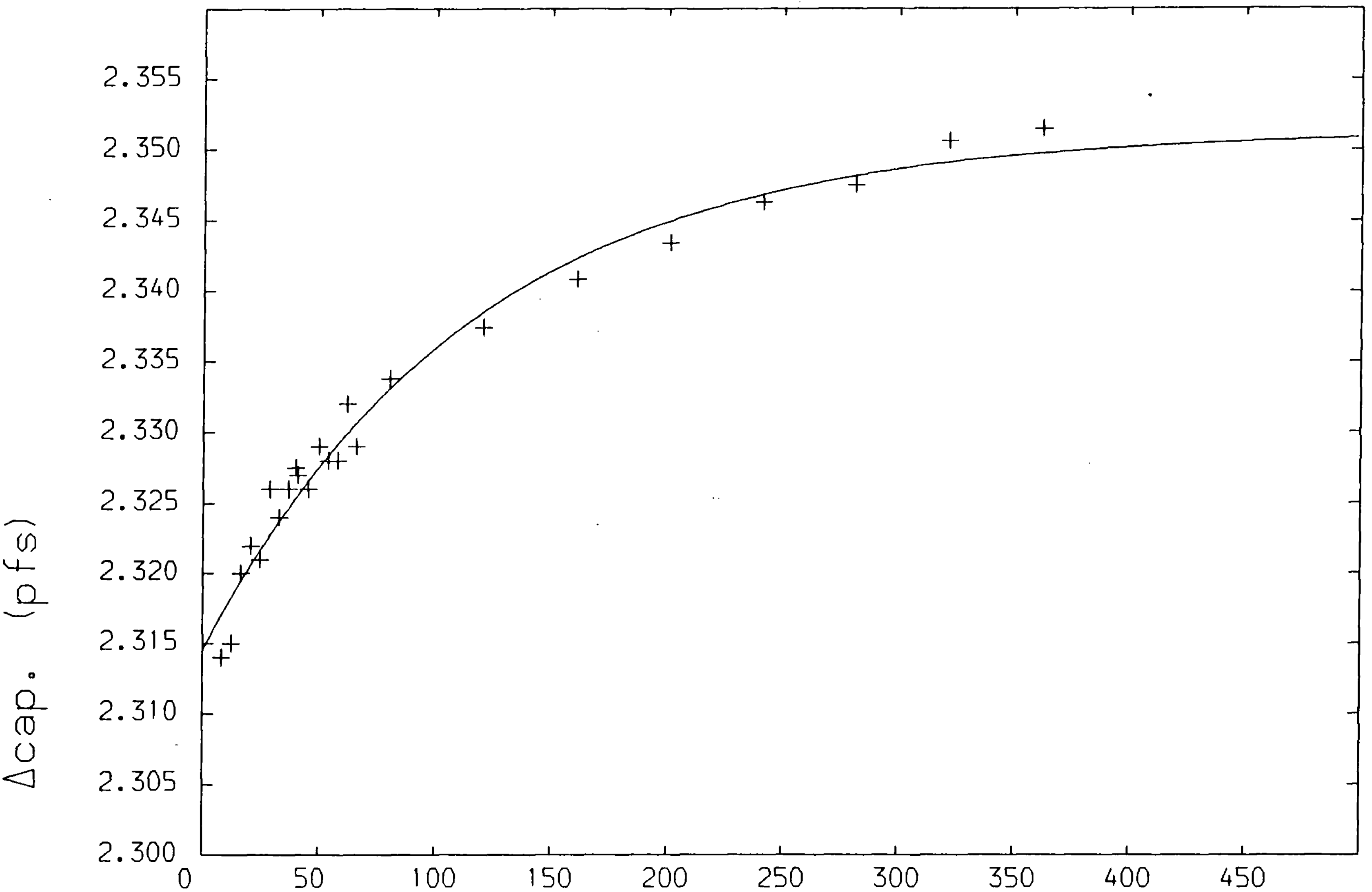


Figure 5.3 Arrhenius plots for electron traps E1 and E2

SAMPLE		$(E_c-E_t)/eV$	σ/cm^2	N_t/cm^{-3}	N_t/N_d
537(A)	E1	NR			
	E2	0.43 ± 0.02	$(1.1\times\div1.2)\times10^{-14}$	1.4×10^{14}	5.9×10^{-3}
537(B)	E1	NR			
	E2	0.45 ± 0.02	$(4.8\times\div1.2)\times10^{-14}$	2.6×10^{13}	9.3×10^{-4}
647	E1	0.30 ± 0.03	$(5\times\div11)\times10^{-15}$	7.3×10^{12}	7.3×10^{-4}
	E2	0.41 ± 0.01	$(2.6\times\div1.6)\times10^{-15}$	1.1×10^{14}	6.4×10^{-3}
732	E1	0.29 ± 0.03	$(4\times\div11)\times10^{-15}$	9.4×10^{14}	2.4×10^{-3}
	E2	0.45 ± 0.01	$(2.5\times\div2.7)\times10^{-14}$	3.4×10^{15}	8.4×10^{-3}
759	E1	NR			
	E2	0.43 ± 0.03	$(5\times\div4)\times10^{-14}$	8.9×10^{13}	3.0×10^{-3}
799	E1	0.29 ± 0.02	$(3\times\div9)\times10^{-15}$	4.7×10^{12}	1.6×10^{-3}
	E2	0.44 ± 0.01	$(1.5\times\div0.4)\times10^{-14}$	6.3×10^{13}	2.1×10^{-2}
808	E1	NR			
	E2	0.45 ± 0.02	$(3\times\div6)\times10^{-14}$	4.7×10^{14}	1.2×10^{-2}

Figure 5.4 Summary of results for electron traps E1 and E2 (NR=not resolved)



FITTED PARAMETERS

P 1 = 0.235E01 P 2 = -0.368E-01 P 3 = 0.114E03

Figure 5.5 Capacitance transient at 140K due to electron emission from E1

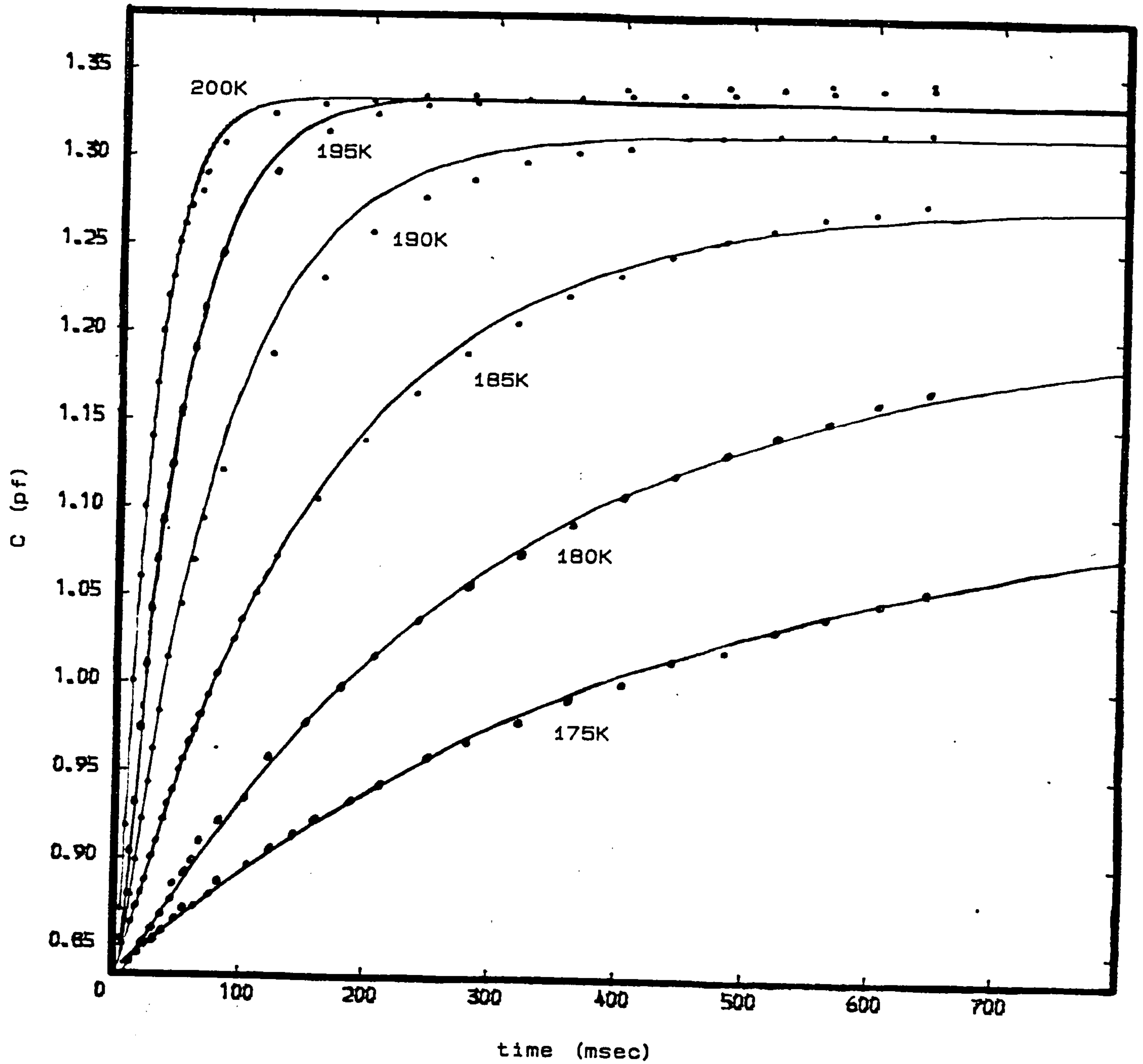


Figure 5.6 Capacitance transients at various temperatures due to electron emission from E2

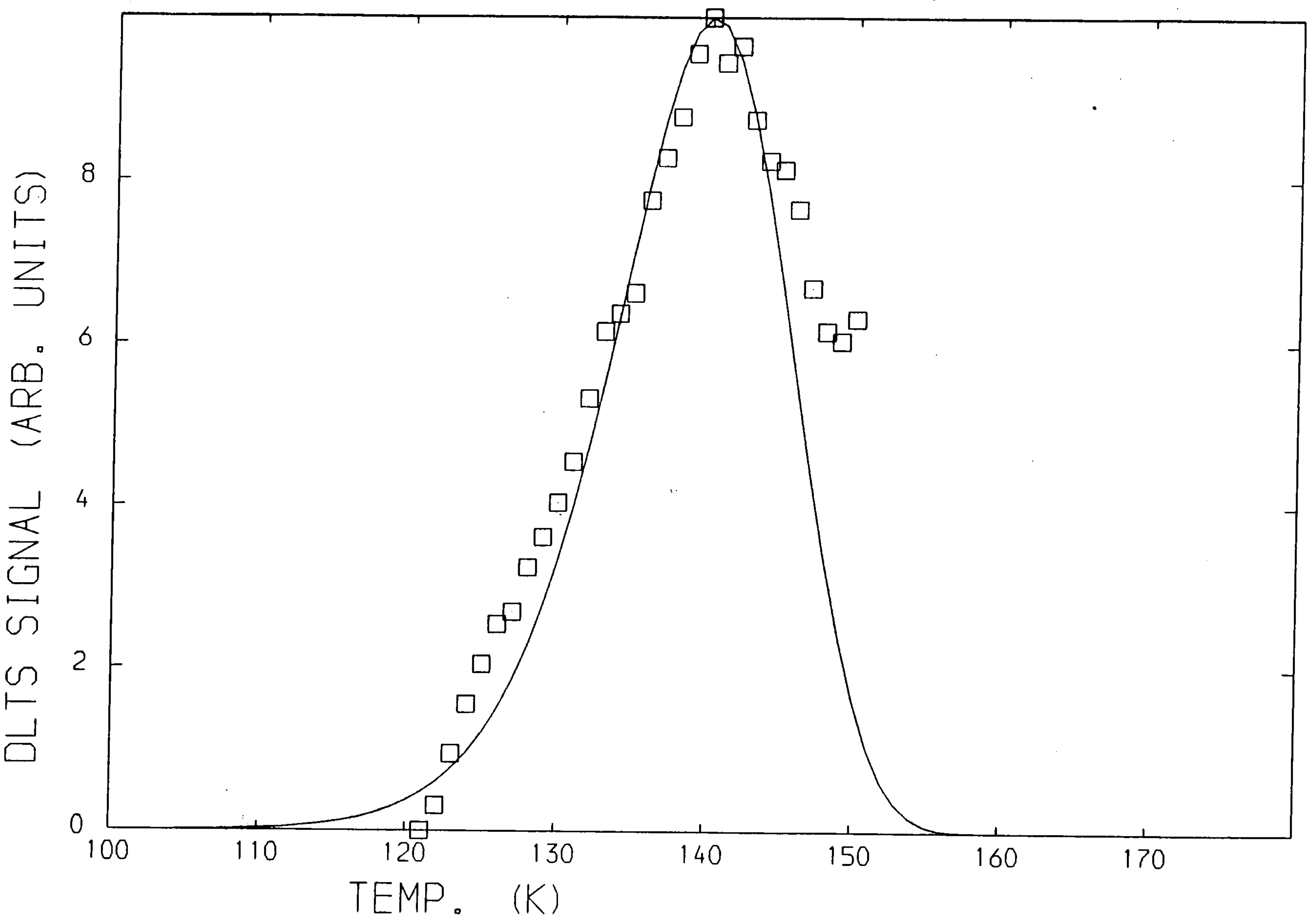


Figure 5.7 Theoretical (——) and experimental (□□□) DLTS curves for E1

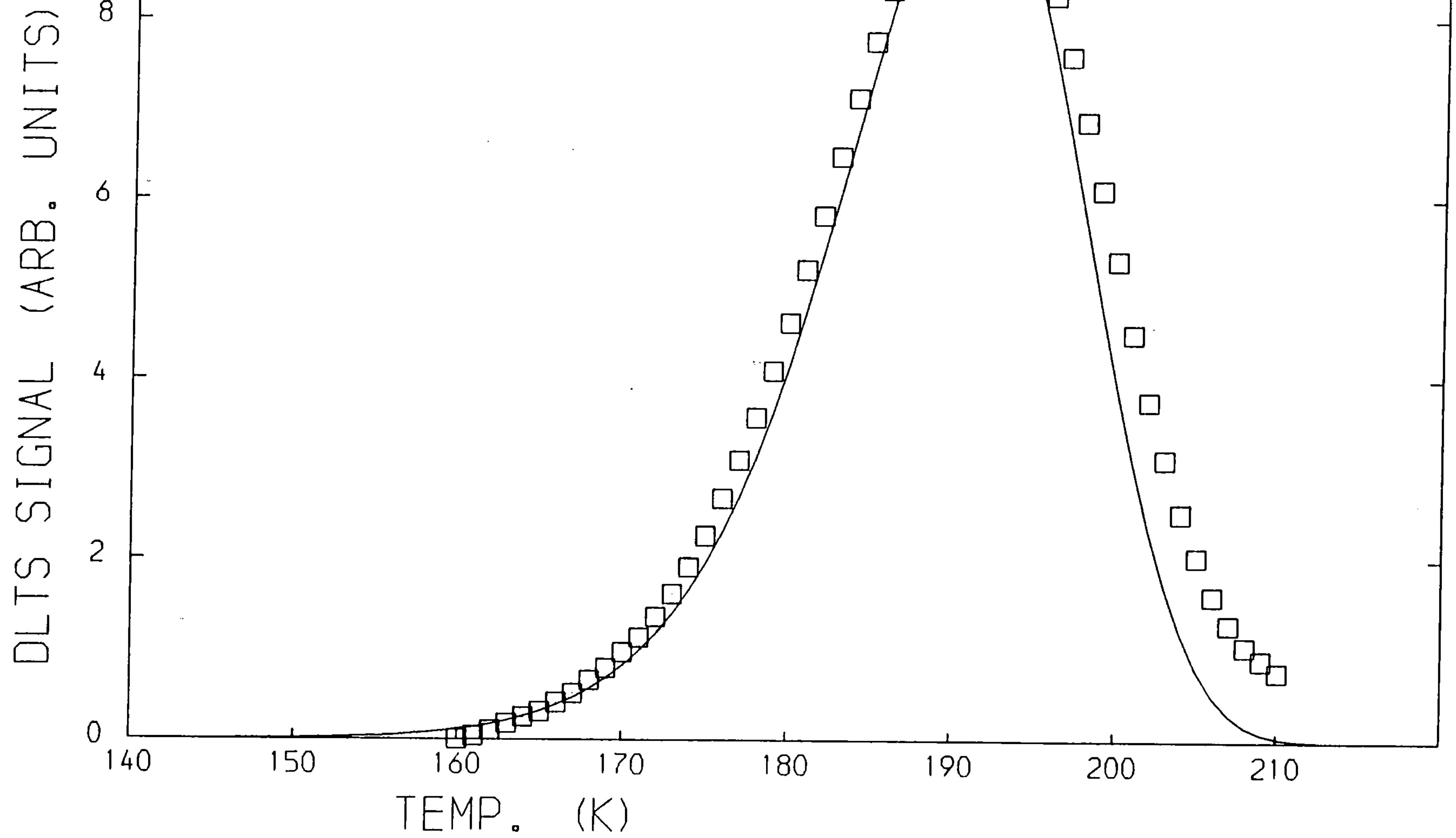


Figure 5.8 Theoretical (——) and experimental (□□□) DLTS curves for E2

5.2.3 Electron Traps E3 and E4

5.2.3.1 DLTS Results

The electron trap E3 observed in the DLTS spectrum in fig. 5.2 was only observed in samples that had undergone a post-growth heat treatment. In addition it appeared to be photoinduced. Fig. 5.9a shows a DLTS run to 350K of a sample which had been previously exposed to room lighting. The spectrum shows the peak corresponding to E3. A further DLTS run after the sample had been in the dark for 44hrs and had been heated to 350K was carried out; the peak associated with E3 disappeared (see fig. 5.9b). Note that the peak at 320K correlated with the high temperature shoulder in fig. 5.9a, due to E4. After the sample had been in the dark for 100hrs and heated to 380K during the course of a DLTS scan there appeared to be no further change in the spectrum (see fig. 5.9c). The sample was again exposed to room lighting at room temperature and a further DLTS run was carried out in the dark - this again showed the presence of E3 (see fig. 5.9d). From a qualitative point of view E3 was a photoinduced trap which disappeared slowly when heated in the dark. The important point was that the effect of 'destroying' the trap was reversible by illumination. These states were denoted 'light' (E3 present) and 'dark' (E3 absent)

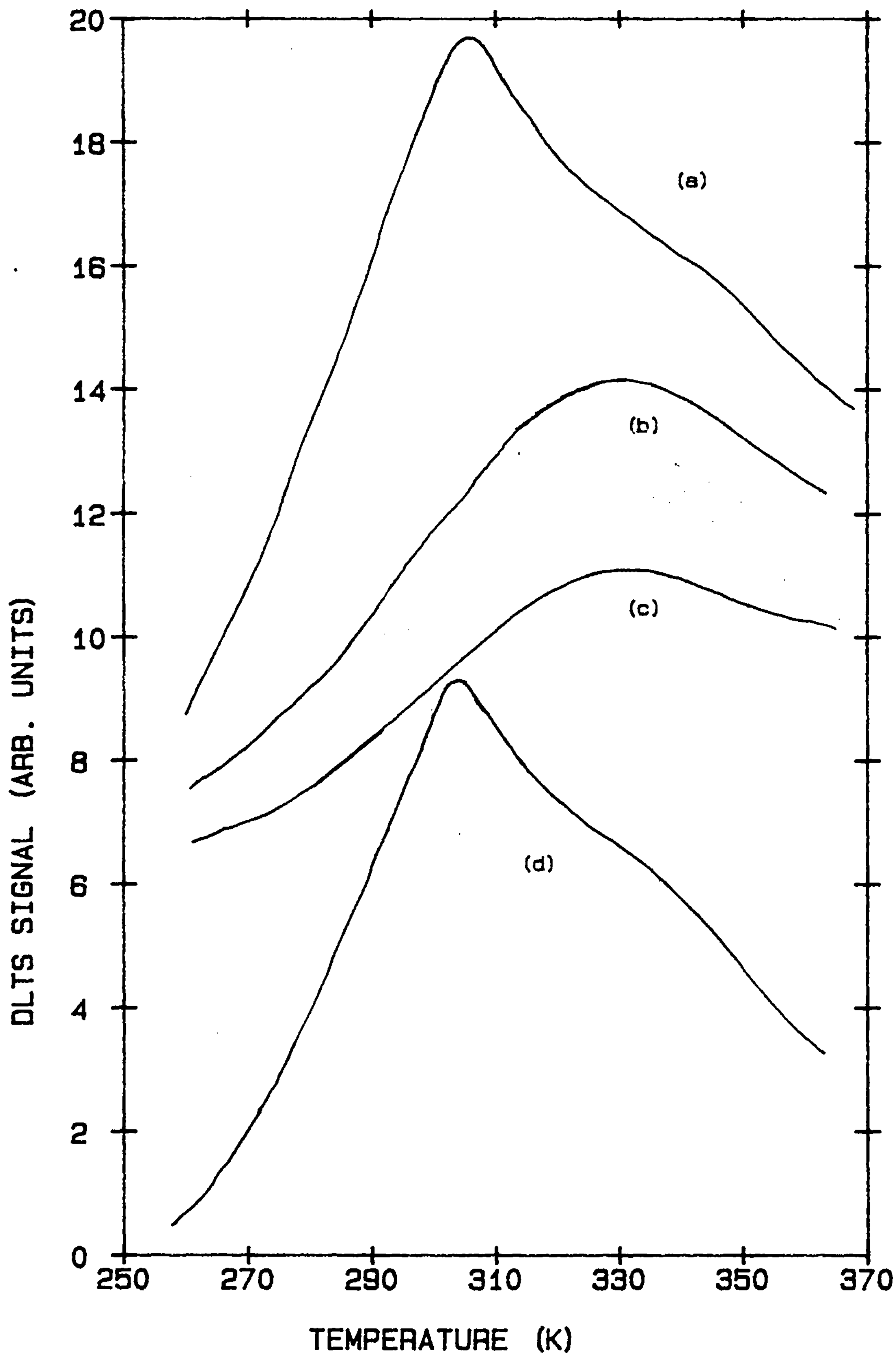


Figure 5.9 DLTS spectra showing the "light" and "dark" states
(a) "light" previously exposed to room lighting
(b) "dark" previously heated to 350K in the dark
(c) "dark" previously heated to 380K in the dark
(d) "light" re-exposed to room lighting

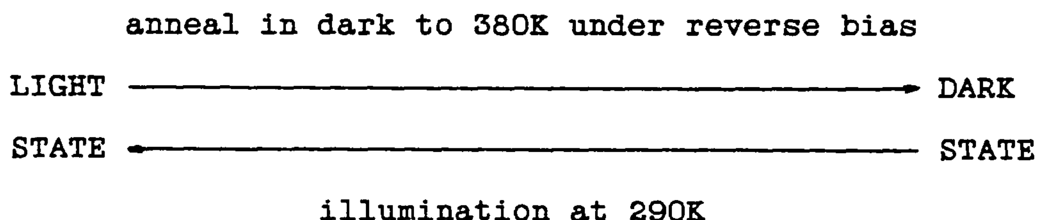


Fig. 5.9b clearly shows the peak corresponding to the electron trap E4; an Arrhenius plot for E4 from the 'light' state spectrum was linear only for short time constants since thereafter the peak ran into E3 and its position was difficult to estimate. Consequently, the Arrhenius plot for E4 from the 'dark' DLTS spectra were used thereby losing the complicating factor of E3. Arrhenius plots for E3 and E4 (from the 'dark' state spectra) are shown in fig. 5.10 and the energies, capture cross-sections and densties are summarised in fig. 5.11.

Capacitance-temperature scans were carried out and correlated with the DLTS runs. There were four thresholds in the C-T scan for all samples; these approximately corresponded in temperature with the peaks due to E1, E2, E3 and E4 (see fig. 5.12). At 290K there was a peak in the C-T scan corresponding to the temperature just below that of the E4 DLTS peak.

The optical threshold for the formation of the electron trap E3 was investigated. Initially the CdS sample was put into its 'dark' state by annealing at 380K for 10min with 1V reverse bias. The sample was subjected to monochromatic light from a tungsten source through a Hilger-Watts monochromator over the wavelength range 550nm to 975nm; from an I.R. Source (Oriel) using a 1200nm interference filter;

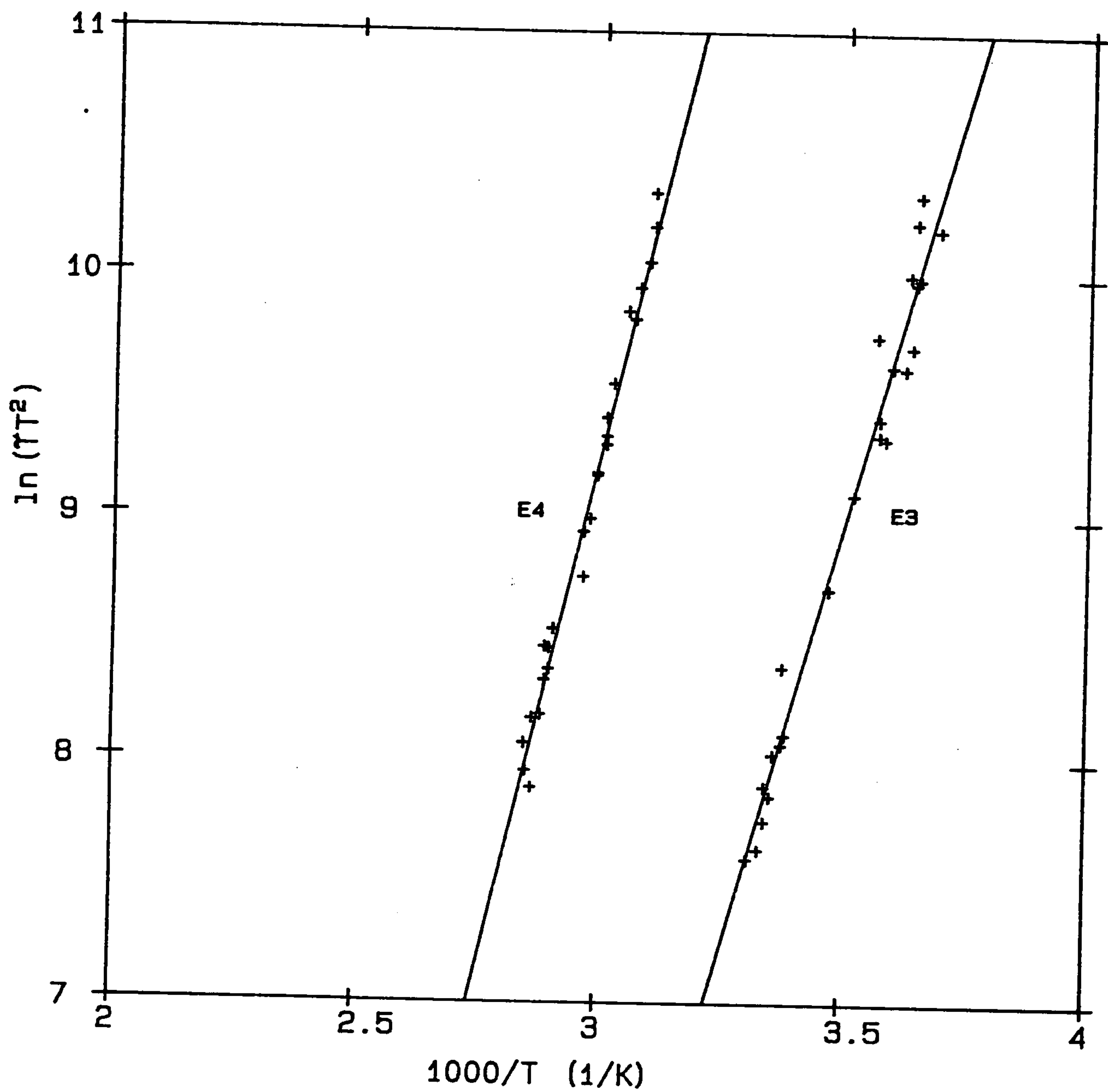


Figure 5.10 Arrhenius plots for electron traps E3 and E4

SAMPLE		(E_c-E_t)/eV	σ/cm^2	N_t/cm^{-3}	N_t/N_d
537(A)	E3	0.63 ± 0.06	$(3^{\times}_{\div}8)\times10^{-15}$	1.5×10^{14}	6.2×10^{-3}
	E4	NR			
537(B)	E3	0.65 ± 0.05	$(5^{\times}_{\div}7)10^{-15}$	2.3×10^{14}	8.7×10^{-3}
	E4	NR			
647	E3	0.60 ± 0.05	$(2^{\times}_{\div}6)\times10^{-15}$	4.1×10^{14}	1.0×10^{-2}
	E4	0.73 ± 0.03	$(2^{\times}_{\div}3)\times10^{-15}$	1.7×10^{14}	9.8×10^{-3}
759	E3	0.61 ± 0.05	$(8^{\times}_{\div}5)\times10^{-15}$	8.9×10^{14}	3.3×10^{-2}
	E4	0.70 ± 0.04	$(4^{\times}_{\div}6)\times10^{-15}$	9.5×10^{14}	3.5×10^{-2}
799	E3	0.61 ± 0.03	$(2^{\times}_{\div}2)\times10^{-15}$	3.2×10^{13}	1.1×10^{-2}
	E4	0.74 ± 0.03	$(3^{\times}_{\div}3)\times10^{-15}$	1.3×10^{13}	1.0×10^{-2}

Figure 5.11 Summary of the results for the states E3 and E4 (NR=not resolved)

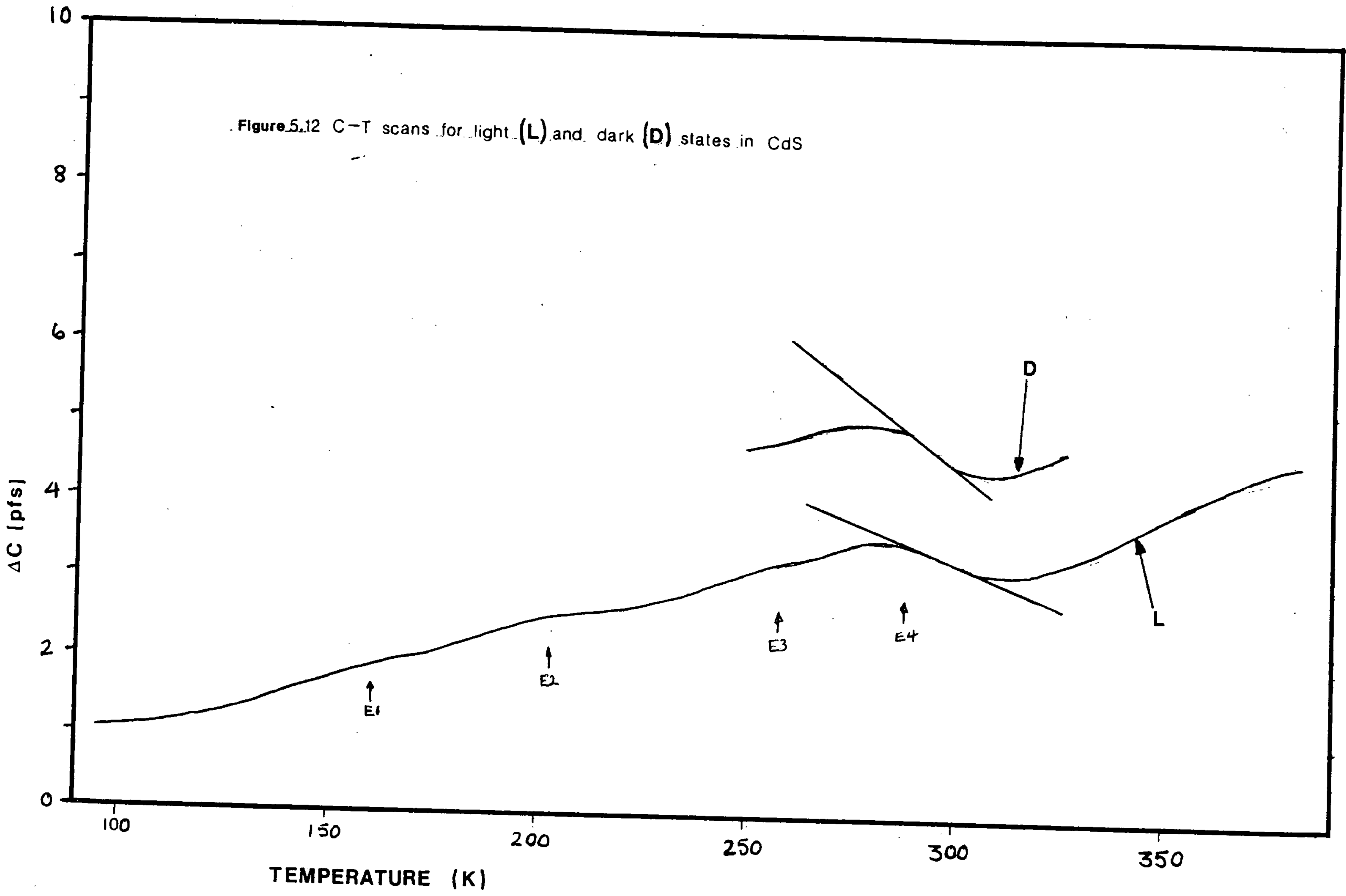


Figure 5.12 C−T scans for light (L) and dark (D) states in CdS

and from an Argon ion laser (Spectra-Physics) operating at 489nm. The photocapacitance (PHCAP) response was monitored during each exposure at 290K until there was negligible change in capacitance (~2hrs). The light was removed and the PHCAP response monitored until thermal equilibrium had been achieved (see fig. 5.13). The DLTS spectra obtained after light exposure at different wavelengths is given in fig. 5.14. The optical threshold for E3 lies between 1eV and 1.3eV. A more accurate value was not possible with this system due to the limitations on the monochromator and availabilty of filters in the 1000nm to 1200nm range. Fig. 5.15 shows a plot of $[N_T(h\upsilon)-N_T(dark)]/N_T(dark)$ as a function of photon energy $h\upsilon$. This shows a threshold at about 1.0eV.

Illumination was also carried out at 77K in order to investigate the possibility that the defect formation by light exposure was thermally activated. Fig. 5.16 shows the DLTS scan after a sample had been treated in this manner; the light source was an Ar ion laser. E3 was clearly present in the material as can be seen from the spectrum. A possible change in the optical threshold was not investigated at this temperature.

The capacitance transients associated with the thermal emptying of E3 and E4 were found to be non-exponential as indicated by the poor agreement between the experimental points and the least-squares best curve-fit to equation 4.5 (see chapter 4) in figs 5.17 and 5.18. The values of activation energy and capture cross-section therefore, were subject to some uncertainty. The real DLTS transients for E3

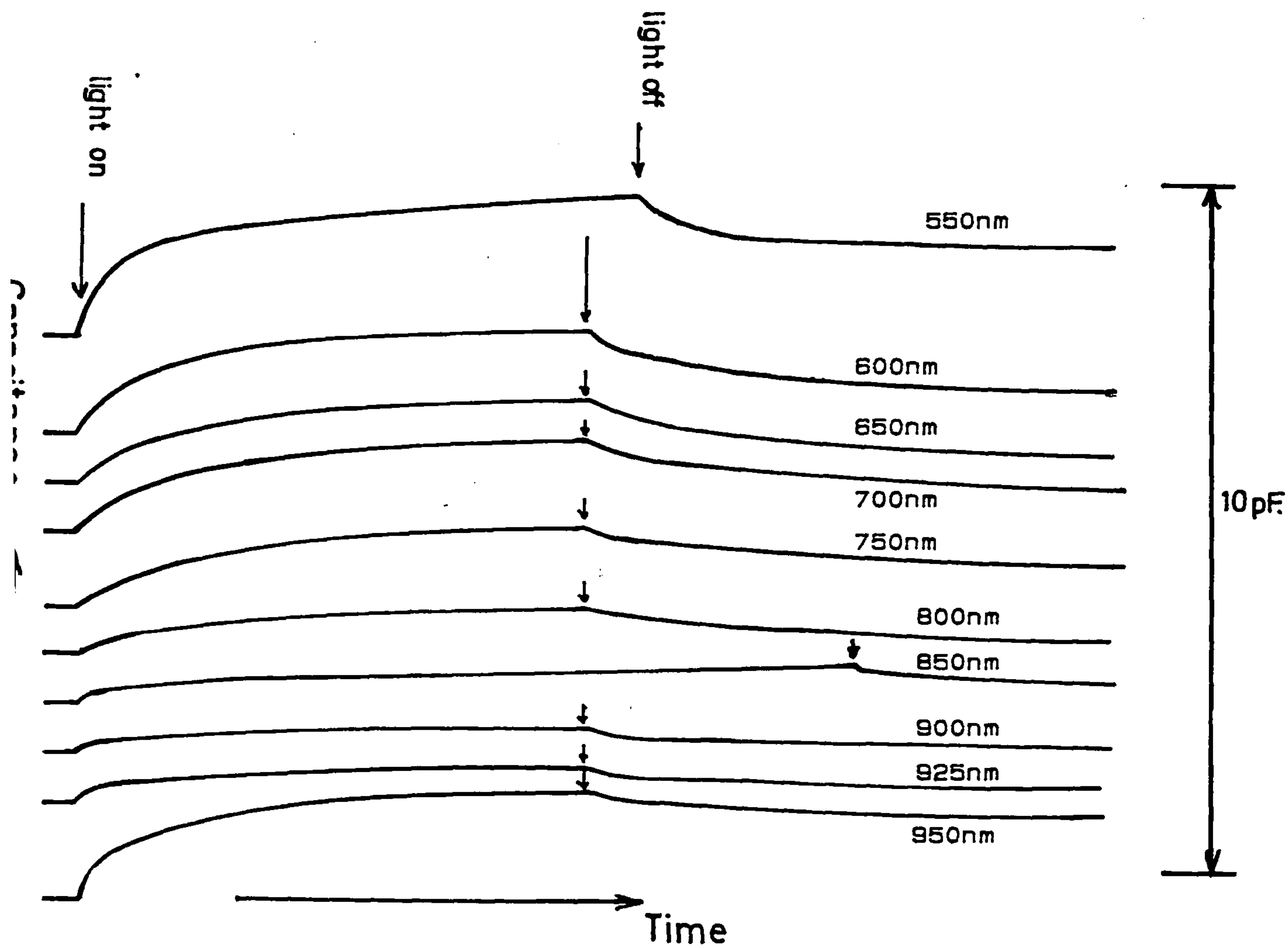


Figure 5.13 Light and dark photocapacitance transients for illumination of CdS at different wavelengths

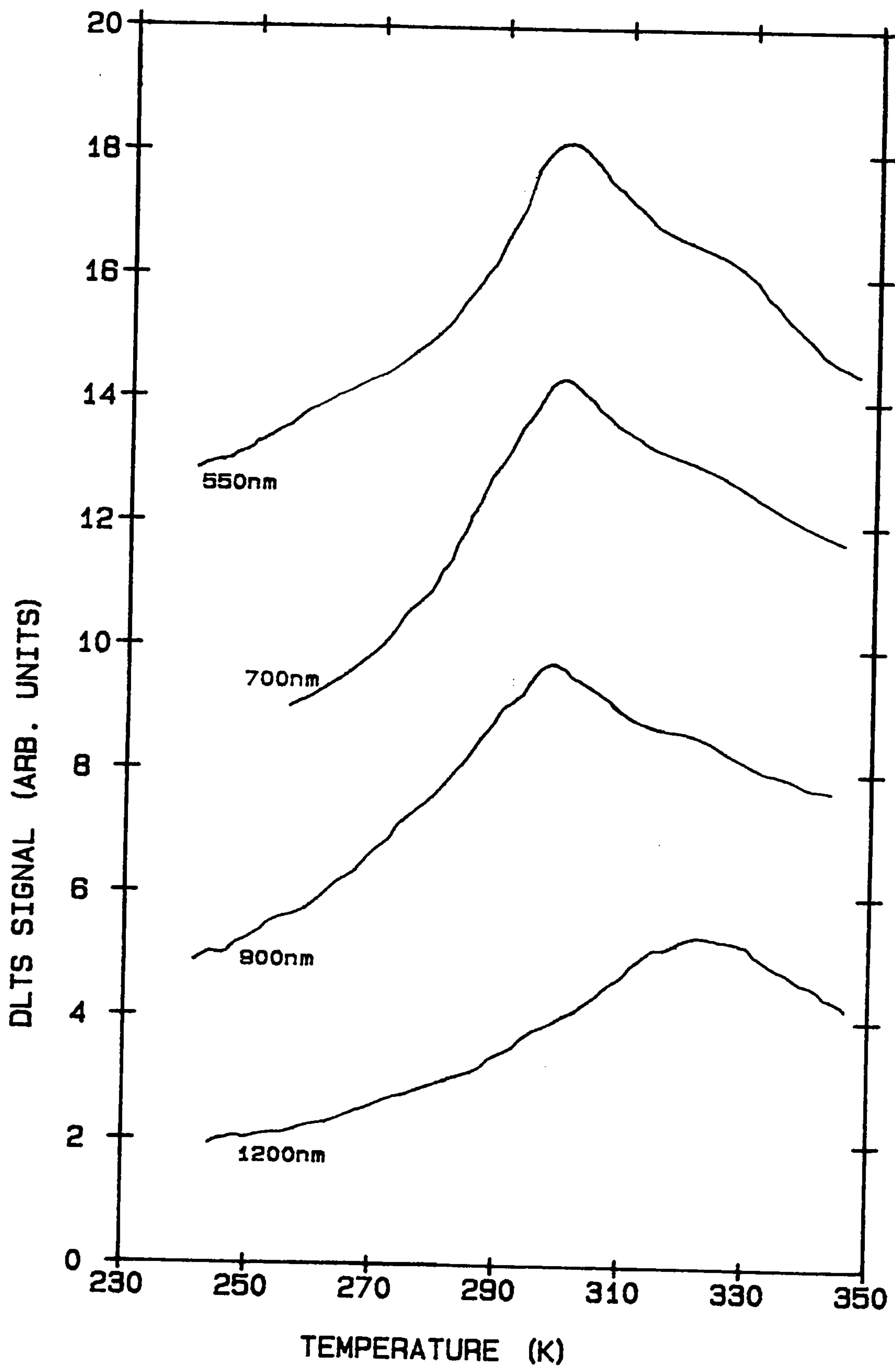


Figure 5.14 DLTS spectra after illumination at different wavelengths

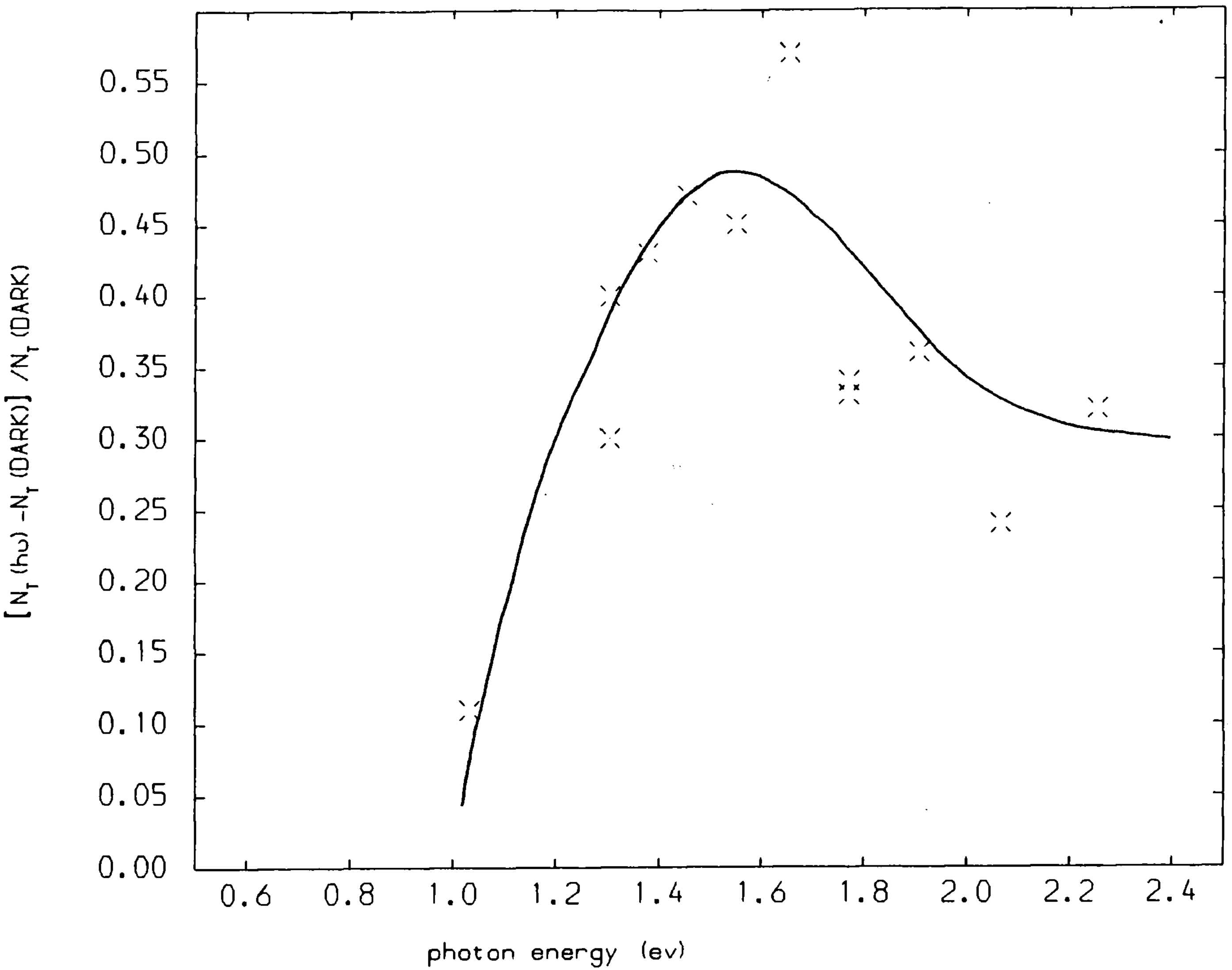


Figure 5.15 Plot of normalised trap density for E3 as a function of the energy of the illumination prior to the DLTS scan

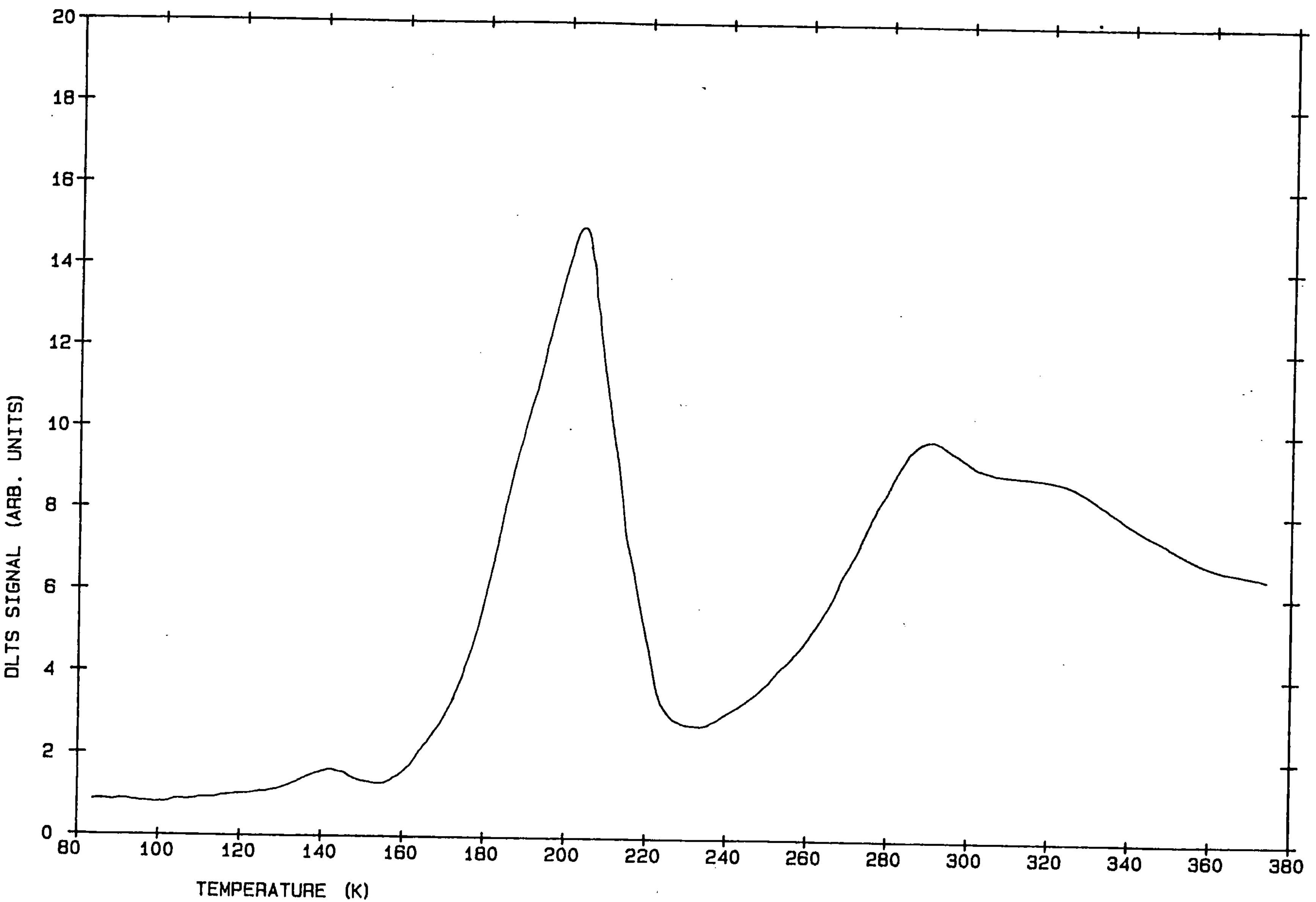
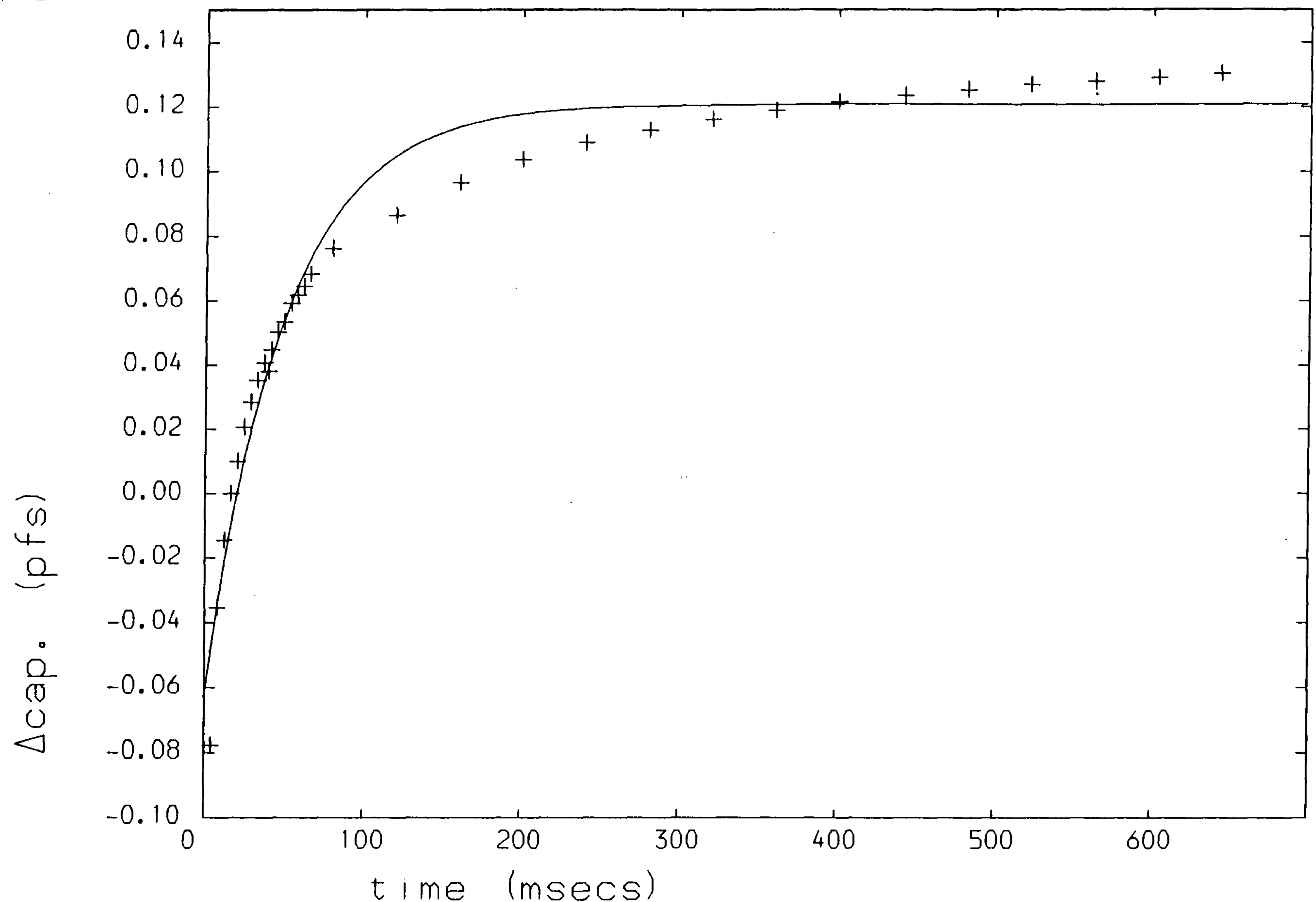


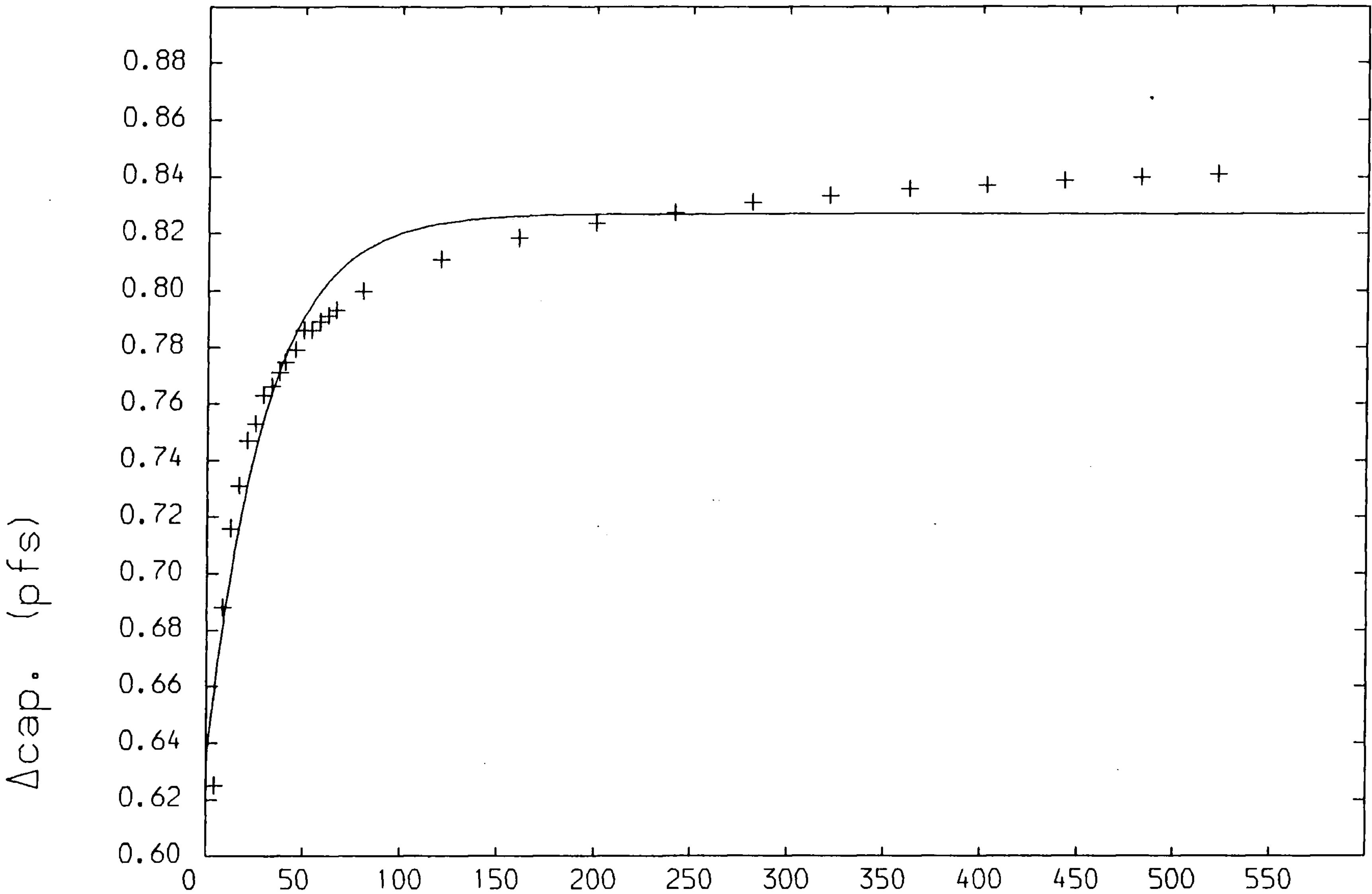
Figure 5.16 DLTS scan after illumination at 77K



FITTED PARAMETERS

P 1 = 0.121E00 P 2 = -0.183E00 P 3 = 0.491E02

Figure 5.17 Capacitance transient due to electron emission from E3 at 270K



FITTED PARAMETERS

P 1 = 0.827E00 P 2 = -0.192E00 P 3 = 0.298E02

Figure 5.18 Capacitance transient due to electron emission from E4 at 320K

were obtained by simply subtracting the 'dark' state transient from the 'light' state transient at each temperature of the scan; a typical decoupled transient is shown in fig 5.18. Fig. 5.19 shows a DLTS spectrum obtained from the decoupled transients - the solid line is the theoretical peak. Fig. 5.20 shows a similar plot for E4 from the 'dark' state spectrum. These plots show that the experimental DLTS spectra were broader than predicted theoretically - in the case of E3, twice and E4, three times as broad.

5.2.3.2 Capacitance-Voltage Measurements

Capacitance-voltage measurements were taken before and after each illumination at the different photon energies and before and after each DLTS scan in order to monitor any change in the free carrier density or the intercept voltage (V(0)). It was found that changing the state ('light'/'dark') gave a simultaneous change in the intercept voltage. Figs 5.21-23 show $1/C^2$ vs V plots for 3 CdS samples - (i)V(0)>>Eg (ii)V(0)=Eg (iii)V(0)<Eg. Fig.5.21(L) was taken immediately following exposure to room lighting and corresponds to the light state. Fig.5.21(D) shows the dark state result after the device had been heated to 380K in the dark under reverse bias - light V(0)=5.5V and dark V(0)=6.5V. This shows the large change in the intercept voltage corresponding to the 'light' state to 'dark' state transformation. A much smaller, but not insignificant change, was found for samples with V(0)=Eg; a typical change in V(0) was about 0.35V (see fig.5.22). For V(0) close to

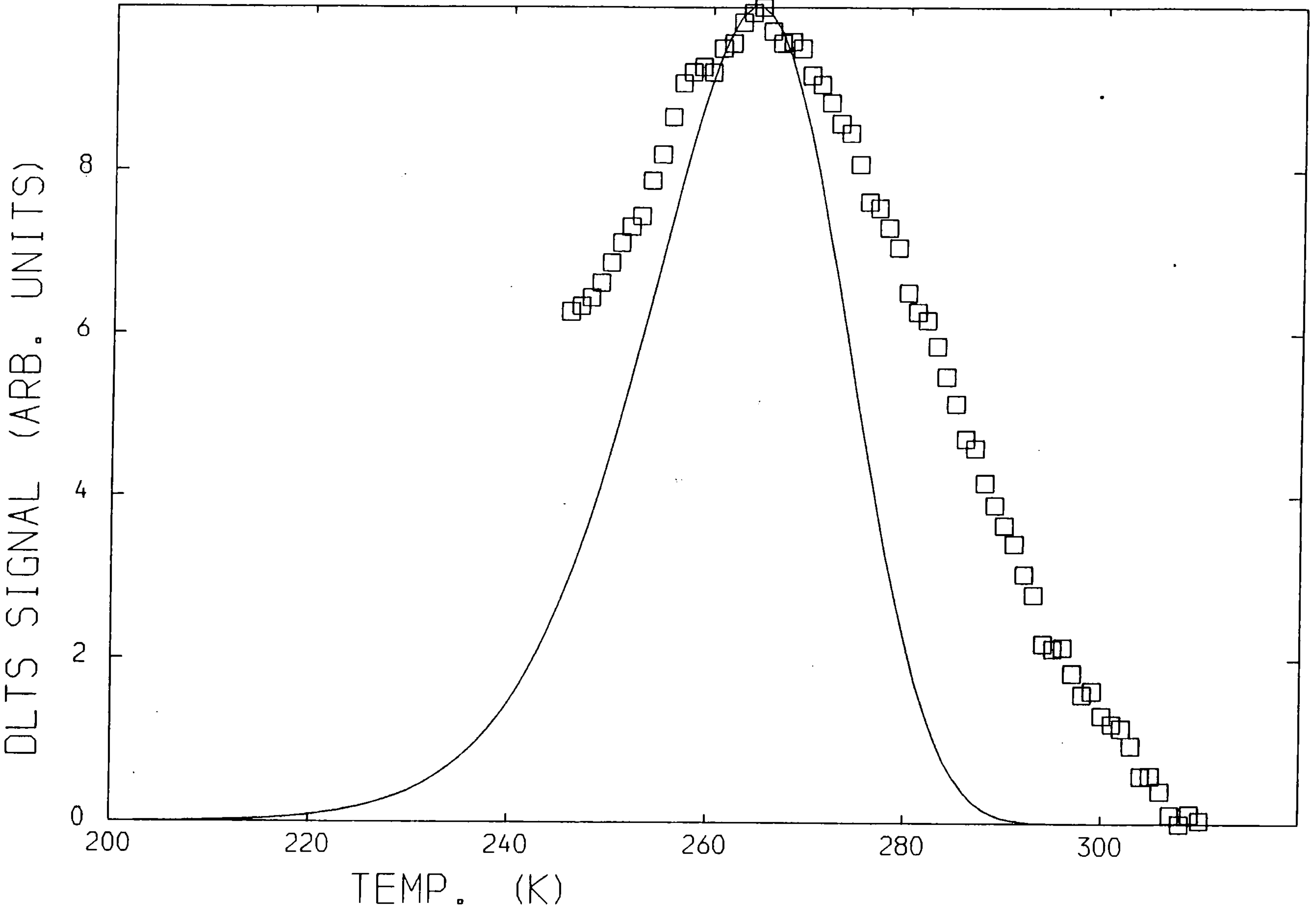


Figure 5.19 Theoretical (——) and experimental (□ □) DLTS curves for E3

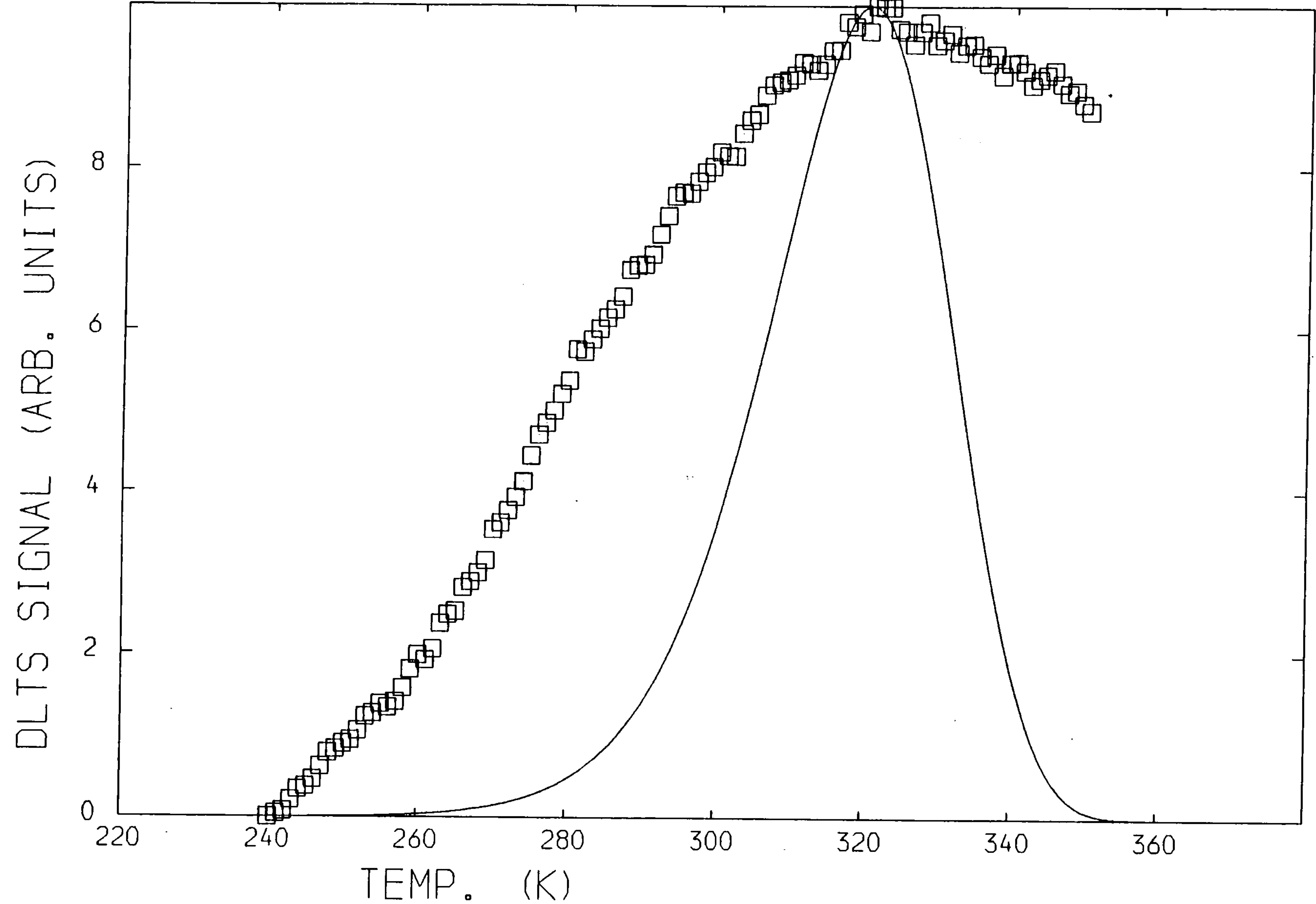


Figure 5.20 Theoretical (——) and experimental (□ □) DLTS curves for E4

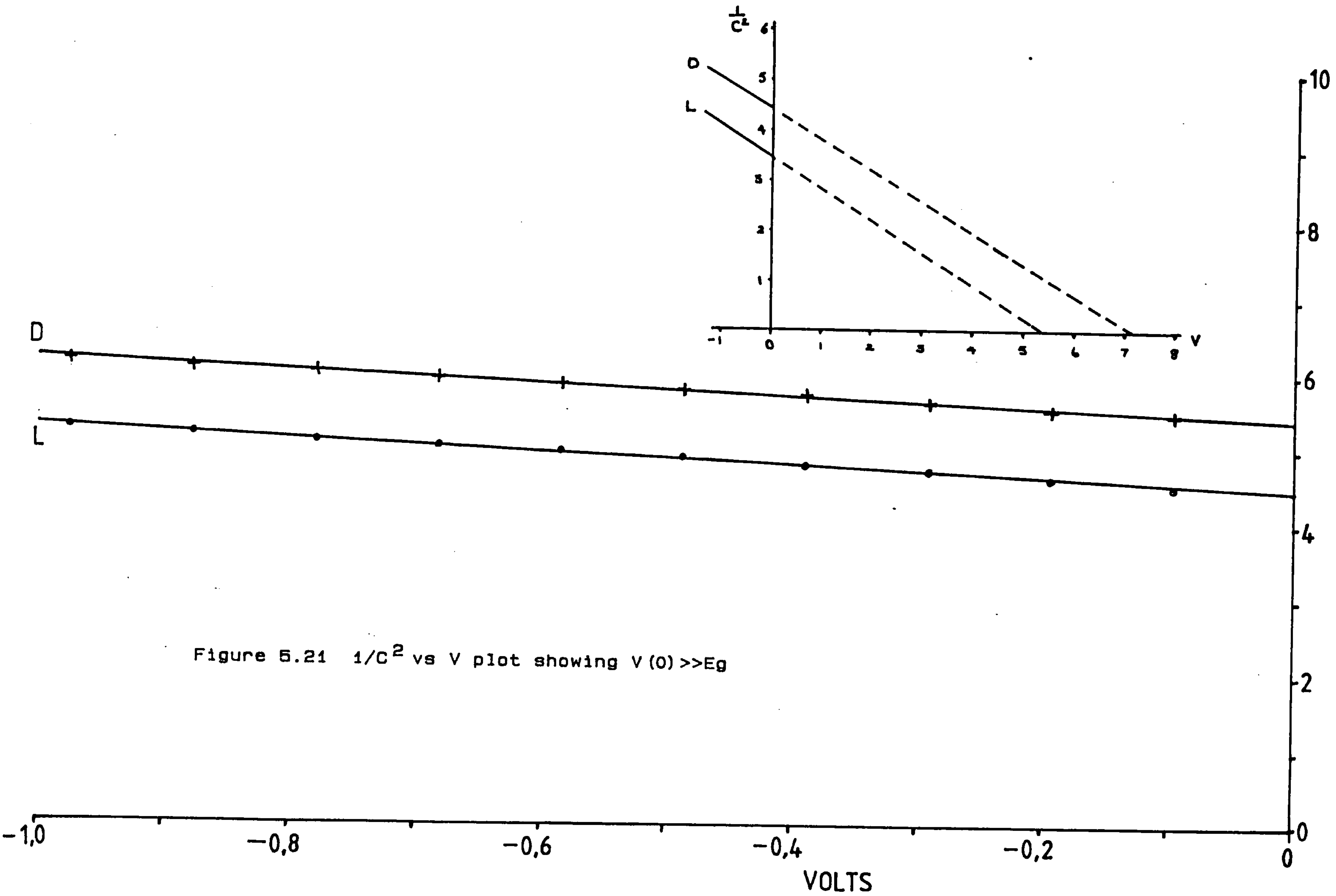


Figure 5.21 $1/C^2$ vs V plot showing V(0) >>Eg

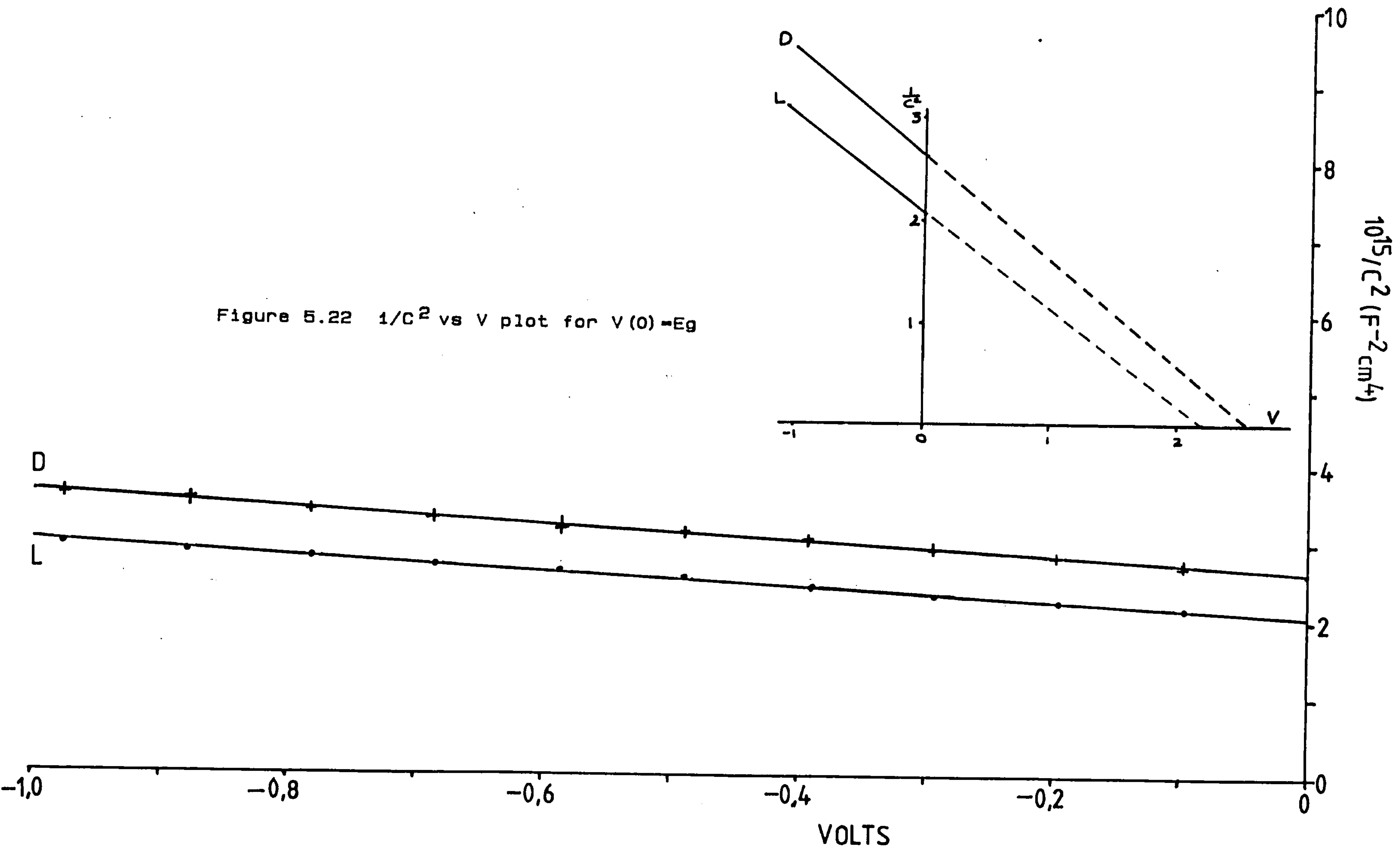


Figure 5.22 $1/C^2$ vs V plot for V(0) = Eg

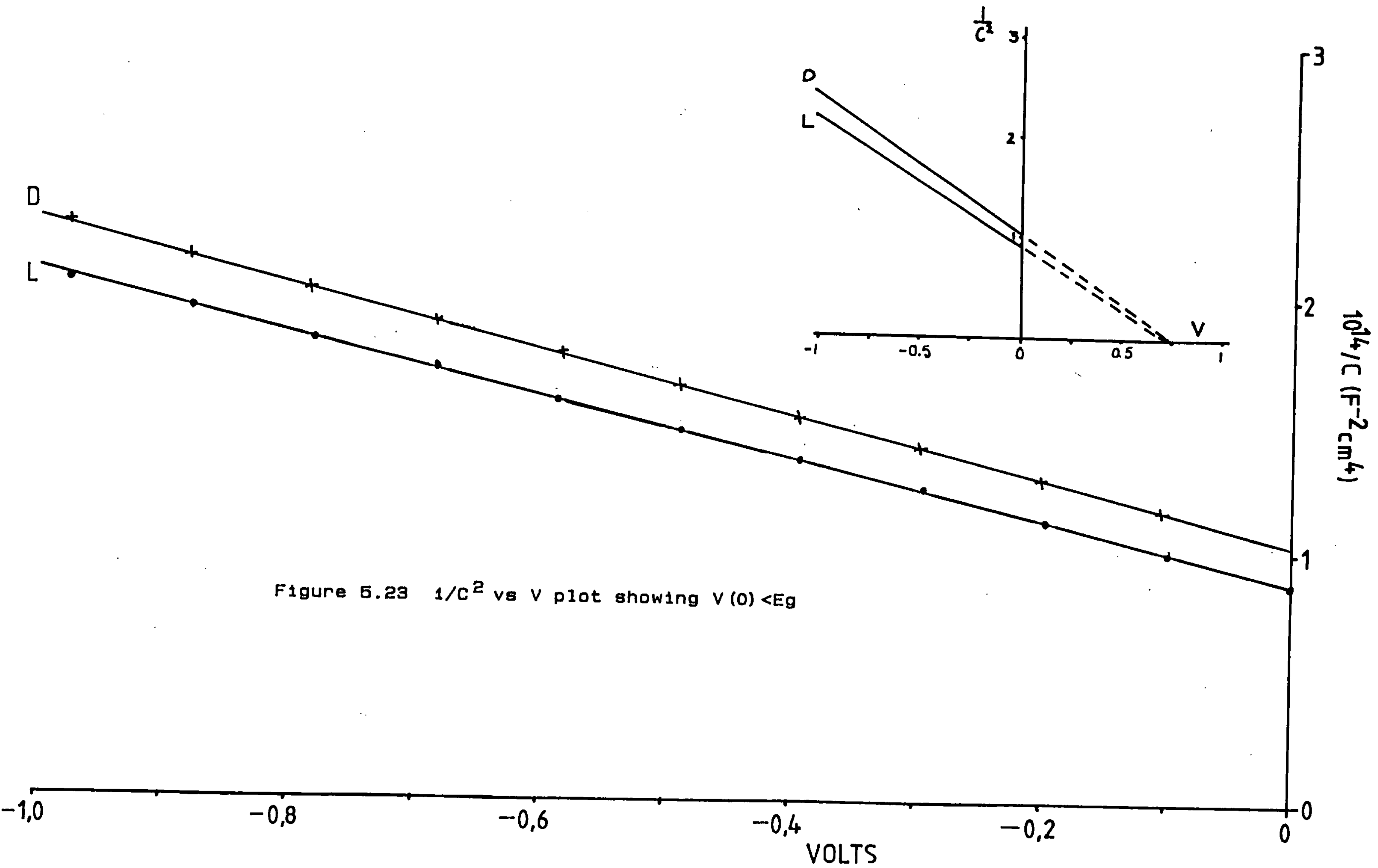


Figure 5.23 $1/C^2$ vs V plot showing V(0) <Eg

its ideal Schottky value, such samples displayed no change in V(0) (see fig. 5.23). Indeed such samples gave no DLTS response to the photoinduced state E3. Those samples that displayed the difference in 'light'/'dark' state gave negligible change in the free carrier concentration between these two states. A summary of the results obtained from the capacitance-voltage measurements on the various CdS samples studied is given in fig. 5.24.

As with the DLTS results the transition in V(0) from the 'light' to 'dark' state was progressive with time for the sample maintained at room temperature in the dark. This process could be reversed with illumination. The rate of change increased with temperature in accordance with the DLTS results taking at room temperature about 100hrs; 8-10hrs at 370K; and at 2-3hrs at 370K under 1V reverse bias. The change in V(0) with time was studied at room temperature, 310K and 370K. After exposure to room lighting for several minutes to ensure the diode was in the 'light' state, it was returned to the dark. Capacitance-voltage measurements were taken as a function of time in order to monitor V(0); fig. 5.25 shows the change in voltage intercept with time at each temperature. From these plots it seemed that there was some exponential decay of V(0) with time. Correlating this with the DLTS results suggested that the decay corresponded with the decay of E3. Subsequently, the time constant for the decay at the different temperatures of the measurements were obtained. The time constants for the voltage intercept decay were obtained by curve-fitting as indicated by the solid lines in fig. 5.25 from

SAMPLE	$N_d(D)/cm^{-3}$	$N_d(L)/cm^{-3}$	$C_o(D)/pf$	$C_o(L)/pf$	$V_o(D)/V$	$V_o(L)/V$
519	$2.3x10^{17}$	$2.4x10^{17}$	799	858	0.73	0.74
537(A)	$2.4x10^{16}$	$2.4x10^{16}$	198	224	1.40	1.10
537(B)	$2.6x10^{16}$	$2.8x10^{16}$	156	175	2.52	2.19
647	$1.73x10^{16}$	$1.75x10^{16}$	143	163	2.05	1.60
759	$3.0x10^{16}$	$2.7x10^{16}$	168	186	2.31	2.09
799	$3.6x10^{15}$	$3.0x10^{15}$	35	38	7.11	5.33
808	$3.4x10^{16}$	$4.0x10^{16}$	528	559	0.47	0.48

Figure 5.24 Summary of results obtained from C-V measurements on the CdS samples

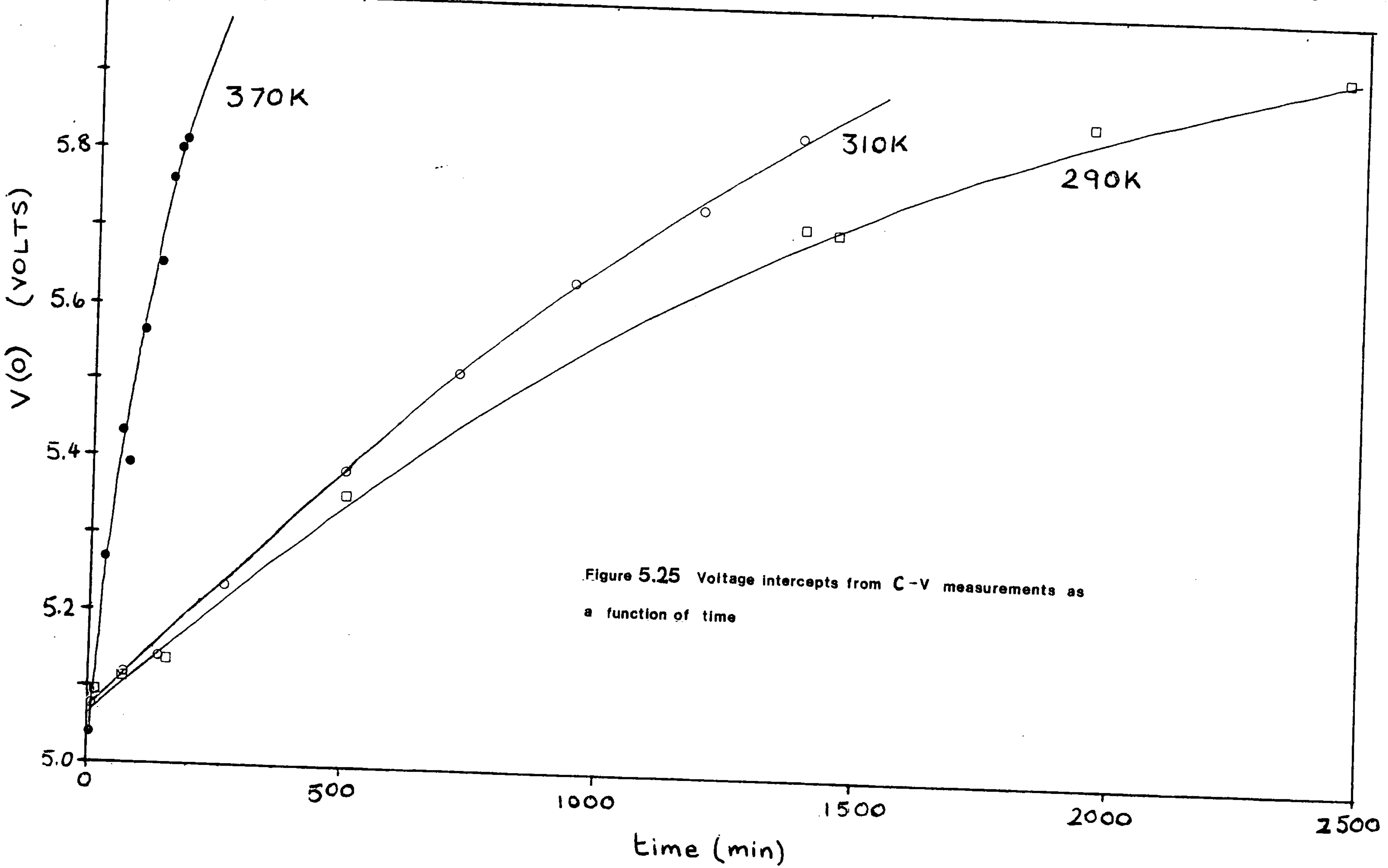


Figure 5.25 Voltage intercepts from C-V measurements as a function of time

$$\Delta V(0) = A + B\exp(-t/\tau) \qquad 5.1$$

where $\Delta V(0)$ is the change in voltage intercept, A is an offset, B a scaling parameter, t the time and τ the time constant. The decay rate was temperature dependent showing a thermal activation for the 'light' to 'dark' state transition. The thermal activation energy for the transition was obtained from the Arrhenius plot (see fig. 5.26):

$$\tau = C \exp(\Delta E/kT) \qquad 5.2$$

where C is a constant, ΔE the thermal activation energy, T the temperature. The thermal activation energy was found to be 0.25eV.

There was a definite relationship between the DLTS and the voltage intercept results for the 'light' and 'dark' states. So in an effort to determine the optical threshold for the formation of E3 by another, independent method, the change in voltage intercept and capacitance at zero bias were monitored with light energy. The sample was put into its 'dark' state by a DLTS run to 380K. After cooling to room temperature a C-V measurement was carried out so that V(0) and free carrier concentration could be determined. The sample was exposed to a photon energy between 1.03eV and 2.53eV; exposure was for 6.5mins followed by 6mins in the dark. The zero bias capacitance was monitored during this period to ensure a steady state. This was followed by a C-V measurement. The sample again underwent a DLTS run to 380K to obtain the 'dark' state. This was followed by a room

temperature C-V run, exposure to another photon energy and a further C-V run. These processes were repeated until the whole energy range had been covered. Fig. 5.27 shows a plot of [V(dark)-V(light)]/V(dark) against photon energy. As for the DLTS results there appeared to be an optical threshold at about 1.0eV corresponding to the formation of E3.

5.2.3.3 SEM Results

The electron traps E3 and E4 were associated with the annealing of the CdS dice. In an effort to identify their origin, it was thought that one possibility was that they were associated in some way with electrically active extended defects such as grain boudaries. This suggestion arises from the fact that the DLTS peaks for these traps were broad and unlike those predicted by DLTS theory. In addition the capacitance-voltage measurements give very high values for the intercept voltage which would be expected if a strong interfacial layer were present. A study of the surface may give some idea of its source.

The etched samples were investigated using scanning electron microscopy (SEM) to image any extended defects, if present, and electron beam induced current (EBIC) to image any electrical activity at these defects.

Fig. 5.28 shows two SEM micrographs. The first of these shows the surface of sample 647 which displayed E3 and E4 and the second of sample 519 which did not. There is clear evidence of subgrain boundaries for 647. These would

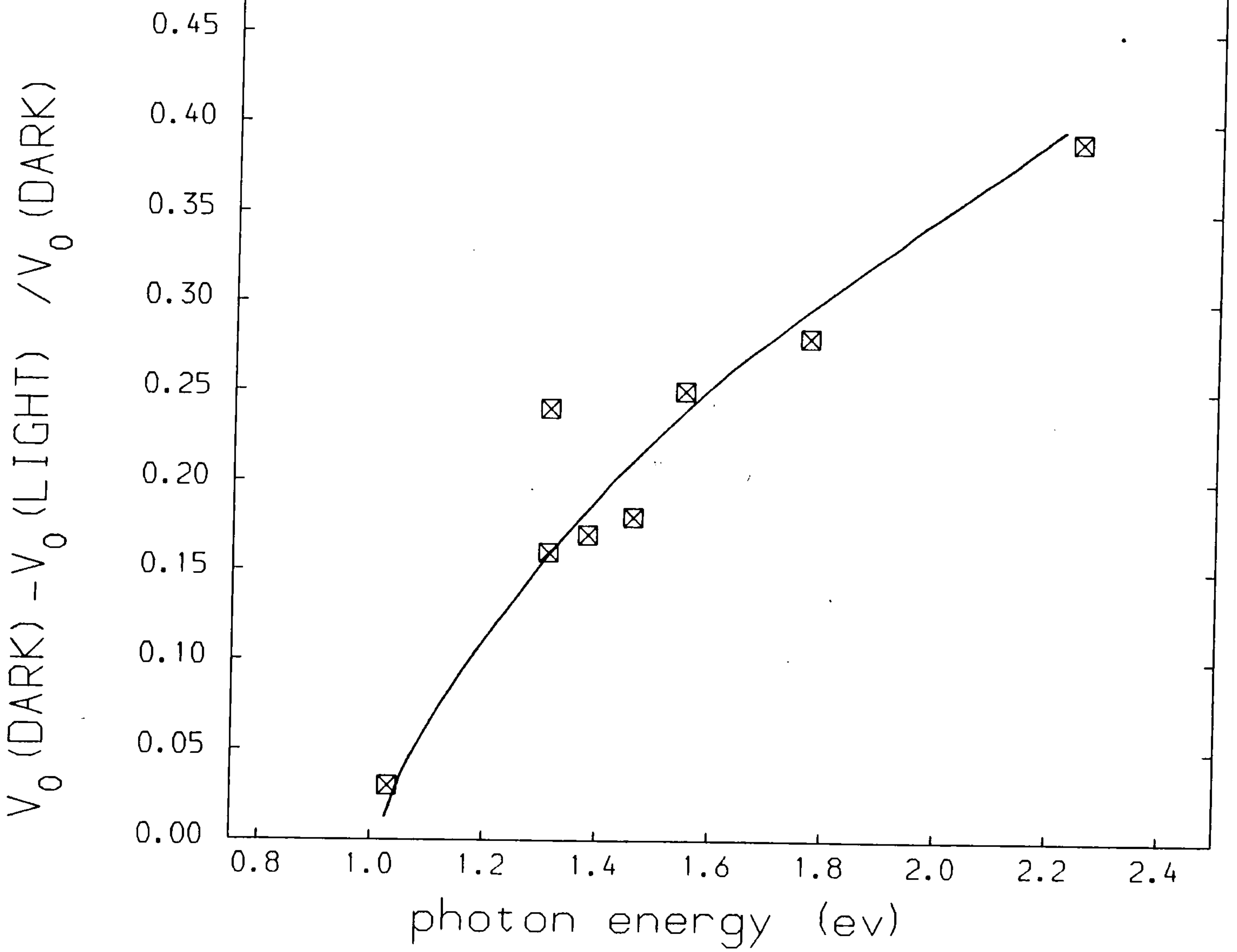
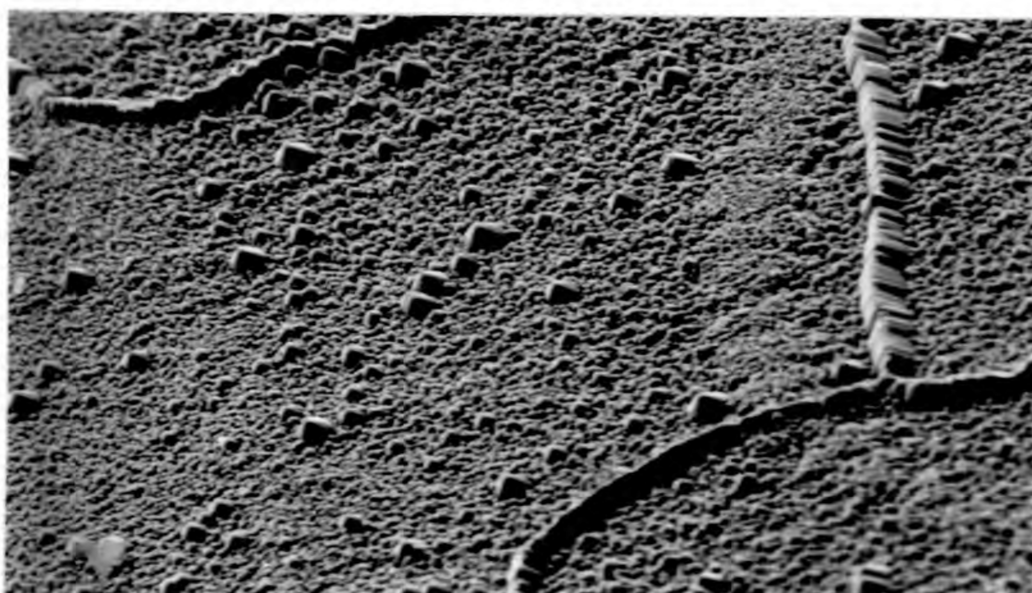
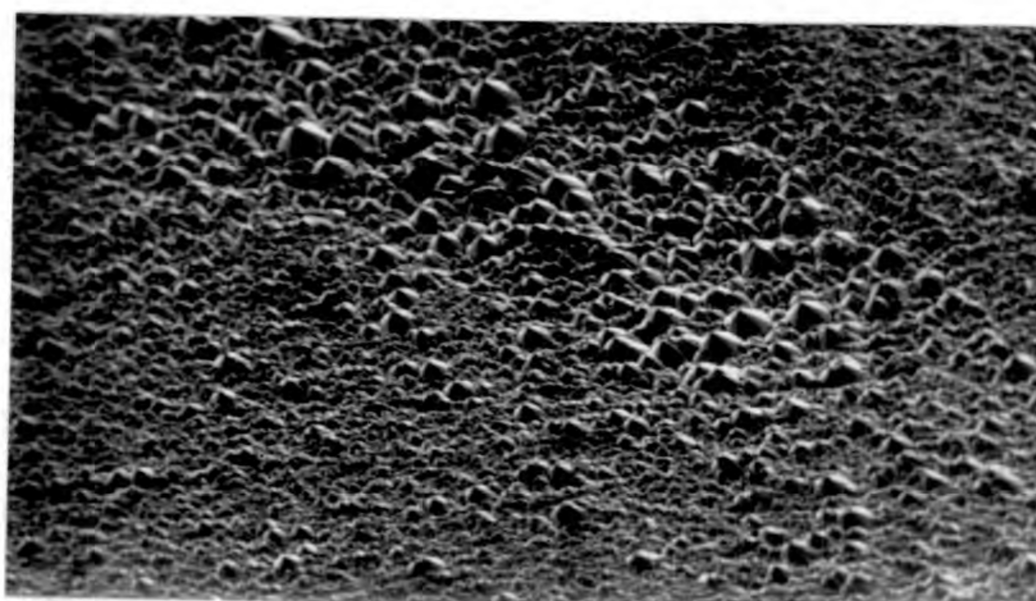


Figure 5.27 Plot of normalised voltage intercept as a function of the energy of illumination prior to the C-V scan



(a)



(b)

Figure 5.28 SEM micrographs CdS showing
(a) surface with subgrain boundaries
(b) without subgrain boundaries

appear at the interface of the CdS/Au junction. The SEM micrograph of the surface of 519 was typical of those samples in which E3 and E4 were not resolved by DLTS - there was no evidence of the surface features seen on 647. Sample 799, also displayed E3 and E4 but only had one grain boundary through the sample; one grain was oriented along the c-axis, the other about 20° off the c-axis. There was no evidence of extended defects in sample 759 although it also contained E3 and E4. EBIC on the Schottky diode of sample 537 which contained E3 and E4, did not show electrical activity along the whole length of the extended defect but only at isolated points - this is shown in fig. 5.29. Sample 647 showed no clear evidence of electrical activity at these extended defects, though this was thought due to a poor device quality. The samples which showed the presence of E1 and E2 only, were well oriented crystals with no indication of extended defects as shown for comparison in fig 5.28.

The SEM results were qualitative inasmuch as they gave credance to the suggestion that E3 and E4 were related to extended defects. There was no clear relation between the density of the extended defects and the density of the traps nor with the high V(0) value. However, the etchant used is not designed to delineate extended defects and in addition, the surface examined was the rough sulphur face. These two factors would make any quantitative assessment difficult from these results.

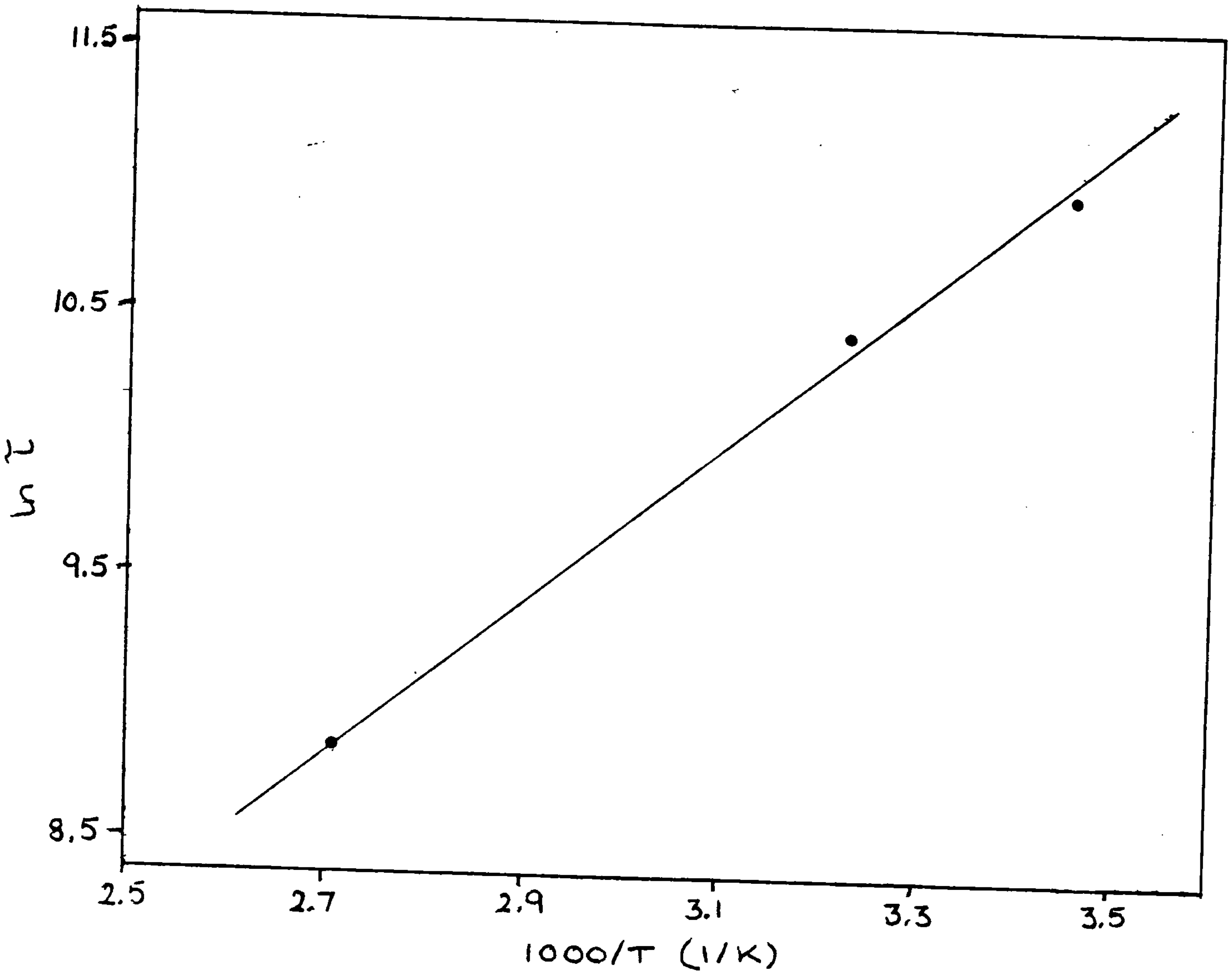
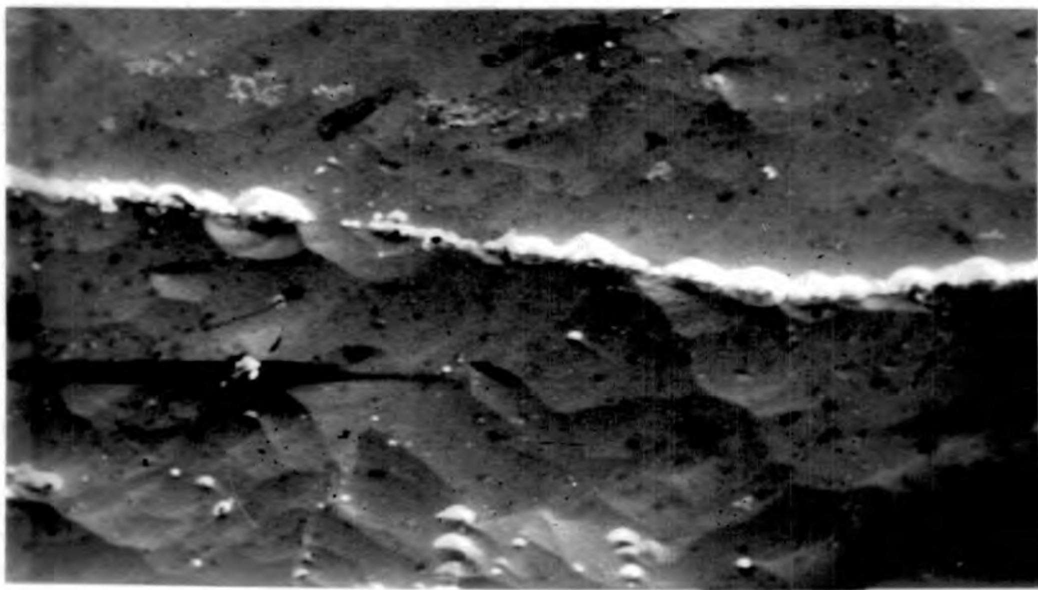


Figure 5.26 Arrhenius plot for the T dependence of V(0)



20μ

(a)

20μ

(b)

Figure 5.29 SEM micrographs of CdS surface through a Au contact
(a) secondary emission mode
(b) EBIC mode

5.2.4 Discussion

Four DLTS peaks have been observed in single crystal CdS each due to an electron trapping centre in the bulk material - E1(0.29eV), E2(0.44eV), E3(0.61eV), E4(0.74eV). These values are compared with DLTS data obtained by other workers in fig. 5.30.

The two peaks associated with E1(140K) and E2(200K) appear in all our as-grown as well as Cd and S annealed CdS. These have been associated with two deep level donor states in the bulk [13]. These two levels have been reported by other workers as shown in fig. 5.30 and it has been suggested that they are due to native defects [13]. From our results, the fact they were present in all our material, it seems very likely that they are indeed due to native defects. Their capture cross-sections are of the order of 10^{-15} cm^2 for E1 and 10^{-14} cm^2 for E2. This suggests that E1 is electrically neutral having negligible coulombic attraction or repulsion for electrons and that E2 is slightly attractive to electrons [29]. Hussein et al [8] have carried out direct measurements of the capture cross-sections of these traps, and although they have reservations about their data, have suggested that E1 as a capturing centre is electrically neutral and capture occurs with a very weak lattice relaxation ($\sigma_n=10^{-14}$ cm^2), and E2 has a strong lattice relaxation ($\sigma_n=10^{-12}$ cm^2). There is a large discrepancy between their value for E2 and that published by others, including these results, (see fig. 5.30).

C.B.

$(E_C - E_T)$ / eV

0, 0·1, 0·2, 0·3, 0·4, 0·5, 0·6, 0·7, 0·8, 0·9, 1·0, 1·1, 1·2, 1·3, 1·4

[8]: 10^{-14}, 10^{-12}, 10^{-11}, 10^{-14}, 10^{-11}

[9]: $1·4 \times 10^{-12}$, $2·2 \times 10^{-13}$, $2·2 \times 10^{-15}$, $4·8 \times 10^{-15}$, $7·3 \times 10^{-15}$, $4·2 \times 10^{-14}$, $1·25 \times 10^{-16}$

[10]: 10^{-14}, 10^{-12}, 10^{-12}

[11]: $1·4 \times 10^{-14}$, $7·0 \times 10^{-16}$, $5·0 \times 10^{-15}$

[12]: $2·6 \times 10^{-11}$, $5·1 \times 10^{-12}$

[13]: $6·4 \times 10^{-16}$, $5·3 \times 10^{-15}$, $2·0 \times 10^{-16}$

[14]: $10^{-16} - 10^{-15}$, $10^{-14} - 10^{-13}$

[15]: $10^{-16} - 10^{-15}$, $10^{-14} - 10^{-12}$, $4·4 \times 10^{-14}$, $5·6 \times 10^{-13}$, $2·7 \times 10^{-16}$, $5·1 \times 10^{-13}$

THESE RESULTS: $4·0 \times 10^{-15}$, $1·5 \times 10^{-14}$, $1·5 \times 10^{-15}$, $2·5 \times 10^{-15}$

Figure 5.30 Summary of the reported DLTS results on CdS

Verity et al [15] have shown that the the density of traps E1 and E2 increases with the free carrier concentration and over 3 orders of magnitude the relation is approximately linear. Verity et al [15] and Krispin [30] have described a model for traps whose density is proportional to the free carrier concentration. The basis for their model is a trapping centre that is an associate formed between native and impurity point defects. To emphasise the relation fig. 5.31 shows a plot of N_T vs N_d including information from various reported data for E2. For this trap Verity et al [15] derived an expression for the concentration of a singly ionised donor associate [C^o] at the high temperature of crystal growth between a singly ionised acceptor impurity [A'] and a doubly ionised native donor [D^{oo}]:

$$[C^o] = K\,[A']\,\frac{N_d}{N_c}\,\exp\left[\frac{E_c - E_d}{kT}\right] \qquad 5.3$$

where K is the rate constant for the formation of the trapping centre and $E_c - E_d$, the depth of the unionised donor below the conduction band. Equation 5.3 clearly shows a linear relation between the free carrier concentration and trap density and this is confirmed over several orders of magnitude in fig. 5.31. Krispin [30] and Verity et al [15] suggest that in such cases it is necessary to identify the defects giving rise to the trapping states as associates formed between native and impurity point defects. It is not clear which native and impurity defects may be involved. However, it is important to correlate possible mechanisms for the formation of defect states with growth conditions since

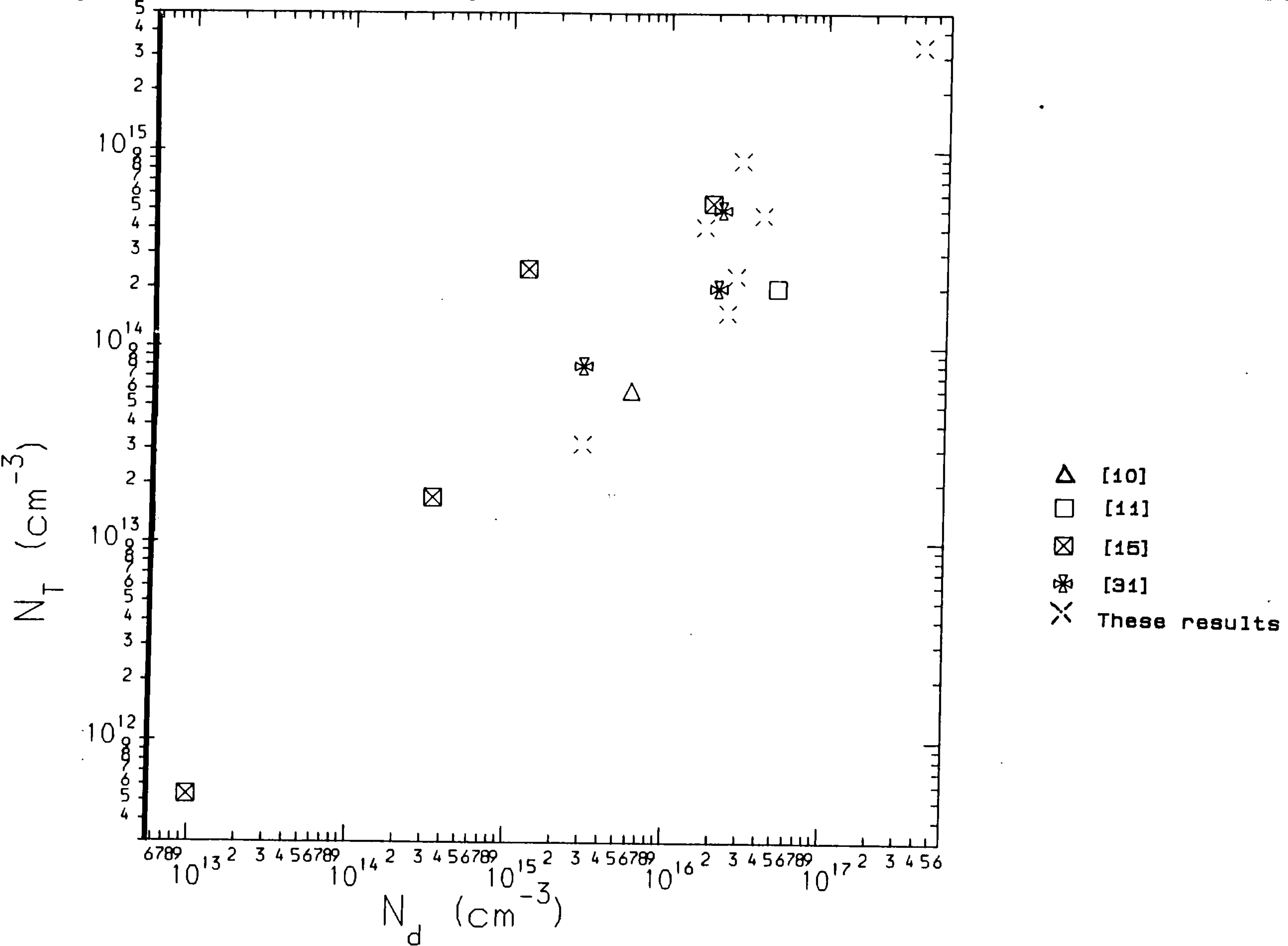


Figure 5.31 Plot of free carrier concentration as a function of the density of E2

they are very much related.

As previously discussed two electron traps, E3 and E4 have been observed in some CdS/Au devices with activation energies and capture cross-sections 0.61eV , 10^{-15} cm^2 , and 0.74eV, 10^{-15} cm^2 respectively. They have only been observed in samples that had undergone some post growth annealing; indeed this has been reported by Verity et al [15] and Poulin [31]. Similar effects have also been reported by other workers although there was no mention of the device history such as annealing treatments. Hussein et al [8,10] reported values for the capture cross-section of a trap with similar activation energy to E4 of the order of 10^{-11} to 10^{-12} cm^2; such a discrepancy with the value given here indicates that they are probably not due to the same trapping centre. Grill et al [9] reported a value of $1.25x10^{-16}$ cm^2 for E4 which is within experimental error for the trap observed here. The values reported by Verity et al [15] were 10^{-13} and 10^{-16} cm^2 for E3 and E4 respectively; the value for E4 is similar to that observed in the samples studied here but that for E3 indicates they may not be the same. Verity et al [15] subjected CdS samples to various Cd anneals and correlated this with DLTS measurements. After a treatment at 650C in molten Cd for 72 hours there was no apparent change in the DLTS spectrum compared to that obtained for the unannealed material. Only when samples were annealed in Cd vapour at 850C for 2 hours were additional trapping centres observed in the spectrum, including those corresponding to E3 and E4. The results presented here show that a much lower temperature (600C) anneal in Cd vapour can induce these traps but with

much longer anneal times (48 hours). It was also shown that they could be formed in samples that had undergone an anneal in S vapour at only 400C for 24 hours. Subjecting CdS to high temperture (>800C) for extended periods (>12hours) caused loss of material by sublimation; polycrystalline CdS formed in the cooler regions of the anneal ampoule.

An important property of E3 that has not been previously reported using DLTS was that it behaved as a photoinduced defect state. Photoinduced effects are well known in CdS and there are many such reported phenomena [1,4,6,32-35]. Albers [32] saw changes in the luminescence spectrum of CdS when illuminated with UV light at 273K and with subsequent heat treatment the original state was restored. Nicholas and Woods [1] observed a photochemically produced electron trap at 0.83eV ($\sigma > 10^{-15} cm^2$) using conductivity glow curve measurements. They found that the glow curve response at 290K was not simply due to electron emission into the conduction band but that this process was accompanied by thermal dissociation of the defect complex that gave rise to the state. It is not clear whether any of the phenomena previously reported corresponds with these results; the discrepancy in the activation energy may have arisen from the different techniques used. Previously reported DLTS results have clearly shown the presence of E3 but not the fact that it is photoinduced as shown by these results (see section 5.2.3.1). The evidence (see below) suggests that the defects are present in the subgrain boundaries; light activates the defect so that the process is electronic and when activated the states have a strong effect on the diode

capacitance-voltage behaviour.

The voltage intercept from a $1/C^2$ vs V plot should be of the order of 0.7V for a CdS/Au at room temperature. The samples that displayed the 'light'/'dark' effect had voltage intercepts larger than this - between 1.1V and 5.4V. The CdS investigated by Verity et al [15] had values of the order of 6V for samples containing the defect states E3 and E4. When the state of the device was changed from 'light' to 'dark' or vice versa there was a simultaneous change in the voltage intercept. The high voltage intercept could be attributed to localised charge near the surface of the junction [36] which could be due to deep interface states or deep levels at the subsurface of the device. This could increase the charge in the depletion region thereby giving an apparent barrier height greater than that expected for such a junction.

The C-V measurements show that although N_d remains constant, the voltage intercept V(0) changed between the 'light' and 'dark' states. However, when E3 was present ('light'), V(0) was smaller than the case when E3 was absent ('dark'). Crowell and Roberts [36] suggested that in the presence of a high density of deep lying impurity states then the apparent barrier height is less than the real barrier height for the metal-semiconductor contact. This is consistent with these results in that with E3 present the voltage intercept is reduced compared to the state when it is absent. The large intercept voltages for these samples are probably due to interface states as suggested by Crowell and Roberts [36] and Fonash [37].

The photoinduced effect observed here for E3 suggests that an electronic state of a specific defect could be induced by illumination. The threshold optical energy was obtained from repeated DLTS measurements after exposure of the sample to light of different energies; the transition energy for 'dark' state to 'light' state was found to be ~1.1eV. The thermal activation energy for the reverse process was obtained by monitoring V(0) from C-V measurements with time at different temperatures. This gave time constants for the decay of E3 in the dark so that from an Arrhenius plot an energy could be determined for the 'light' state to 'dark' state transition; this was found to be ~0.25eV. However, the mechanism for these processes and how these states relate to the DLTS results, is not clear.

The absolute nature of E3 and E4 is not clear from the DLTS measurements. However, they seem to appear only in samples that have been annealed in some manner; this has been observed by other workers [15,31]. It was thought that they may be due to clouds of point defects associated with extended defects such as dislocations at the sample surface. Vyvenko and Schröter [14] have come to such a conclusion for two deep levels near midgap in CdS which were only observed in the presence of low angle grain boundaries. They used DLTS for their measurements which showed peaks at 410K and 470K. These had activation energies 0.9eV and 1.3eV. Using SEM and EBIC they observed that electrically active subgrain boundaries were present in samples containing these two centres. In addition to these two traps two others were observed in their samples which correspond in temperature

with E3 and E4 observed here; however, they made no comment on these traps. They did however, present results showing that E3 and E4 were not present in samples devoid of the electrically active subgrain boundaries. The possibility that E3 and E4 could result from deep states at extended defects can be linked to the annealing process by the fact that grown-in or stress induced dislocations could aggregate to form subgrain boundaries (dislocation polygonisation [38]) which has been observed for CdTe [39,40]. The dislocation density around such systems would be high. The DLTS signal may be due to electrically active dislocations with sites along its length that give electronic states within the band gap, or it may be due to point defects that aggregate at the extended defects during the annealing process. These types of defects give rise to states with a broad distribution in energy [41]; this could account for the DLTS peaks which are broader than predicted from theory. EBIC measurements showed that only specific sites along the subgrain boundaries were electrically active. This suggests that the the defect levels arise from core states in specific types of electrically active dislocations rather than point defect clouds which would be more likely to be homogeneously spread along these extended defects.

It seems probable that the formation of E3 and E4 is not sensitive to the annealing ambient since they were seen in Cd and S annealed samples. This may seem inconsistent bearing in mind the high temperature of crystal growth and that in as-grown samples E3 and E4 were not observed. However, after crystal growth the boules were cooled to room temperature

over a period of three days whereas after annealing the samples were quenched to room temperature in water within a few seconds. Such a process is likely to induce strain in the crystal and produce a high density of dislocations [38] which could give rise to a sufficiently high density of deep defect states that they were observed by DLTS. Such states may indeed be present in as-grown CdS but were outside the limits of resolution of the DLTS system.

Simoen et al [42] have studied dislocations in Ge using DLTS. They found that their DLTS peaks were 3-4 times broader than that expected for a single level peak. Figs 5.19 and 5.20 show the theoretical peaks for E3 and E4 compared with the experimental results - E3 was found to be twice and E4 three times as broad as that theoretically predicted. Such broadening is thought to be indicative of a continuum of states such as those associated with extended defects [41]. The capacitance transients for E3 and E4 were non-exponential as shown in figs 5.17 and 5.18; Schröter and Seibt [43] suggest that the occurrence of non-exponential emission transients is typical for extended defects.

The C-T results for such samples at quiescent reverse bias shown in fig. 5.12 display a steep drop at about the same temperature at which E4 was observed. This was due to carrier freeze out into the donor levels The drop was observed in both 'light' and 'dark' samples. Simoen et al [42] saw similar effects in Ge samples in which high dislocation densities were observed. A model was proposed by Mantovani [44]. Consider a diode with a dislocation density

D perpendicular to the junction; the effective diode area is

$$A = A(0)\ (1 - D\pi\lambda^2) \qquad 5.4$$

where A(0) is the geometrical diode area and λ the Debye length. Using the depletion approximation, $C=A\epsilon/w$ and so

$$C = C(0)\ (1 - D\pi\lambda^2) \qquad 5.5$$

where C(0) is the capacitance for D=0. The Debye screening length is given by

$$\lambda = \left\{\frac{kT\epsilon}{q\ N_d}\right\}^{1/2} \qquad 5.6$$

Therefore

$$C = C(0)\left\{1 - \frac{D\ kT\epsilon\pi}{N_d\ q}\right\} \qquad 5.7$$

To a first approximation this predicts a linear drop in the capacitance with increase in temperature and this becomes more pronounced with higher dislocation densities as shown by Simoen's results. Using this approximation, the dislocation density for sample 799 was 3×10^{10} cm^{-2} for the 'light' state and 7×10^{10} cm^{-2} for the 'dark' state. Similar results were obtained for other CdS samples containing E3 and E4. Vyvenko and Schröter [14] obtained much lower dislocation densities ($\sim10^5$ cm^{-2}) although it is not clear how they obtained this value.

Four dominant electron traps have been characterised in CdS; these have been denoted E1, E2, E3 and E4. E1 was found in most samples studied. E2 was thought to have its origin in associates between native and impurity point defects resulting from the high temperature of growth and consequently, it was observed in all the samples. E3 and E4 were observed only in samples that had undergone some post-growth annealing treatment. They have been associated with annealing induced dislocations although their absolute origin is not clear. The trap E3 was found to be photoinduced and decaying when left in the dark.

5.3 Hole Traps in CdS

5.3.1 Introduction

ODLTS, DLOS and PHCAP measurements have been carried out on undoped and copper doped CdS Schottky devices and CdS/Cu_2S heterojunctions. This was in an effort to characterise the thermal and optical properties of deep level acceptor states in undoped material. These measurements were correlated with results on copper doped CdS and the heterojunctions to study the states induced by the copper. It is well known that copper diffuses across the junction of a CdS/Cu_2S device during the optimising heat treatment [45]. This results in a reduction of the short circuit current; the acceptor states act as recombination centres leading to a reduction in the free carrier lifetime. Therefore it is important to understand the nature of these defects. Indeed, several studies have been carried out using various techniques - IRQPHCAP - CdS/Cu_2S [18], CdS:Cu[19]; ODLTS - CdS/Cu_2S,

CdS:Cu [13]. The results presented here show the properties of these defects as revealed by ODLTS and DLOS.

5.3.2 Copper Doping of CdS

Copper doping of CdS was achieved by evaporating a thin film of copper onto one surface of the previously etched CdS single crystal dice. The solubility of Cu in CdS is [45]

$$[Cu]=6.6x10^{22}exp(-0.505eV/kT)\ cm^{-3} \qquad 5.8$$

To ensure a homogeneous distibution of Cu, the crystals were annealed at 600C for 24hrs in an argon atmosphere. Grimmeiss et al [19] annealed their samples at 800C for 10hrs in vacuum, however, using this method of doping the CdS samples suffered substantial material loss (5% by weight). CdS/Cu_2S heterojunctions have been prepared by the dry barrier technique [46]. CuCl was evaporated onto one surface of the previously etched CdS dice and this was followed by a heat treatment at 200C for 2mins to give the ion exchange reaction

$$CdS + 2CuCl \longrightarrow CdCl_2 + Cu_2S$$

The $CdCl_2$ was washed off in ethanol. From the above equation (5.8) one expects a copper concentration of the order of 10^{17} cm^{-3} for an anneal at 200C. A gold layer was evaporated onto the Cu_2S to give the top contact to the sample. In all cases the Ohmic contact was made by annealing indium onto the back surface at 200C in an argon atmosphere.

Atomic absorption measurements were carried out to determine the copper concentrations in the doped and undoped samples; the results are shown in fig. 5.32. This shows the disturbing result that copper was present in undoped CdS.

5.3.3 ODLTS Measurements

ODLTS measurements were carried out on undoped CdS and Cu doped CdS Schottky diodes and CdS/Cu_2S heterojunctions in the temperature range 80-380K. The ODLTS response was found to be dependent upon light intensity - the higher the intensity, the stronger the ODLTS reponse giving a larger peak; and upon the photon energy of the light source (see fig. 5.33). For ODLTS scans using the Ar laser one peak at -120K (H1) gave a good response. Using a He/Ne laser or 'sweet spot' LED (820nm), H1 was poorly resolved and a second trap, H2 at 330K, became prominent - this is shown in fig. 5.33. Fig. 5.34 gives the Arrhenius plots for H1 and H2. The activation energies and capture cross-sections were determined to be 0.34eV, 10^{-12} cm^2 and 1.1eV, 10^{-12} cm^2 for H1 and H2 respectively. For levels H1 and H2 the capacitance transients gave a reasonable exponential response as indicated in figs 5.35 and 5.36. The transient for H1 is given for a scan using the Ar laser, a similar scan using an IR bias light (1200nm), and again with a He/Ne laser giving the bias light. Both clearly show a resonable exponential decay and differ only in the magnitude.

All the samples studied showed the presence of H1 and H2, including the undoped material, although such material

SAMPLE	COPPER CONC. (ppm)	
808 (A)	0.92	copper doped
808 (B)	0.009	undoped
519	0.005	undoped
537	0.008	undoped
732	0.016	undoped
759	0.004	undoped
799	0.003	undoped

Figure 5.32 Copper concentrations in the CdS samples as determined by atomic absorption measurements

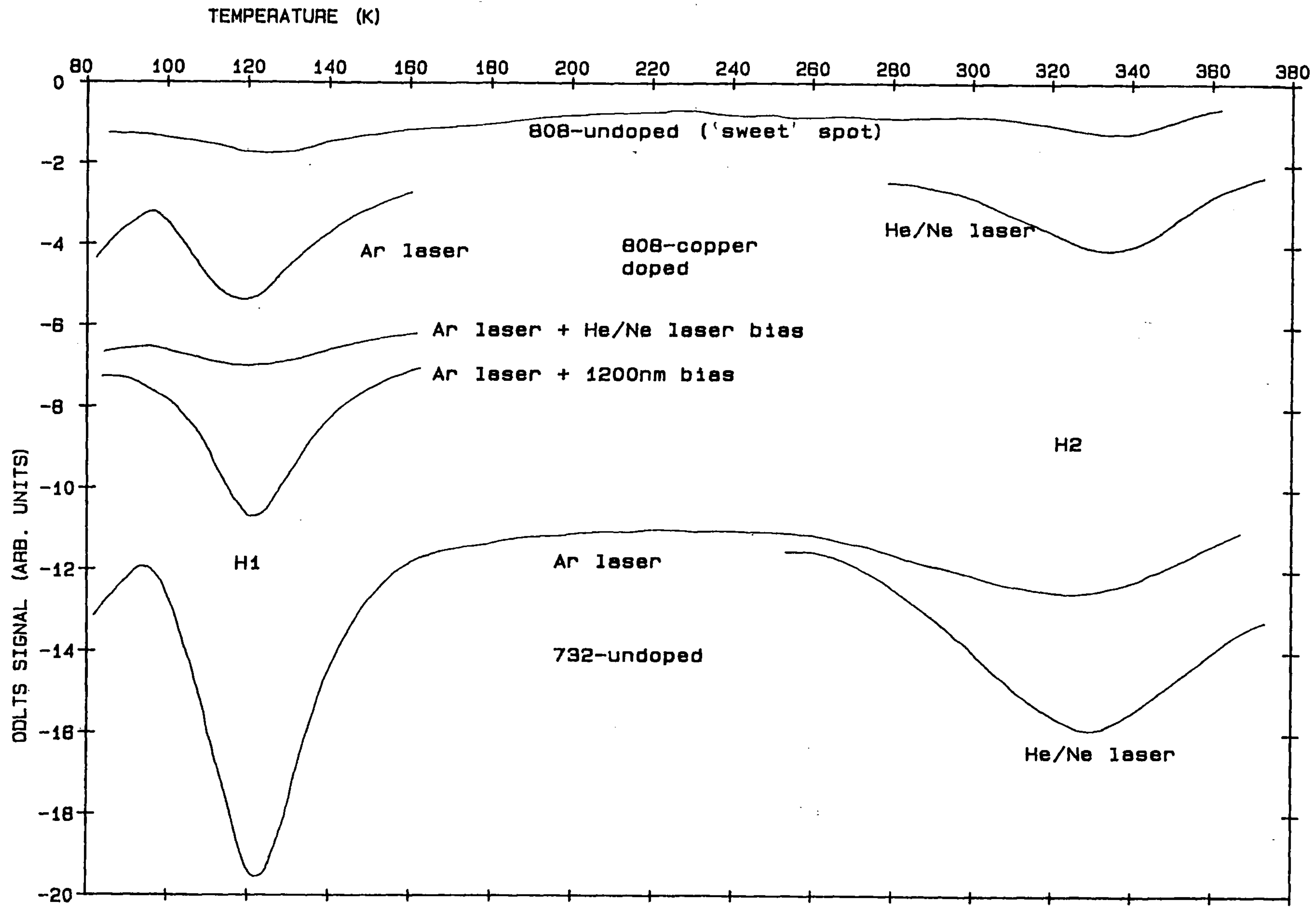


Figure 5.33 ODLTS spectra for CdS

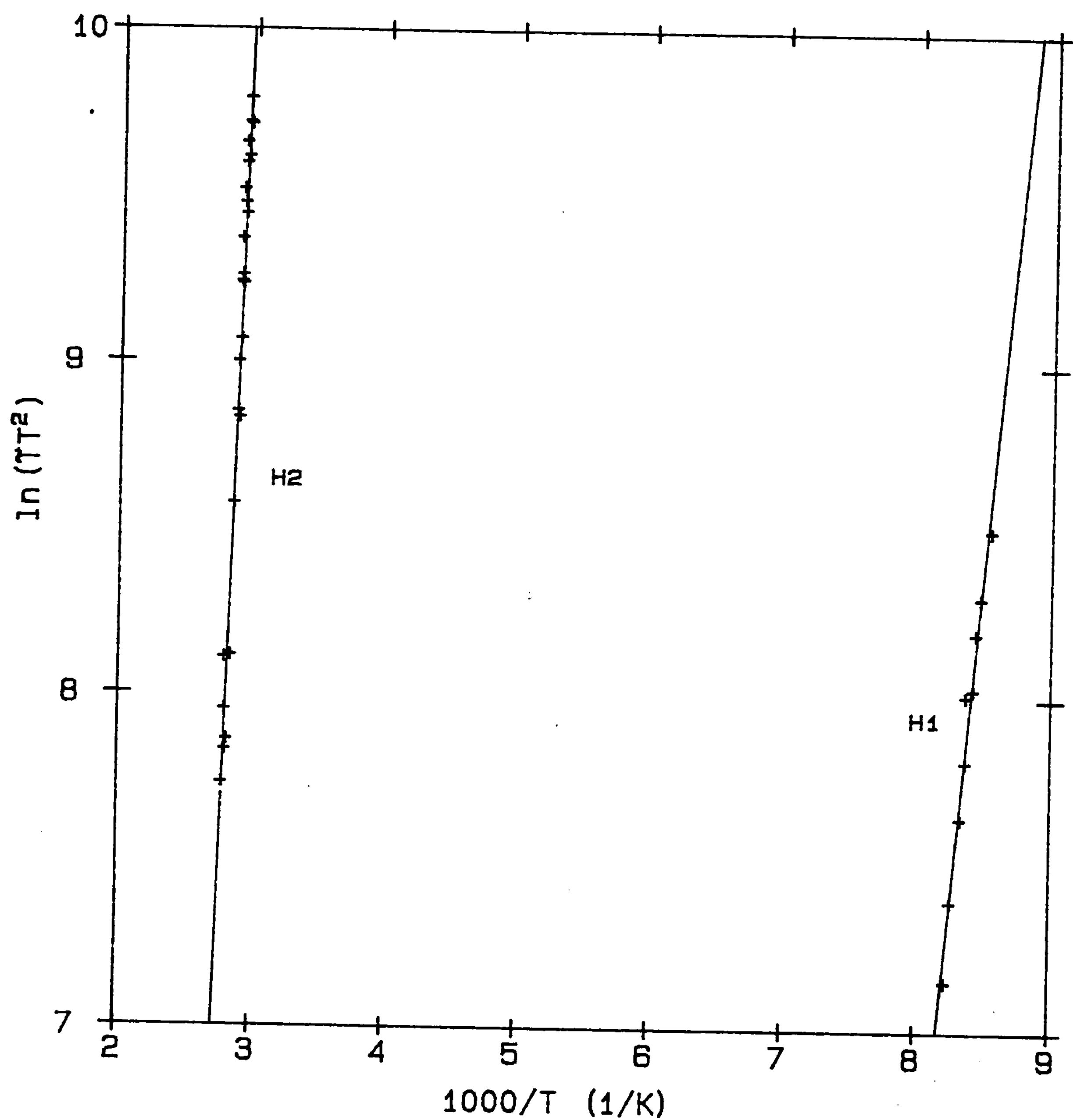
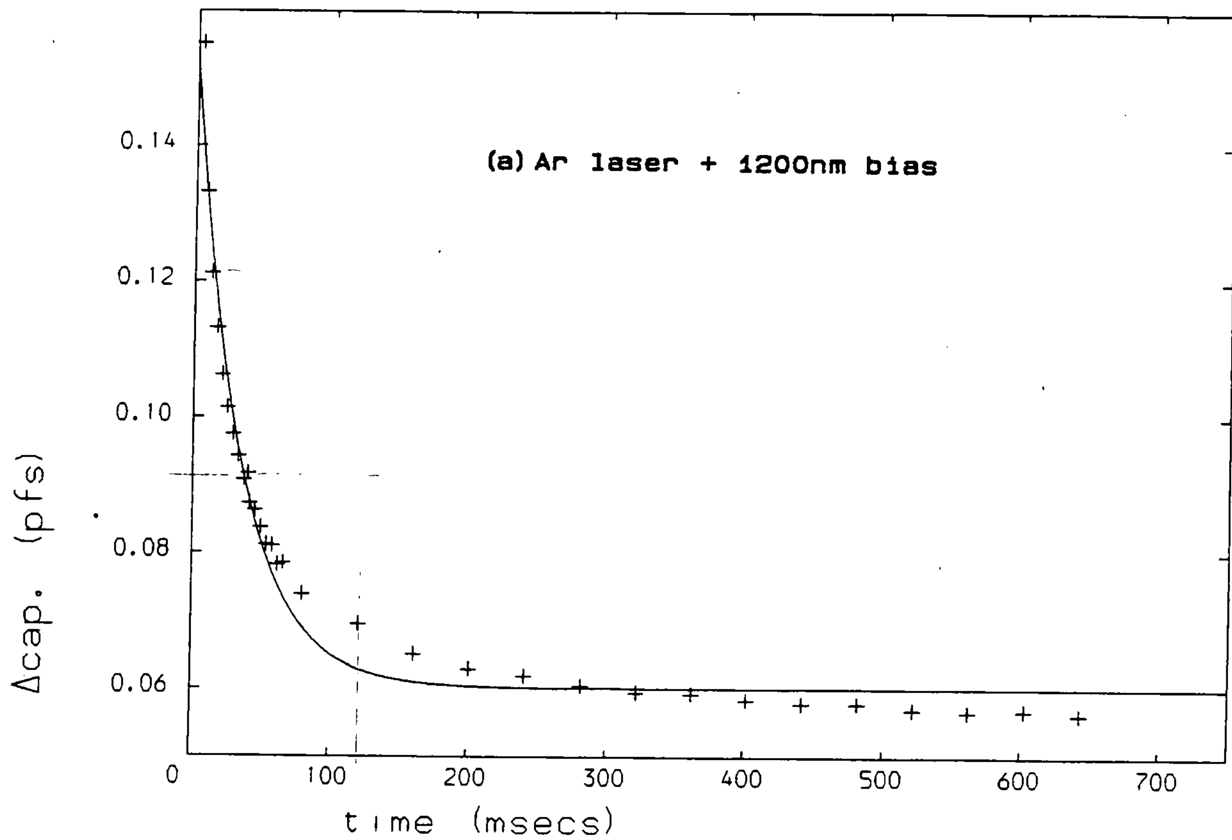
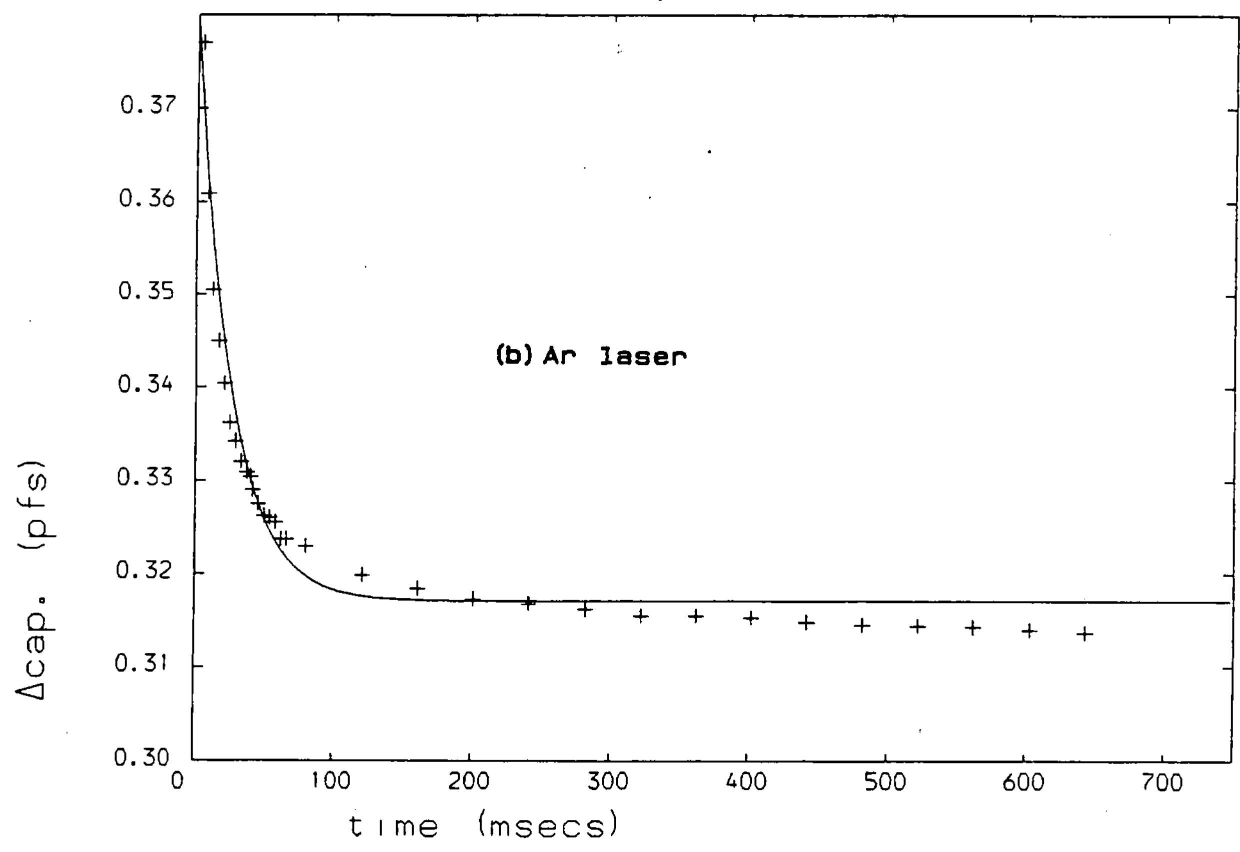


Figure 5.34 Arrhenius plots for the hole traps H1 and H2



FITTED PARAMETERS

P 1 = 0.601E-01 P 2 = 0.927E-01 P 3 = 0.343E02



FITTED PARAMETERS

P 1 = 0.317E00 P 2 = 0.635E-01 P 3 = 0.253E02

gure 5.35 Capacitance transients due to hole emission from H1 at 120K

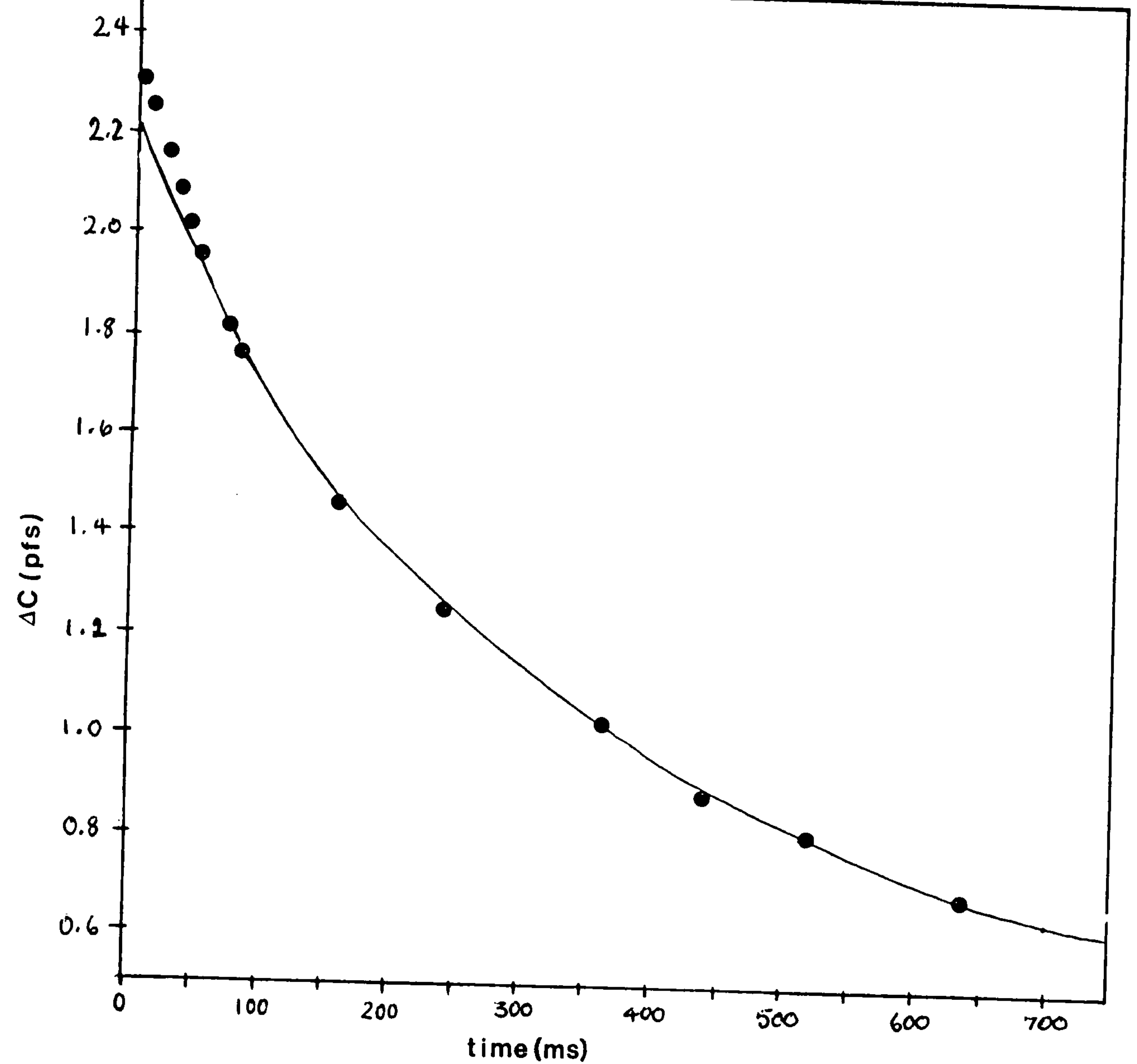


Figure 5.36 Capacitance transient due to hole emission from H2

gave a poor response - the ODLTS peaks only just being resolved. This reflects the problem of copper as a ubiquitous impurity in crystal growth and can only be eradicated with great difficulty. The 'undoped' photoconductive CdS sample gave the best ODLTS response

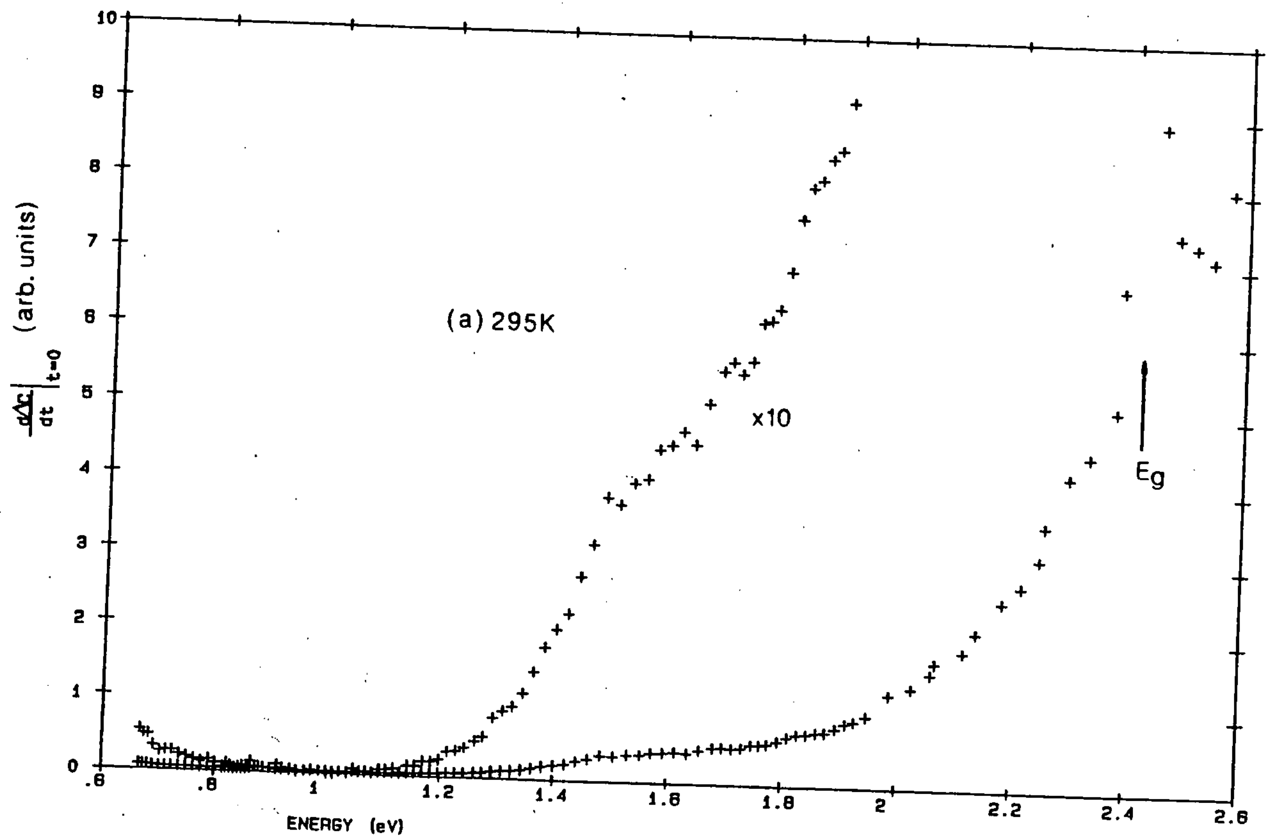
5.3.4 DLOS Results

DLOS was carried out in the manner described in section 4.7 to investigate the optical depth of traps from the conduction band in the range 0.7eV to 2.5eV. The main aim was to probe the deep levels near midgap which were inaccessible using the thermal dependent measurements DLTS and ODLTS, and the optical depth of the copper states.

Experiments were carried out at 290K and 85K. Fig.5.37 shows typical DLOS runs at these temperatures for 'undoped' and doped CdS. The room temperature spectrum has several thresholds : 2.09±0.02eV, 1.69±0.02eV, 1.30±0.02eV, the peak at 2.4eV is due to band-gap transitions. The DLOS curve giving the threshold corresponding to H2 is shown in fig. 5.38. The solid line is the theoretical Chantre fit [47]

$$\sigma_n^o = \frac{P1(h\upsilon - P2)}{h\upsilon(h\upsilon + P3)^2} \qquad 5.9$$

described in sections 3.4.4 and 4.7. The theoretical fit



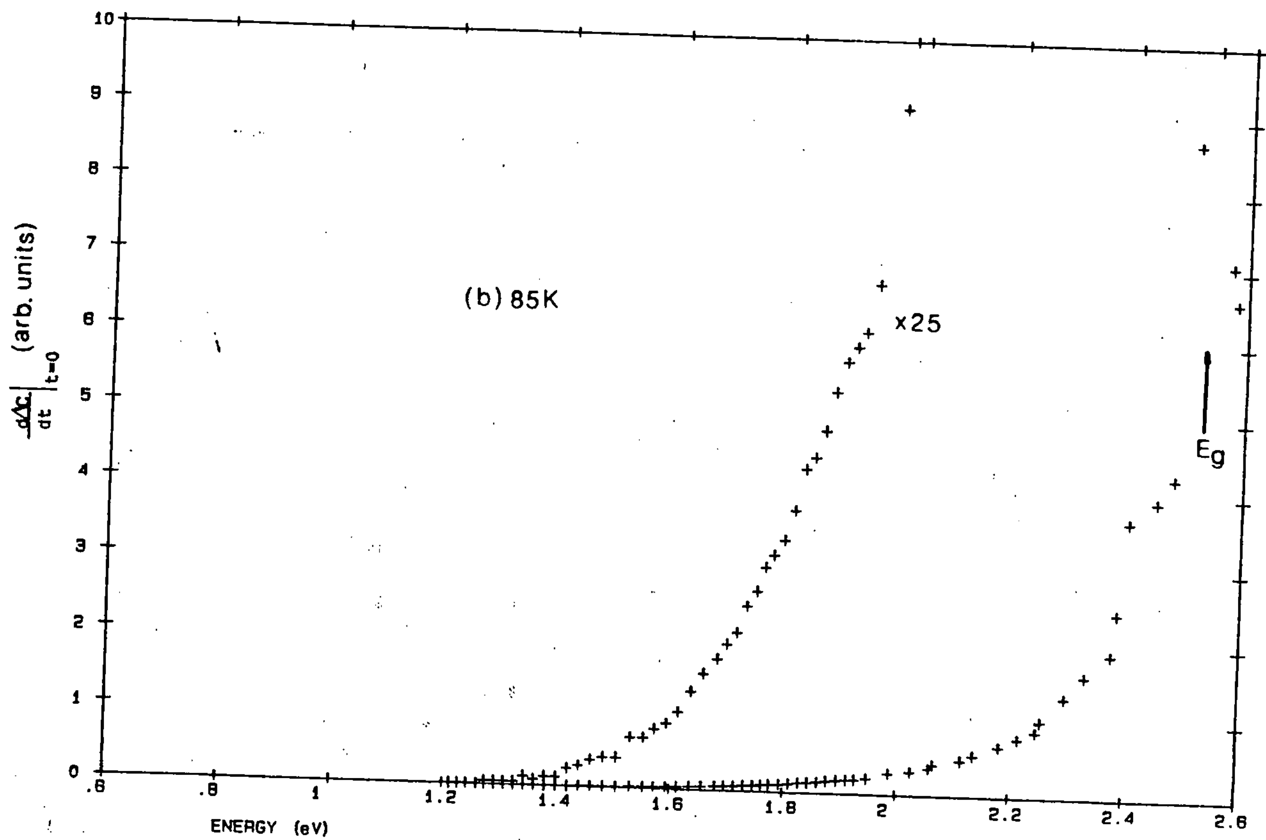


Figure 5.37 DLOS spectra for CdS

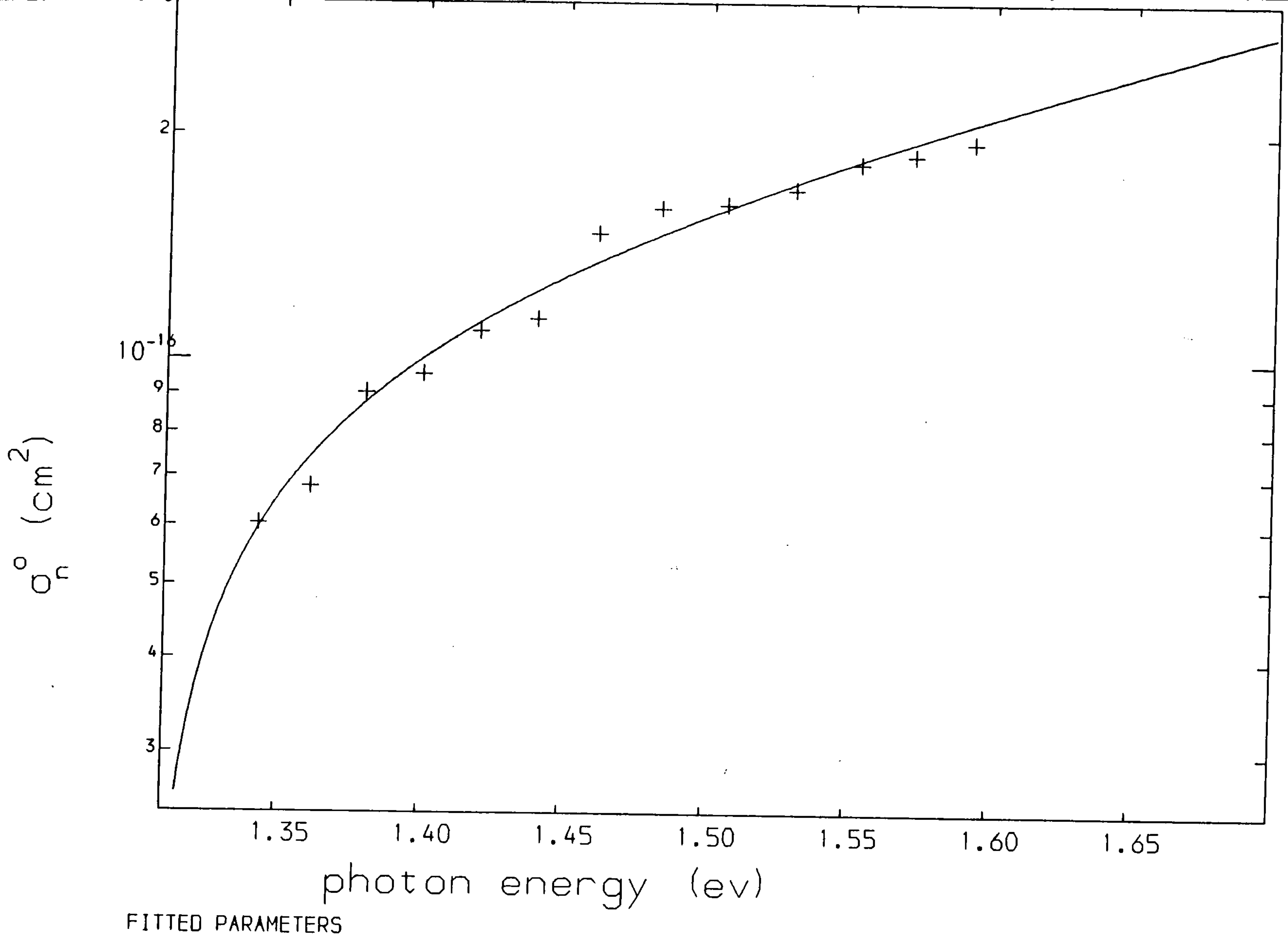


Figure 5.38 DLOS curve due to H2 showing the Chantre fit (solid line)

gave a threshold of 1.31±0.01eV. These optical thresholds correspond to depths below the conduction band and so, taking Eg=2.42eV their depth from the valence band is : 0.33±0.02eV, 0.73±0.02eV, 1.12±0.02eV. At 85K, the spectrum shows a similar trend but the deeper traps near midgap were much reduced. The DLOS spectra shown in fig. 5.37 were typical of 'undoped' and copper doped CdS and CdS/Cu_2S heterojuctions.

5.3.5 Discussion

The deep levels introduced by copper into CdS have been studied using ODLTS and DLOS. Two hole traps have been observed in ODLTS with thermal activation energies and capture cross-sections 0.34eV, 10^{-12} cm^2 and 1.1eV, 10^{-12} cm^2 for H1 and H2 respectively. The two states were clearly observed in all samples studied including undoped material although the ODLTS response was poor in such samples. The ODLTS transients gave a reasonable exponential decay indicating that the states obey the emission process required by DLTS theory [28]. Indeed, the ODLTS peak H1 correlated well with that theoretically predicted.

The DLOS spectra gave three threshold energies for traps below the conduction band - 2.09eV, 1.69eV, 1.31eV; these are 0.33eV, 0.73eV, 1.11eV respectively above the valence band. Two of these correspond well with the copper states observed in ODLTS. The remaining state had no obvious correpondence - no trap at 0.73eV above the valence band was seen in ODLTS. Indeed no such acceptor state has been reported although

Pande [16,22] observed a level 1.7eV below the conduction band from steady state photocapacitance. It was suggested that this was the copper level H2 and that the difference in activation energies arose from a Frank-Condon shift. However, this is clearly not the case since DLOS shows a threshold at 1.3eV below the conduction band (H2) in addition to the 1.7eV threshold. The fact that this state was not observed in ODLTS with an energy of 0.72eV suggests that it either has a large Frank-Condon shift such that its thermal activation energy is very much greater than its optical activation energy or it has a very small capture cross-section for holes. If the latter was the case then its capture cross-section would be less than 10^{-21} cm^2 (see equation 3.31). This would show it to be hole repulsive centre [29].

It is thought that the defect states attributed to copper result from substitutional copper ions on cation sites [19] as in the case of ZnS:Cu [48]. Broser et al [48] have suggested that the copper is in the 2+ state due to a charge transfer process which can change the ionisation state to the most stable ionised form. Photocapacitance results on CdS [18,19] and $CdS_{1-y}Se_y$ [49] have shown two acceptor states which have energies that correlate well with those obtained here. The two states arise from a crystal field splitting of the unperturbed Cu d^9 state assuming that the defect is a substitutional Cu^{2+} - this has been discussed in section 2.5.4. The ground state corresponds to a hole trapped on the ^2E level - this is H2, 1.1eV above the valence band. The excited state corresponds to the hole tapped on the $^2T_2$

level, giving H1, 0.34eV above the valence band (see fig.5.39). Grimmeiss et al [19] have proposed an internal transition between the states H1 and H2; this would be a dipole forbidden, d-d transiton which will be allowed since the real wavefunctions are probably not of pure d character in the environment of CdS. The lifetime of the dipole allowed transition is of the order of 10ns, whereas the lifetime for the internal transition observed by Grimmeiss was two orders of magnitude greater.

Poulin at al [13] also showed two states for CdS/Cu_2S and CdS:Cu using ODLTS with energies of 0.34eV and 0.93eV. The value for H1 is similar to that obtained by Poulin but H2 does not give such a good correlation although it is just within experimental error.

EPR measurements on CdS:Cu have been reviewed by Watts [50] and there is considerable evidence for resonances due to copper. Schulz [51] obtained a value for the crystal field splitting, that is, the difference in energy between the ground and excited copper states, of 0.69eV which correlates well with previous results as well as those presented here. Cluster calculations of copper impurity states in CdS, ZnS and ZnO [52] give satisfactory agreement with the experimental crystal field splitting confirming the validity of the interpretation used above. These results with those obtained by other workers are summarised in fig 5.40.

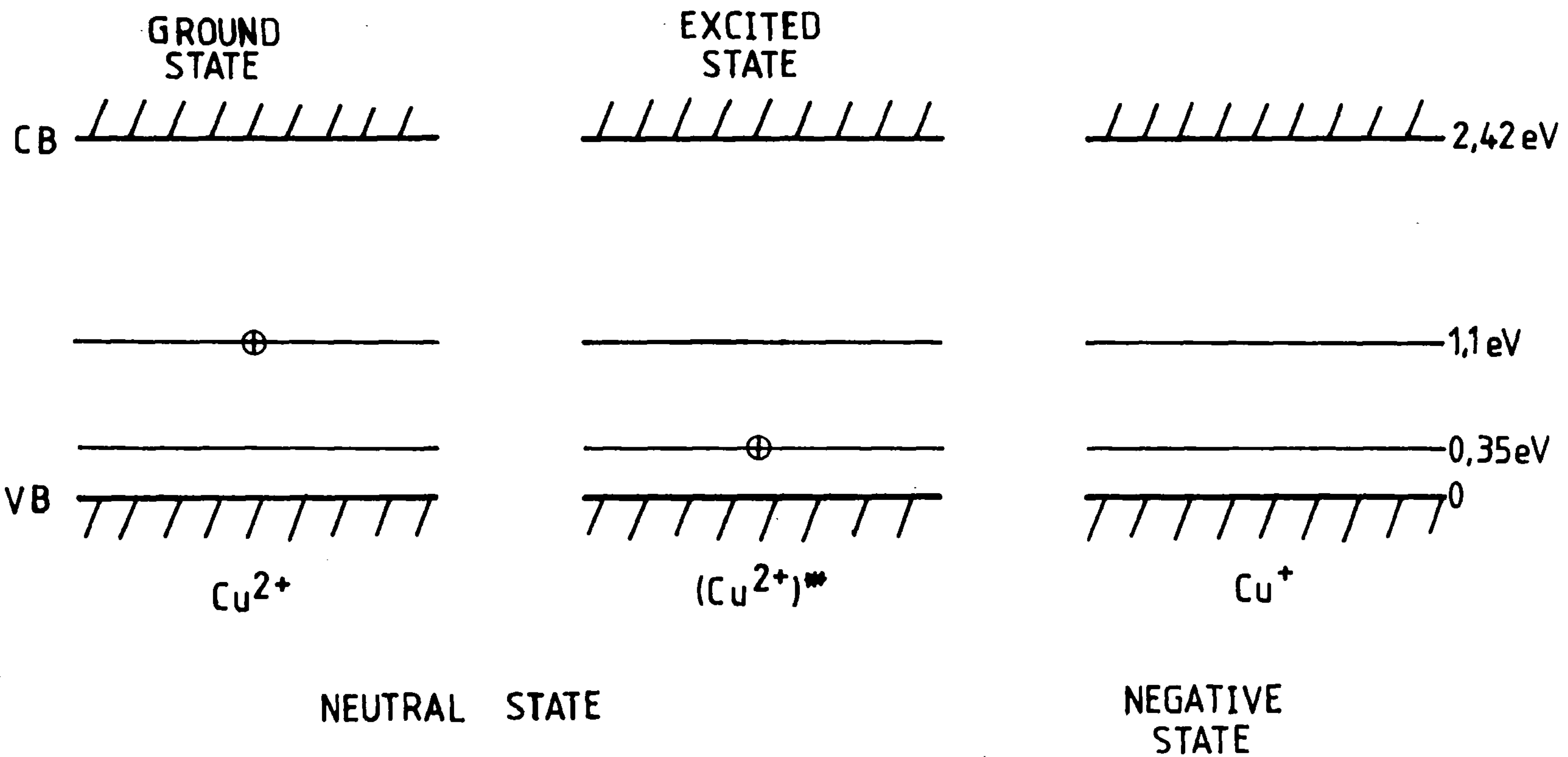


Figure 5.38 Energy level scheme for the copper states in CdS [18]

Analysis	Crystal Field Splitting of the Cu d^9 state
Theory	0·67eV [52]
PHCAP	0·76eV [19]
EPR	0·69eV [50]
ODLTS	0·59eV [13]
ODLTS	0·70eV } These Results
DLOS	0·70eV } These Results

Figure 5.40 Reported values for the crystal field splitting of the copper d^9 state in CdS

5.4 Tellurium Doped CdS

5.4.1 Introduction

$CdS_{1-y}Te_y$ is recognised as a potentially useful material. However, one of the main difficulties in its preparation is that Te has a low solubility in CdS. Kurik and Vitrikhovskii [53] could only obtain compositions for x up to $3.5x10^{-3}$. Recent reports have shown that the material can be obtained over the whole compostion range but only in thin film form [54]. At low concentrations, Te can behave as an isoelectronic, substitutional impurity, occupying sulphur sites in the lattice [55]. It is one of the few isoelectronic impurity systems that forms bound states in II-VI semiconductors [23]. Tellurium doped CdS exhibits a high luminescence efficiency [23-25,55,56]. And its potential as a γ-ray detector has been reported [57].

The tellurium states may also be detrimental to the operation of a photovoltaic device. There have been several publications reporting sintered CdS/CdTe solar cells [26,27,58]. Nakayama et al [58] have shown that at the interface there is a thin layer consisting of a solid solution of CdS-CdTe. This infers the possibility that there is diffusion of S into the CdTe and Te into the CdS.

It was the purpose of this work to characterise the main trapping centres in Te doped CdS using DLTS, ODLTS and DLOS.

5.4.2 Materials

Two types of samples were used in this study obtained from boules 519 and 537. Both were grown using the vertical growth method described in section 4.2. Boule 537 was grown in excess cadmium with 500ppm Te included in the CdS charge. Boule 519 was grown in excess sulphur and the Te doping achieved by adding CdTe to the charge. Atomic absorption measurements gave the following tellurium and copper concentrations

Sample	[Te]/ppm	[Cu]/ppm
519	0.01	0.005
537	0.59	0.008

Resistivities were in the range 100 Ω cm to 5k Ω cm. Schottky devices were prepared in the usual way for CdS as described in section 4.3. Capacitance-voltage measurements gave free carrier concentrations of the order of 10^{16} cm^{-3}.

5.4.3 DLTS Results

DLTS was used to characterise the main electron traps in CdS:Te (see fig. 5.41). The spectra were typical for the undoped samples as described in section 5.2.2; samples from boule 519 gave a good response for E2, whereas, E1 was poorly resolved and there was no indication of E3 and E4. Samples from 537 gave a clear response for all the electron traps previously observed in CdS - E1-E4 and diplayed the 'light' - 'dark' transition for E3 as described above. Samples 537(a)

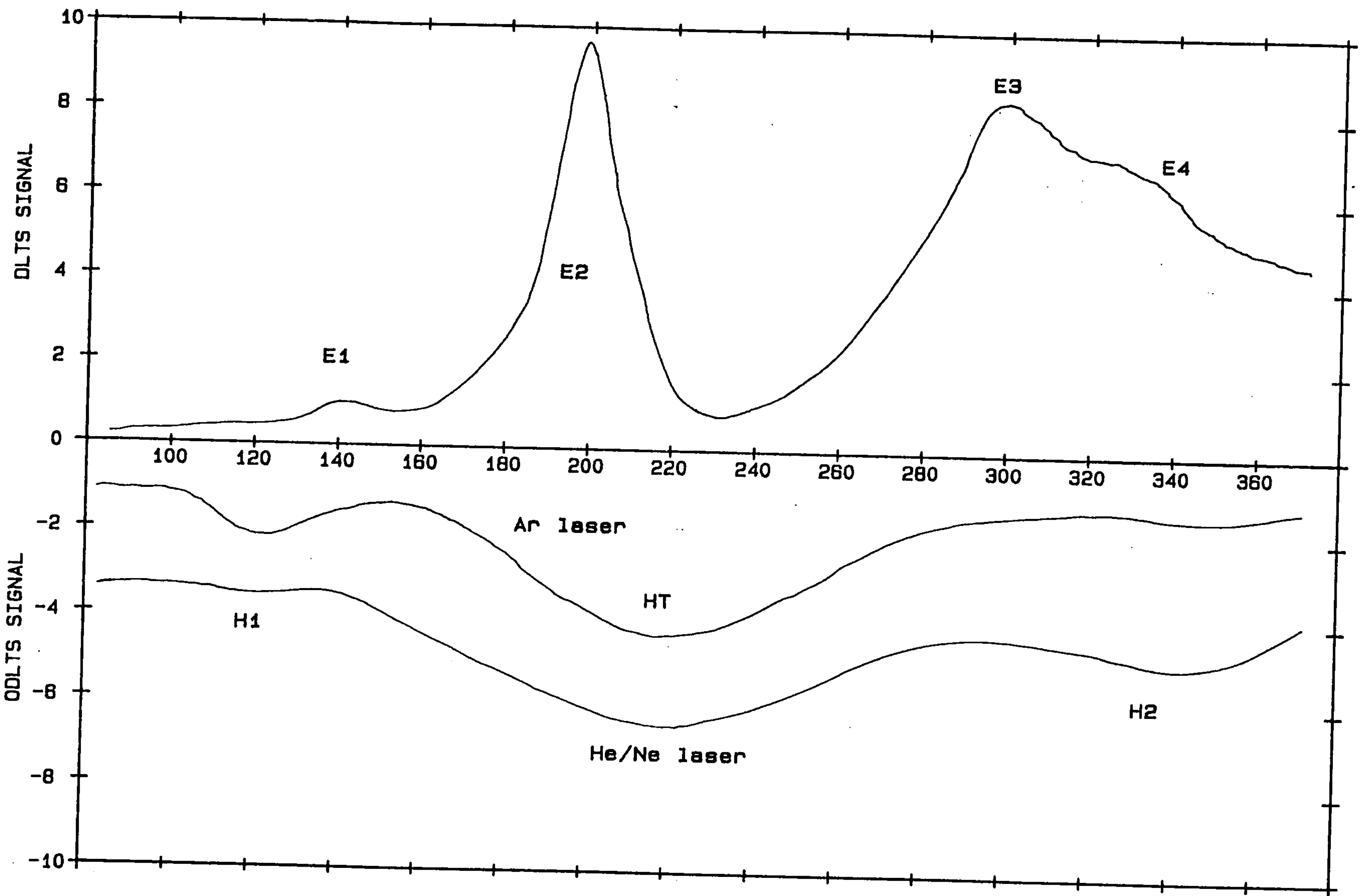


Figure 5.41 DLTS and ODLTS spectra for Te-doped CdS

and 537(b) had a high density of subgrain boundaries at the surface as imaged by SEM and these showed electrical activity in EBIC mode (see fig. 5.29). Samples from 519 indicated no such extended defects and as expected neither E3 nor E4 were present.

5.4.4 ODLTS Results

The main hole trapping centres were studied using ODLTS; all samples gave an ODLTS response similar to copper showing two peaks, H1 and H2, at 120K and 350K. In addition, a broad peak, HT, was observed at 200K; this occurred in all spectra. This corresponded to a hole trap not observed in undoped CdS. Using Ar laser, He/Ne laser and 'sweet spot' LED light sources, ODLTS scans gave spectra as shown in fig. 5.41. From the Arrhenius plot (see fig. 5.42) the activation energy and capture cross-section were found to be 0.21eV and $10^{-20}cm^2$. The capacitance transient for HT at 215K is given in fig. 5.43 and is clearly nonexponential.

5.4.5 DLOS Results

DLOS was carried out at 290K and 85K in the photon energy range 0.7eV - 2.5eV to determine the energy distribution of the optical electron capture cross-section. A typical spectrum is shown in fig. 5.44. In addition to the thresholds usually observed in undoped CdS at 1.3eV, 1.7eV and 2.1eV which were dicussed in section 5.3.4, a fourth threshold occurred at 2.2eV corresponding to a hole trap 0.22eV above the valence band.

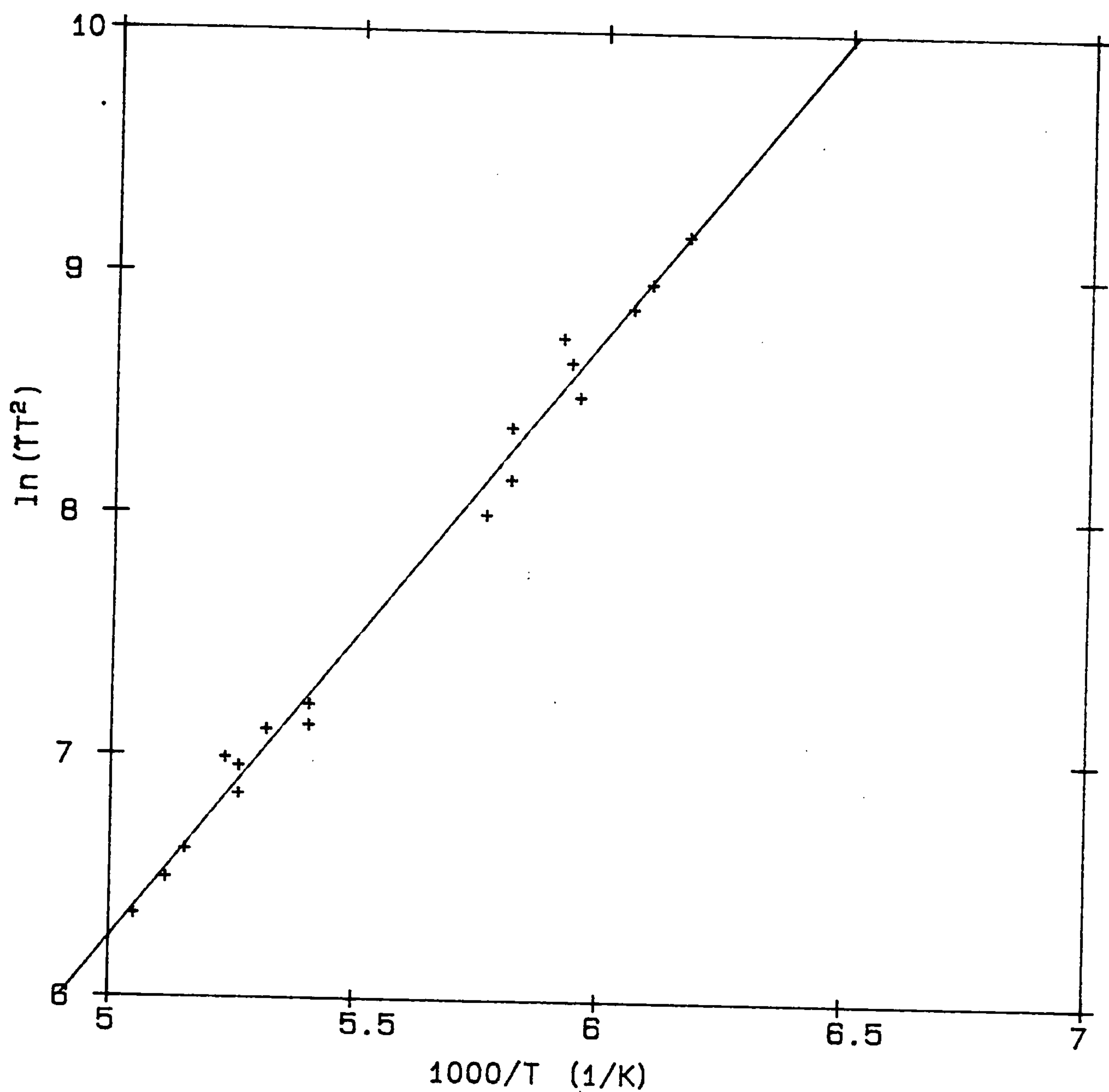
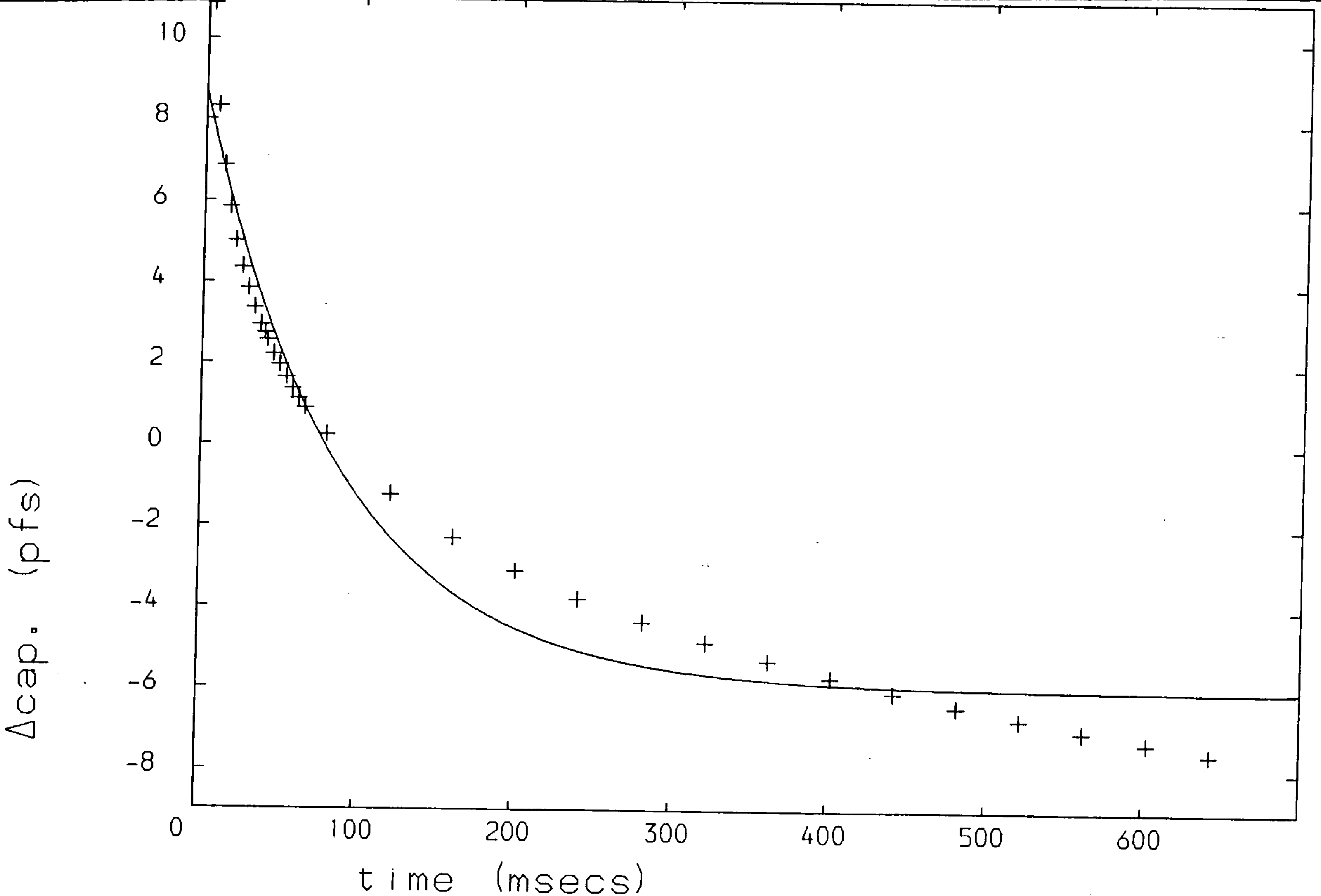


Figure 5.42 Arrhenius plot for the hole trap HT



FITTED PARAMETERS

P 1 = -0.603E01 P 2 = 0.147E02 P 3 = 0.881E02

Figure 5.43 Capacitance transient due to hole emissiom from the hole trap HT

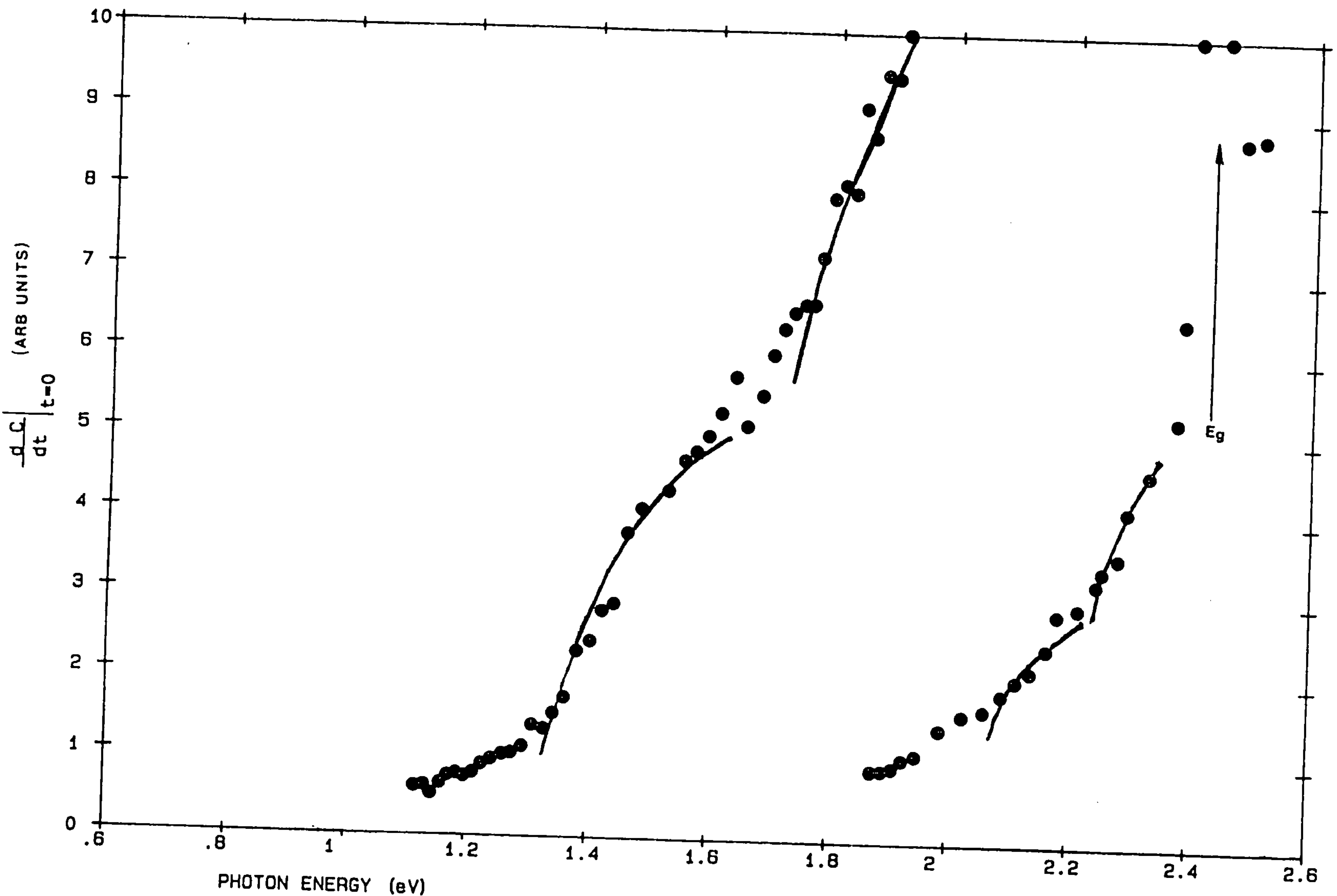


Figure 5.44 DLOS scan for CdS:Te

5.4.6 Discussion

DLTS, ODLTS and DLOS have been used to characterise the main trapping centres in tellurium doped CdS. DLTS spectra were typical of those for undoped material - all contained E2 with E1 poorly resolved. Two samples from boule 537 gave E3 and E4, and both displayed the 'light'/'dark' effect for E3 as discussed in section 5.2.3. These latter samples also had extended defects at the surface which were electrically active confirming the correspondence between E3 and E4, and the previous suggestion that they are due to states associated with for example dislocations.

ODLTS measurements revealed one further peak in addition to those associated with copper. This had an activation energy of 0.21eV and capture cross-section of 10^{-20} cm^2 . Such a small hole cross-section indicates that it probably behaves as a hole repulsive centre [29]. The optical activation energy from DLOS for this trap was found to be 0.22eV above the valence band. The difference between these two values was within experimental error.

There is much reported evidence that tellurium acts as an isoelectronic, substitutional impurity at low concentrations in CdS. As such it is able to bind an exciton with an energy of 0.21-0.24eV [23,55,56,59]. At high concentrations ($>10^{19} cm^{-3}$) Te pairs form in nearest neighbour anion sites also giving bound exciton states but with a significantly higher binding energy (~ 0.7eV) [23,55,56,59]. However, the Te concentration did not exceed about 10^{17} cm^{-3}

so this level was not detected. In both cases a hole is bound in a strongly localised state above the valence band by a short range potential resulting from the large electronegativity difference between S and Te [59] - 1.87 and 1.47 respectively [50]. An electron can then be bound coulombically leading to a bound exciton whose optical creation or annihilation gives characteristic excitation and emission bands. Fukishima and Shionoya [60] have observed a third luminescence band due to recombination at pairs of Te traps and donor levels; again the Te acceptor state is 0.21eV above the valence band.

The Te centre observed in the ODLTS and DLOS spectra had a similar energy to that reported for the isolated Te point defect states [23,54,55,58,59]. If the centre has a hole trapped then one would expect that it would capture further holes with difficulty - that is a hole repulsive centre; this would be the case for a small hole cross-section as seen in ODLTS. Indeed, this suggests that the centre behaves as an electron trap which would be consistent with the high efficiency luminescence band by electron capture at this state. However, the fact that the ODLTS response was very broad and that the emission process was non-exponential suggests that there was a broad distribution of states. If one considers the fact that Te has a low solubility in CdS ,then it is likely to aggregate at for example, dislocations. How this correlates with the luminescence studies by other workers is not clear in view of the proposed model.

5.5 Conclusion

DLTS, ODLTS, DLOS and photocapacitance have been used to characterise the main electron and hole traps in CdS. DLTS has shown the presence of 4 electron traps in the material grown in the manner described in section 4.2. E1 and E2 were found in all samples and are thought to be associated with native defects such as sulphur vacancy, interstitial cadmium, or cadmium on a sulphur site. Two of the traps, E3 and E4, were observed in a few samples only; E3 was found to be photoinduced and could be destroyed by leaving the sample in the dark or more rapidly by a heat treatment. The process was found to be reversible by illumination; having an optical threshold between 1eV and 1.3eV. The two traps E3 and E4 may have resulted from states associated with extended defects, although this could not be confirmed.

Optical DLTS of undoped and copper doped CdS Schottky diodes and CdS/Cu_2S heterojunctions have shown the presence of two hole traps denoted H1 and H2 with thermal activation energies of 0.34eV and 1.1eV resectively. These traps have been attributed to Cu ions on cadmium sites and two states arise due to a crystal field splitting of the copper d orbitals. Optical measurements of these traps using DLOS and PHCAP have have shown that H1 has an optical depth from the valence band of 0.34eV correlating with the value obtained by ODLTS. A third trap was observed in DLOS at 1.7eV below the conduction band showing no correlation with the ODLTS results, however, its thermal activation energy for hole emission may be too large to be observed in the temperature

range of ODLTS. This suggests a large Frank-Condon shift for the state.

Defect states arising from the doping of CdS with Te have been observed in ODLTS and DLOS with an activation energy of 0.2eV. The trap was associated with the Te impurity which from the broad ODLTS response suggested gave a broad distribution of states. The poor solubility of Te in CdS suggests that the impurity may form aggregates of point defects at for example dislocations. Although this may account for the ODLTS peak broadening, there was no direct evidence for this.

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CHAPTER 6

SINGLE CRYSTAL (ZnCd)S

6.1 Introduction

DLTS, ODLTS, DLOS and photocapacitance (PHCAP) have been used to study the dominant deep level defects in undoped and copper doped $Zn_xCd_{1-x}S$ Schottky devices and $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions in the composition range $0<x<0.5$ with reference to the effect of change in composition on deep level parameters. Very little previous work has been carried out using methods based on DLTS for the study of deep levels in ternary and quaternary semiconductors; to date these have included InGaP and InGaAsP [1], AlGaAs [2], ZnSSe [3], and CdSSe [4]. The aims of this study were twofold: firstly to characterise the effect of a compositional change on the dominant electron trap E2 and the two hole traps H1 and H2 associated with copper, seen in CdS. Such a study, for example on ZnS_YSe_{1-Y} [3] has shown that the dominant electron trap at ~0.3eV remains fixed in energy but the DLTS response shifts in temperature indicating that the emission rate from the level changes with composition for a fixed temperature. Such studies are important in the investigation of the nature of these deep trapping centres.

The second study undertaken was concerned with the deep levels introduced during the processing of the mixed crystal

heterojuction $Zn_xCd_{1-x}S/Cu_2S$; these may have a detrimental effect on the operating efficiency of the solar cell. The reason for this study stems from the idea that by using $Zn_xCd_{1-x}S$ instead of CdS for the heterojunction, then improved open circuit voltages (OCV) and short circuit currents (SCC) should be achieved. However, in practice the SCC is smaller than expected, so there is no overall increase in the efficiency of the device. A lattice mismatch of 4% occurs between CdS and Cu_2S which results in an interface state density of approximately $5x10^{13}cm^{-2}$ [5]. In addition, an electron affinity mismatch of 0.2eV occurs between CdS and Cu_2S which causes a step in the potential energy at the junction [5]. Introducing Zn gives better lattice and electron affinity matching [5,6] and this should have two effects : firstly, it increases the junction barrier height and so, increase the OCV of the solar cell; and secondly, the interface state density is reduced which should reduce the interface state recombination velocity and thus, increase the current collection. These phenomena should improve the properties of the heterojunction solar cell [5,6].

Higher OCVs have been reported [7], however, current densities have been lower than that for the CdS solar cell made under similar conditions. Oktik et al [8], quoted values of 0.499V and 0.548V for the OCVs of CdS and $Zn_{0.2}Cd_{0.8}S$ cells respectively; this confirms the predicted increase. However, SCCs were $12.75mA/cm^2$ (CdS) and $10.36mA/cm^2$ ($Zn_{0.2}Cd_{0.8}S$). This trend was consistently observed at least up to the composition x=0.4. Possible explanations for the anomalous behaviour have been suggested, for example Böer

[9] proposed that a potential spike exists at the junction which is transparent to electrons for x=0. However, as Zn is introduced, the spike decreases in amplitude but its width increases; this makes the tunnelling process more difficult and thus reduces the current collection. Another additional effect has been proposed by Pande et al [10], namely, that a deep level defect is formed near midgap as a result of the device processing. This centre is thought to provide a recombination route for the photogenerated carriers and therefore, reduces the current collection efficiency of the solar cell. These results are extended here.

6.2 Materials

The single crystals used in this study were grown using the Clark-Woods [11] and the Piper-Polich [12] methods described in chapter 4. The compositions of the samples were obtained from x-ray diffraction and confirmed from optical band gap measurements. X-ray diffraction was carried out on a Philips X-Ray Diffractometer. The crystals had been previously oriented and cut along the c-axis so that only (0001) reflections were observed. The lattice constants were obtained from

$$1/d^2_{hkl} = 4(h^2+hk+k^2)/3a_o + (1/c_o)^2 \qquad 6.1$$

There seems some controversy as to how the lattice parameters a_o and c_o vary with compostion. Vegard's law (linear relation) is widely accepted for most ternary compounds, however, there are inconsistencies in the reported

experimental results. Kane et al [13] and Ballentyne and Ray [14] both show a downward bowing with some scatter amongst their respective data points. However, a linear variation has been observed by others [15-18]. As a reasonable approximation since most results were obtained for x up to 0.2, Vegard's law was assumed. These relationships are shown in fig. 6.1.

The nonlinear relationship of composition with band gap is well known [19-21], indeed, the variation has been shown to be quadratic [21]. Each of the II-VI ternary compounds has been assigned a bowing parameter which defines the degree of bowing in the graph of band gap vs composition. For Zn_xCd_{1-x}, the bowing parameter is 0.61 [22] which gives from equation 1.1 a relationship of the form

$$Eg(x) = 2.42+0.69x+0.61x^2 \qquad 6.2$$

where Eg(x) is the band gap at the composition x. Fig. 6.2 shows this relationship graphically.

The lattice parameter data for the determination of composition was correlated with that obtained from band gap measurements to obtain compositions of the samples used in this study. Boule 826, grown by the Clark-Woods method showed, a compositonal variation from x=0.02 to x=0.19 as a gradation along the boule length although the charge contained 10% ZnS and 90% CdS. This was the only boule grown by this technique that was studied. Boules 799, 819 and 820 were grown by the modified Piper-Polich technique and gave

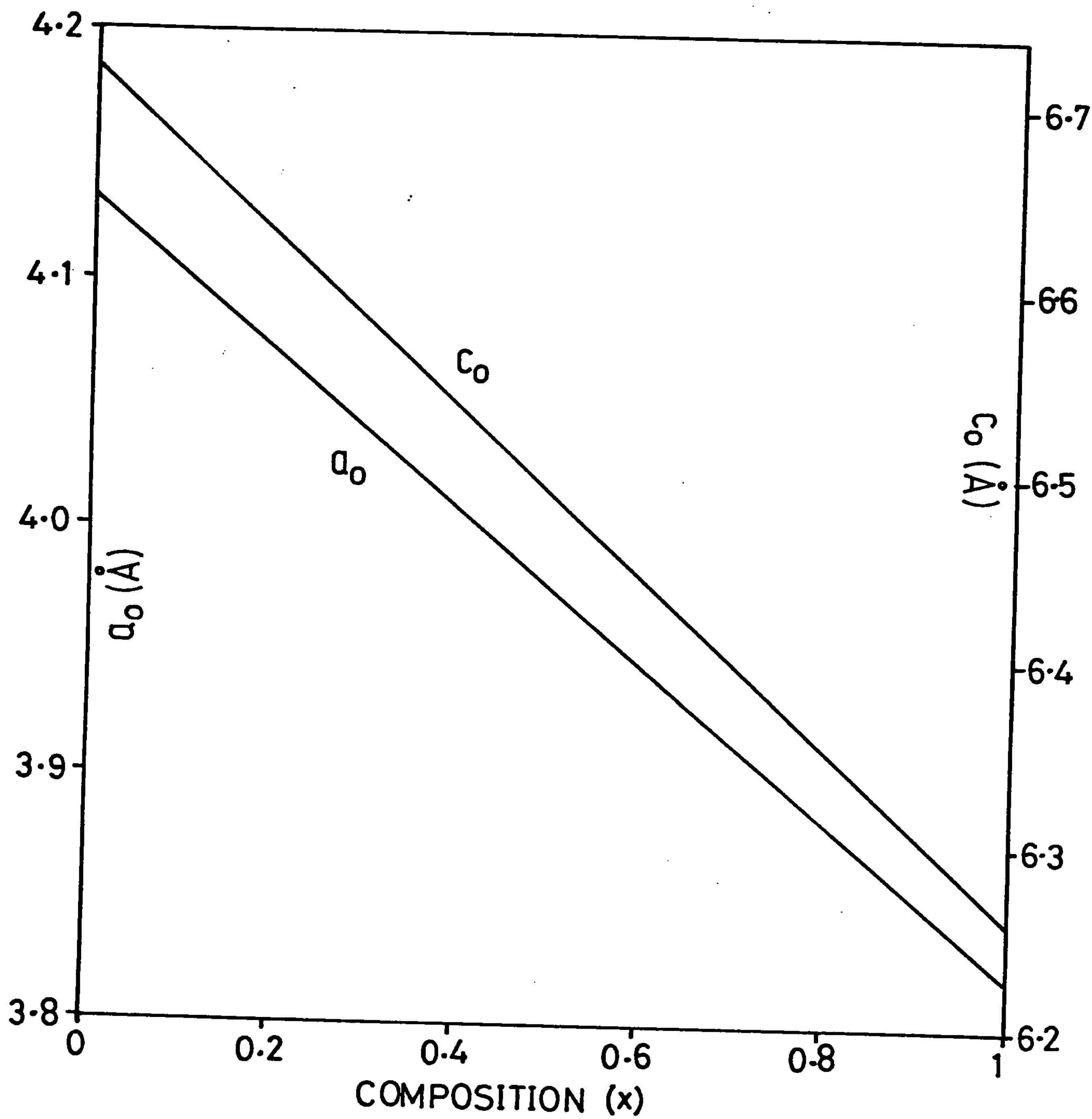

Figure 6.1 Variation of the lattice parameters a_o and c_o with composition for $Zn_xCd_{1-x}S$

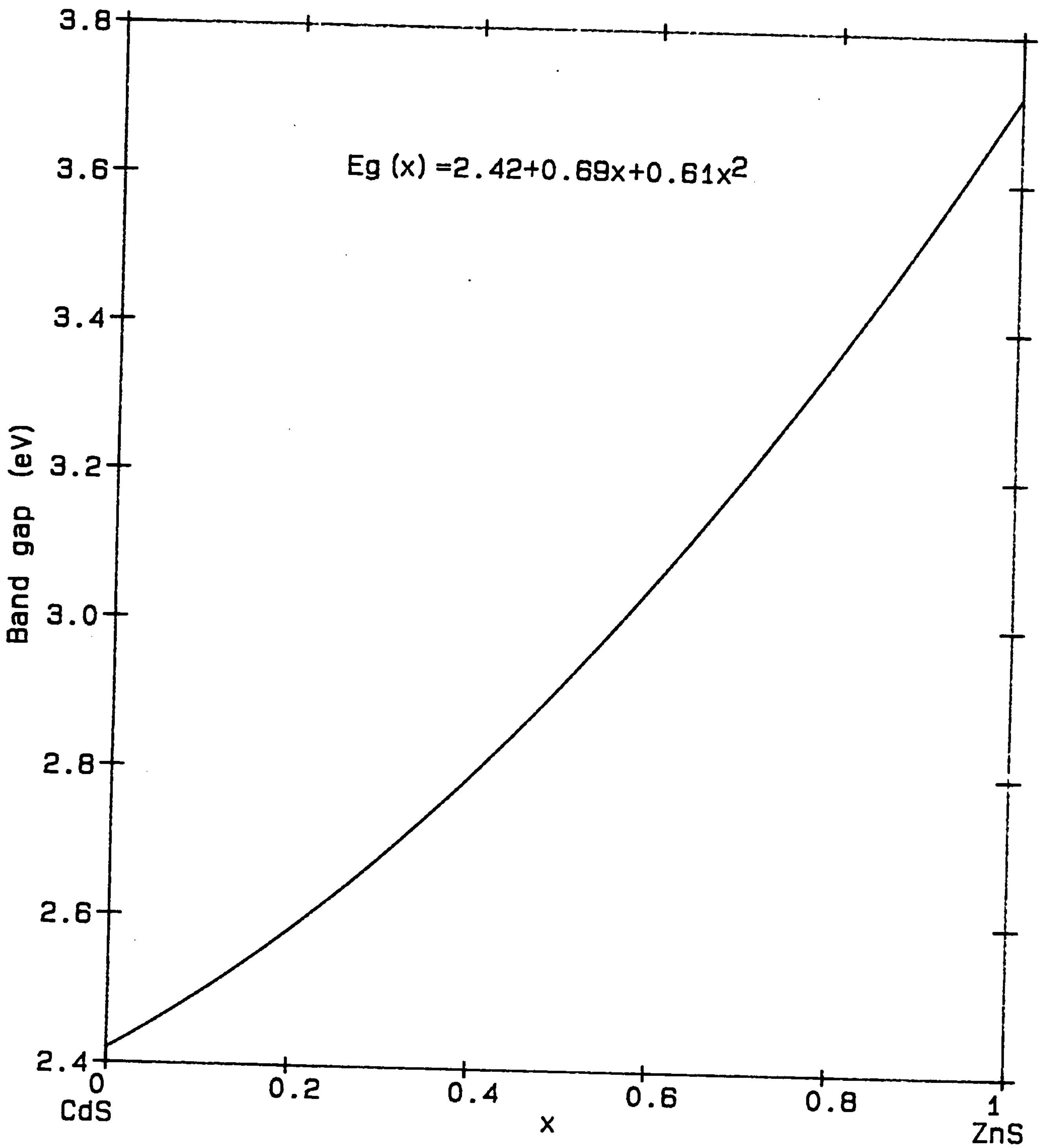

Figure 6.2 variation of band gap with composition for $Zn_xCd_{1-x}S$ (300K)

compositions over the range x=0.35 to x=0.45. Resistivity measurements for 0<x<0.5 showed an order of magnitude increase for x up to 0.2 followed by a 5 orders of magnitude increase to x=0.35 (see fig. 6.3). This confirms the dark conductivity results obtained by Davis and Lind [19].

Both Schottky devices and heterojunctions were studied. The Schottky devices were prepared in a manner similar to that for CdS: ohmic contacts were formed on one face of the $Zn_xCd_{1-x}S$ dice by annealing indium onto the surface at 300C in an argon atmosphere. Schottky barriers were obtained by evaporation of gold onto the opposite surface in vacuum. The heterojunctions were prepared by the dry barrier technique as described for CdS in section 5.3.2: evaporation of CuCl onto one surface of a $Zn_xCd_{1-x}S$ dice, followed by an optimising heat treatment at 200C for 2mins. The static dielectric constants were assumed to be linear over the composition range studied. The effective masses for electrons over the whole composition range was known to be linear with band gap [23] (see fig. 6.4), this was also assumed for the hole effective masses. Capacitance-voltage measurements were used to determine the free carrier density and typical $1/C^2$ vs V plots are shown in fig. 6.5. The N_d values obtained for boule 826 were in the range 10^{16} cm^{-3} to 10^{17} cm^{-3}. DLTS, ODLTS, DLOS and PHCAP were carried out on all samples in an effort to characterise the main trapping centres in the material.

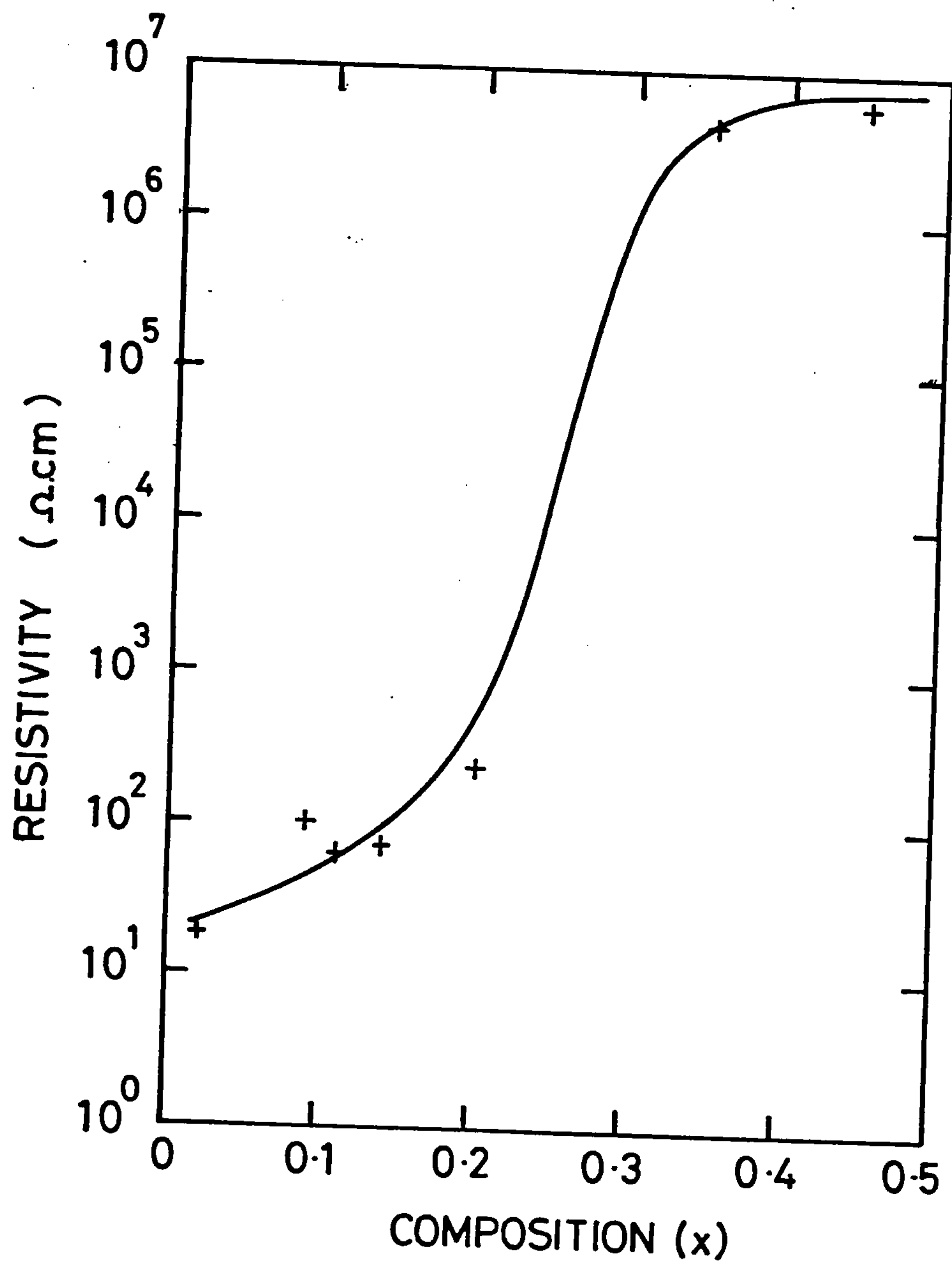

Figure 6.3 Variation of resistivity with compositionfor $Zn_xCd_{1-x}S$

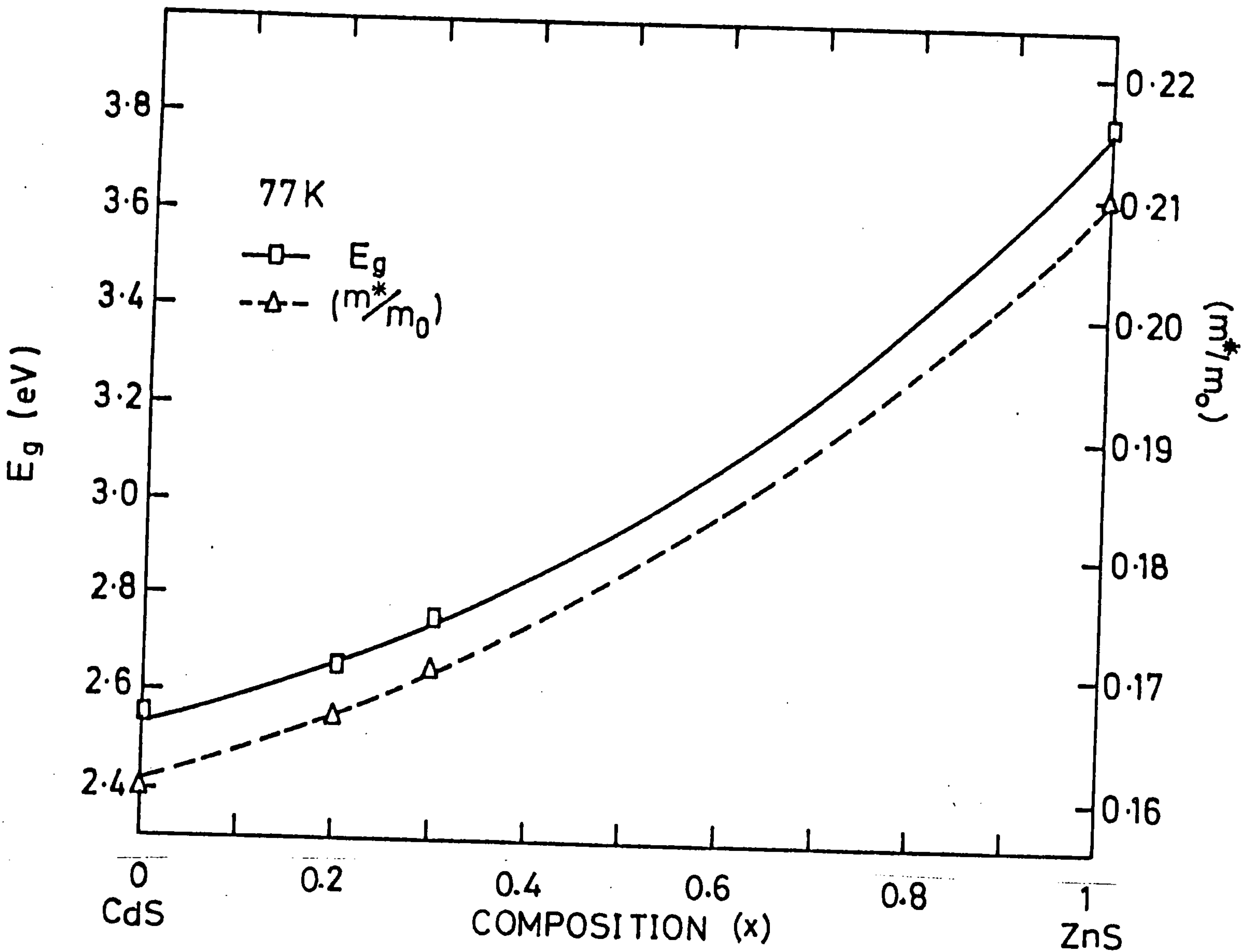

Figure 8.4 Variation of electron effective mass and band gap with composition (77K) [23]

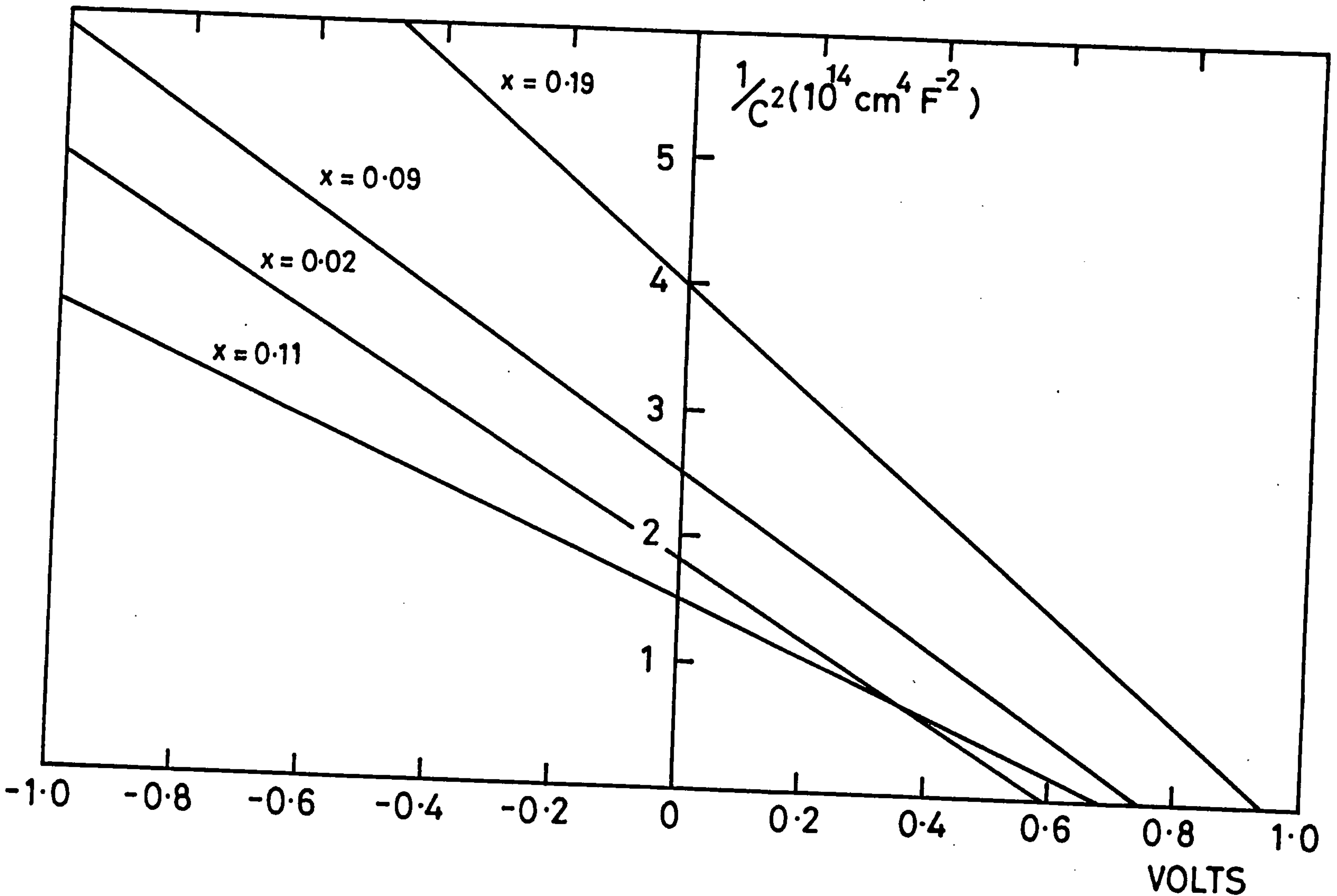

Figure 6.5 $1/C^2$ vs V plots for $Zn_xCd_{1-x}S$ at various compositions (295K)

6.3 DLTS of (ZnCd)S

DLTS was used to characterise the main electron traps in $Zn_xCd_{1-x}S$/Au Schottky diodes for $0<x<0.45$ over the temperature range 80-400K. Fig. 6.6 shows DLTS spectra for x=0, 0.11, 0.19 and a capacitance-temperature scan for x=0.11. The samples with $x>0.2$ did not give a DLTS response over the temperature range studied. A peak similar to that observed for E2 in CdS was observed in some samples but not all. Arrhenius plots for E2(x) are given in fig. 6.7 and the calculated activation energies were 0.41eV (x=0), 0.43eV (x=0.02), 0.50eV (x=0.09), 0.52eV (x=0.11), 0.65eV, (0.19). These results, together with the capture cross-sections and trap densities, are summarised in fig. 6.8. There was no consistency in the strength of DLTS response through the boule 826. Slices 2, 5 and 11 gave weak responses whereas, slice 7 and 9 gave no indication of the presence of E2(x). Between slices 7 and 9, E2(x) seemed to have become prominent, indeed slice 8 gave the strongest response. This shows the difficulty in controlling the defect states during growth. One further important point was that E2(x) was not observed in the Piper-Polich grown material. The DLTS peaks for E2(x) in fig. 6.6 are seen to be broader than that for E2 in CdS. Fig. 6.9 shows a theoretical DLTS spectrum for E2(0.11) with the experimental results and it is apparent that the experimental curve is much broader than the predicted DLTS response.

This particular sample was also studied [24] by constant capacitance DLTS [25] whereby the capacitance was maintained

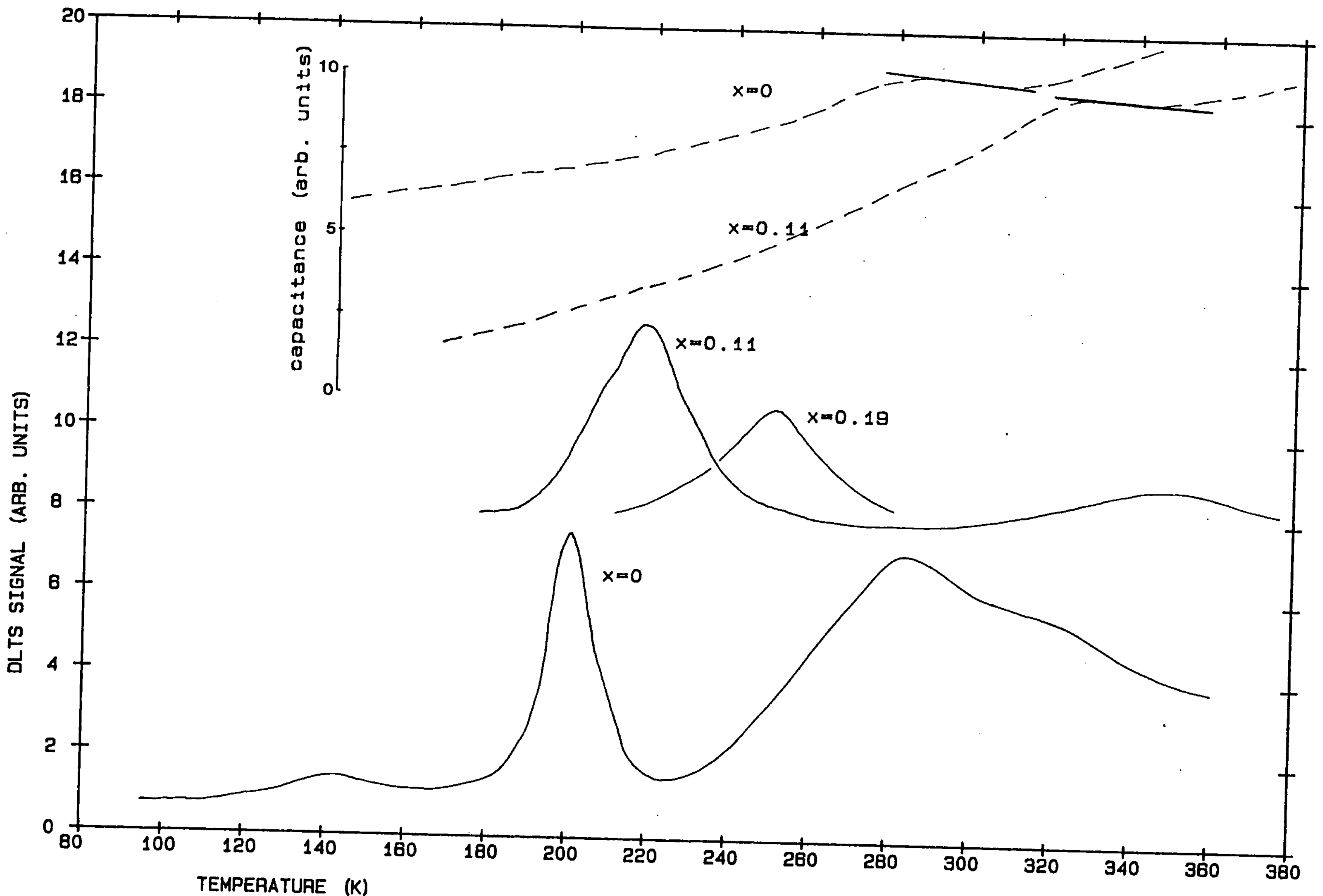

Figure 6.8 DLTS spectra and capacitance-temperature scans for $Zn_xCd_{1-x}S$

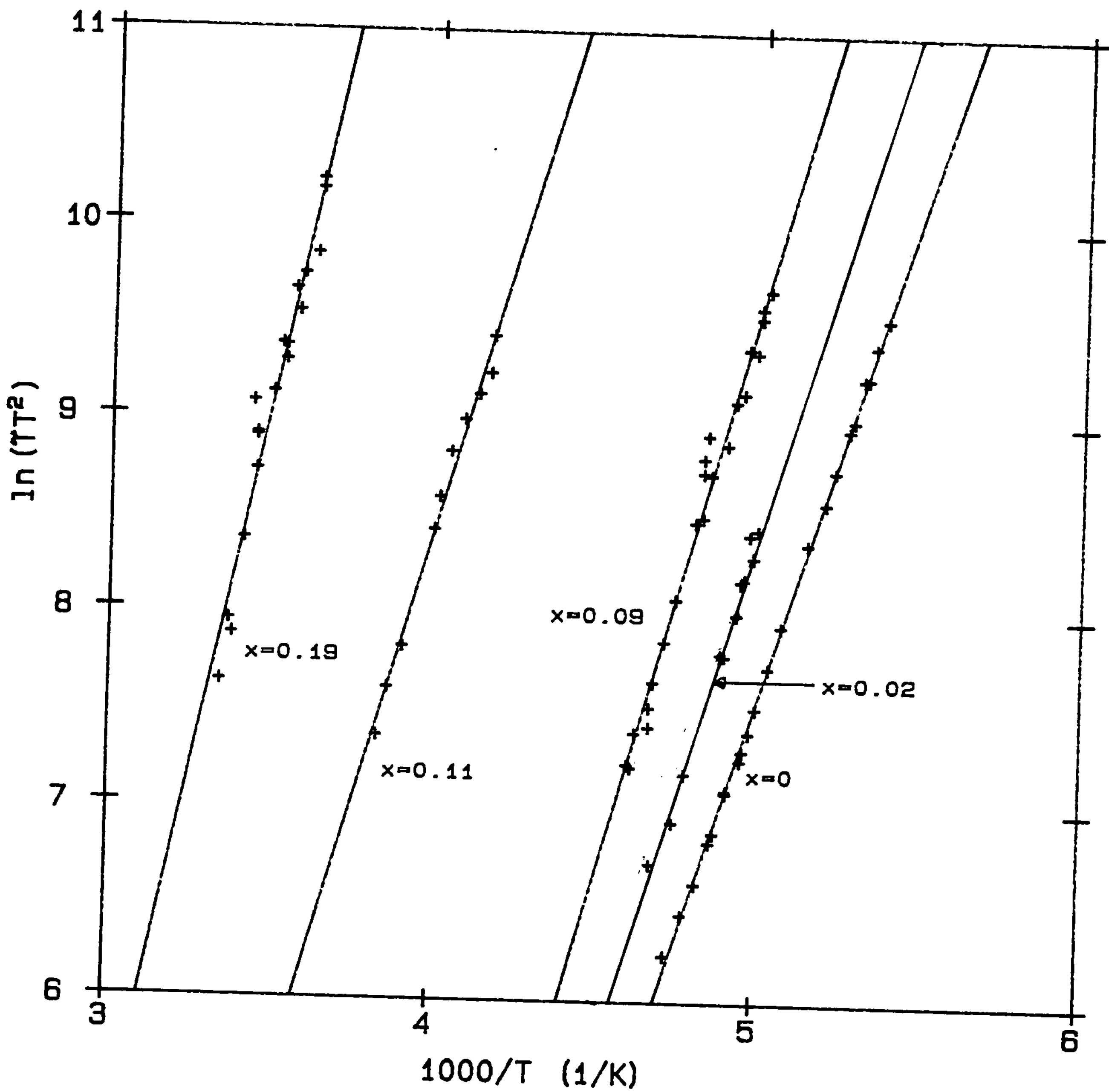

Figure 8.7 Arrhenius plots for the electron traps E2(x)

SAMPLE	$\Delta E(E2)/eV$	σ_n/cm^2	N_T	N_T/N_d
799 CdS	$0{\cdot}41 \pm 0{\cdot}01$	$1{\cdot}4 \times\!\div 0{\cdot}3 \times 10^{-14}$	$6{\cdot}3 \times 10^{13}$	$0{\cdot}021$
826 $Zn_{0{\cdot}02}Cd_{0{\cdot}98}S$	$0{\cdot}43 \pm 0{\cdot}03$	$2{\cdot}0 \times\!\div 9{\cdot}0 \times 10^{-15}$	$1{\cdot}2 \times 10^{14}$	$5{\cdot}7 \times 10^{-4}$
826 $Zn_{0{\cdot}09}Cd_{0{\cdot}91}S$	$0{\cdot}50 \pm 0{\cdot}02$	$1{\cdot}0 \times\!\div 2{\cdot}0 \times 10^{-13}$	$1{\cdot}9 \times 10^{15}$	$0{\cdot}01$
826 $Zn_{0{\cdot}11}Cd_{0{\cdot}89}S$	$0{\cdot}52 \pm 0{\cdot}02$	$4{\cdot}0 \times\!\div 6{\cdot}0 \times 10^{-16}$	$4{\cdot}3 \times 10^{15}$	$0{\cdot}04$
826 $Zn_{0{\cdot}19}Cd_{0{\cdot}81}S$	$0{\cdot}65 \pm 0{\cdot}05$	$2{\cdot}0 \times\!\div 9{\cdot}0 \times 10^{-14}$	$1{\cdot}3 \times 10^{13}$	$2{\cdot}3 \times 10^{-4}$

Figure 6.8 Summary of results for the electron traps E2(x) at various compositions

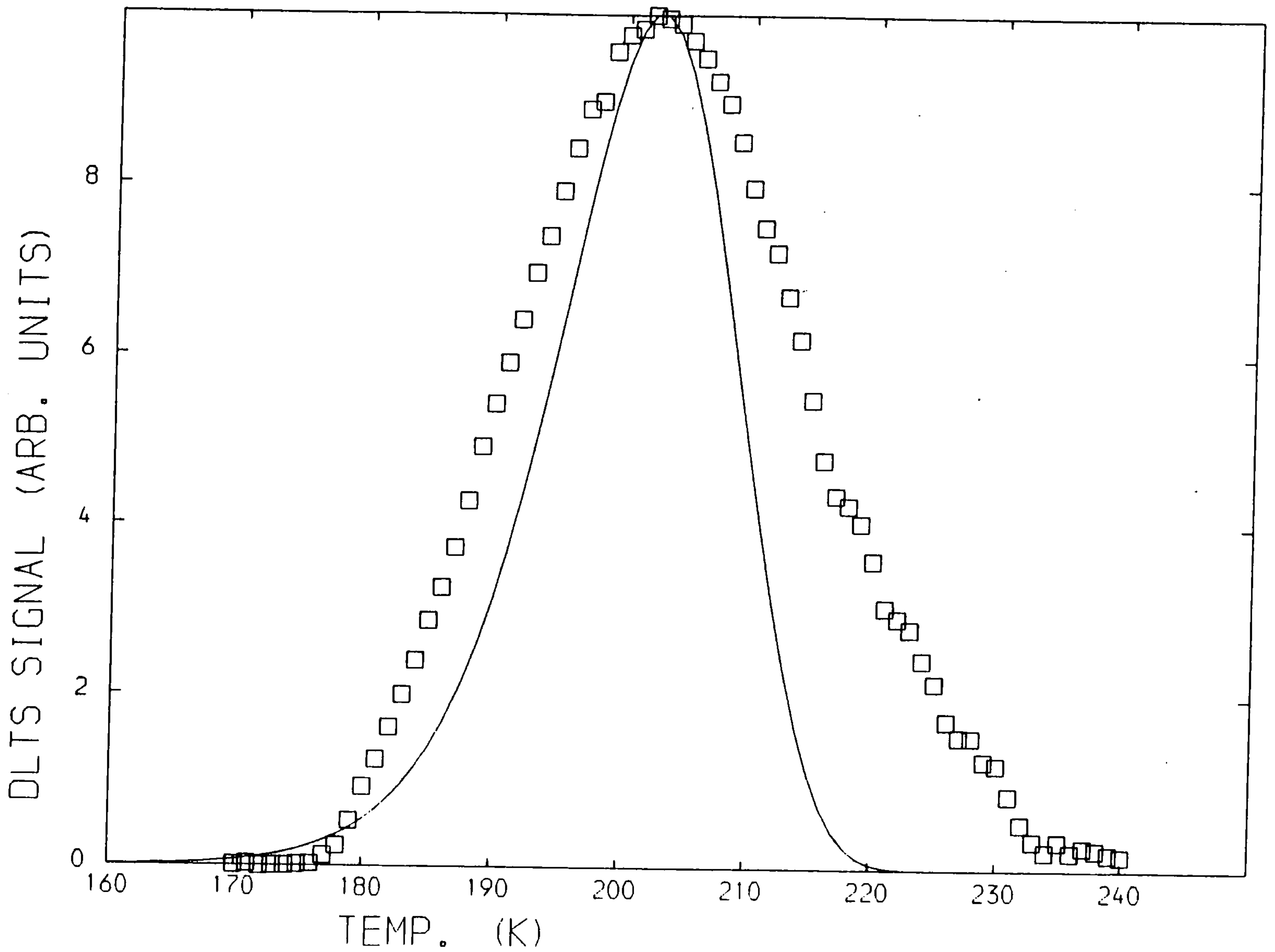

Figure 6.9 Theoretical (——) and experimental (□ □) DLTS peaks for E2(0.11)

constant by a fast feedback circuit which applied an appropriate bias to the sample; this gave a voltage transient. The DLTS and CCDLTS spectra are shown in fig. 6.10. As can be seen from these scans, the maximum response occurred at the same temperature. The activation energy and capture cross-section determined in the same manner for DLTS, from an Arrhenius plot, gave the same values as those obtained from DLTS. The peak sign reversal for the CCDLTS signal is due to the fact that the feedback voltage was made more negative to maintain the depletion capacitance. This gave a negative decaying voltage transient as opposed to the positive going capacitance transient for DLTS. The CCDLTS signal S(T) is given by

$$S(T) = V(t_2) - V(t_1) \qquad 6.3$$

Since the voltage at time t_2 was less than that at t_1 then a peak sign reversal would occur as was observed.

It is interesting to note that the peak E2(x) moves to higher temperature with increasing x. As can be seen, this general trend of increase in activation energy with x holds over the composition range x=0 to x=0.2 whereas the capture cross-sections fluctuate with no apparent trend.

Two other high temperature peaks were observed for x=0.09 and 0.11, and were only detected in these two particular samples. They occurred at about 390K (see fig. 6.6) and had activation energies and capture cross-sections of 0.81eV, 6×10^{-15} cm^2 for x=0.09 and 0.88ev, 10^{-15} cm^2 for

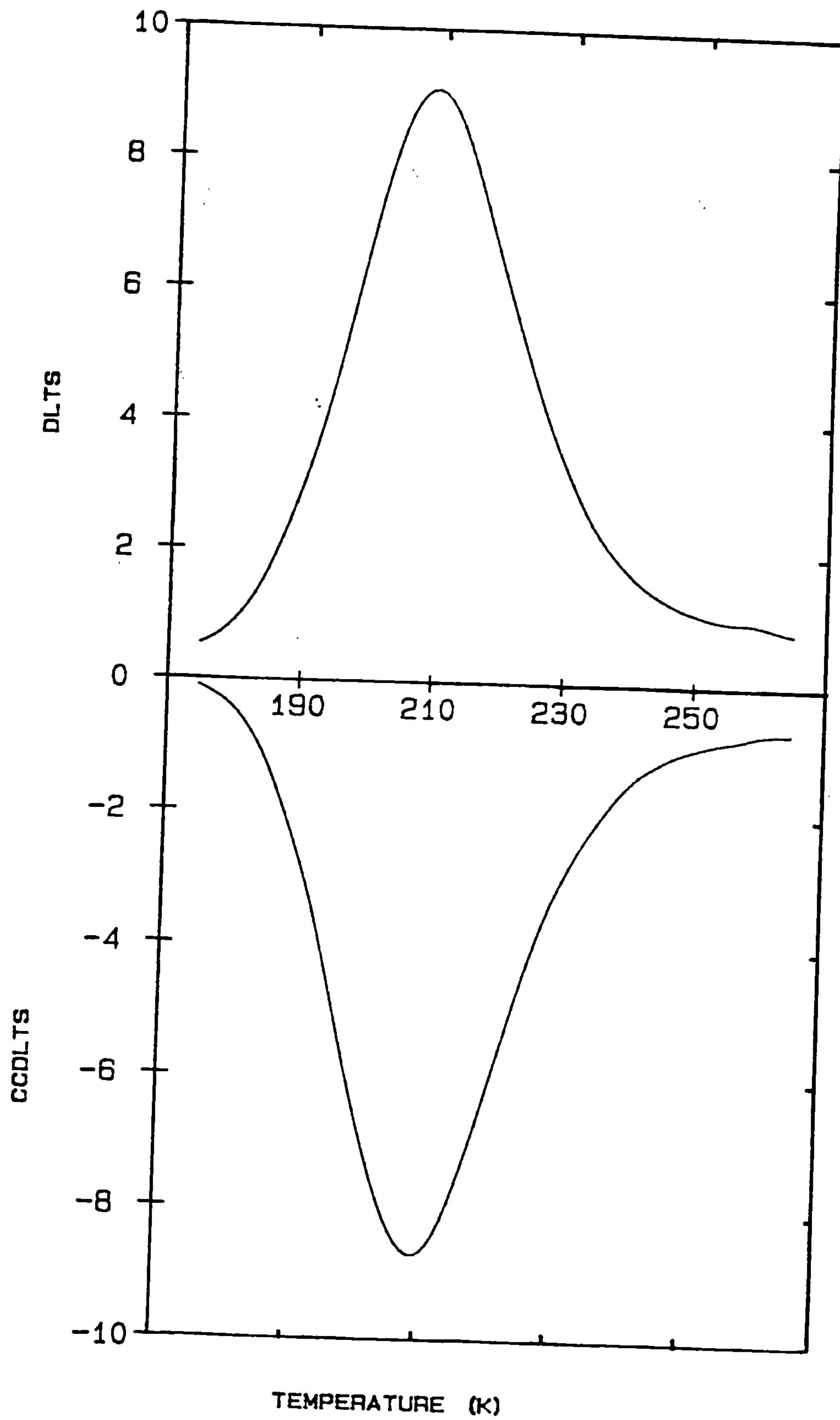

Figure 6.10 DLTS and CCDLTS spectra for E2(0.11)

x=0.11. It is interesting to note that the C-T scan for x=0.11 in fig. 6.6 showed a peak just below the temperature at which the DLTS peak for the 0.88eV trap was observed. As discussed in chapter 5 for CdS this response is thought to be due to extended defects such as dislocations. Using Simoen's analysis [26] (see also chapter 5) a dislocation density of $10^9 cm^{-2}$ was calculated. No traps were observed that seemed to correlate with E3 or E4 in CdS and no sample displayed the 'light'/'dark' response discussed in chapter 5.

6.4 ODLTS Results for (ZnCd)S

ODLTS was carried out on undoped and copper doped $Zn_xCd_{1-x}S$ Schottky devices for x in the range 0 to 0.45 and a $Zn_{0.1}Cd_{0.9}S/Cu_2S$ heterojunction, over the temperature range 80-400K. This was to investigate the effect of a compositional change on the hole traps due to copper observed in CdS (H1 and H2); to characterise any new hole traps resulting from the introduction of Zn; and to observe any defect state that may explain the reduced SCC for the heterojunction. The experiments were carried out using an acousto-optically chopped laser (Ar or He/Ne). ODLTS spectra for all the samples studied are shown in fig. 6.11. The copper doped material over the composition range studied gave a response for the ground copper state H2(x) and a less well defined response for H1(x). Copper doped mixed crystal Schottky devices and the heterojunction gave an ODLTS response for the copper levels. All the undoped material grown by the Piper-Polich method gave a response for H2 but not for H1; the reason for this was that the light source

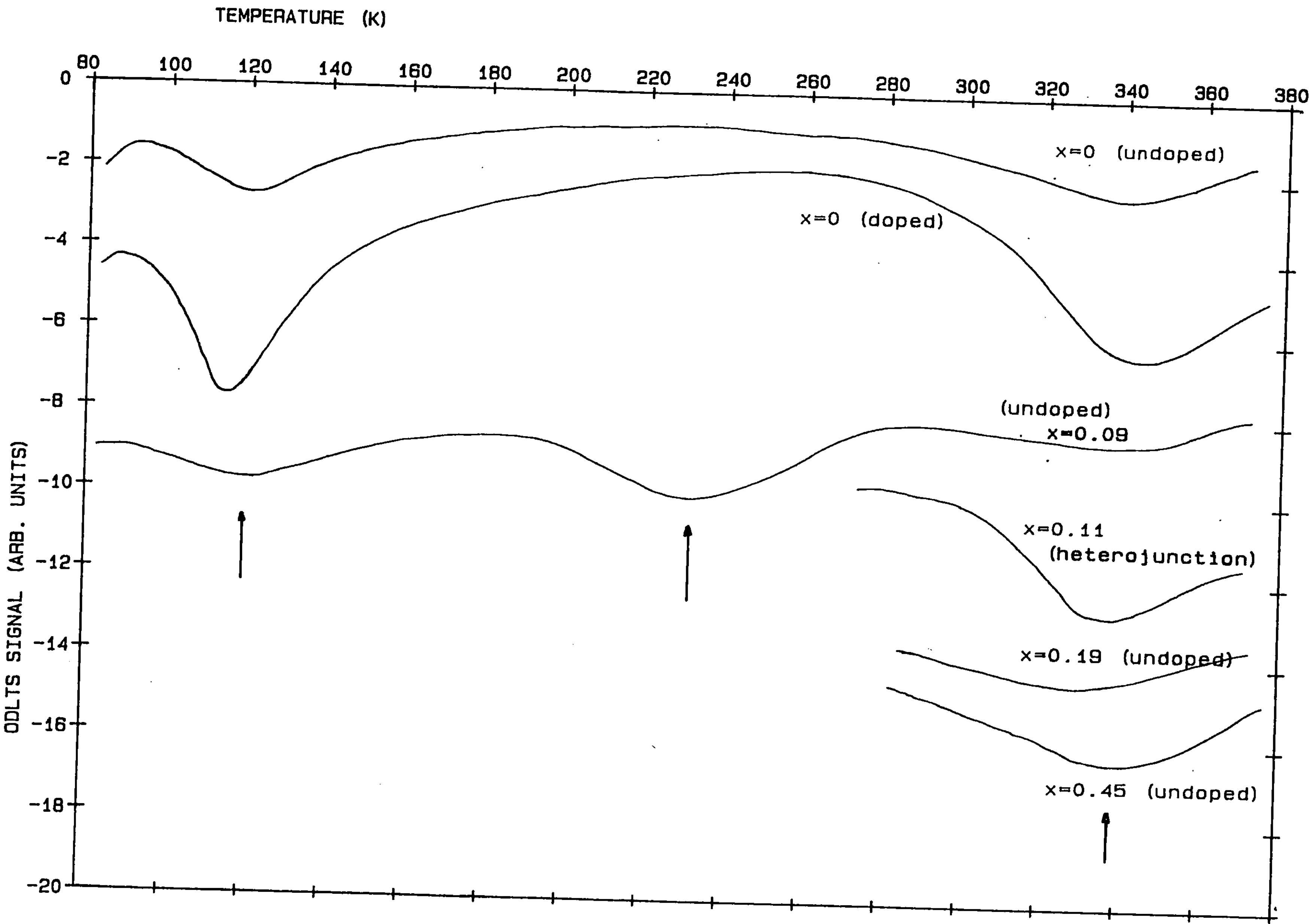

Figure 6.11 Typical ODLTS spectra for undoped and copper doped $Zn_xCd_{1-x}S$

available for the experiment (Ar laser operating at 489nm) could not penetrate deeply enough into the band gap to empty the acceptor state H1 into the conduction band. The undoped material grown by the Clark-Woods technique only gave a response for a few samples with the ODLTS system operating at its limits of resolution. Fig. 6.12 gives Arrhenius plots for the samples studied and the results are summarised in fig. 6.13. In addition to the copper states, a trap was observed at 0.49eV for a sample with composition x=0.09 but was not observed in any others. The heterojunction did not give any other hole trapping centres apart from the copper associated states.

6.5 DLOS and Photocapacitance Results for (ZnCd)S

No new traps were observed in the undoped and copper doped Schottky devices and the heterojunction in DLTS or ODLTS. In an effort to probe further into the band gap than was accessible by the thermal techniques, DLOS and photocapacitance (PHCAP) were used.

PHCAP was carried out on CdS/Au and $Zn_xCd_{1-x}S/Au$ Schottky devices, and CdS/Cu_2S and $Zn_xCd_{1-x}S/Cu_2S$ heterojunctions. Measurements were made at 85K and 290K by scanning the photon energy very slowly over the range 0.5 to 2.8eV. Figs 6.14 and 6.15 show the PHCAP spectra for the Schottky devices and heterojunctions respectively. For both types of heterojunctions there was a capacitance decrease at room temperature with a threshold of about 0.75eV. At 85K this was not observed, although, a pronounced decrease was

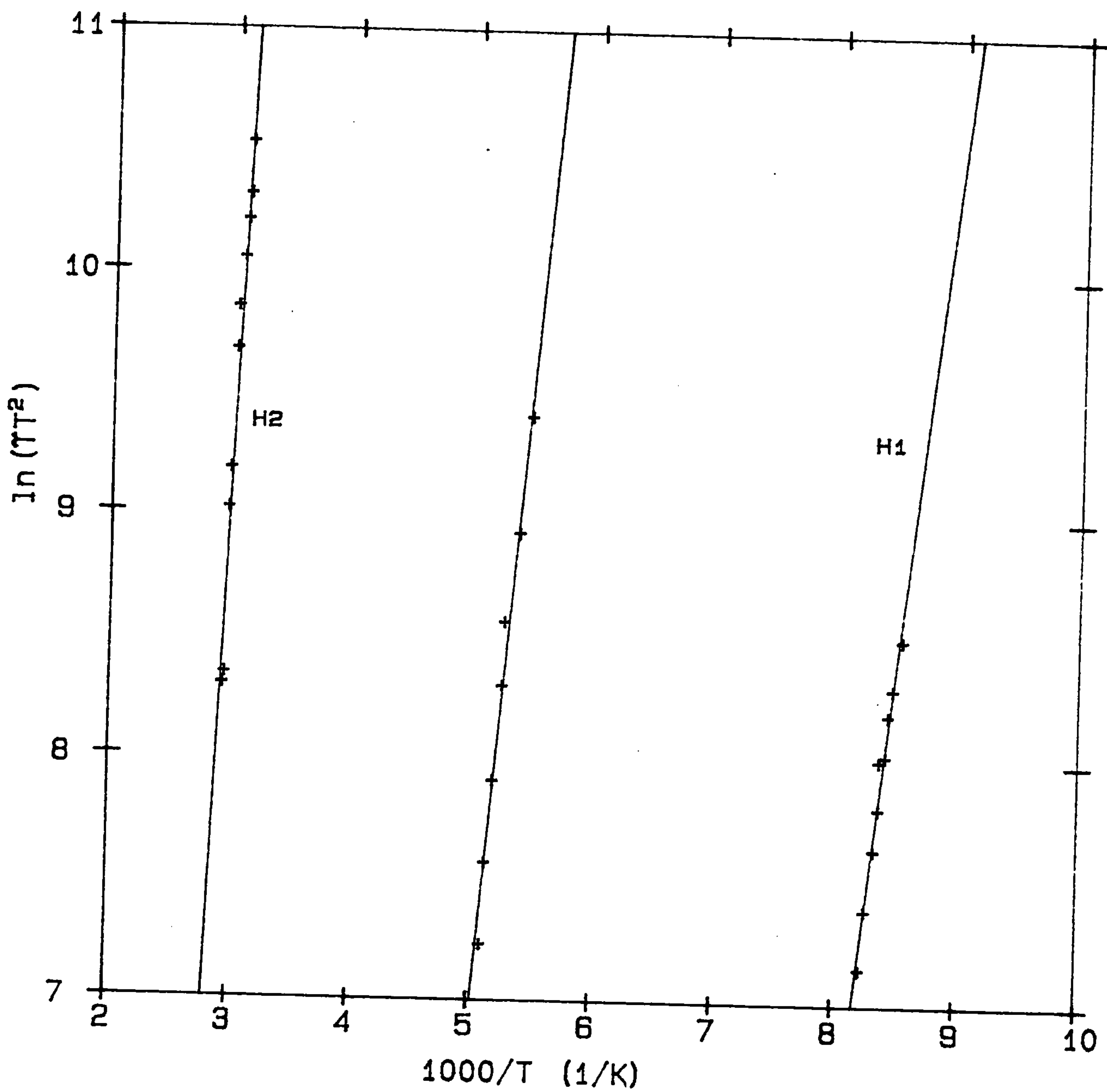

Figure 8.12 Typical Arrhenius plots for the hole traps in $Zn_xCd_{1-x}S$

x	ΔE/eV	σ_p/cm^2
0	0·34	$10^{-12\pm1}$
	1·06	$10^{-12\pm1}$
0·02	0·30	$10^{-12\pm1}$
	1·10	$10^{-11\pm1}$
0·09	0·32	$10^{-11\pm2}$
	0·49	$10^{-13\pm1}$
	1·08	$10^{-11\pm1}$
0·11	1·00	$10^{-12\pm1}$
0·14	1·08	$10^{-11\pm1}$
0·45	1·09	$10^{-10\pm2}$

Figure 6.13 Summary of ODLTS results for $Zn_xCd_{1-x}S$

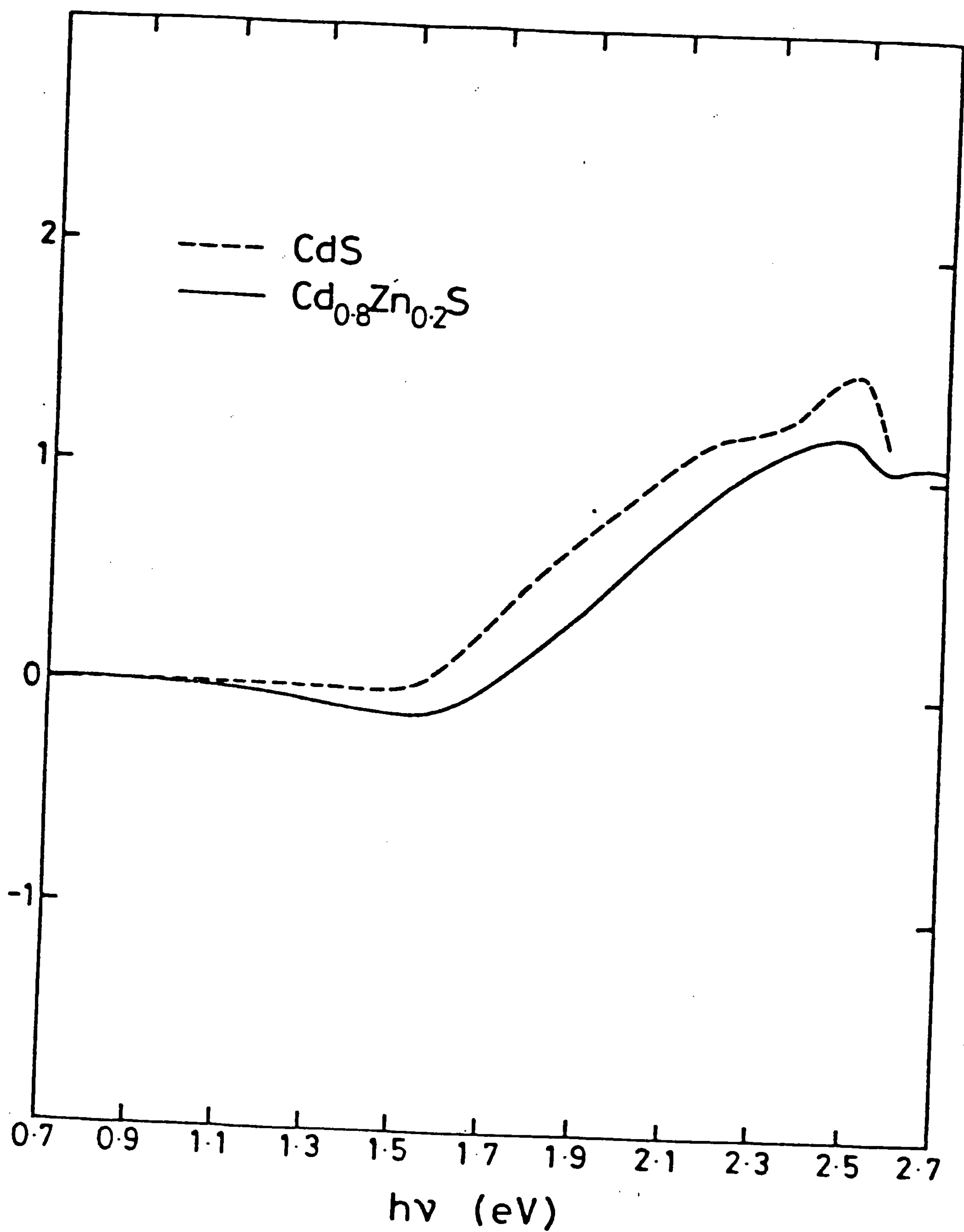

Figure 6.14 PHCAP for the Schottky devices at 85K

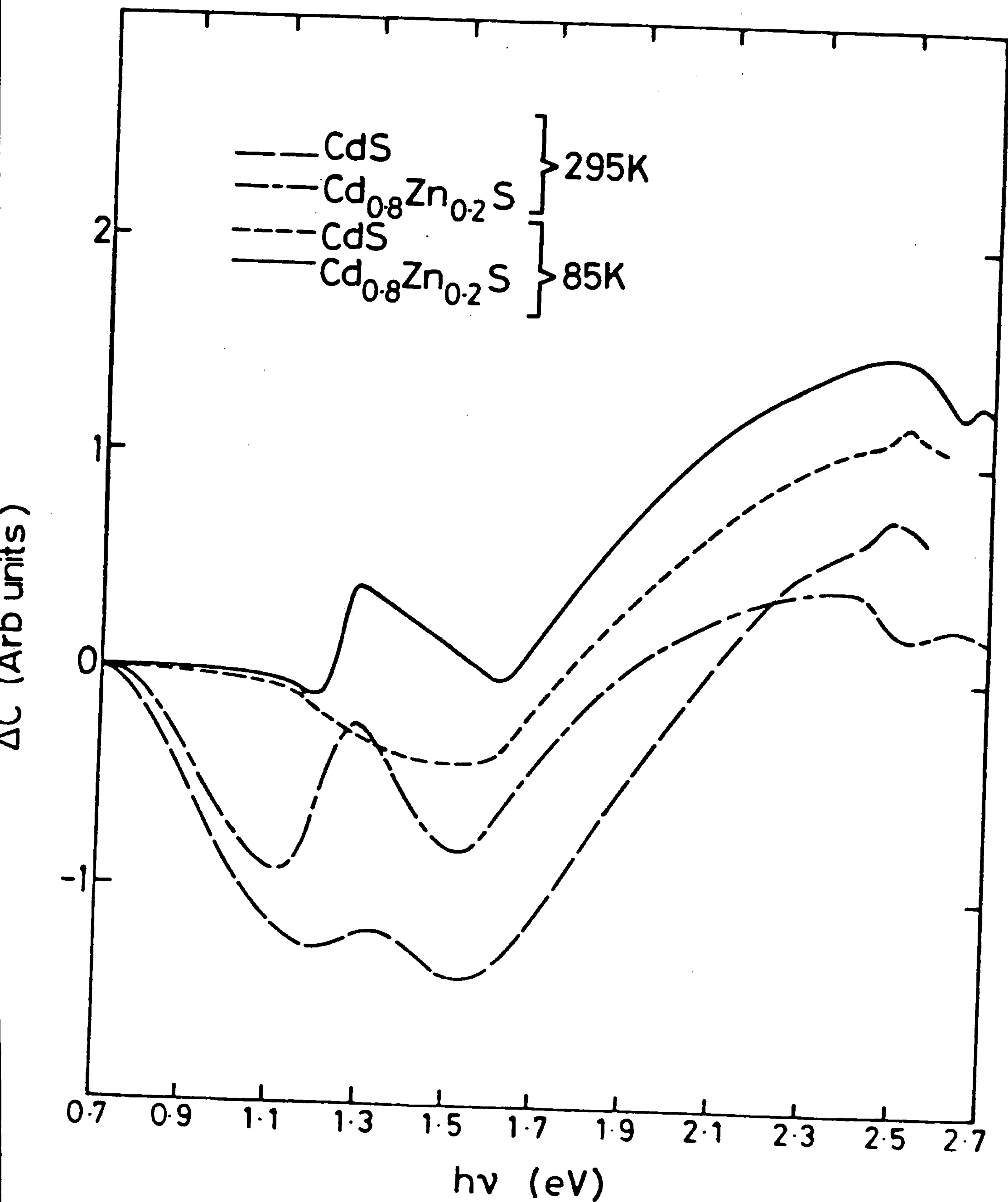

Figure 6.15 PHCAP for the heterojunctions

seen at 1.1eV. For the mixed crystal heterojunction (x=0.2), there was an increase at 1.15eV to 1.27eV which was not observed in the CdS/Cu_2S device. For photon energies greater than 1.6eV there was a steady capacitance increase to band gap with only the heterojunction giving a response at ~0.17eV below the band gap.

For the Schottky devices there was very much less structure in the PHCAP spectra. The 1.1eV threshold was not observed in CdS but was just detectable in the mixed crystal. There was no evidence of structure in the range 1.1 to 1.5eV. Again the 0.17eV threshold was observed in the $Zn_xCd_{1-x}S$ but not in CdS.

DLOS spectra were obtained at room temperature for undoped and copper doped Schottky diodes over the composition range x=0 to x=0.45 and the heterojunction for x=0.09. Fig. 6.16 gives DLOS spectra for the Schottky devices at room temperature in the photon energy range 0.7 to 2.5eV. There were three thresholds for all the compositions studied at 1.3-1.4eV, 1.7-1.8eV and 2.2eV which correlate with those observed in CdS. Fig. 6.17 shows the result for a mixed crystal heterojunction for x=0.1. In addition to the characteristic thresholds previously observed there was a further feature with a threshold at 1.23eV. A summary of the traps observed by DLOS and PHCAP is given in fig. 6.18.

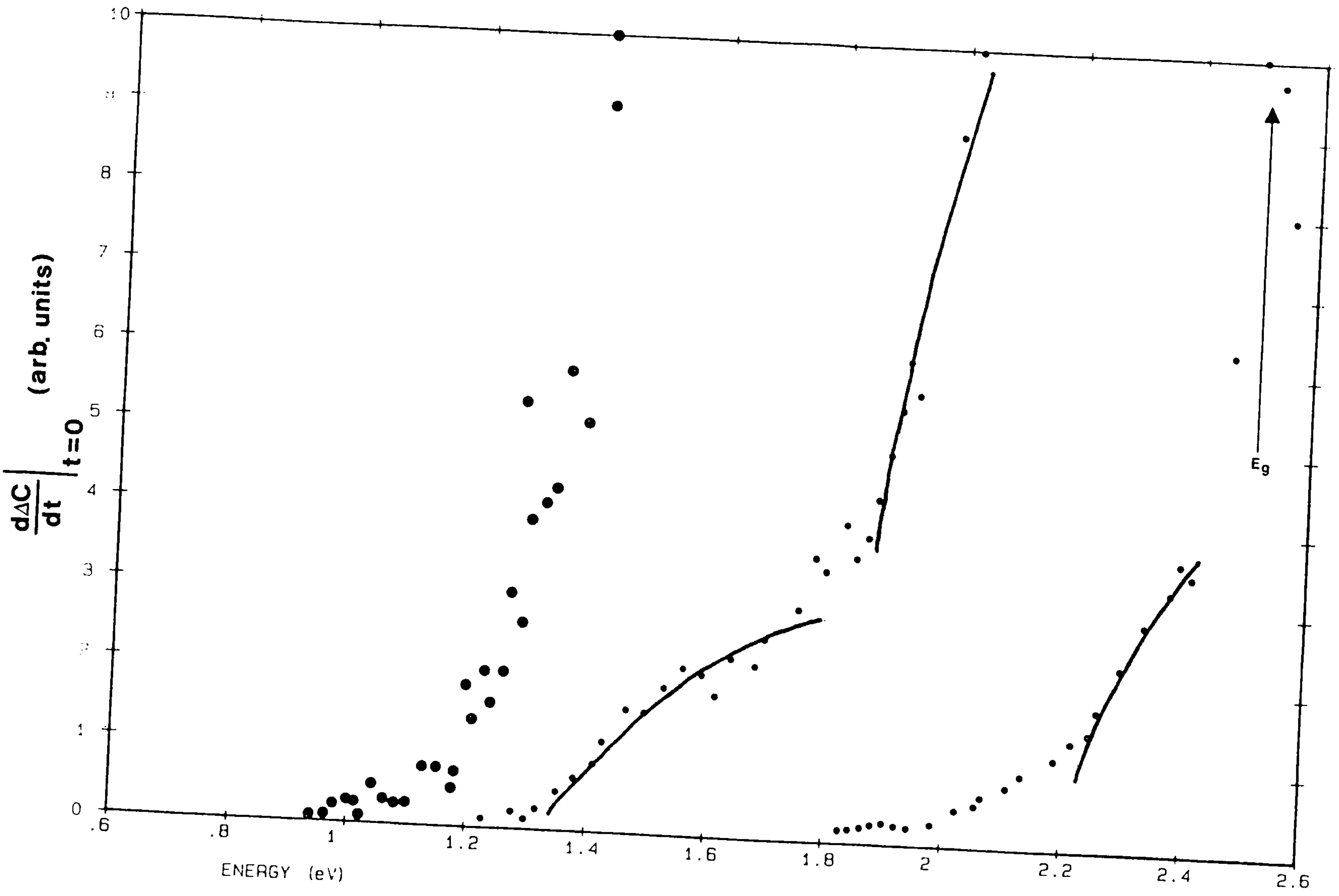

Figure 6.16 DLOS scan for $Zn_{0.1}Cd_{0.9}S$

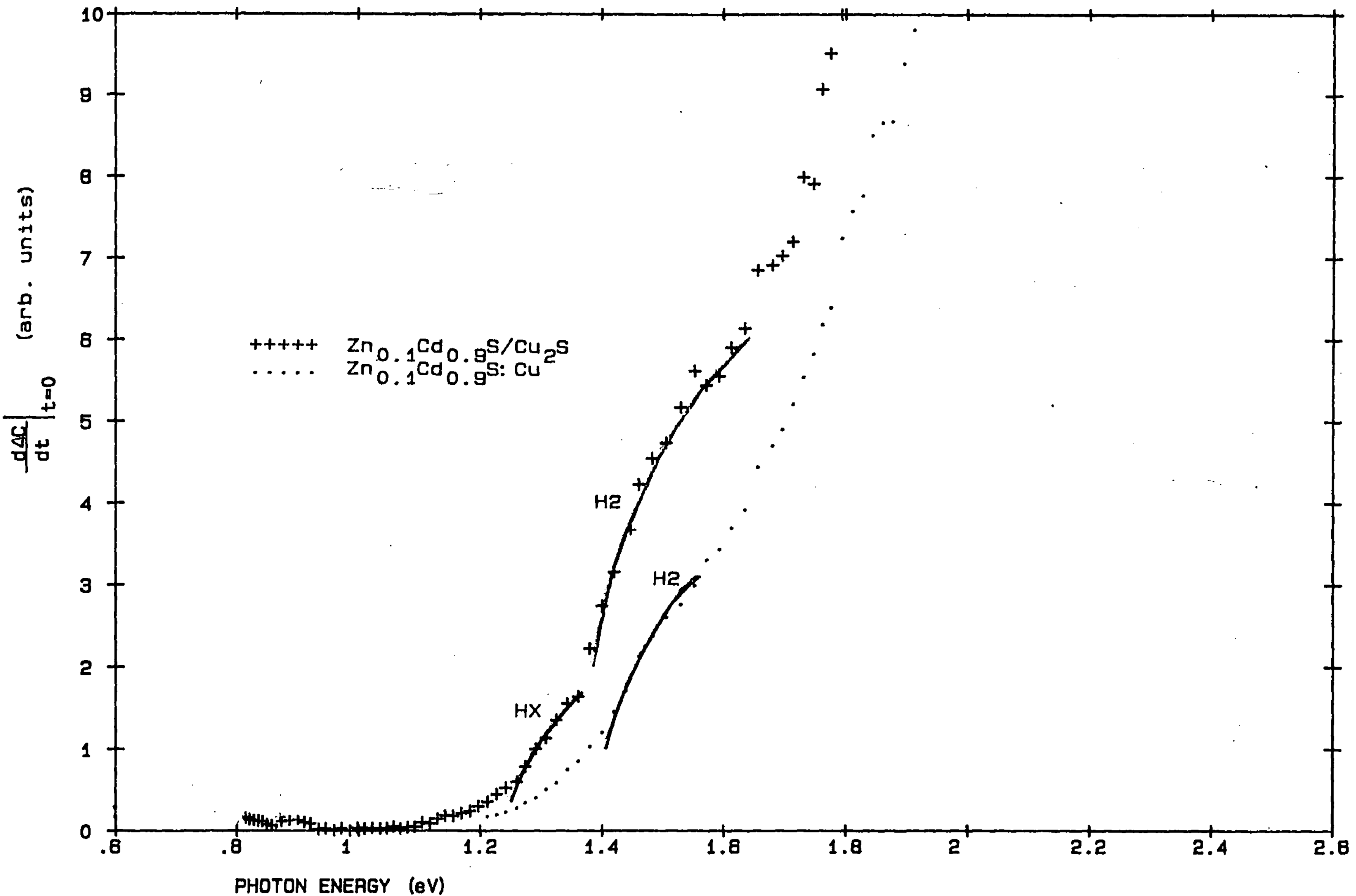

Figure 6.17 DLOS spectra for copper doped $Zn_{0.1}Cd_{0.9}S$ and the $Zn_{0.1}Cd_{0.9}S/Cu_2S$ heterojunction

Sample	Method	H1 (E_T-E_V)/eV	H2 (E_T-E_V)/eV	HX (E_C-E_T)/eV
CdS	DLOS	0·32 ± 0.03	1·11 ± 0.05	—
	PHCAP	0·35 ± 0.05	1·10 ± 0.05	—
$Zn_{.02}Cd_{.98}S$ (Cu-doped)	DLOS	—	1·15 ± 0.1	—
	PHCAP	—	—	—
$Zn_{0.1}Cd_{0.9}S$	DLOS	0·35 ± 0.03	1·16 ± 0.08	—
	PHCAP	—	—	—
$Zn_{0.1}Cd_{0.9}S$ / Cu_2S	DLOS	0·30 ± 0.03	1·16 ± 0.1	1·25 ± 0.05
	PHCAP	—	—	—
$Zn_{0.2}Cd_{0.8}S$	DLOS	0·38 ± 0.03	1·16 ± 0.05	—
	PHCAP	0·35 ± 0.05	1·10 ± 0.05	—
$Zn_{0.2}Cd_{0.8}S$ / Cu_2S	DLOS	—	—	—
	PHCAP	0·35 ± 0.05	1·10 ± 0.05	1·22 ± 0.05
$Zn_{.45}Cd_{.55}S$ (Cu-doped)	DLOS	—	1·13 ± 0.05	—
	PHCAP	—	—	—

Figure 6.18 Summary of states observed in $Zn_xCd_{1-x}S$ using DLOS and PHCAP

6.6 Discussion

6.6.1 Discussion of DLTS Results

DLTS has shown the presence of a dominant electron trap in CdS which has been denoted E2. With incorporation of Zn giving a composition range up to x=0.19, a similar, dominant electron trap was observed. This has been correlated with E2 and it is apparent that the peak DLTS response moves to higher temperature with an increase in Zn concentration; this level has been denoted E2(x). Arrhenius plots for the thermal emission rates for E2(x) have displayed an increase in its activation energy with composition 0.41eV (x=0), 0.43eV (x=0.02), 0.50eV (x=0.09), 0.52eV (x=0.11), 0.65eV (x=0.19). Fig. 6.19 shows a plot of the activation energy of E2(x) with composition; the band gap variation is included. It seems that the level is pinned to the valence band. In that event it would have a functional relationship with composition similar to that for the band gap. A least squares fit to the data gives the relation

$$E(x) = 0.41 + 0.68x + 2.98x^2 \qquad 6.4$$

for the activation energy dependence of E2(x) with composition x; this is shown as the solid line in fig. 6.19. This implies that for the defect E2(x), the thermal emission rates are defined by

$$e_n(x) = N_c \sigma_n V_{th} \exp[-(0.41 + 0.68x + 2.98x^2)/kT] \qquad 6.5$$

where $e_n(x)$ is the emission rate for the trap E2(x), N_c is

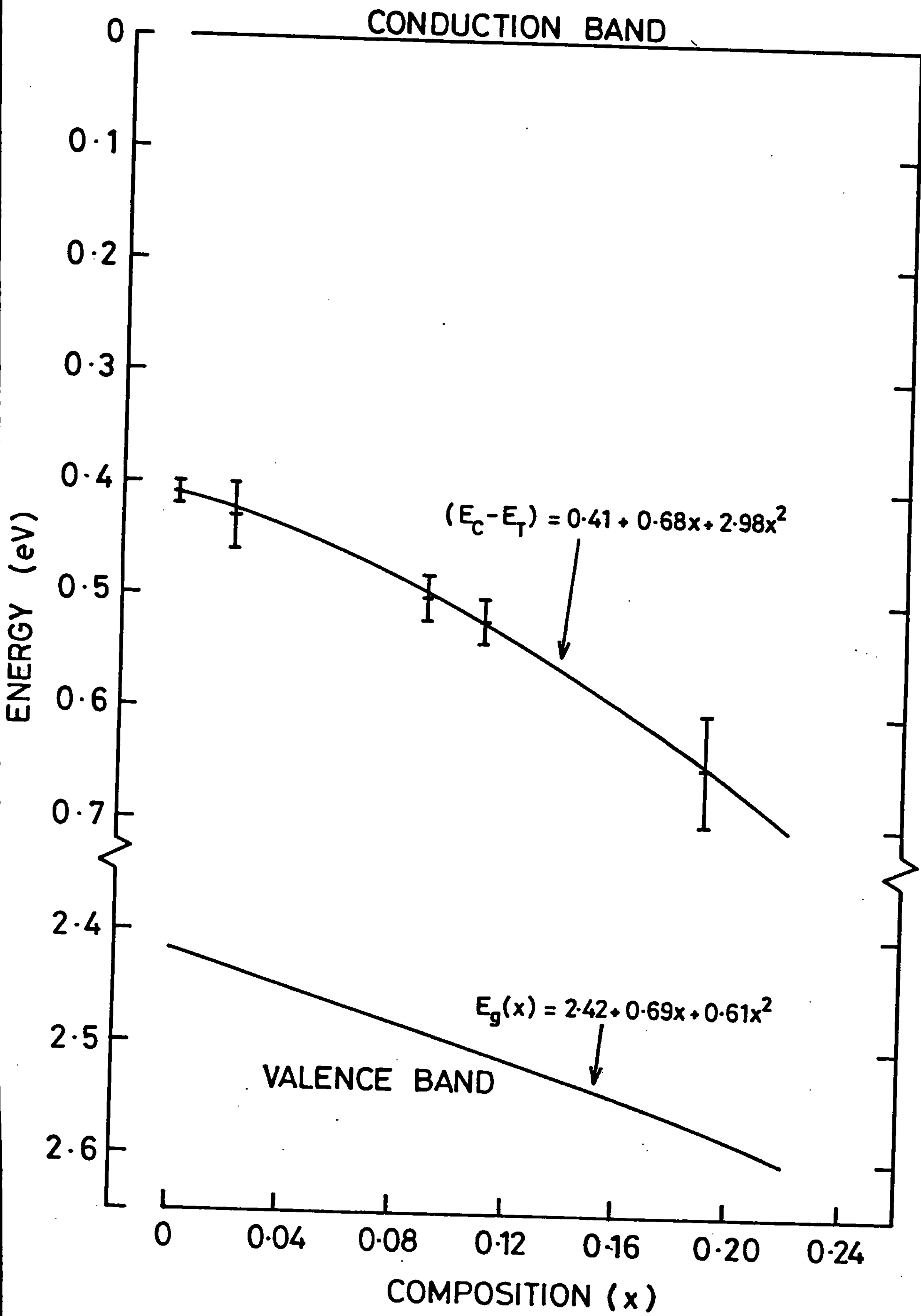

Figure 6.19 Variation in the activation energy for E2(x) with composition

the effective density of states in the conduction band, σ_n is the capture cross-section, and V_{th} the thermal velocity of the electron. This shows that at a fixed temperature, the electron emission rate decreases with x.

E2(x) was only observed in 826 with no consistency in response through the boule. Only one sample from slice 8 with x=0.11 gave a strong DLTS signal. The most striking result was that E2(x) was not observed in the material grown by the Piper-Polich method although the level may have been present but outside the limits of resolution of the DLTS system. This demonstrates the effect of growth conditions on the defect signature of the material.

One important feature of the DLTS peaks was the broadening with increasing x. This may be due to a macroscopic fluctuation in the mixed crystal composition giving locally varying band gaps. Another possibility is microscopic fluctuations in the atomic arrangement. Assuming that the state arises from an associated native-impurity centre, as suggested in chapter 5 for E2, then the broadening may arise from a statistical variation in the arrangement of Cd and Zn atoms around the defect site. The DLTS signal would then consist of a combination of responses from each of these configurations. The position of the peak response would depend upon the statistical distribution of these configurations.

The 0.88eV level detected for the material with composition x=0.11 seemed to correlate with the response to

extended defects observed in the capacitance-temperature scan. Consequently, it is probable that this level is similar to E4 observed in CdS which is thought to be associated with subgrain boundaries. The dislocation density was found to be an order of magnitude less for the ternary sample and this was reflected in the much reduced DLTS response compared to that for CdS.

6.6.2 Discussion of Hole Traps Observed in (ZnCd)S

The preparation of an efficient CdS/Cu_2S heterojunction solar cell involves a sensitising bake at 200C which results in copper migration into the II-VI material [27]. The impurity produces two acceptor states, H1 and H2, in CdS at 0.34eV and 1.1eV above the valence band as has been discussed more fully in chapter 5. They arise from the crystal field splitting of the copper d^9 state [28].

ODLTS gave a clear response for H2 in copper doped $Zn_xCd_{1-x}S$ and in the $Zn_{0.1}Cd_{0.9}S/Cu_2S$ heterojunction. However, for the undoped material copper states were observed in the Piper-Polich grown boules (799, 819, 820) but not in the Clark-Woods grown boule. The reason for this is that the Piper-Polich crystals were grown at a much higher temperature and therefore, were more susceptible to accidental contamination with copper. The excited state, H1, of the defect was only observed in the doped sample and poorly resolved in the heterojunction for $x<0.2$. Up to this composition the activation energies and capture cross-sections for H1 and H2 were 0.35eV, 10^{-12} cm^2 and 1.1eV,

10^{-12} cm^2 respectively displaying no variation with composition, indeed these results were identical to those for the binary compound CdS as discussed in chapter 5. This suggests that the states H1 and H2 are pinned to the valence band. H2 was also observed in the Piper-Polich material (for x up to 0.45) with similar thermal parameters to those found for other samples. H1 was not seen in these samples due to practical limitations of the system as was mentioned above.

The PHCAP results on samples with x=0, x=0.1, x=0.2 and x=0.3 also showed a response to the copper levels. At room temperature the PHCAP spectrum showed a negative going response at 0.75eV. This corresponded to an internal transition between the copper ground and excited states [28,29]: an electron trapped at H1 and a hole trapped at H2 (band bending in the depletion region allows this level to rise above the Fermi level) correspond to the neutral ground state; at photon energies close to 0.75eV electrons were excited from H1 to H2 giving the neutral excited state. The photocapacitance response came about by the thermal excitation of electrons from the valence band into H1. This reduced the positive space charge in the depletion region thereby reducing the capacitance. This was not observed at 85K since H1 could not be thermally refilled.

DLOS showed the spectral dependence of the optical electron capture cross-section. Thresholds were observed that corresponded to the copper levels at 1.1eV and 0.34eV for all the samples studied. Indeed even for the undoped material DLOS gave a response for the copper states which

were not characterised by ODLTS.

The important point about these results was that the activation energies of the copper states H1 and H2 were unaffected by changes in the composition. Therefore, the crystal field splitting of the copper d^9 state was little affected by the incorporation of zinc. Müller et al [30] have obtained theoretical values for the splitting in ZnS:Cu and CdS:Cu - 0.65eV and 0.67eV respectively. The experimental value from the ODLTS, PHCAP and DLOS results was about 0.7eV and was similar to that obtained by others [eg 28].

Kullendorf et al [31] have discussed the effect of composition on the copper states for CdS_ySe_{1-y} and showed that there was a shift in the energy positions of H1 and H2 relative to the valence band edge, with the incorporation of Se. The change in energy was explained in terms of the symmetry of the defect site. Assuming the defect is a substitutional impurity on the metal site [28] then it is surrounded tetrahedrally by S as well as Se nearest neighbours. Depending upon the distribution, the impurity may have T_d symmetry (4S or 4Se), C_{3v} symmetry (3S and 1Se, or 1S and 3Se) or C_{2v} symmetry (2S and 2Se). This change in symmetry will affect the degree of crystal field splitting. The replacement of S with Se causes an additional perturbation that alters the covalent bonding between the impurity and its nearest neighbours. This change in the configuration of the defect site would result in a change in the activation energies of the copper ground and excited

states; this was shown by Kullendorf et al [31].

The fact that there was little change in the crystal field splitting with an increase in Zn content for $Zn_xCd_{1-x}S$ may also be explained in terms of the symmetry of the defect site. In this case the copper defect site is surrounded by 4 sulphur atoms, that is, the nearest neighbours are identical; the impurity centre has T_d symmetry. The perturbation introduced by replacing Cd with Zn on the impurity site would be much less than replacing S by Se, since the metal atoms are not nearest neighbours; indeed they may be shielded by the sulphur nearest neighbours. The overall effect as shown experimentally is that there would be little change in the crystal field splitting and the states pinned to valence band.

In addition to the copper states, the PHCAP and DLOS results indicated a further level in the heterojunction. In the PHCAP spectrum there was a threshold at 1.22eV and 1.27eV suggesting a recombination centre near midgap. Electron excitation from this centre to the conduction band gave a positive going threshold at 1.22eV. This was followed by a decrease at 1.27eV corresponding to a refilling of the centre from the valence band. DLOS gave a similar threshold for a sample with composition x=0.1 at 1.2eV below the conduction band. The important point is that this trap was not observed in the CdS heterojunction nor in the mixed crystal Schottky devices. The indication is that this centre was an artefact of the processing of the device. During the formation of the CdS/Cu_2S junction an ion exchange reaction occurs - for

example, the dry barrier process involves the solid state reaction

$$2CuCl + CdS \longrightarrow Cu_2S + CdCl_2$$

In the case of the ternary compound, Zn is thought to be involved to a lesser degree than the Cd during the reaction. In fact it has been shown that the processing leaves a Zn rich layer at the interface [32]. Pande et al [10] suggested that the defect state observed in the present work was an artefact of this step of the fabrication of the device. It was suggested that the state was probably due to an associated copper-vacancy complex in the Zn rich layer. The defect state is likely to behave as a recombination centre and so will have the effect of reducing the carrier lifetime of the photogenerated carriers in the solar cell. A reduced short circuit current has been observed for the $Zn_xCd_{1-x}S/Cu_2S$ compared to the CdS/Cu_2S solar cell [8]. The presence of this recombination centre would contribute to the poor current collection efficiency in addition to other phenomena proposed by others [9] and mentioned in the introduction to this chapter.

6.7 Conclusion

The main deep level electron and hole trapping centres in $Zn_xCd_{1-x}S$ have been investigated by DLTS, ODLTS, DLOS and PHCAP. These results have been summarised in fig. 6.20.

DLTS has shown a dominant electron trap in the mixed

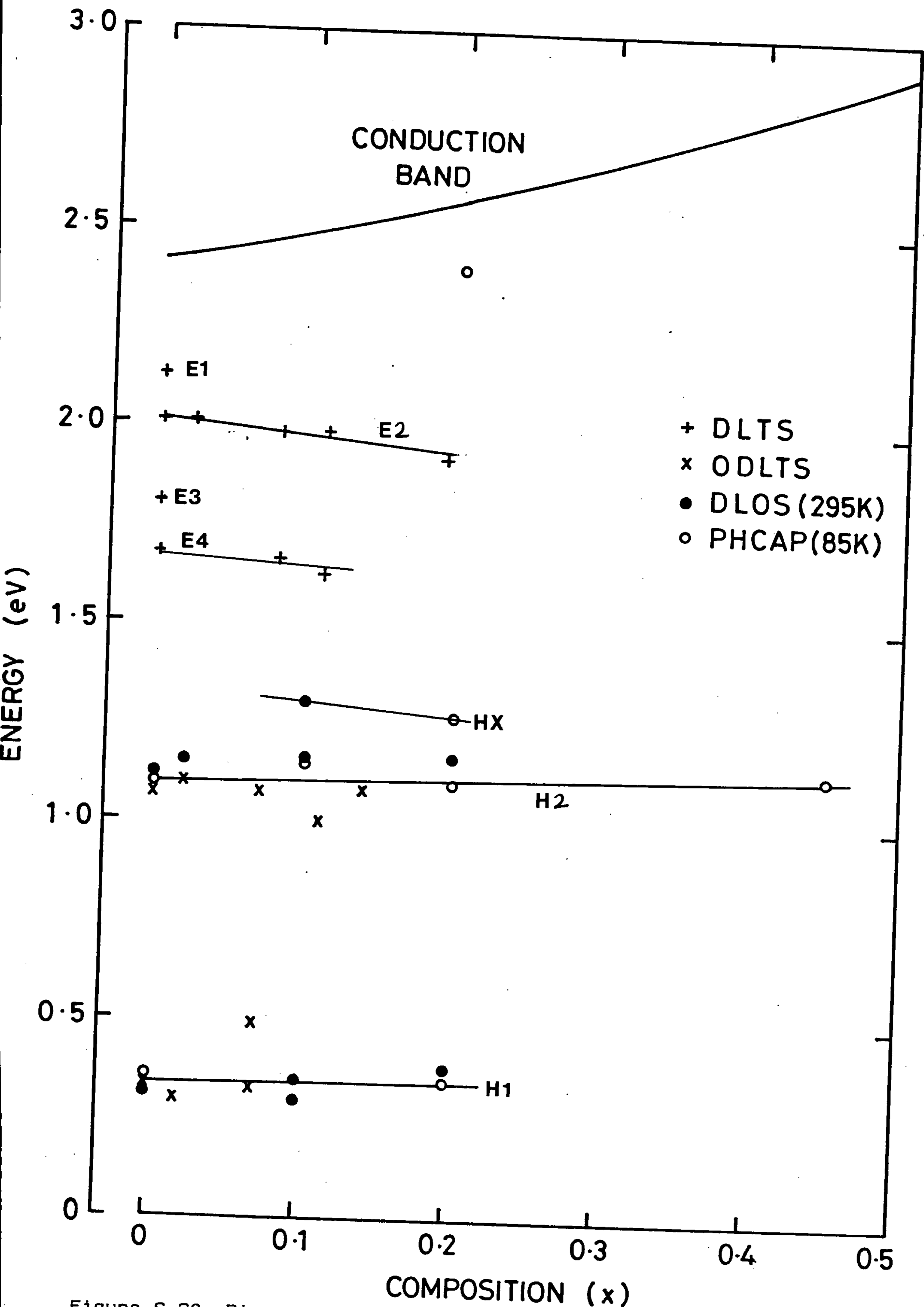

Figure 6.20 Diagram to summarise the deep defect states observed in $Zn_xCd_{1-x}S$ using DLTS, ODLTS, DLOS and PHCAP

crystal similar to E2 found in CdS. With incorporation of Zn, the peak moved to a higher temperature and the thermal activation energy for electron emission increased. Another electron trap was observed at 0.88eV (x=0.11) and was probably similar to the centre E4 characterised in CdS in that it may be associated with extended defects.

The hole traps were investigated using ODLTS, DLOS and PHCAP. Two traps were seen predominantly throughout the samples studied; these were thought to be the same as the copper states seen in CdS - an excited state (H1) and a ground state (H2) due to the crystal field splitting of the copper d^9 state. There was no significant change in the activation energies and capture cross-sections over the composition range studied nor was there any apparent change in the crystal field splitting of these states. In addition, these states appeared to be pinned to the valence band. An explanation for this has been offered in terms of the symmetry of the defect site (assuming substitutional copper) which effectively does not change over the whole composition range. There is little perturbation on the crystal field at the defect site and negligible change in the covalent bonding between the impurity and its neighbours since its nearest neighbours are sulphur atoms throughout.

PHCAP and DLOS showed the presence of a deep hole trap near midgap in the mixed crystal heterojunction. This was not observed in the CdS/Cu_2S heterojunction nor in the mixed crystal Schottky devices. This trap was thought to be a recombination centre which could reduce the free carrier

lifetime during the operation of the solar cell. This would reduce the photogenerated current and thereby reduce the short circuit current as has been observed. This is thought to be one of the contributory factors for the reduced short circuit current, so that, higher efficiency, mixed crystal solar cells have not been realised.

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CHAPTER 7

POLYCRYSTALLINE CdS FILMS

7.1 Introduction

Thin film CdS has been studied extensively in an effort to produce low cost solar cells. The advantage of this material is that it can be produced cheaply with a high purity and be deposited in film form relatively economically compared to the III-V semiconductors and Si. The CdS/Cu_2S solar cell [eg 1-3] consisting of a Cu_2S absorber layer and CdS collecter, has excited much interest. The properties of the copper sulphide absorber layer include a band gap of 1.2eV which is close to the peak solar radiation; it has a high absorption coefficient and therefore, only thin films are required (0.1μ compared to -100μ for Si); and it can be deposited onto CdS using low technology, thereby, maintaining minimum cost [4]. Other types of CdS solar cells have been investigated with a view to improved properties of the absorber layer. One example is the CdS/CdTe heterojunction solar cell [eg 5,6] which has a theoretical solar energy conversion efficiency of 17% - the CdTe layer has the parameters for an absorber layer close to the optimum [4]. There are many techniques used for the deposition of CdS films for application to solar cells, for example, spray pyrolysis [7], electrophoresis [8], evaporation [9] and silk screen printing [10]. Whichever of these is used, the

primary consideration is the cost of processing which must be minimised to have a commercially viable solar cell.

This chapter deals with polycrystalline CdS films prepared by screen printing and by thermal evaporation. Their preparation was optimised for crystallinity and their deep level defect signatures investigated using DLTS and ODLTS.

7.2 Silk-Screen Printed CdS

7.2.1 Introduction

Silk screen printing is one of the simplest techniques for the deposition of a powdered semiconductor and potentially of great use for the fabrication of large area solar cells. This technology has a good grounding based on work carried out during the 1950's [eg 11,12] when CdS was considered an important phosphor material. More recently, Vodjani et al [13] reported on a screen printed CdS/Cu_2S solar cell but its efficiency did not exceed 1%. Further work by Matsumoto et al [2] has improved this to 9%. As a result of the simplicity of the screen printing technique, other types of heterojunction solar cells have been fabricated on CdS. These include CdS/CdTe [5,6,14] and $CdS/CuInSe_2$ [15] which have achieved efficiencies of 6.3% and 3% respectively.

Silk screen printing offers a cheap method of producing films of CdS without the wastage of materials associated with evaporation. This study was primarily concerned with the

preparation of thick films of CdS followed by the characterisation of deep levels by DLTS/ODLTS which may affect the operation of a device made on the material. This was extended to a DLTS/ODLTS study of the CdS/Cu_2S heterojunction produced by the dry barrier method [16] for comparison with the corresponding device made on single crystal CdS.

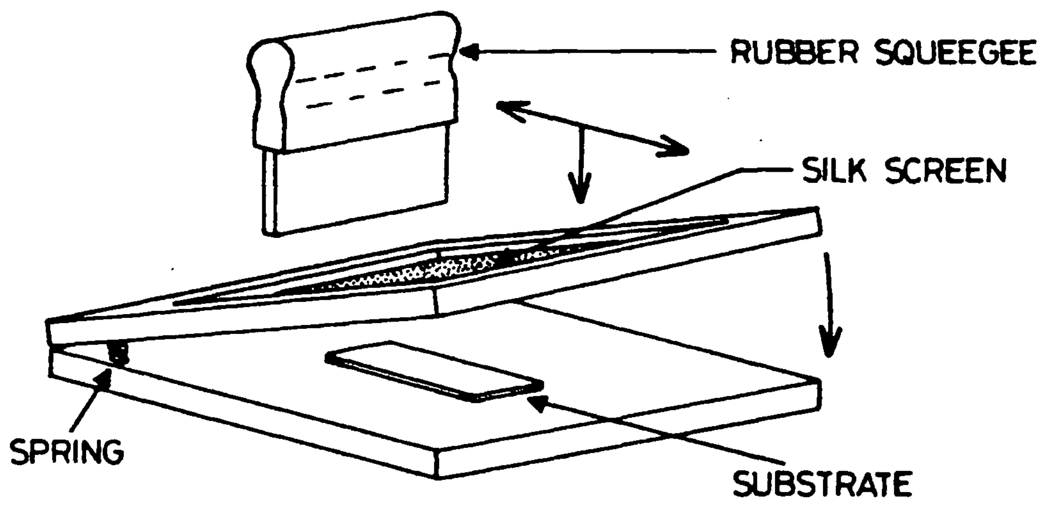
7.2.2 Preparation of Silk Screen Printed CdS

The primary considerations for producing a screen printed CdS film were crystallinity, thickness and adherence to the substrate. Adherence to the substrate presented no problem and indeed after a heat treatment the films could only be removed with difficulty; robustness of a thin film is of great importance in any subsequent application.

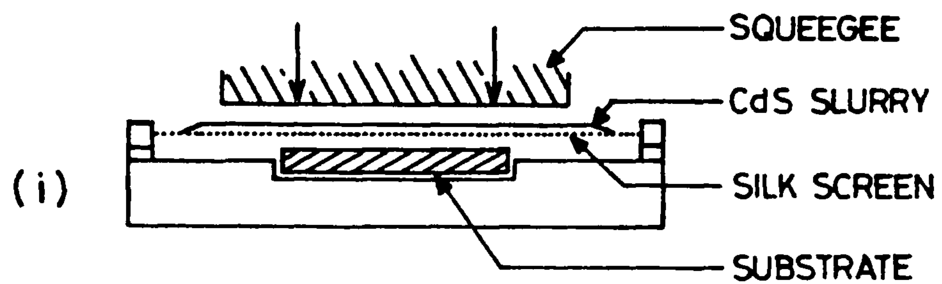
The material used for the preparation of the films was General Electric Company electronic grade CdS. This was in powdered form with a wide distribution of particle size - 1-20μ. The as-received powder was ball-milled in order to obtain a smaller distribution in particle size and improve the packing of the subsequent layer. Ball-milling for about 2hrs gave particles 0.5-2μ in diameter. For silk screen printing the CdS was dispersed in a propylene glycol (PPG) which acted as a binder. In addition $CdCl_2$ was added as a flux for the annealing process. The ratio by weight was 60% CdS, 25-30% PPG and 10-15% $CdCl_2$. Initially the $CdCl_2$ was dissolved in the PPG by ultrasonic stirring. Into this solution the milled CdS was added and thoroughly mixed by

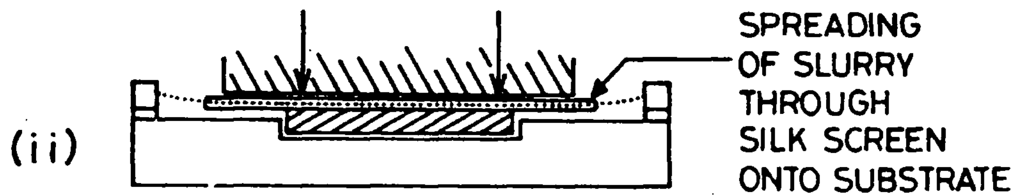
stirring to give the slurry used in the printing stage of the process. At this point it was occasionally necessary to add a few drops of PPG in order to make the slurry thixotropic - this was essential for uniform spreading of the film. Fig. 7.1 shows the basic design of the equipment for silk screen printing. It consisted of an aluminium frame over which was stretched the silk-screen (120 mesh). The substrates were SnO_x coated glass slides (Photon Power). They were degreased in trichloroethane vapour for about 1 hr, washed in methanol and maintained in isopropanol vapour until ready for use. The reason for these procedures was to minimise the contamination of the substrate surface which might have disrupted the semiconductor film. For the printing process, the cleaned substrates were placed in a recess in the base of the equipment and covered by the silk screen (see fig. 7.1). The CdS slurry was poured onto the screen and spread over the substrate as evenly as possible with a rubber squeegee. Subsequently, the films were dried in an oven at 120C for about 12hrs giving a powdery film about 20-30μ thick.

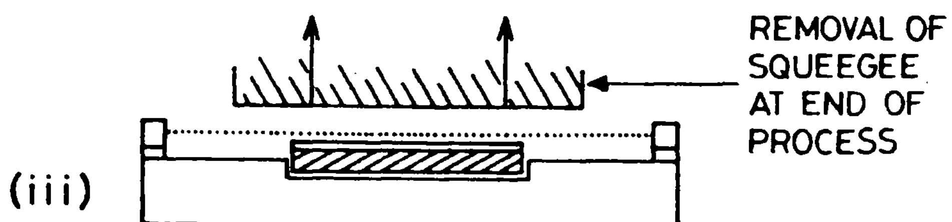
For annealing, the slides were mounted on a silica plate and inserted into a horizontal furnace. The plate gave some support for the glass substrate during the heating process. The films were annealed in an argon atmosphere flowing through the furnace at about 100mls/min with a duration ranging from 40min to 3hr and a temperature between 600C and 700C. The films studied had undergone the following heat treatments



SILK SCREEN PRINTER







SILK SCREEN PRINTING SEQUENCE

Figure 7.1
A schematic diagram of the equipment and illustration of the silk screen printing process of CdS layers

Sample	Treatment
SP1	640C 40min
SP2	640C 1hr
SP3	640C 3hr
SP4	670C 1hr
SP5	670C 3hr
SP6	700C 1hr

The annealed layers were assessed by scanning electron microscopy for degree of grain growth and crystallinity, and to estimate film thickness.

CdS/Cu_2S heterojunctions and CdS/Au Schottky devices were prepared on these films. For the heterojunctions, the Cu_2S was deposited topotaxially using the dry barrier process [16] as described for single crystal CdS in section 5.3.2. Contact was made to the Cu_2S layer by evaporation of a gold dot with a slightly smaller diameter. The Schottky barrier was made, again by gold evaporation onto the CdS surface. In both devices ohmic contacts were made by annealing indium onto the CdS at 200C in argon atmosphere fo 10min. Current-voltage, capacitance-voltage, DLTS and ODLTS measurements were carried out in order to characterise the junctions and the material.

7.2.3 SEM and RHEED

The scanning electron microscope (Cambridge Stereoscan 600) was used for film assessment. This gave feedback for the optimisation of the annealing process and also to

determine the layer thickness. The as-deposited films were powdery with an open structure. For an anneal at 640C for 40mins or 1hr there was negligible grain growth and the film retained its unprocessed structure although it adhered much more strongly to the substrate. At 640C for 3hrs the grains began to melt and fuse together (see fig 7.2) There was progressive fusion up to 670C for 3hrs and at 700C for 1hr the grains had almost completely fused together (see fig 7.3 and 7.4). Some voids were observed in these films but there seemed not to be the problem of pinholes so often encountered in thin film preparation. Annealing at higher temperatures was impracticable since the glass substrate began to melt.

Fig 7.5 shows a RHEED pattern taken on a TEM (JEM 120) operating at 100kV of a film annealed at 700C for 1hr. The (102) and (103) lines show that the material was hexagonal. The spottiness in the pattern indicated that there were some large oriented grains randomly distributed.

7.2.4 Current-Voltage Characteristics

The current-voltage (I-V) characteristics of the CdS/Au and CdS/Cu_2S devices showed a clear dependence on anneal temperature and duration. The I-V results for the Schottky diodes prepared on the variously treated films are given in fig. 7.6. For the material annealed at 640C for 1hr the diode showed a poor reverse bias characteristic with breakdown at about -0.5V. After annealing for a 1hr at 700C, this decreased to -2.0V. In forward bias the samples that had been annealed at the higher temperatures or for a longer

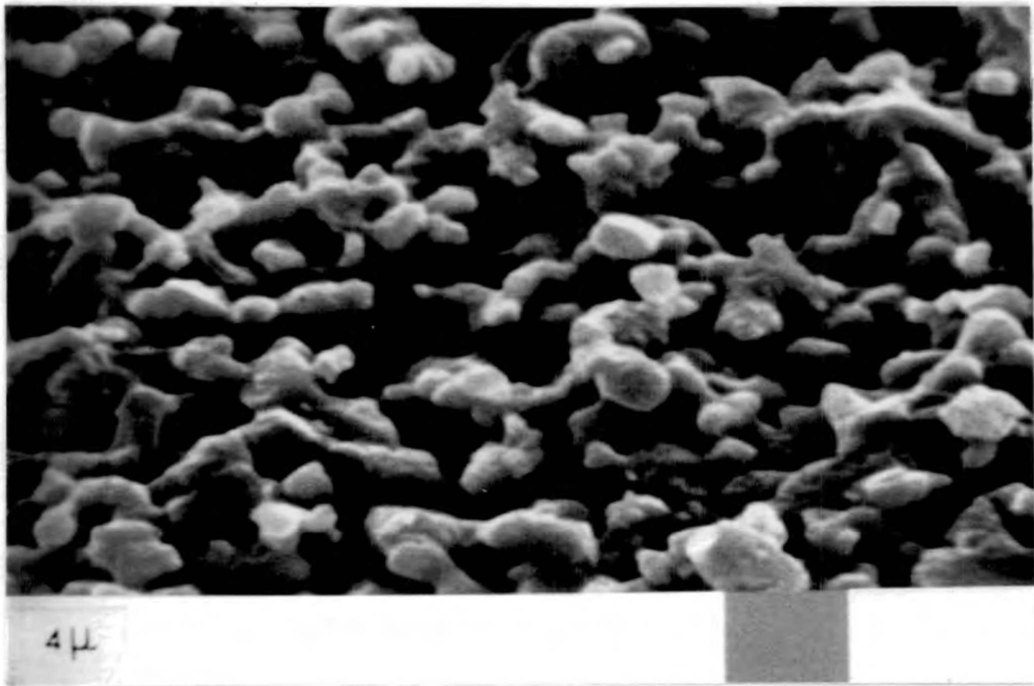


Figure 7.2 Surface of SP film annealed at 640C for 3hrs

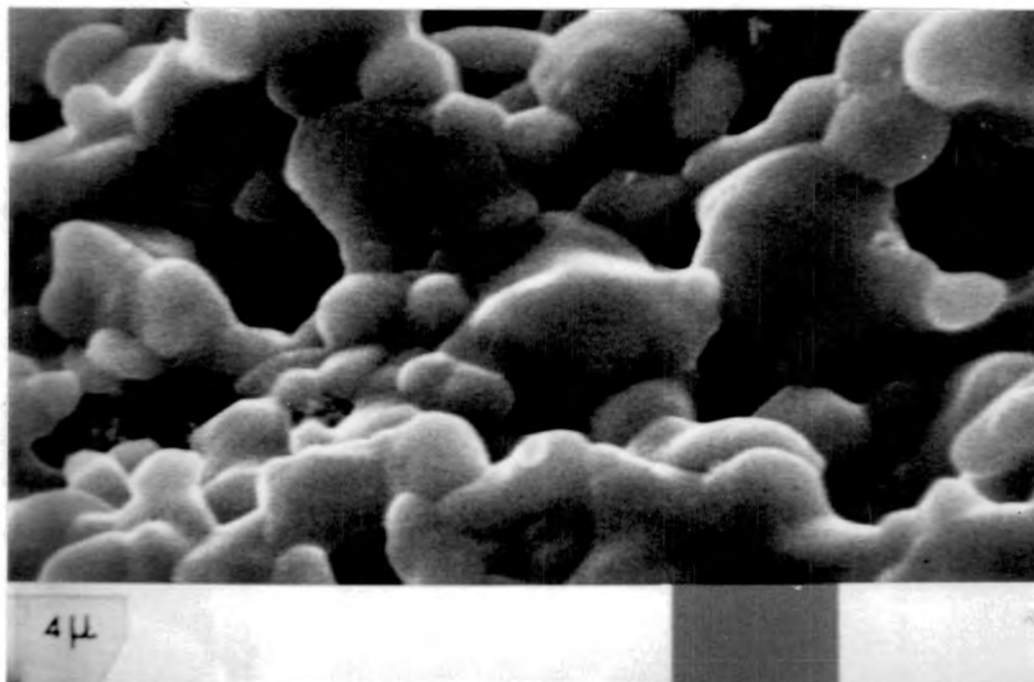


Figure 7.3 Surface of SP film annealed at 670C for 3hrs

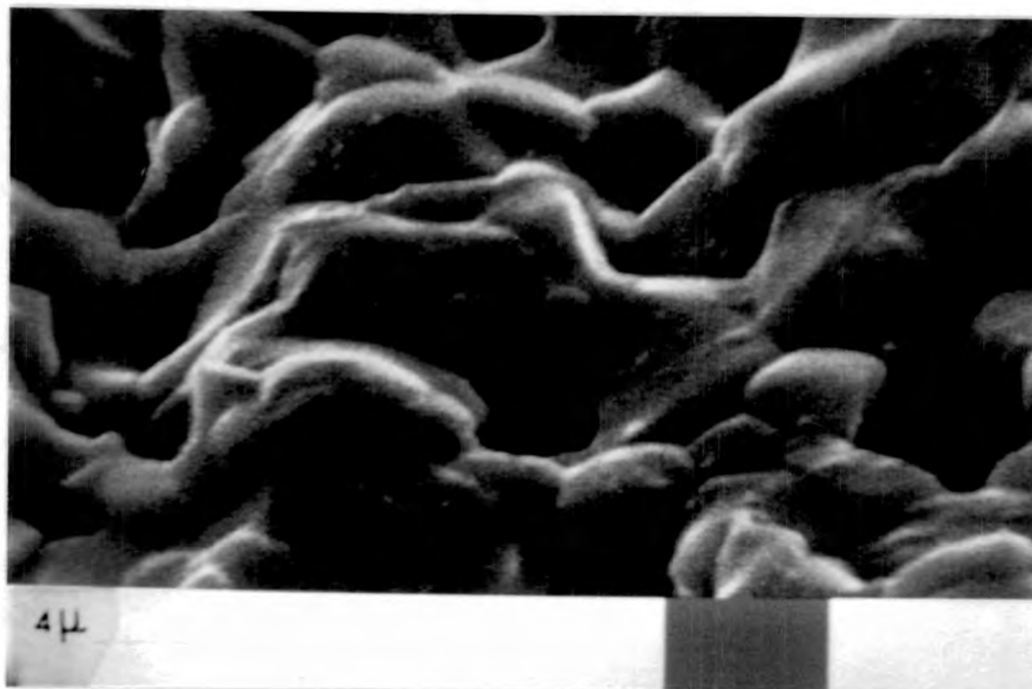


Figure 7.4 Surface of SP film annealed at 700C for 1hr

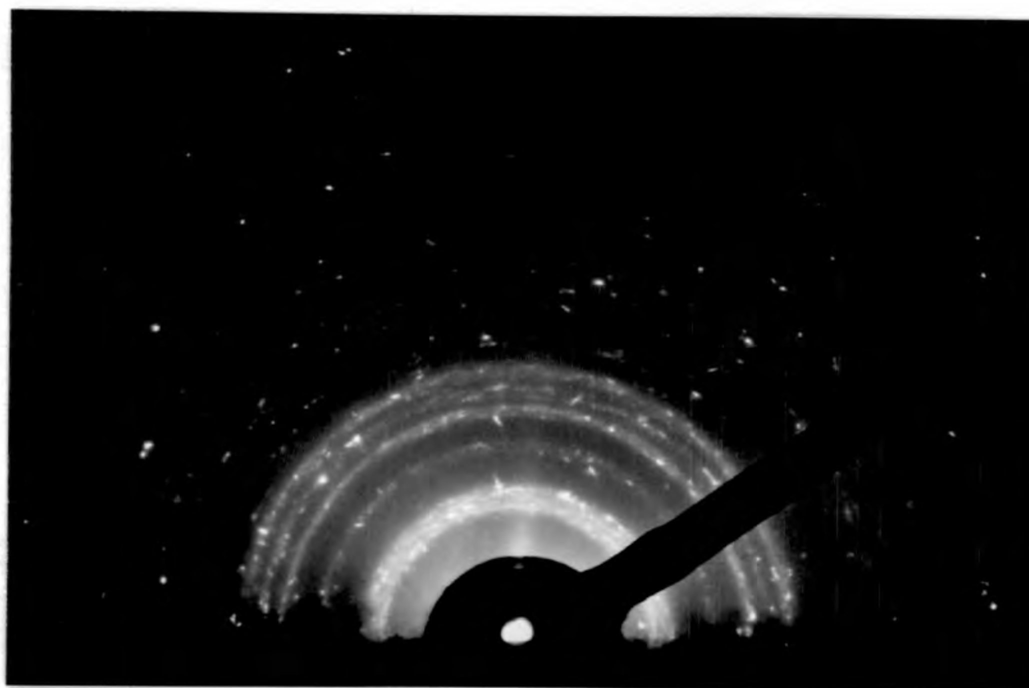


Figure 7.5 RHEED pattern of the above film

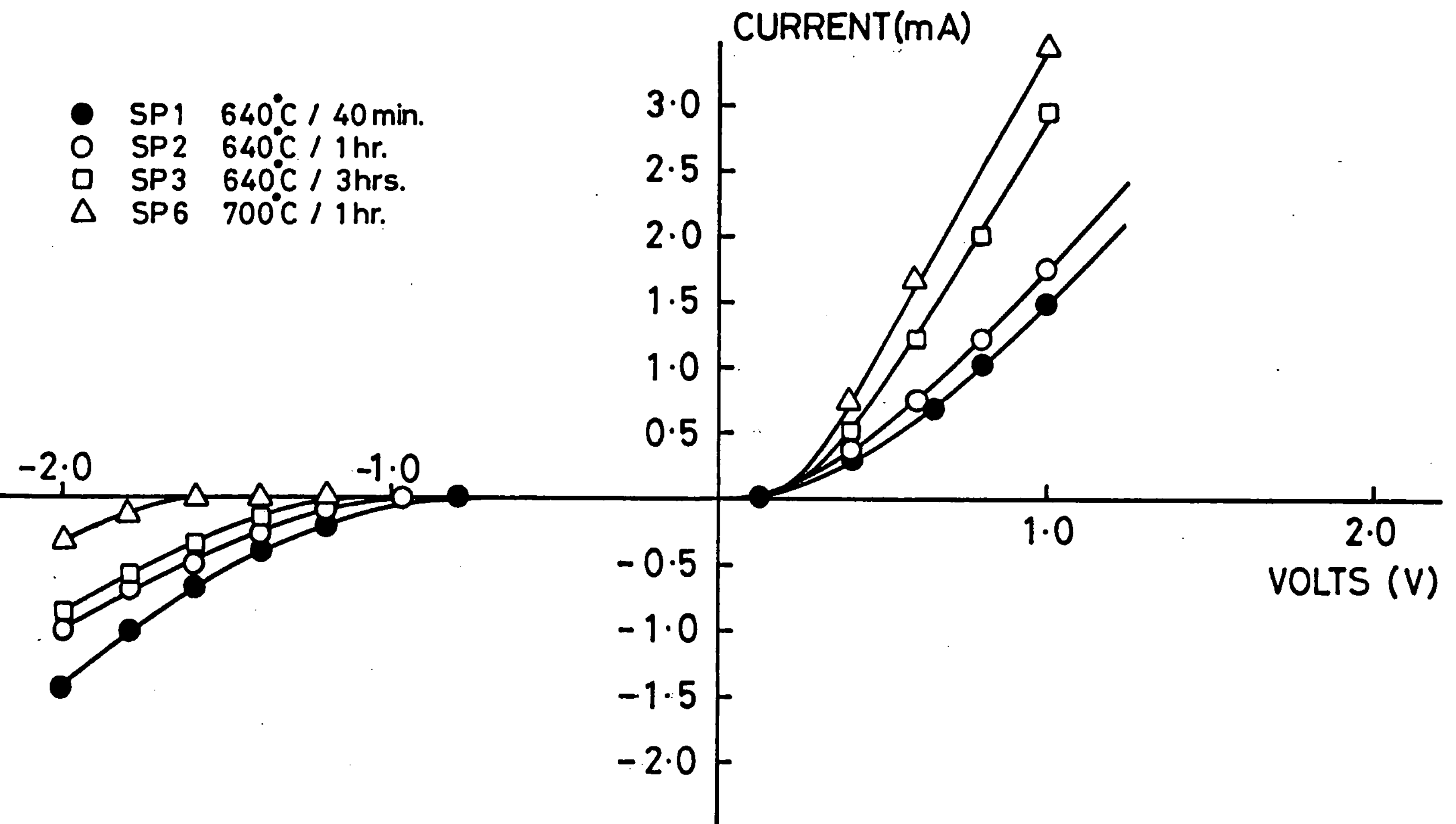


Figure 7.8 Current-voltage characteristics of the Schottky diodes

duration, were more conducting due to the reduction in the number of grain boundaries which provide potential barriers to the flow of carriers; and in addition, chlorine from the flux provides shallow donor levels which increase the free carrier concentration and therefore, reduce the resistivity of the films.

The photovoltaic behaviour of the heterojunctions was investigated from the current-voltage characteristics of the devices. The current was monitored with voltage in the dark and under AM1 illumination - equivalent to $1kW/m^2$. Fig. 7.7a shows the results for heterojunctions on CdS annealed at 640C for 3hrs. As can be seen there was negligible photovoltaic effect with no measurable open circuit voltage (OCV) nor short circuit current (SCC). The material annealed at 670C for 3hrs gave heterojunctions with the current-voltage response as shown in fig. 7b. The OCV and SCC for junctions on this material were typically 0.26V and 0.22mA respectively. The fill factor was determined from [4]

$$FF = \frac{\text{max power output}}{\text{OCV x SCC}} \qquad 7.1$$

and had a value of 0.6. After annealingat at 700C for 1hr (fig. 7.7c) the subsequent heterojunctions gave poorer OCV and SCC than with the material annealed at 670C for 1hr. Typical OCV, SCC and FF values were 0.2V, 0.15mA and 0.5 respectively.

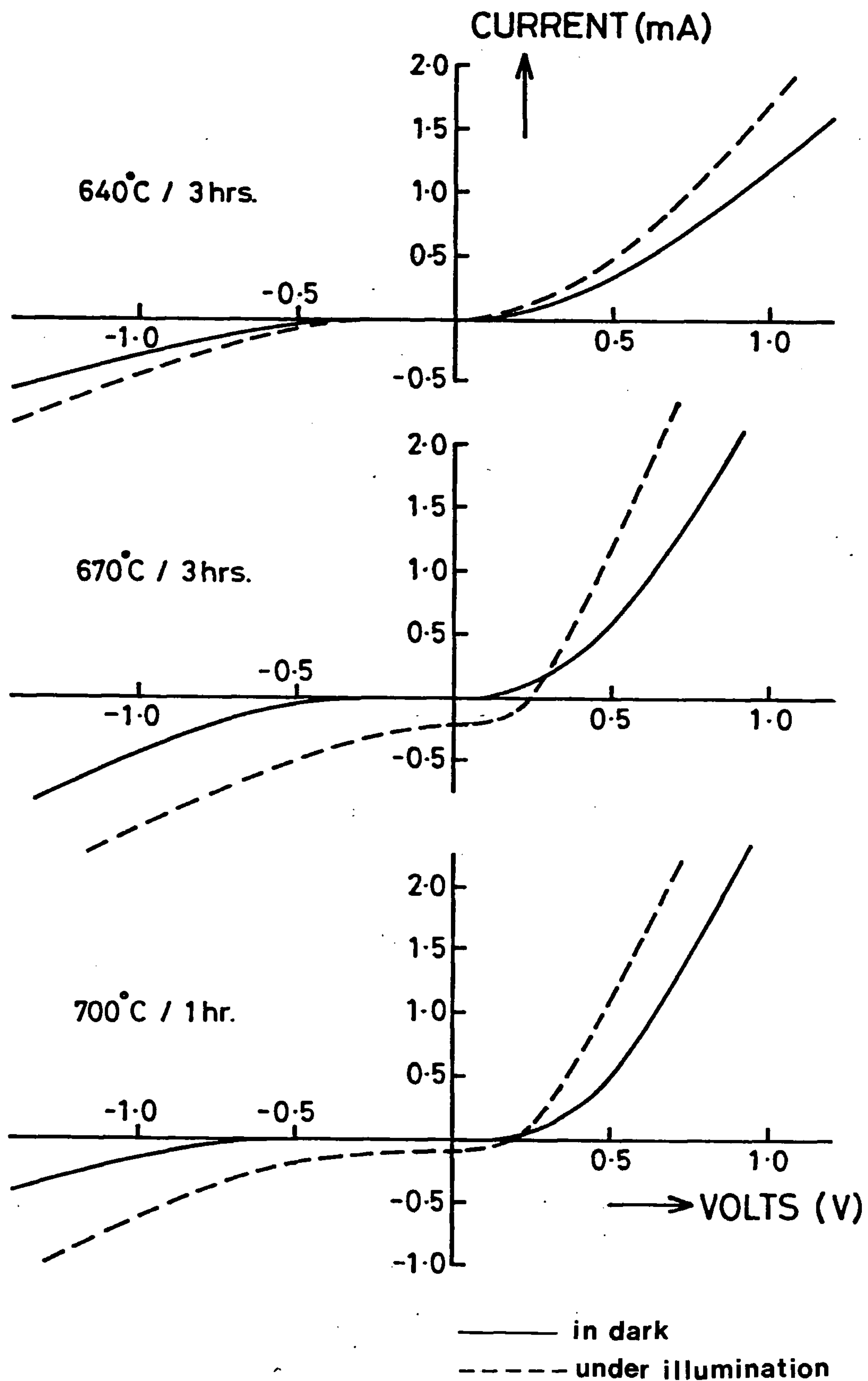


Figure 7.7 Current-voltage characteristics of the heterojunctions

7.2.5 Capacitance-Voltage Results

Capacitance-voltage measurements were made on the CdS/Au Schottky devices and CdS/Cu_2S heterojuntions. The free carrier concentrations were obtained from the $1/C^2$ vs V plots.

The measurements on Schottky devices showed that there was an increase in the free carrier concentration with increase in duration and temperature of anneal. The Schottky diodes gave linear plots for $1/C^2$ vs V for all the samples studied as shown in fig. 7.8. For the material annealed at 640C the free carrier concentration was typically of the order of $2x10^{15}$ cm^{-3}. Increasing the duration and/or the temperature of the anneal raised the free carrier concentration, so that for an anneal at 700C for 1hr resulted in a value for N_d that was some two orders of magnitude greater. The results for free carrier concentrations as a function of anneal conditions are summarised in fig. 7.9.

The heterojunctions displayed an unusual behaviour in the capacitance-voltage charateristic as shown in fig. 7.10. There was an initial increase in capacitance upto a reverse bias of -0.5V. This behaviour was not observed in the Schottky devices and shows the inapplicabilty of the ideal Schottky-Mott theory for the free carrier determination in this case.

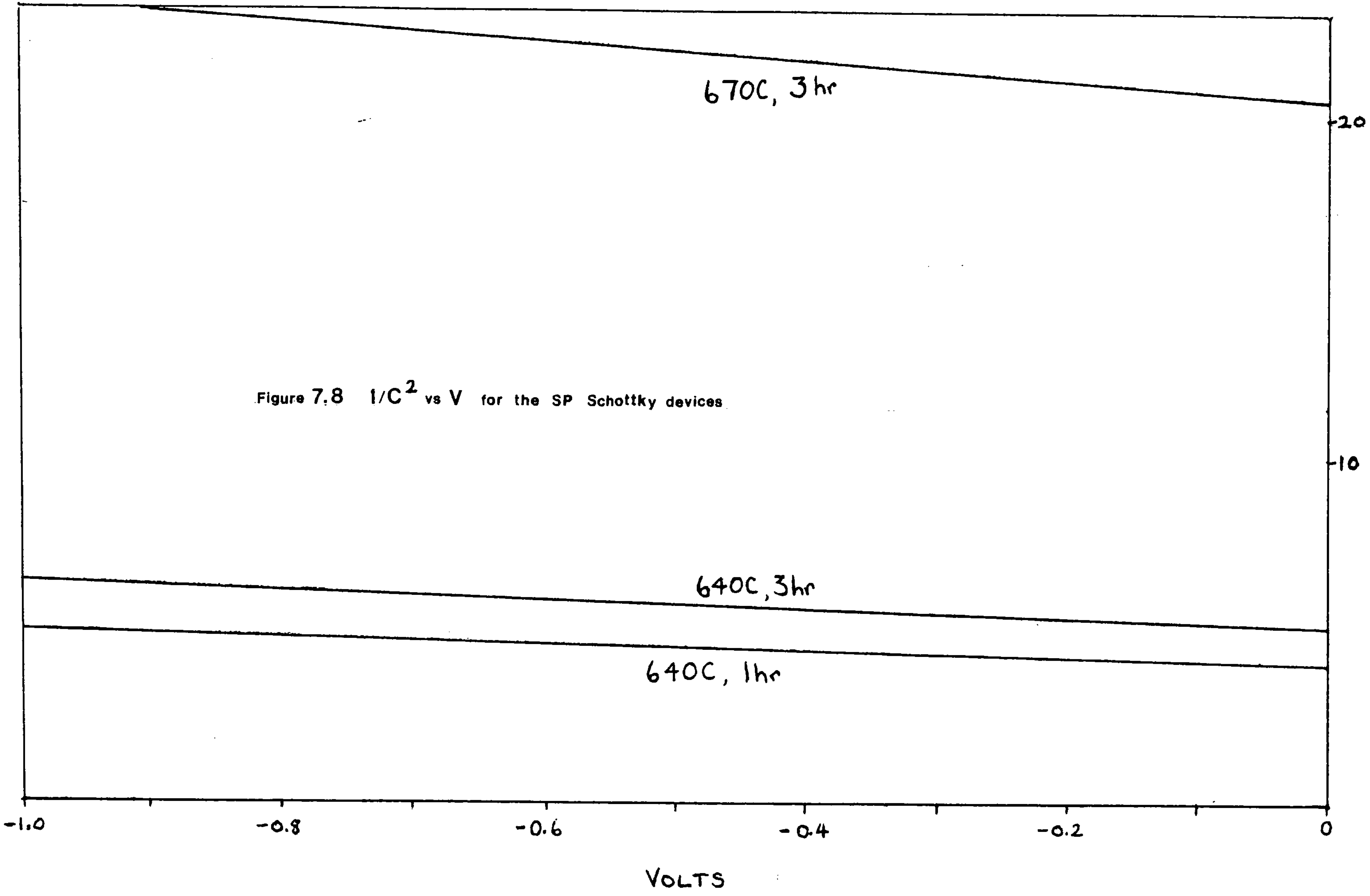


Figure 7.8 $1/C^2$ vs V for the SP Schottky devices

SAMPLE	Nd/cm^{-3}	ANNEALING CONDITIONS
SP1	$2{\cdot}3 \times 10^{15}$	640°C - 40mins
SP2	$2{\cdot}9 \times 10^{15}$	640°C - 1 hr.
SP3	$1{\cdot}5 \times 10^{16}$	640°C - 3 hrs.
SP4	$2{\cdot}5 \times 10^{16}$	670°C - 1 hr.
SP5	$1{\cdot}3 \times 10^{17}$	670°C - 3 hrs.
SP6	$2{\cdot}2 \times 10^{17}$	700°C - 1 hr.

Figure 7.8 Free carrier concentrations from C-V measurements for the screen printed films

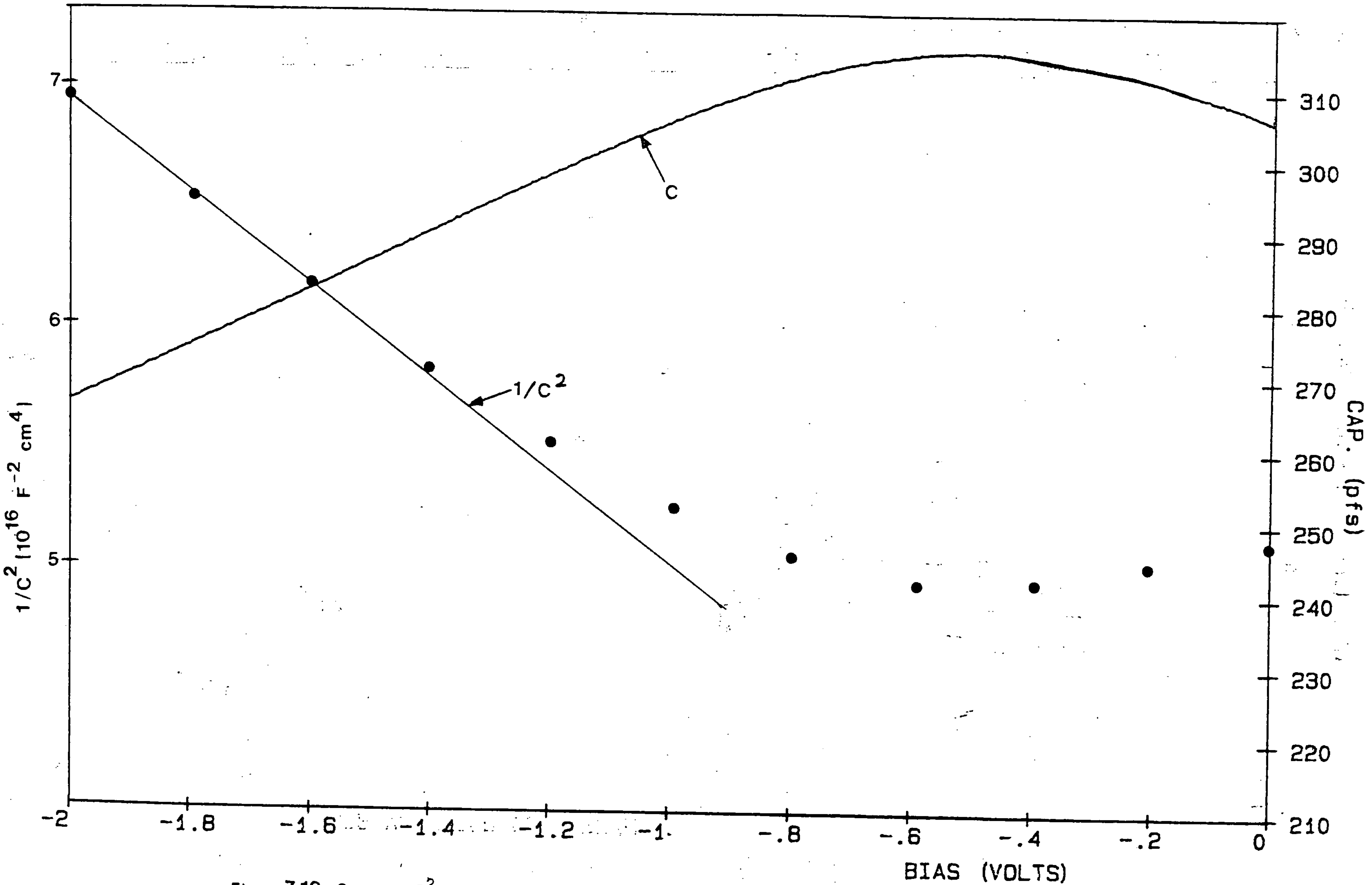


Figure 7.10 C and $1/C^2$ as a function of V for the heterojunction

7.2.6 DLTS and ODLTS Results for Screen Printed CdS

DLTS measurements were made on the Schottky devices over the temperature range 80-380K. SP1 (annealed at 640C for 40min) gave no indication of the presence of any electron trapping centres. For the sample SP2 (annealed at 640C for 1hr), the DLTS spectrum showed two peaks clearly (see fig. 7.11) corresponding to electron traps ES2 and ES3. From the Arrhenius plots (see fig. 7.12) the activation energies and capture cross-sections were calculated to be 0.16eV, 10^{-19} cm^2 , and 0.48, 10^{-19} cm^2 respectively. SP3 and SP4 showed no evidence of the presence of deep electron traps. However, SP5 and SP6, gave a DLTS response at 100K corresponding to the level denoted ES1 (see fig. 7.11). The Arrhenius plot indicated an activation energy of 0.13eV and capture cross-section of 10^{-19} cm^2 . No other traps were detected in the Schottky devices.

The heterojunctions generally gave a poor DLTS response with only that for SP5 giving clear a indication of peaks (see fig. 7.11). In fact this sample showed 3 peaks corresponding to electron traps denoted ES1, ES4 and ES5. ES1 was observed in the Schottky device on the same material SP5 - 0.13eV, 10^{-19} cm^2 . ES4 occurred on the shoulder of ES5 and was difficult to resolve and so its deep level parameters were not determined. The remaining level had an activation energy and cross-section of 1.1eV and 10^{-12} cm^2 respectively. These were the only electron traps observed by DLTS in the heterojunctions. The capacitance transients due to ES1, ES2, ES3 and ES5 are shown in figs 7.13-7.16 respectively; the

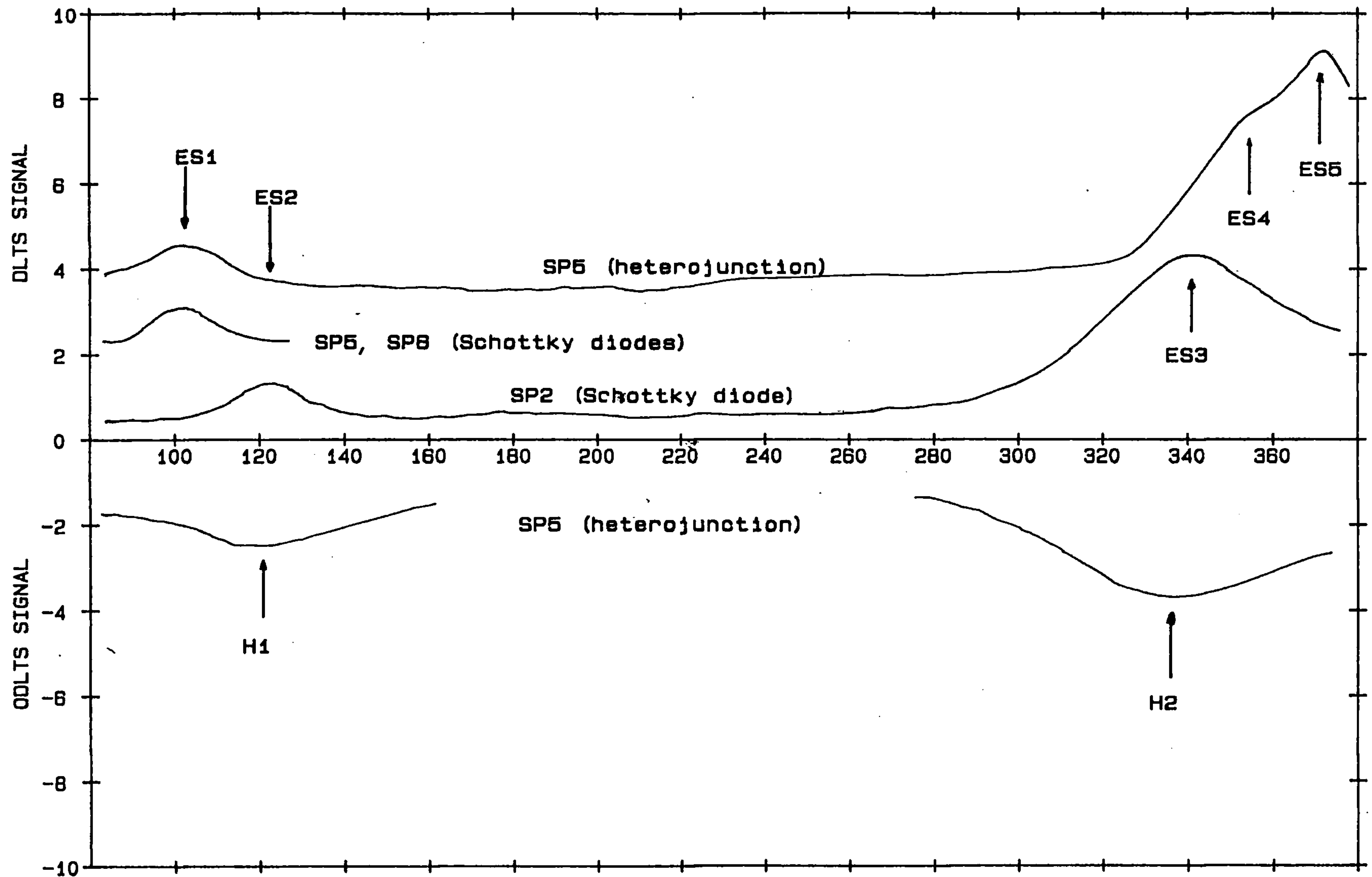


Figure 7.11 DLTS and ODLTS spectra for the screen printed films

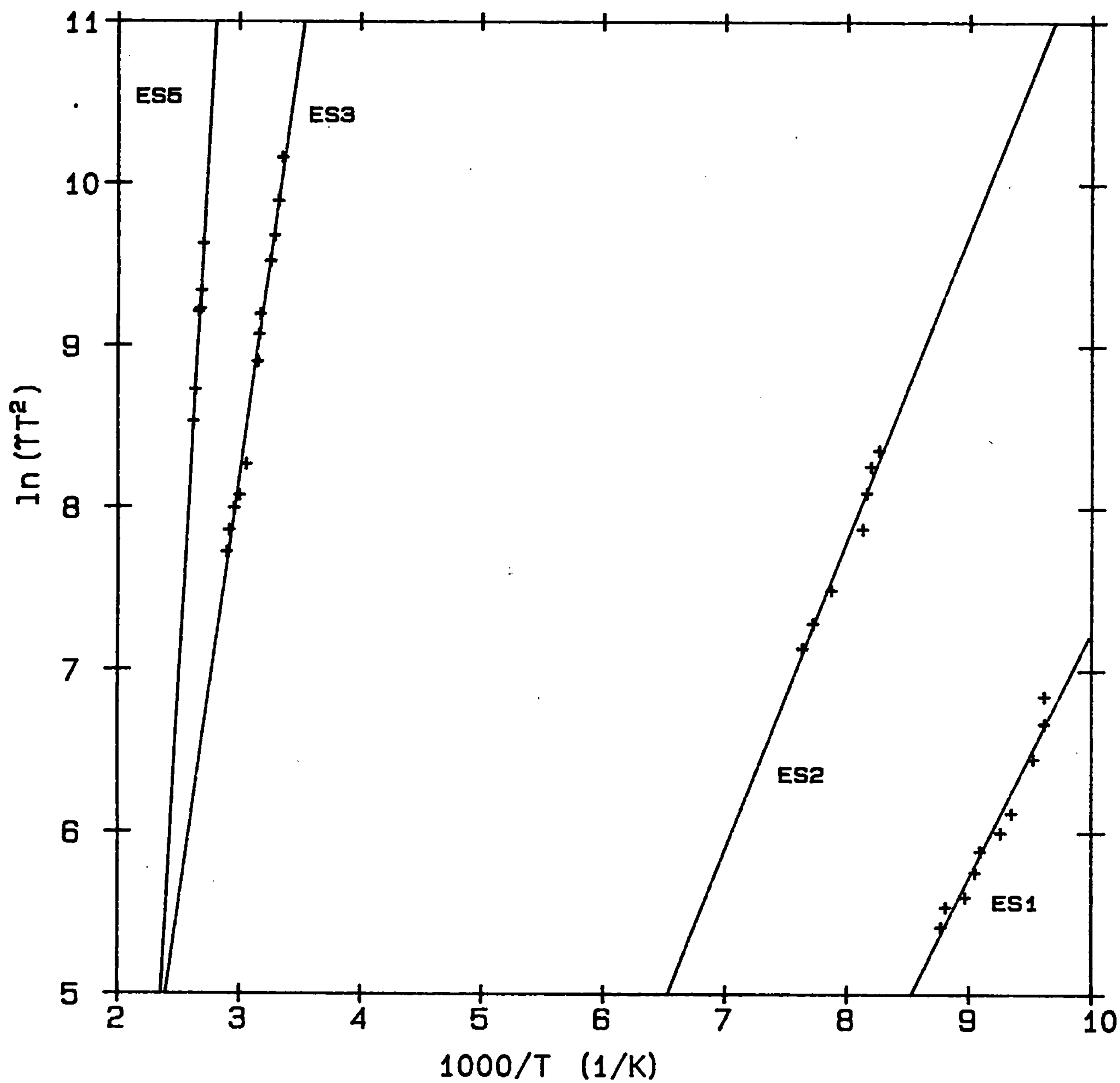


Figure 7.12 Arrhenius plots for the electron traps ES1, ES2, ES3 and ES5

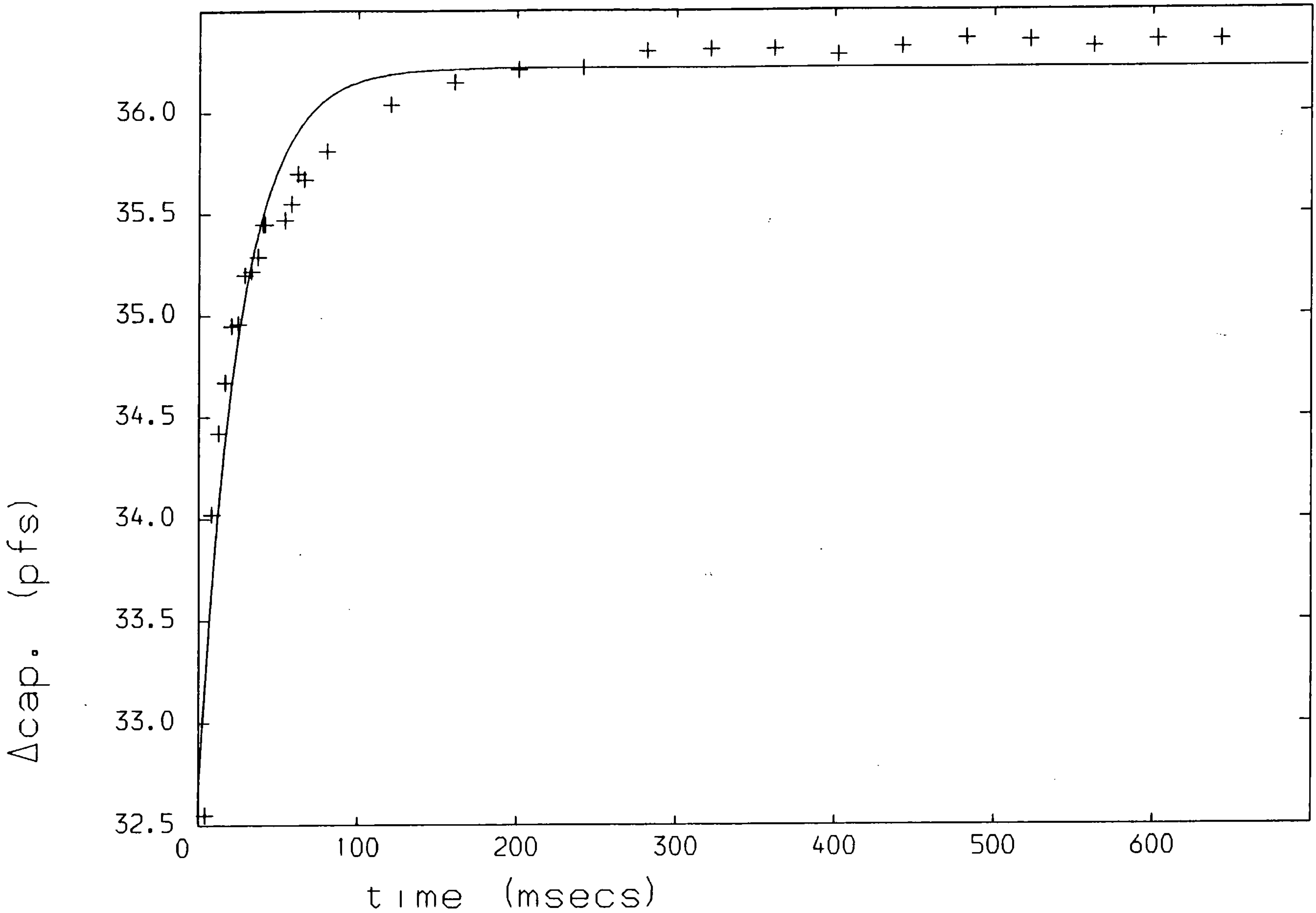


Figure 7.13 Capacitance transient due to electron emission from ES1 at 100K

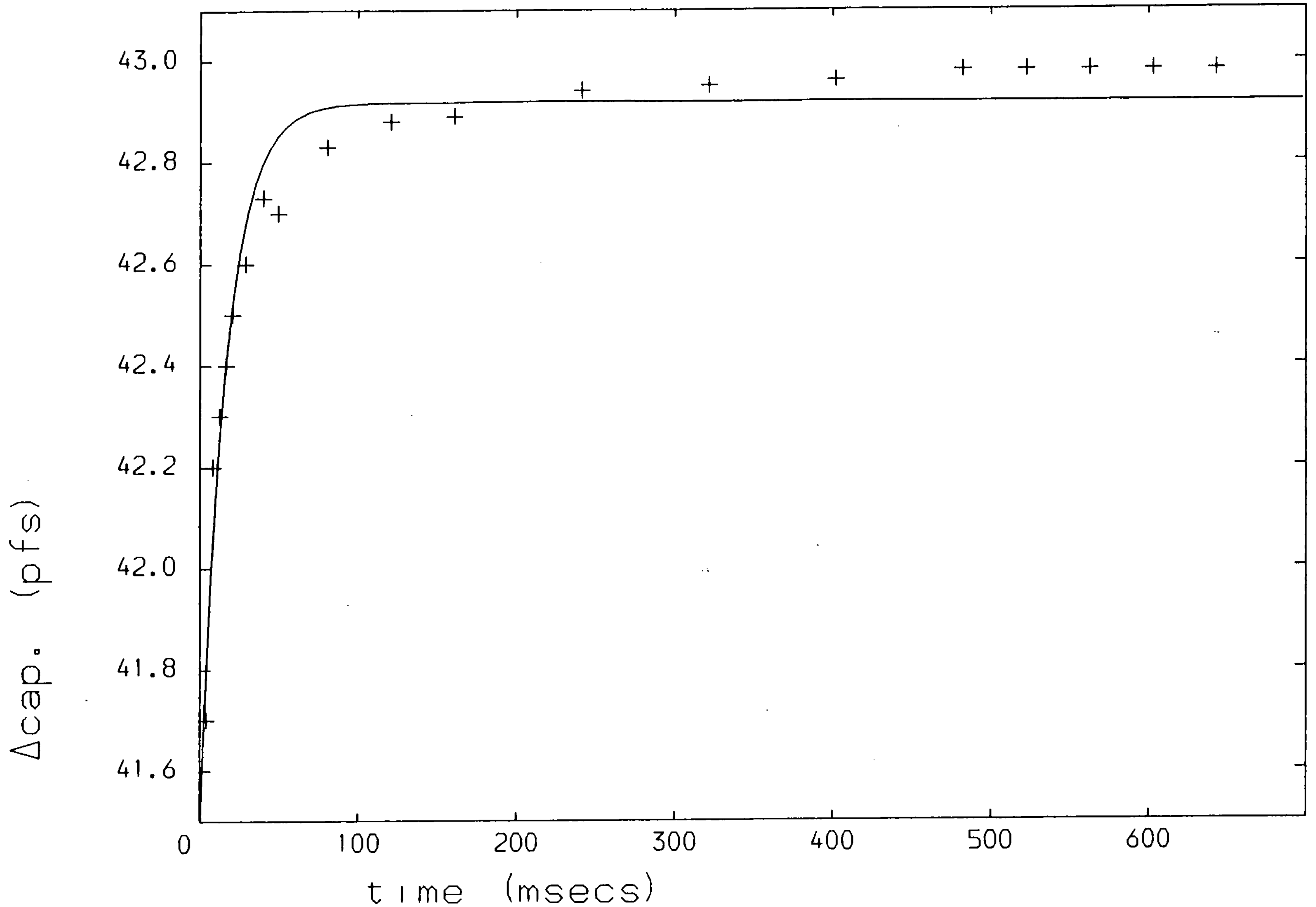


Figure 7.14 Capacitance transient due to electron emission from ES2 at 120K

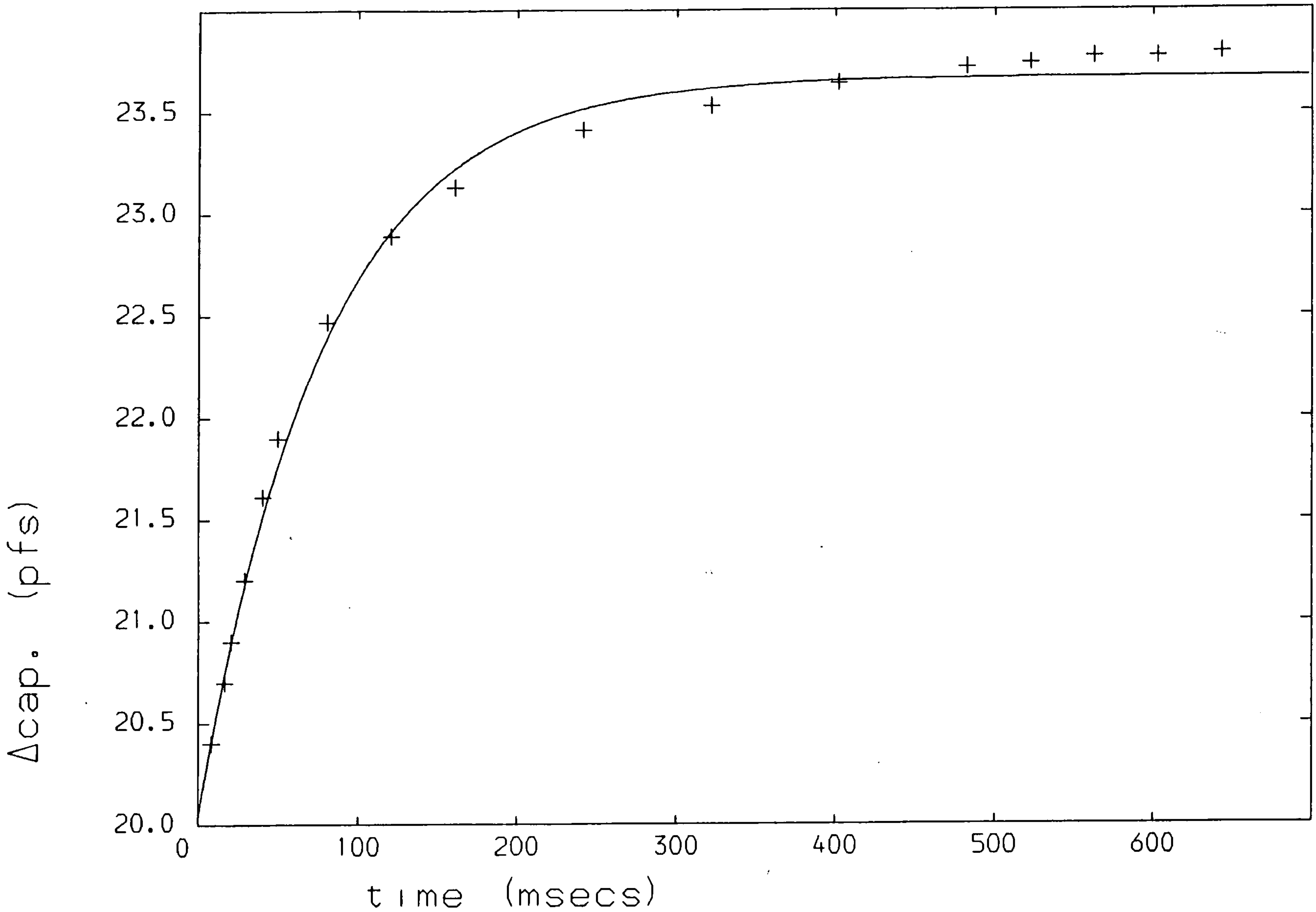
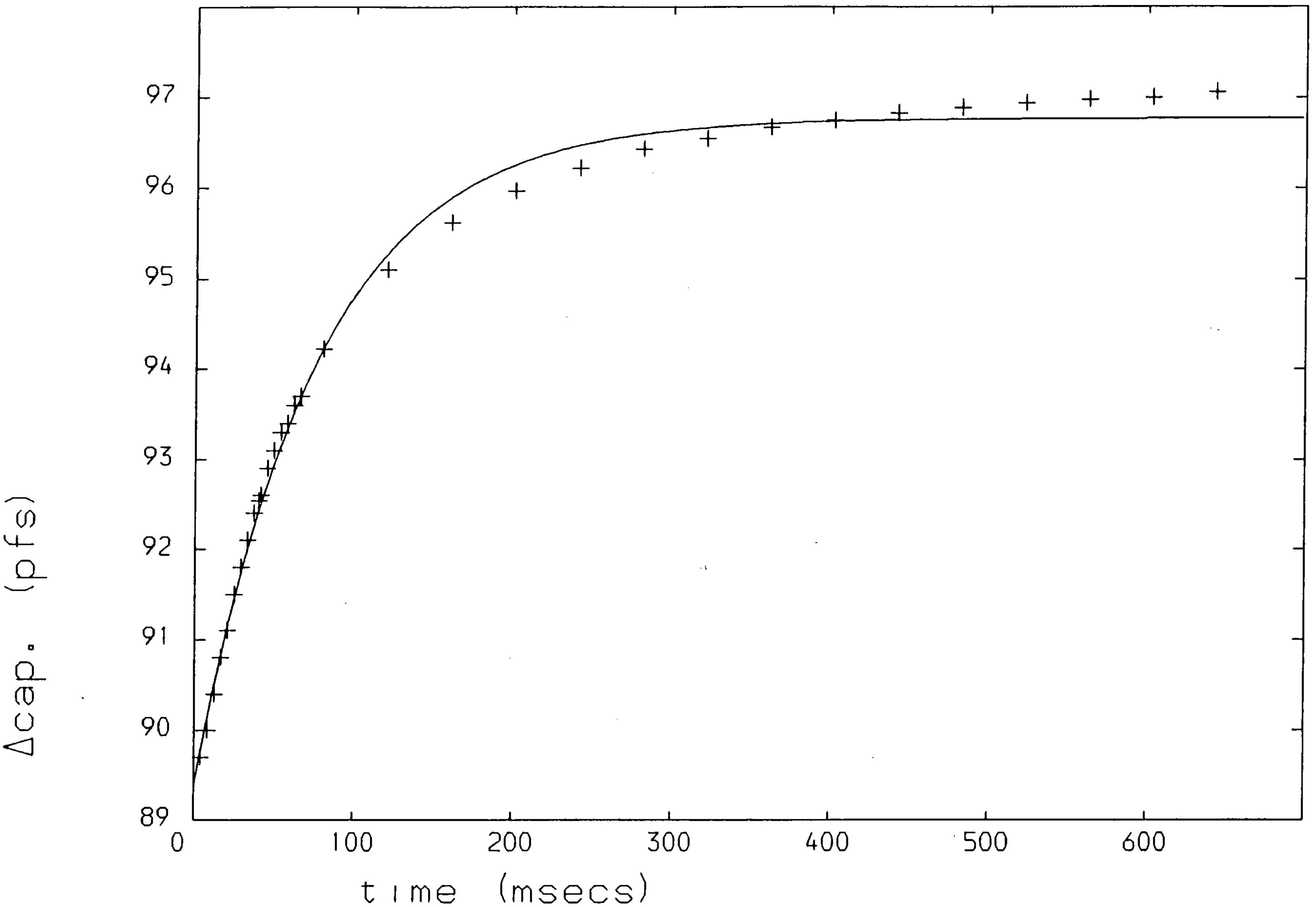


Figure 7.15 Capacitance transient due to electron emission from ES3 at 330K



FITTED PARAMETERS

P 1 = 0.968E02 P 2 = -0.740E01 P 3 = 0.754E02

Figure 7.18 Capacitance transient due to electron emission from ES5 at 370K

solid lines are the theoretical exponential fits to the data. They all follow an exponential decay as predicted by DLTS theory [17] for the rapidly decaying part of the transient. However, for longer times, there is gradual decay giving a deviation from the theoretical dependence.

ODLTS was carried out using either a chopped Ar or He/Ne laser as descibed in chapter 4. There was no evidence of hole trapping centres in the Schottky devices. The heterojunctions on SP5 and SP6 gave a small ODLTS response to the copper levels H1 and H2, see fig. 7.11, at 0.35eV and 1.1eV (cf copper levels in single crystal CdS discussed in chapter 5) above the valence band as determined from the Arrhenius plots in fig. 7.17. The DLTS and ODLTS results are summarised in fig. 7.18.

7.2.7 Discussion

Thick film CdS has been prepared by the screen printing process on SnO_x coated glass substrates. The powdered films were annealed under various conditions using SEM for film assessment. Fusion of the CdS particles seemed almost to be complete after 1hr at 700C. RHEED has shown that these films were hexagonal with some large, oriented grains randomly distributed. The annealing process required a flux in order to promote grain growth. The melting point of CdS is 1750C [18] which is far in excess of the melting point of the glass substrates. To induce the CdS to flow $CdCl_2$, flux was incorporated in the slurry prior to screen printing. The behaviour of $CdCl_2$ as a flux for the sintering of CdS is well

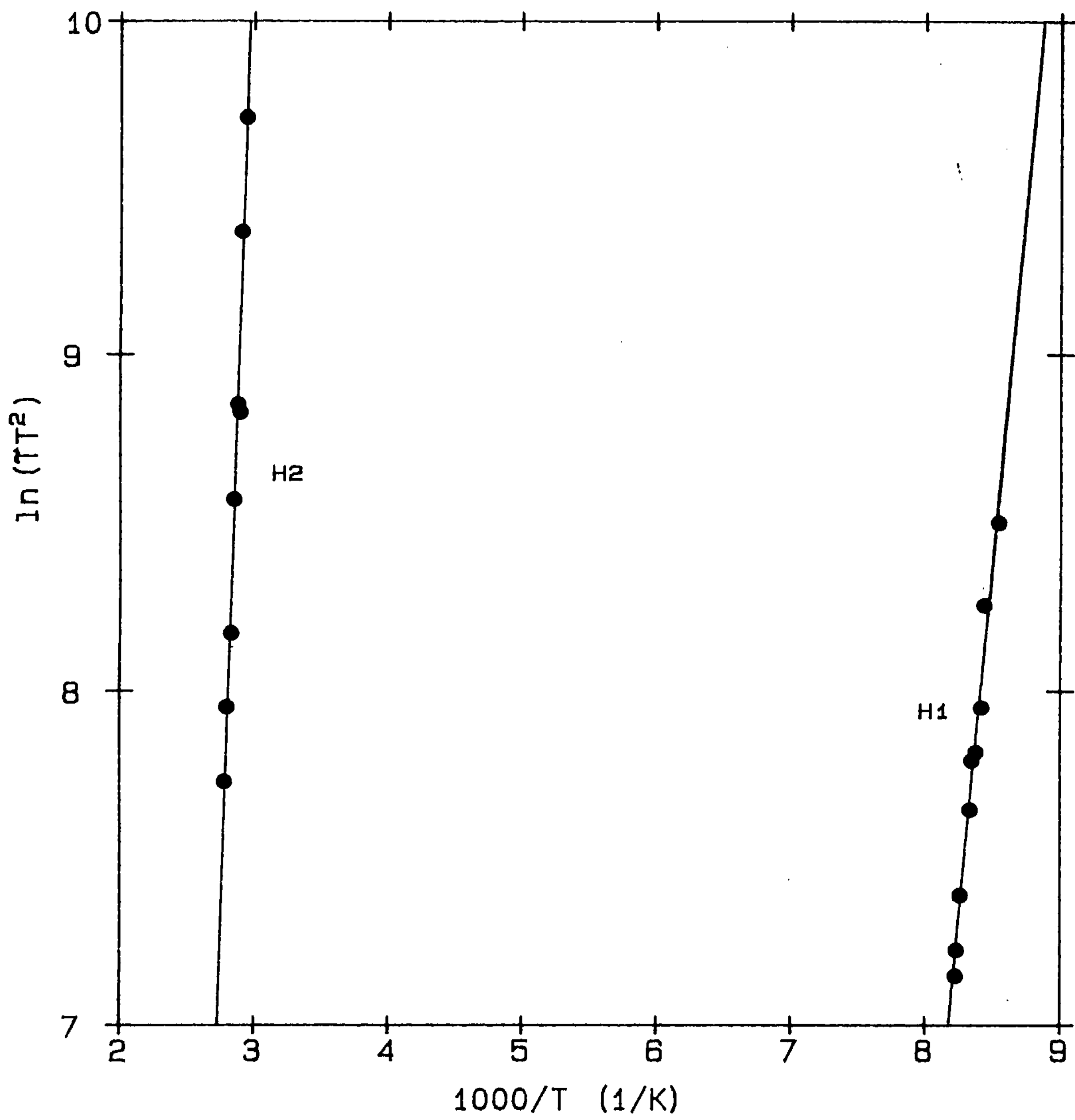


Figure 7.17 Arrhenius plots for the hole traps H1 and H2

SAMPLE	ΔE /eV	σ /cm^2
ELECTRON TRAPS		
SP2 (Schottky)	ES2 $0{\cdot}16 \pm 0{\cdot}02$eV ES3 $0{\cdot}45 \pm 0{\cdot}02$eV	$2 \stackrel{\times}{\div} 6 \times 10^{-19}$ $3 \stackrel{\times}{\div} 3 \times 10^{-19}$
SP5 (Schottky)	ES1 $0{\cdot}13 \pm 0{\cdot}01$eV	$4 \stackrel{\times}{\div} 7 \times 10^{-19}$
SP5 (Heterojunction)	ES5 $1{\cdot}10 \pm 0{\cdot}10$eV	$10^{-12\pm1}$
SP6	ES1 $0{\cdot}13 \pm 0{\cdot}02$eV	$10^{-19\pm1}$
HOLE TRAPS		
SP5 (Heterojunction)	H1 $0{\cdot}35 \pm 0{\cdot}05$eV H2 $1{\cdot}10 \pm 0{\cdot}10$eV	$10^{-12\pm1}$ $10^{-12\pm1}$

Figure 7.18 Summary of defect states in screen printed films

known [12]. The results shown here indicate the CdS particles beginning to fuse at about 670C.

The current-voltage curves of the Schottky devices showed a better reverse bias characteristic with an increase in duration and temperature of anneal. This was consistent with the SEM observations in that the powdery films gave poorer characteristics whereas those that were annealed for longer showed a greater degree of crystallinity and improved performance. The powdery films have a larger number of grain boundaries which could act as current leakage channels leading to poor current-voltage characteristics. The heterojunctions on SP5 and SP6 showed a photovoltaic response although the conversion efficiency was poor (~0.1%). Those that had been annealed for shorter periods or at lower temperatures did not give a photovoltaic effect.

In the Schottky devices DLTS showed the presence of three electron traps ES1-3. ES2 and ES3 were present in samples that had undergone an anneal at 640C for 1hr and had activation energies and cross-sections of 0.16ev, $10^{-19}cm^2$ and 0.48eV, $10^{-19}cm^2$ respectively. ES3 was by far the strongest DLTS peak observed in the Schottky devices; it was much broader than that predicted in theory suggesting it may be related in some way to extended defects such as grain boundaries; and had a small cross-section suggesting it might have been an electron repulsive centre [19]. Only the SP5 and SP6 Schottky devices gave further evidence of an electron trapping centre. This was found at 0.13eV below the conduction band (ES1). The capture cross-sections for ES1

and ES2 were similar to that for ES3 indicating that they possibly behaved as electron repulsive centres [19].

Only the heterojunction on SP5 indicated the presence of electron traps - ES1, ES4 and ES5. The presence of ES1 was consistent with the result for the Schottky device on the same material which also gave a DLTS reponse for this trap. ES4 could not be resolved since it was obscured by the presence of ES5 in the DLTS scan. ES5 at 1.1eV below the conduction band had a large cross-section of 10^{-12} cm^2 indicating the probability it had a double positive charge, thus behaving as an electron attractive centre [19].

The origin of these electron trapping centres is not clear. However, the presence of chlorine from the flux indicates an obvious source of impurity. In fact this element is known to create both shallow donors which increase the free carrier concentration and reduce the resistivity of CdS, and deep donor levels which can behave as trapping centres [20]. Chlorine is thought to be a substitutional impurity in CdS [21]. Pande [20] has observed a level at 0.2eV below the conduction band and suggested that it was associated with chlorine. The reason for his suggestion was that $CdCl_2$ was used as a flux for sintering powdered CdS and such material was compared with similarly sintered CdS but without the flux. Photocapacitance showed that the 0.2eV level was only present in material that had been annealed using the flux. The energy for this trap is similar to that observed for ES1 and ES2, the difference being accounted for by a Frank-Condon shift. However, both ES1 and ES2 cannot be

the same as the trap observed by Pande but which of these it may be, is not clear.

ES4 and ES5 were observed in the heterojunction only and they may be artefacts from the processing of the device which involved a thermal treatment at 200C and hence copper diffusion into the CdS. However, copper may not be implicated since it was not observed in single crystal CdS (see chapter 5).

ODLTS gave no response for the Schottky devices, indeed only the SP5 and SP6 heterojunction showed the presence of two levels at 0.35eV and 1.1eV above the valence band. Copper is known to diffuse across the junction from the Cu_2S into the CdS during the optimising process for the solar cell [1]. Consequently, it forms deep acceptor states [22,23] as discussed in chapter 5. The hole trapping centres observed by ODLTS were the excited (0.35eV) and ground (1.1eV) copper states resulting from the crystal field splitting of the copper d^9 level (see chapter 5).

It is difficult to compare these results with those reported for CdS films since there are many techniques available and very few deal with screen printed material. DLTS has been used to investigate the electron traps in electron beam evaporated CdS [24] and CVT CdS [25]. Only in the CVT material was a trap observed with similar characteristics to ES2 at 0.16eV. This also had a small cross-section and occurred over a similar temperature range. None of the traps observed correlated with those in single

crystal CdS - see chapter 5, except for the copper states.

These DLTS results have shown that the defects induced in screen printed CdS are sensitive to the processing of the the film. By changing the annealing process one trap disappeared and one appeared. During the processing of the heterojunction two new electron traps were observed that were not detected in the Schottky device. Such results indicate the care required for the optimisation of each processing step since these deep levels may in some way effect the device operation.

7.3 Evaporated CdS Films

7.3.1 Introduction

Evaporation has proved a convenient method for the deposition of CdS films on a variety of substrates for the preparation of the CdS/Cu_2S solar cell. However, one of the main problems has been that of reproducibility and degradation of the heterojunction [1]. Bloss and Pfisterer [26] have developed a technology for preparing CdS/Cu_2S films that has minimised these problems. One feature of their process involves the evaporation of CdS onto silver substrates rather than those often used, namely, SnO_x coated glass and Zn coated kapton. In a subsequent investigation Pande et al [20,27] suggested that the silver plays an important role in the improved properties the solar cell. A deep Ag-associated level was observed by photocapacitance in the CdS and Pande subsequently suggested that its presence prevented the in-diffusion of copper which is involved in the

degradation process.

This study was concerned with the investigation of deep levels induced by Ag. CdS was evaporated onto Ag coated glass and for comparison SnO_x coated glass. DLTS and ODLTS were used to characterise the deep level defect signatures of the material deposited on these different substrates.

7.3.2 Preparation of Evaporated Films

The material used in this study was commercial BDH Optran grade CdS. It was purified by the flow run process which involved heating the CdS to 1150C in a silica tube with an argon flow of 0.2mls/min. CdS platelets were deposited in a cooler part of the tube. This process effectively removed volatile impurities. Subseqently, the CdS was slightly crushed and this provided the source material for the evaporation.

Two types of substrates were used. The first of these was commercially available SnO_x coated glass slides (Photon Power) with dimensions of the coating surface approximately 1in x 3in. The second type of substrate was a glass slide coated with Cr and Ag. Initially, the slides were thoroughly cleaned by degreasing in trichloroethylene vapour for 1hr and then washed in methanol. The coating procedure was by electron beam evaporation. First of all Cr was deposited onto the heated glass slide (300C) giving a film thickness of about 1000Å. This provided a base layer for the Ag which does not adhere well to glass. The Ag was deposited in a

similar manner with a thickness of about 1μ. Using the conditions optimised by Pande [20], CdS was thermally evaporated in vacuum (10^{-5} torr) with a substrate temperature of 200C and source temperature of 1000C for 25-30mins. This gave films 20μ thick.

Schottky barrier devices were obtained by evaporation of Au onto the CdS. Indium provided the ohmic contact.

7.3.3 Properties of the Films

The deposited material was hexagonal as shown by RHEED (see fig. 7.19) and from SEM observations the layer consisted of columnar CdS crystallites (see fig. 7.20). Pande showed that the main controlling factor in the growth was the substrate temperature since there was a lower degree of orientation and crystallinity for temperatures higher or lower than 200C.

Resistivities of these films were found to be 600Ω cm with a capacitance of 600pf for a geometrical contact area of 1mm. Capacitance-voltage measurements gave a free carrier concentration of 10^{15} cm^{-3}.

7.3.4 DLTS Results for Evaporated CdS

DLTS was used to characterise deep levels in the thin films evaporated on to Ag/Cr and SnO_x coated glass substrates. Measurements were made over the temperature range 80-400K. This was in order to investigate the

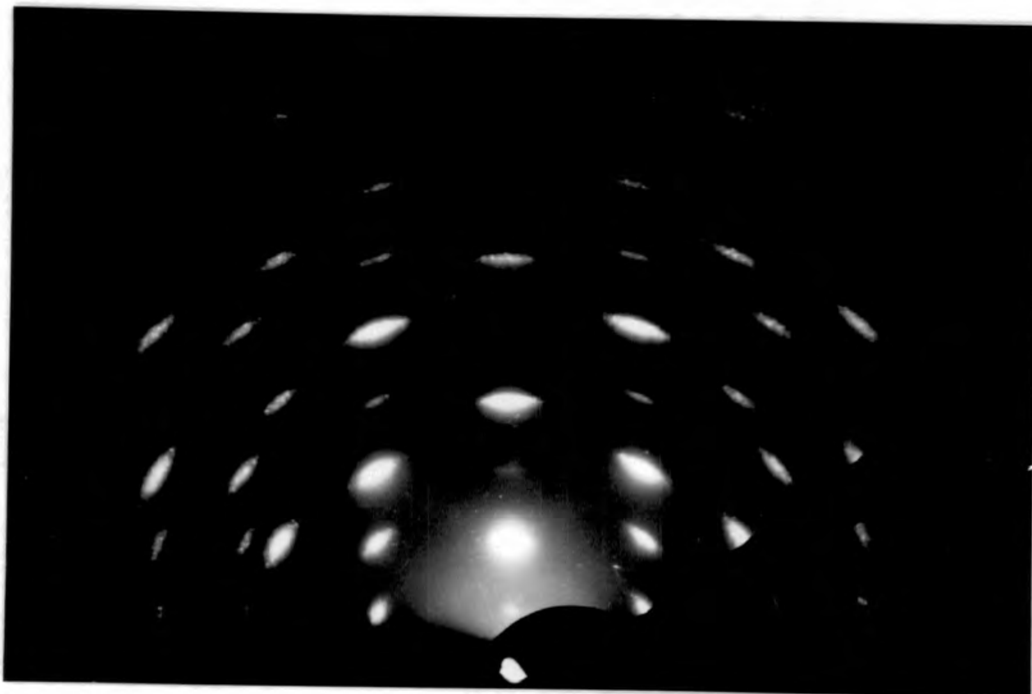


Figure 7.19 RHEED pattern of the evaporated film

Figure 7.20 X-section through the evaporated film

difference in DLTS signatures from the different substrates.

CdS on Ag typically gave a DLTS spectrum as shown in fig. 7.21. Three peaks were observed at about 250K, 300K and 370K and these were denoted EL1-3. The Arrhenius plots for EL1 and EL2 are shown in fig. 7.22. EL3 was poorly resolved and therefore, its deep level parameters not determined. EL1 and EL2 had activation energies and capture cross-sections of 0.48eV, 1.2×10^{-16} cm^2 and 0.98eV, 10^{-12} cm^2 respectively. The material deposited onto SnO_x did not give a DLTS response for EL1 and EL2 although a poorly resolved peak occurred at 370K and was likely to be the same as EL3. The capacitance transient due to EL1 is shown in fig. 7.23 and clearly indicates a nonexponential behaviour as shown by the exponential fit to the data (solid line). This may be due to the overlap of the DLTS responses from EL1 and EL2.

None of the samples studied gave a DLTS response corresponding to those traps observed in single crystal CdS and none showed the 'light'/'dark' effect. In addition, none of the samples gave an ODLTS response and so no hole traps were characterised.

7.3.5 Discussion

Polycrystalline CdS films of 20μ thickness were deposited onto Ag/Cr and SnO_x coated glass substrates by vacuum evaporation. These had good crystallinity and crystallite orientation (columnar with the c-axis perpendicular to the substrate surface). DLTS was used to

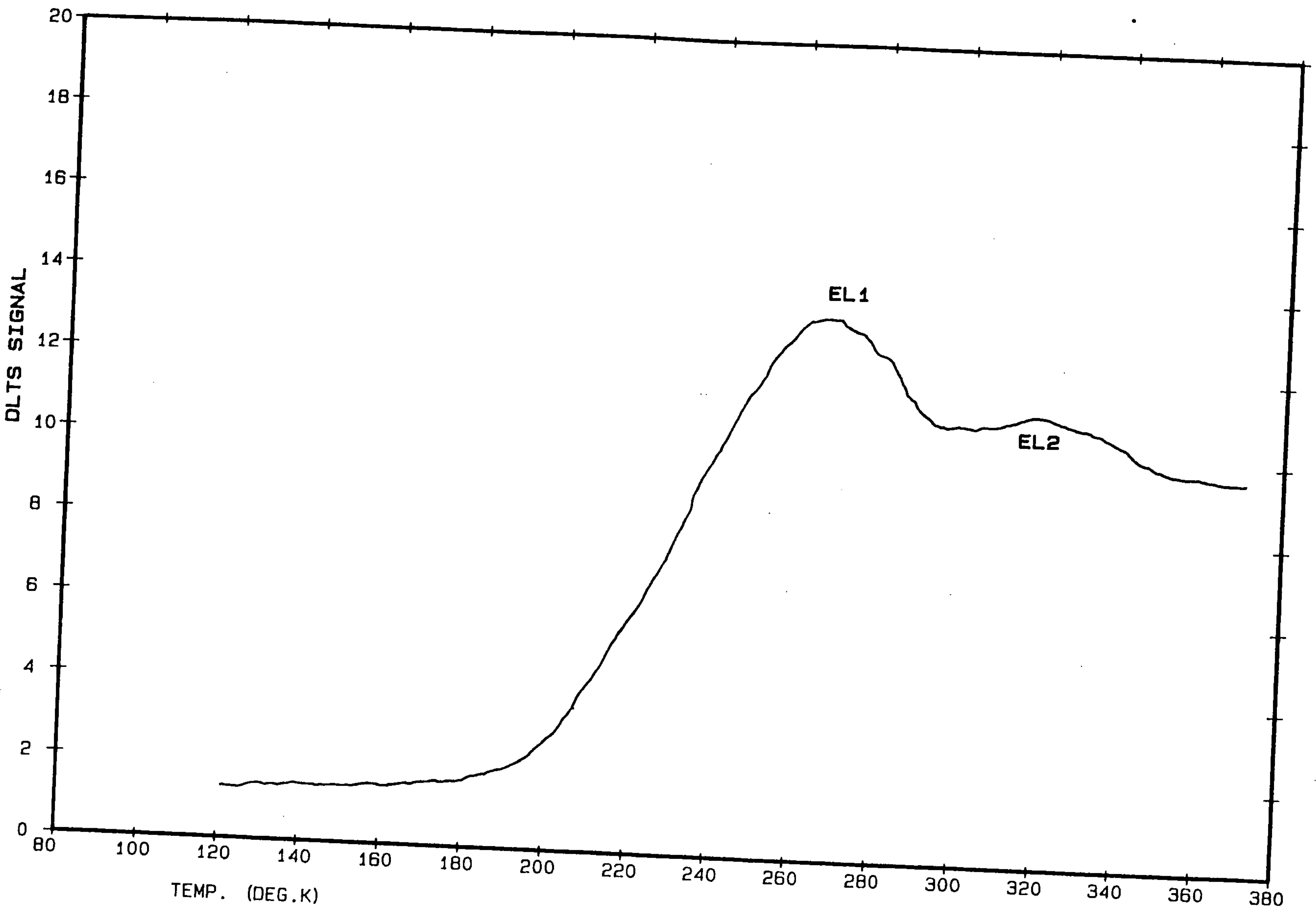


Figure 7.21 DLTS scan for evaporated CdS

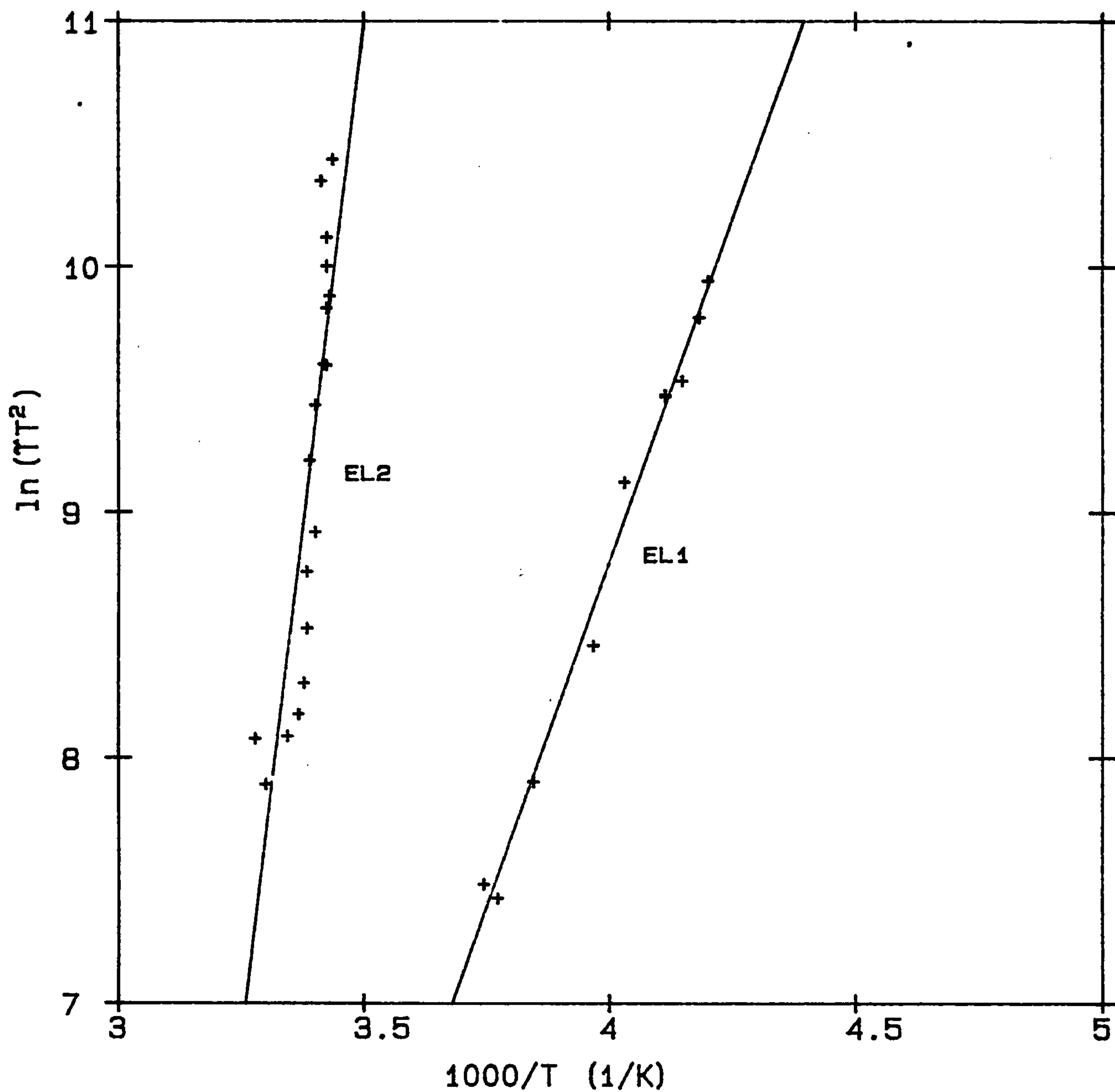
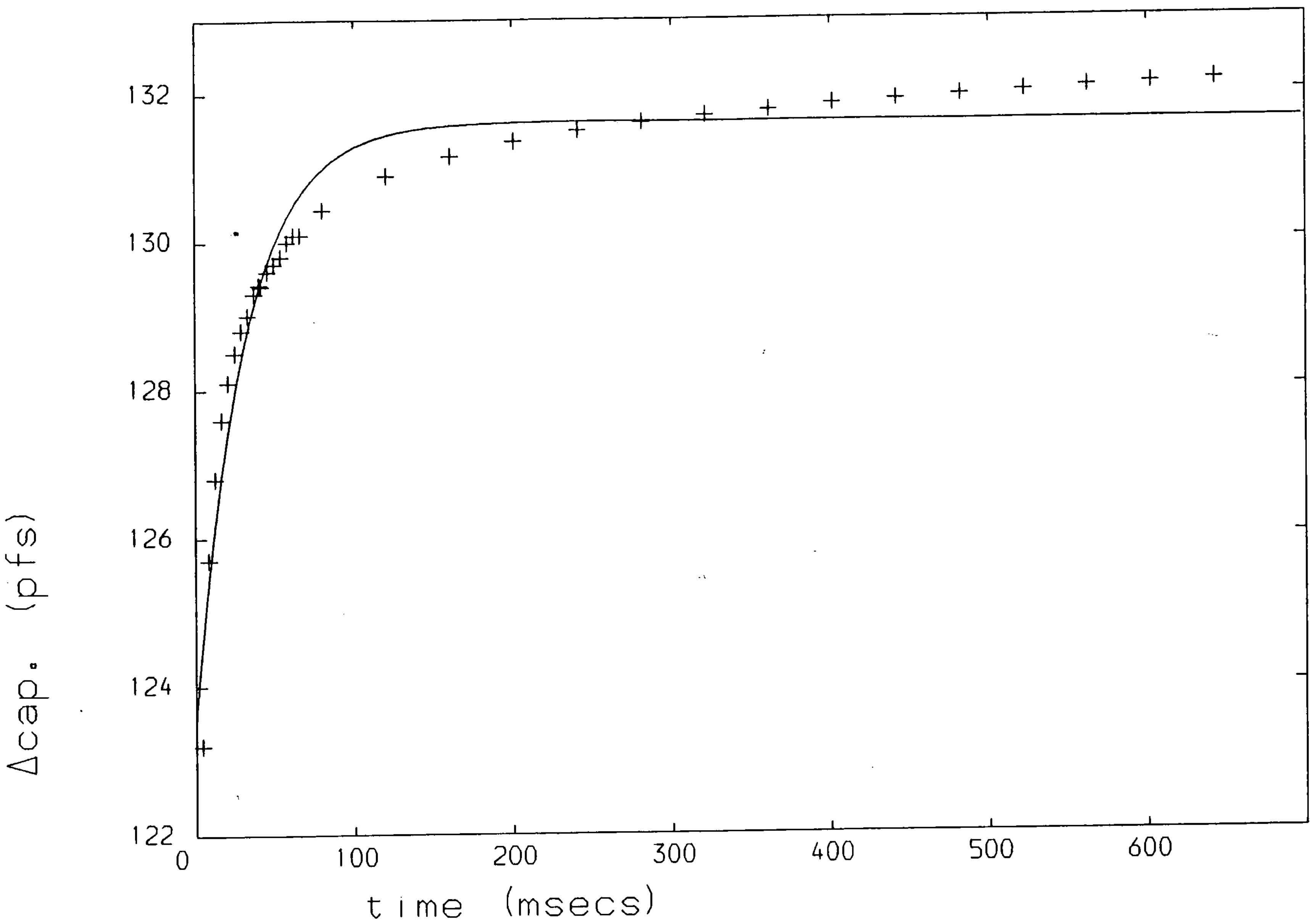


Figure 7.22 Arrhenius plots for the electron traps EL1 and EL2



FITTED PARAMETERS

P 1 = 0.132E03

P 2 = -0.811E01

P 3 = 0.313E02

Figure 7.23 Capacitance transient due to electron emission from EL1 at 270K

investigate the CdS films grown on these two substrates so the effect of Ag could be examined.

DLTS from CdS on Ag/Cr coated glass gave three peaks corresponding to three electron traps, EL1-3, EL1 and EL2 had activation energies of 0.48eV and 0.98eV respectively. EL3 could not be resolved. Only EL3 was present with the material on SnO_x coated glass deposited under identical conditions and this was poorly resolved. Therefore, the use of Ag substrates appears to induce two deep defect states into the CdS evaporated films.

Ag has a diffusion coefficient similar to that of Cu [28]. The films were polycrystalline and so this suggests that there would be a high density of Ag in the CdS resulting from diffusion through the CdS crystallites and along the grain boundaries during the evaporation process which involved heating the substrate to 200C. Ag impurity centres have been studied in CdS [28] and it has been shown that they produce two defect states at 1eV and 0.5eV below the conduction band. It seems from these values that they could be the same as those observed in the present work. EL1 and EL2 may be considered as deep defect states associated with Ag.

Bloss and Pfisterer [26] have overcome the problems of reproducibility and degradation of the CdS/Cu_2S solar cell by using Ag substrates and Pande et al [27] suggested that Ag in CdS improves the properties of the heterojunction solar cell. Over a long period the solar cell maintained its initial

properties compared to severe degredation for cells prepared on other substrates.

Pande et al [27] reported photocapacitance (PHCAP) study on evaporated CdS/Au Schottky diodes and CdS/Cu_2S heterojunctions deposited on Ag/Cr and SnO_x coated glass. This was to investigate the improved properties of heterojunctions prepared in the manner described by Bloss and Pfisterer. The PHCAP results showed a deep electron trap sited 0.95eV below the conduction band edge which was only observed in material deposited on Ag substrates. The DLTS results presented here also show a trap with a similar thermal activation energy and in addition another electron trap at 0.48eV not observed in the PHCAP work of Pande.

One important result reported by Pande was that after the sensitising bake at 200C for optimising the solar cell efficiency, the PHCAP response for the devices on Ag gave no infrared quenching. This was unusual in that the copper levels introduced during the heating gave a strong quenching at 0.75eV at room temperature [20,27] as was observed in film prepared on SnO_x.

It seems that the Ag inhibits the formation of the copper states. The mechanism is not clear but the presence of the Ag plays some part in the process. One possibility may be that the Ag and Cu compete for identical sites in the CdS lattice and so if these are already occupied by Ag, then the migration of Cu into the CdS will be reduced. The inhibition of the in-diffusion of Cu would maintain the

stoichiometry of the Cu_2S and it is this that Pande suggests gives the improved stability of the solar cell on Ag substrates.

7.4 Conclusion

Silk screen printing and evaporation of CdS provide convenient methods for fabricating large area, low cost films. DLTS and ODLTS have been used to study deep electron and hole trapping centres in these CdS films.

The work on the silk screen printed films was initially concerned with the optimisation of the annealing process so that the powdered films could be converted to those with an increased degree of crystallinity, grain growth and crystallite orientation. Schottky devices (CdS/Au) and heterojunctions (CdS/Cu_2S) were then fabricated on these films. The heterojunctions have shown a photovoltaic response with an efficiency of 0.1%. DLTS and ODLTS were used to characterise the main electron and hole trapping centres. In all, five electron traps were observed; there was no apparent correlation with those observed in CdS prepared by other techniques including single crystal CdS. Hole traps were only observed for the heterojunctions, displaying the usual peaks due to the copper states H1 and H2. The best films prepared still had voids and a large number of grain boundaries as shown by SEM. These would have to minimised if better solar energy conversion efficiencies were to be achieved.

Evaporated CdS films were investigated to determine the effect of substrate type on the defect signature for films prepared under identical conditions. Ag and SnO_x substrates were used for this study. DLTS showed the presence of two electron traps in CdS on Ag; neither of which were observed in CdS on SnO_x. These Ag related states were clearly seen in all such samples. PHCAP [27] has shown that the copper states induced in the processing of the CdS/Cu_2S heterojunction were not present in CdS on Ag although clearly obvious in CdS on SnO_x. It is not known how the presence of Ag prevents the formation of the states but it has been suggested that Ag prevents the indiffusion of copper [21] thereby maintaining the stoichiometry of the Cu_2S layer; it is this that gives an improved stability of the solar cell.

DLTS and ODLTS have proved useful in the investigation of electron and hole traps in polycrystalline CdS prepared by silk screen printing and evaporation. Several centres have been characterised and correlated in some way with the processing of the material.

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CHAPTER 8

SINGLE CRYSTAL CdSe, CdTe, ZnS

8.1 Introduction

The II-VI compounds have excited much interest over the past 2-3 decades because of their potential applications. Some examples of these are thin film transistors (CdSe [1]), optical detectors (nCdS/pSi [2]), photoresistors (CdS [3]), solar cells (CdS/Cu_2S [4], Zn Cd_{1-x} S/Cu_2S [5], nCdS/pCdTe [6], CdSe/Cu_2Se [7]), nuclear detectors (CdTe [8]), light emitting diodes (ZnS:Mn [9], ZnSe:Mn,Al [10]) etc. The applications and properties of these materials have been reviewed by several authors [eg 11-14].

One of the major problems of the II-VI compounds has been the control of crystalline imperfections which may produce electronic states in the semiconductor band gap. Such states can have a detrimental effect on the electrical and optical properties of the material by behaving, for example, as recombination centres, thereby, reducing the free carrier lifetimes [15,16]. There are several techniques available for the investigation of defect centres and one that is of primary importance here is DLTS [17]. Apart from CdS as discussed in chapters 5 and 7, DLTS has been used to study deep level defects in other II-VI materials: CdTe [18-25], ZnTe [26,27], ZnSe [26,28,29], and CdSe [30,31]. The present

work is concerned with deep levels in CdTe which is presently of great technological importance; low resistivity ZnS; and undoped and copper doped CdSe. A complete study of all the II-VI compounds was not possible within the limits of this work, so, this investigation was restricted to certain aspects of the deep defect levels of the materials mentioned above.

8.2 Cadmium Selenide

8.2.1 Introduction

CdSe has a room temperature band gap of 1.7eV and, consequently, it is thought to be a potential solar cell material [13]. A device based on this compound is the CdSe/Cu_2Se heterojunction [7]. However, one problem with the device is that copper diffuses readily into the CdSe from the Cu_2Se where it produces deep defect states [32]. These copper centres play an important role in controlling the electrical and optical properties of CdSe [31-35]. In an effort to gain further understanding of the defect states in CdSe, undoped and copper doped material have been investigated using the techniques of DLTS and ODLTS. These results have been correlated with those reported by others.

8.2.2 Growth, Device Preparation and Characteristics

Growth from the vapour phase was carried out using the vertical sublimation technique described in section 4.2. The oriented CdSe boule was cut into 4x4x2mm dice with the large faces parallel with the (0001) basal plane. The high

resistivity of the as-grown material was reduced by annealing in selenium vapour at 550C under reduced pressure ($6x10^{-3}$ atm) for 1 month. This gave resisivities of the order 100-1000Ωcm. Copper doping was achieved by evaporation of the metal on to one surface of the crystal followed by an annealing process at high temperature and low pressure. The dice were mechanically polished with alumina powder (1μ). Surface damage was removed by chemical etching first in 2% bromine/methanol for 3min and then in concentrated hydrochloric acid for a further 2mins. After thorough rinsing in methanol, contacts were evaporated onto opposite faces to give a Schottky barrier (gold) and an Ohmic contact (indium). The free carrier concentrations obtained from capacitance-voltage measurements were of the order of $10^{16}cm^{-3}$.

8.2.3 DLTS and ODLTS

DLTS in the temperature range 80-450K was carried out to investigate the electron traps in undoped CdSe. The resultant spectra are shown in fig. 8.1(a). There were three peaks at ~135K, ~250K and ~410K corresponding to three electron traps denoted EU1, EU2 and EU3 respectively. The Arrhenius plots (see fig. 8.2) gave activation energies and capture cross-sections - 0.16eV, $2.4x10^{-18}cm^2$; 0.46eV, $2.6x10^{-16}cm^2$; and 0.9eV, $2x10^{-13}cm^2$ for EU1-3 respectively. The copper doped material gave typical DLTS spectra as shown in fig. 8.1(b). Three peaks were observed at temperatures of about 240K, 430K, 450K corresponding to three electron traps denoted EC1-3. From the Arrhenius plots (see fig.

EU1

EU2

EU3

(a)

DLTS SIGNAL (a.u.)

100 200 300 400 500

TEMPERATURE (K)

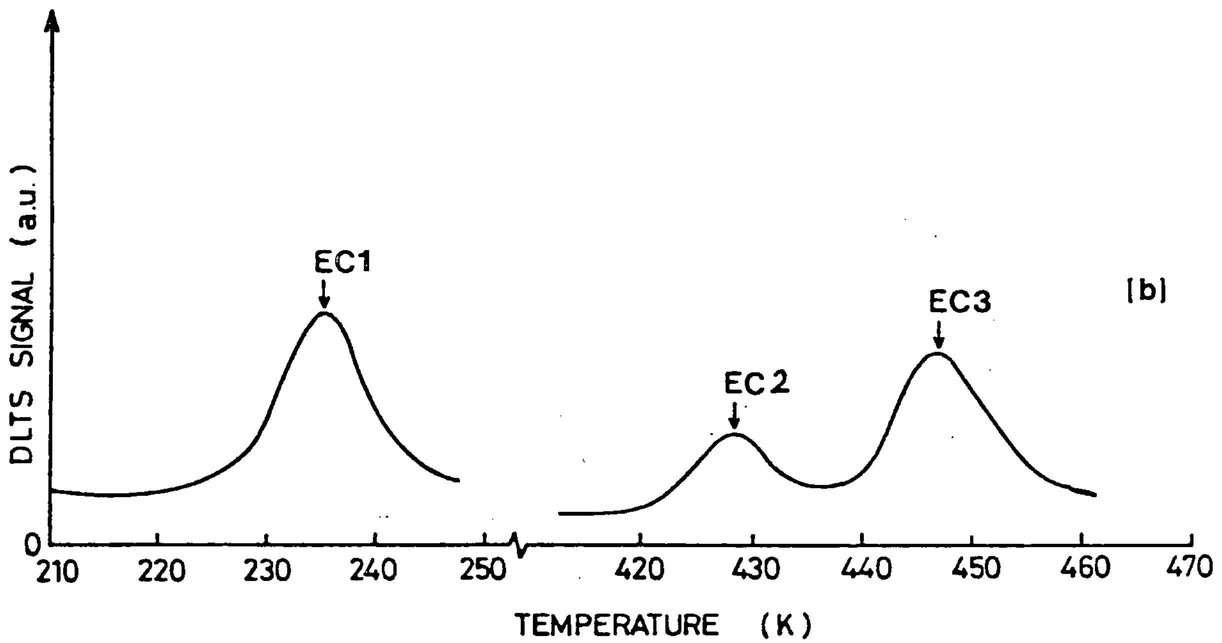


Figure 8.1 DLTS spectra for (a) undoped and (b) copper doped CdSe

8.2), these had the characteristics 0.47eV, $1.5x10^{-16}cm^2$ (EC1); 0.69eV, $8x10^{-18}cm^2$ (EC2); and 0.9eV, $2.4x10^{-15}cm^2$ (EC3).

ODLTS was carried out using a pulsed high intensity 'sweet spot' LED with peak output at 820nm in conjunction with a 799.5nm interference filter (FWHM=8nm). This corresponded to an energy just below the band gap. The ODLTS spectra are shown in fig. 8.3 and the Arrhenius plots in fig. 8.4 for undoped and copper doped CdSe. The ODLTS spectrum for the undoped material shown in fig. 8.3(a) gave only one dominant peak at 290K corresponding to a hole trap denoted HU1. This had an activation energy of 0.64eV and capture cross-section $10^{-14}cm^2$ as determined from the Arrhenius plot in fig. 8.4. In the undoped spectrum there was also a peak to the low temperature side that could not be resolved since for the shortest available time constant of ~4msec it could not be brought into the experimental temperature window.

The copper doped CdSe gave four ODLTS peaks denoted HC1-4 at temperatures of ~100K, ~315K, ~330K and ~345K. - (see fig. 8.3(b)). The Arrhenius plots in fig. 8.4 gave activation energies and capture cross-sections : HC1 - 0.22eV, $5x10^{-13}cm^2$; HC2 - 0.67eV, $10^{-14}cm^2$; HC3 - 0.78eV, $8x10^{14}cm^2$; and HC4 - 0.94eV, $4x10^{-12}cm^2$. The DLTS and ODLTS results are summarised in fig. 8.5.

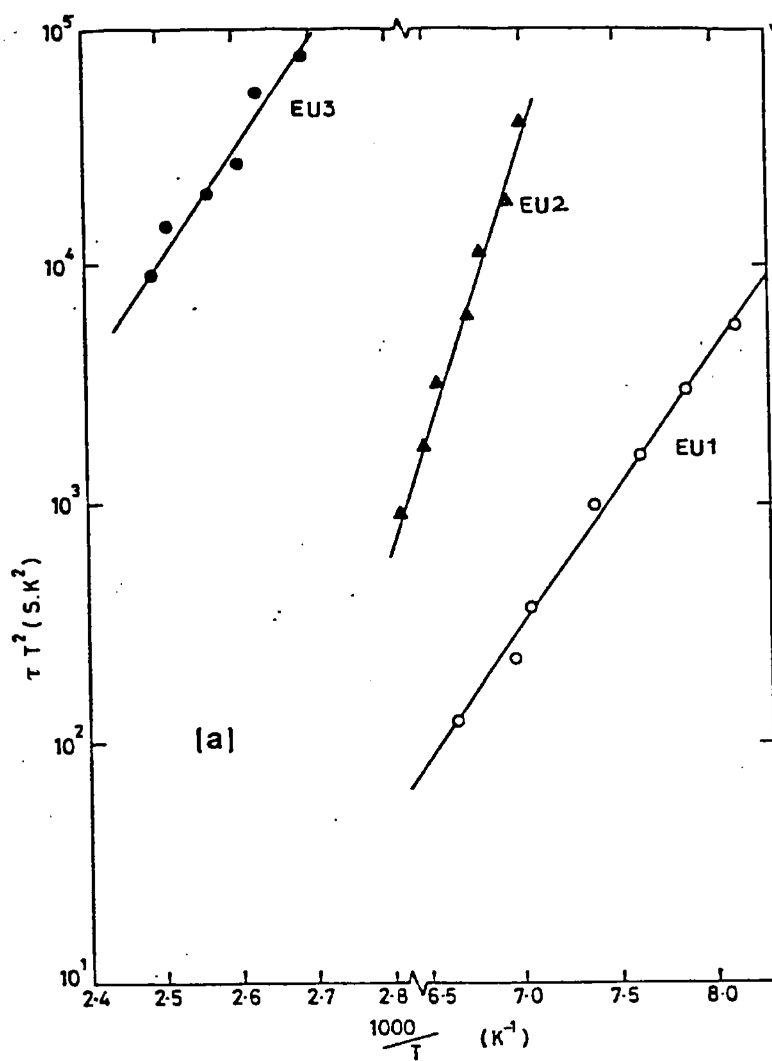
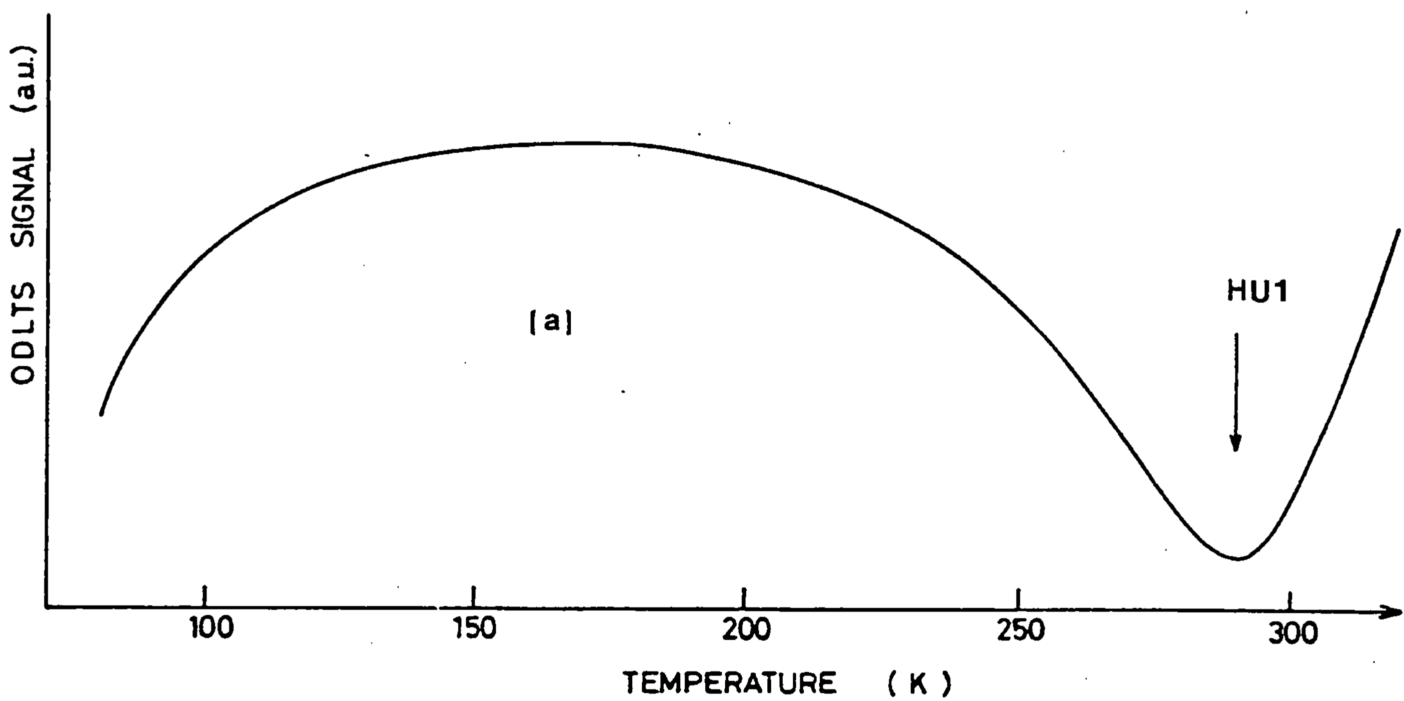


Figure 8.2 Arrhenius plots for (a) undoped and (b) copper doped CdSe



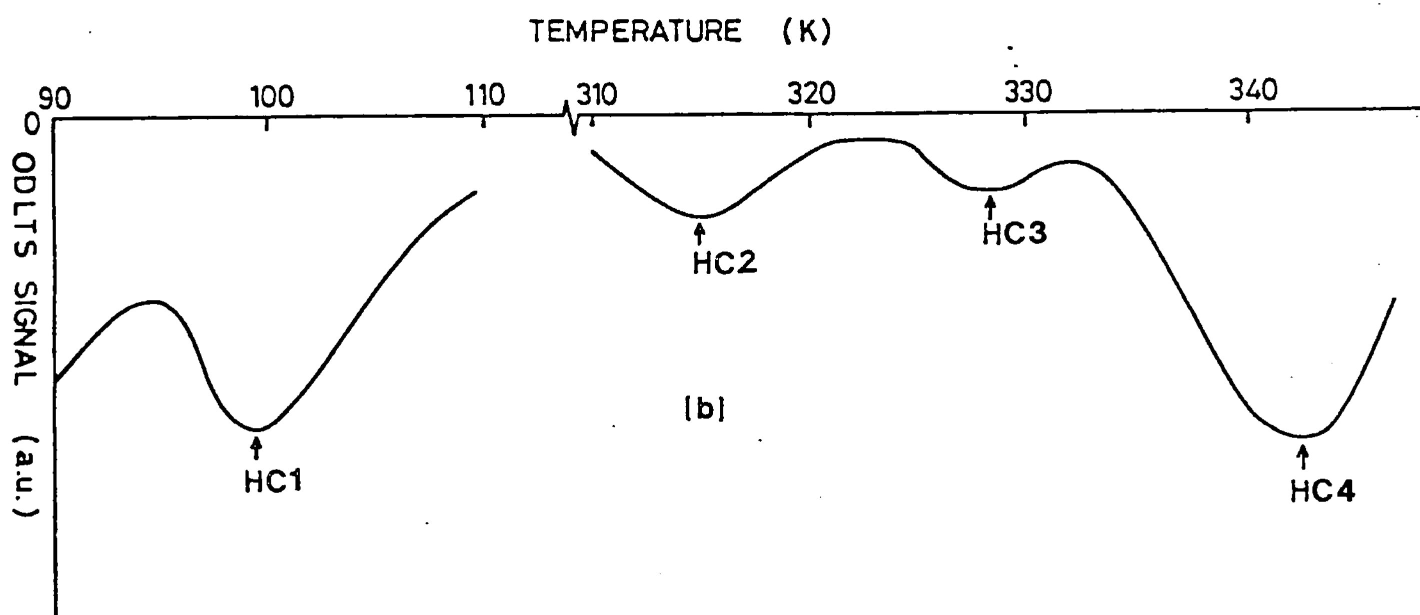


Figure 8.3 ODLTS spectra for (a) undoped and (b) copper doped CdSE

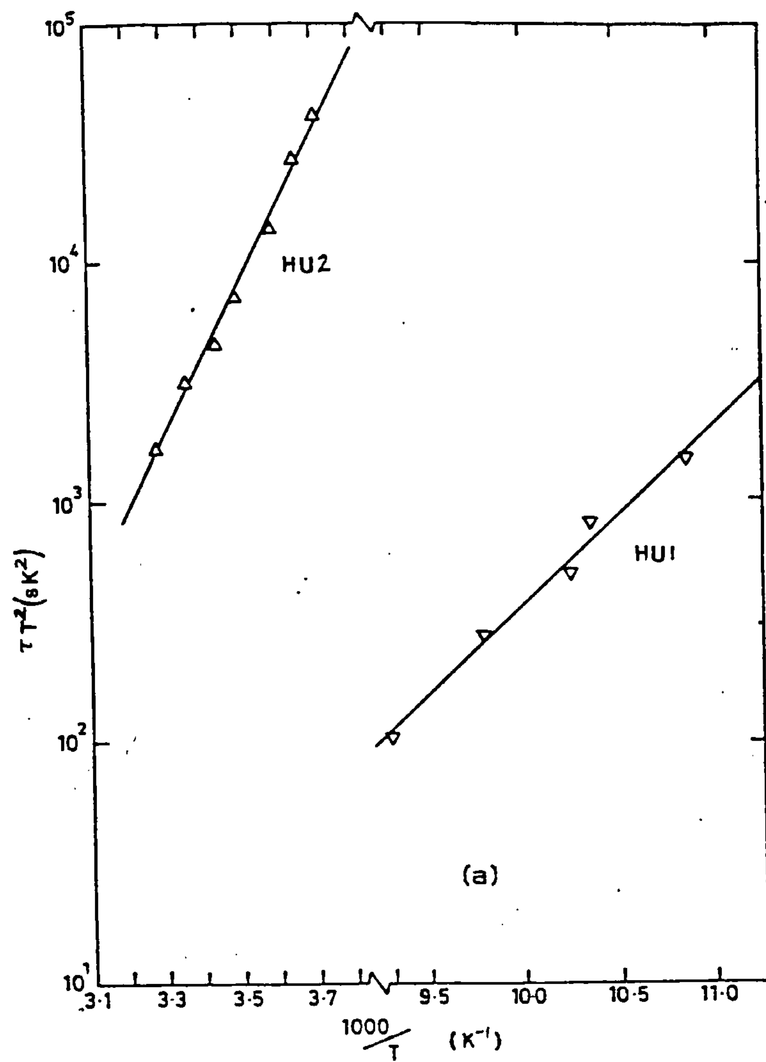


Figure 8.4 Arrhenius plots for (a) undoped and (b) copper doped CdSe

(a) Undoped

Electron Trap	Activation Energy (CB) ΔE(eV)	σ_n Cm^2
EU1	0.16 ± 0.01	$2 \times 10^{-18 \pm 1}$
EU2	0.46 ± 0.01	$2 \times 10^{-16 \pm 1}$
EU3	0.90 ± 0.03	$2 \times 10^{-15 \pm 1}$

Hole Trap	Activation Energy (VB) ΔE(eV)	σ_p cm^2
HU1	0.64 ± 0.02	$5 \times 10^{-16 \pm 1}$

(b) Copper doped

Electron Trap	Activation Energy (VB) ΔE(eV)	σ_n Cm^2
EC1	0.45 ± 0.01	$10^{-16 \pm 1}$
EC2	0.68 ± 0.02	$\times 10^{-18 \pm 1}$
EC3	0.91 ± 0.03	$2 \times 10^{-15 \pm 1}$

Hole Trap	Activation Energy (VB) ΔE(eV)	σ_p cm^2
HC1	0.22 ± 0.01	$5 \times 10^{-14 \pm 1}$
HC2	0.64 ± 0.01	$7 \times 10^{-16 \pm 1}$
HC3	0.77 ± 0.03	$1 \times 10^{-15 \pm 1}$
HC4	0.95 ± 0.05	$4 \times 10^{-13 \pm 1}$

Figure 8.5 Summary of traps observed in CdSe

8.2.4 Discussion

8.2.4.1 Undoped CdSe

In undoped CdSe three electron traps at 0.16ev, 0.46eV and 0.9eV below the conduction band, and one hole trap at 0.64eV above the valence band have been characterised. The 0.16eV centre was not seen in the copper doped material; it had a small capture cross-section of $10^{-18}cm^2$ suggesting it behaves as an electron repulsive centre [36]; and was probably due to a native defect such as a selenium vacancy. This trap has also been observed by Türe et al using PHCAP and attributed to a native defect [31]. The 0.46eV electron trap was observed in both undoped and copper doped CdSe. Its small cross-section suggests it behaves as a repulsive centre but to a lesser degree than the 0.16eV level. The deep electron trap at 0.9eV is thought to be a recombination centre [31,35] and is discussed later.

The dominant acceptor level in undoped CdSe was found at 0.64eV; this has been previously reported by Türe et al [30,31,35] using the techniques of ODLTS and PHCAP; by Robinson and Bube [33] using TSC and by Manfredotti et al [34] using TSC. This trap is thought to be the main sensitising centre in CdSe [30-35]. The large hole capture cross-section, $10^{-14}cm^2$, supports this suggestion. One would expect to have observed a deep level 1-1.2eV below the conduction band corresponding to this supposed sensitising centre, however, no such trap was observed in a DLTS scan upto 480K. This implies from the equation 3.31 that there is an upper upper limit of $10^{-18}cm^2$ for the electron capture

cross-section from the rate windows experimentally available. This gives a minimum cross-section ratio $\sigma(p)/\sigma(n)$ of 10^4 which is consistent with the idea that the level behaves as a sensitising centre. Robinson and Bube [33] discovered an acceptor level at 0.67eV above the valence band with a cross-section ratio $\sigma(p)/\sigma(n) = 2x10^7$. If this is the same centre observed in this work then it implies that the electron thermal capture cross-section for HU1 should be of the order $10^{-21} cm^2$. This suggests that the centre has a double negative charge as indicated by Robinson and Bube [33].

8.2.4.2 Copper Doped CdSe

The copper doped material showed the presence of three electron traps from DLTS at 0.45eV, 0.68eV and 0.9eV below the conduction band and four hole traps from ODLTS at 0.22eV, 0.64eV, 0.77eV and 0.95eV above the valence band. The electron trap at 0.45eV and hole trap at 0.64eV were observed in the undoped CdSe. The 0.64eV level is the native sensitising centre. The hole trapping level at 0.22eV has been observed using photocapacitance techniques [31,35]. It was only detected in copper doped material and has been attributed to this impurity centre [35]. It is thought possibly to be due to an excited state of copper by analogy with CdS [37] or a complex centre of the form $(Cu_i^{+} + V_{Cd}^{2-})$ [38,39].

The hole trapping centre at 0.95eV has been attributed to the copper impurity [31,33,35] since it only appears

clearly in intentionally doped CdSe. The DLTS results show a peak at 420K corresponding to the electron trap at 0.68eV as mentioned above. The band gap at this temperature is 1.66eV, and assuming that the level is pinned to the valence band then the DLTS and ODLTS responses originated from the same centre. This gives a cross-section ratio $\sigma(p)/\sigma(n) = 10^5$ thus indicating the copper level behaves as a sensitising centre in CdSe [31,35]. Robinson and Bube [33] also observed the copper centre but concluded that it was not involved in the sensitisation process. They suggested that the level 0.64eV above the valence band was the main sensitising centre. However, they did not directly measure the cross-section ratio for the copper centre as determined here which would have been conclusive.

The state at 0.77eV above the valence band and that 0.9eV below the conduction band are probably due to the same centre; their sum, within experimental error, gives the band gap. The 0.9eV level was also observed in undoped CdSe but not the 0.77eV level. This was due to the fact that the temperature was not taken high enough during the ODLTS scan for the 0.77eV level to be seen. The cross-section ratio for this centre is approximately unity, that is the electron capture cross-section is approximately equal to that for holes. This shows that the level behaves as a class I recombination centre [31]. Türe et al [35] suggested that this centre was involved in an anomalous photoconductivity response. As the photon energy to the sample was increased, there was a gradual increase followed by a sharp reduction in the photocurrent. The initial increase was attributed to

electron emission from the sensitising centre (EC2/HU4) into the conduction band. As the energy increased such that it was equal to the energy difference between this centre and the valence band then it would emit holes to the valence band. These would be immediately captured by the recombination centre, thereby switching on a fast recombination route. This reduces the carrier lifetime in the conduction band consequently, giving the reduction in the photoconductivity response as observed.

8.2.4.3 Summary

DLTS and ODLTS have been used to characterise the main trapping centres in undoped and copper doped CdSe. Two sensitising centres have been observed, one with a level at 0.64eV above the valence band, thought to be due to a native defect such as a cadmium vacancy and the other level at 0.95eV due to copper impurity. Only the native centre was observed in the undoped material, whereas, both were seen in the doped CdSe. A class I recombination centre has also been characterised in both types of material at 0.9eV below the conduction band. This would probably affect the operation of the CdSe/Cu_2Se solar cell by reducing the free carrier lifetime and, thereby, reducing its efficiency.

Several other centres have been observed - the 0.45eV electron trap which was common to undoped and doped CdSe; a level at 0.22eV above the valence band, thought to be a copper impurity centre; and a native defect centre at 0.16eV below the conduction band.

8.3 Cadmium Telluride

8.3.1 Introduction

Cadmium telluride has a narrower bandgap than most other II-VI compounds - 1.56eV at room temperature - and can easily be made n- or p-type. As a result CdTe has attracted considerable interest with a view to its applications. It has been shown to be an efficient room temperature nuclear detector [40] since it has suitable properties such as high average atomic number, large band gap and reasonable mobility and lifetimes for free carriers [40]; several thin film CdTe solar cells have been described, for example, based on the screen printing technology [6] with power conversion efficiencies >8% [eg 41].

One of the main difficulties has been the control of point and extended defects during the growth and post-growth treatments of the material. For example, Verity et al [21,26] have shown that the defect signature of a CdTe sample varied significantly depending upon its history. The performance of CdTe as an electronic material is strongly influenced by such electrically active defect levels. This has motivated several studies of deep levels using different techniques : photoluminescence [42], thermally stimulated conductivity [43-45], and DLTS [18-26].

The present work is concerned with the deep trapping levels present in single crystal n-type CdTe grown by the Piper-Polich technique [46], using DLTS and ODLTS.

8.3.2 Material Growth and Device Preparation

Single crystals of CdTe were grown using a modified Piper-Polich technique as discussed in chapter 4. The CdTe charge was maintained in the flat region of the temperature profile at 1000C. Crystal growth was found to occur at 900C giving boules 3cm in length after 72hrs growth time with grain sizes $>$5mm.

The unoriented boule was cut into 4x4x2mm dice for the purpose of device preparation. The as-grown material was n-type with resistivity of the order of 1kΩcm. The dice were annealed in liquid cadmium at 600C for 72hrs after which they were quenched to room temperature in water. This gave material with resistivity of about 5Ωcm. They were mechanically polished using 1μ alumina and subsequently etched in 2% bromine/methanol for 30secs to reduce surface damage and then thoroughly washed in methanol. Gold and indium were evaporated onto opposite faces to give the Schottky barrier contact and Ohmic contact respectively. Free carrier concentrations determined from capacitance-voltage measurements (see fig 8.6 for $1/C^2$ vs V plots) showed little variation over the temperature range 80-380K used for DLTS : at 80K - $3.2\times10^{15}cm^{-3}$; at 295K - $5.3\times10^{15}cm^{-3}$; at 376K - $5.7\times10^{15}cm^{-3}$.

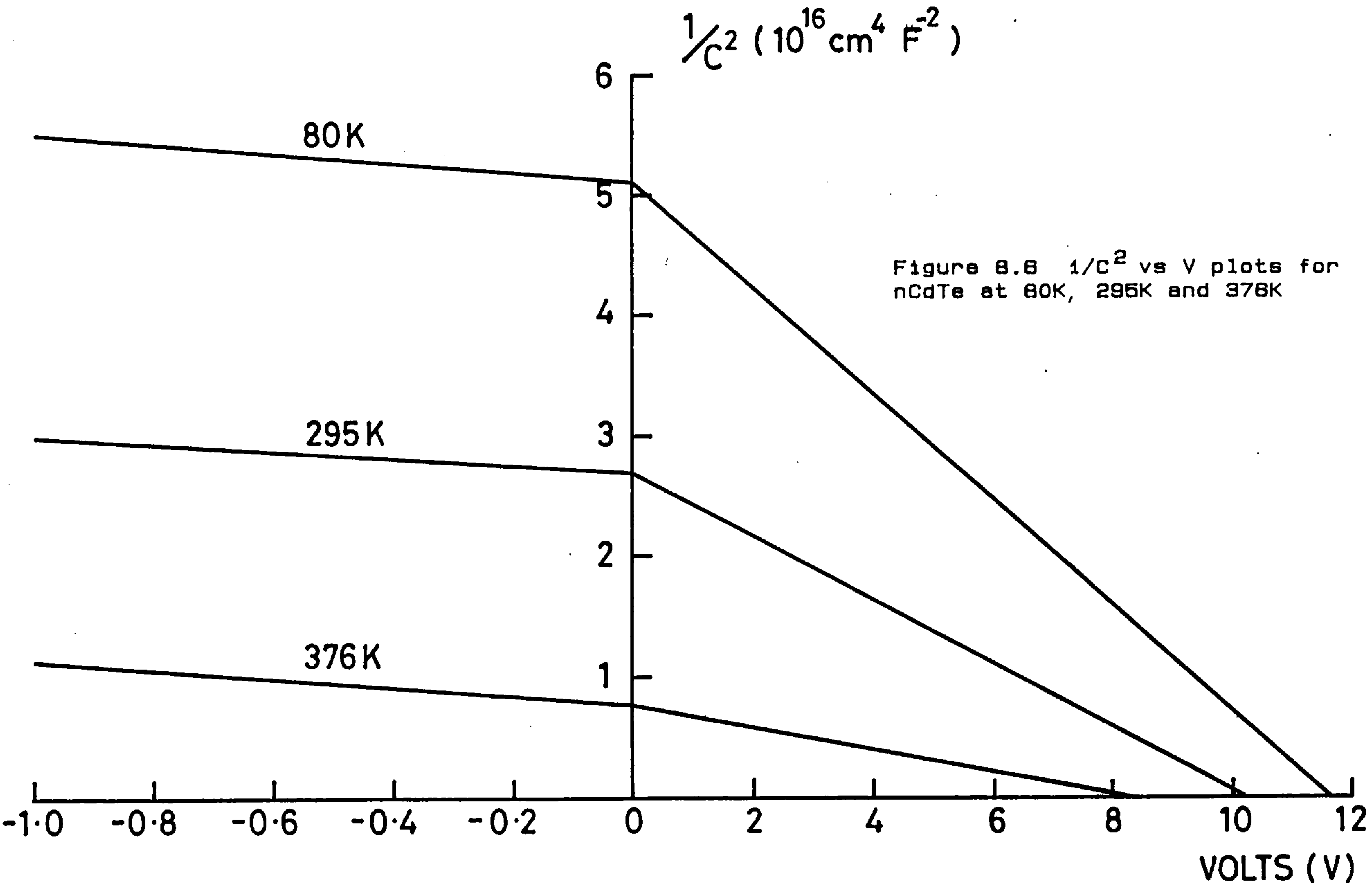


Figure 8.6 $1/C^2$ vs V plots for nCdTe at 80K, 295K and 376K

8.3.3 DLTS and ODLTS

DLTS was carried out over the temperature range 80-380K. The resultant spectrum is shown in fig. 8.7 clearly displaying 6 peaks; these correspond to 6 electron traps denoted EP1-6. Arrhenius plots of $\ln(\tau T^2)$ against 1000/T are given in fig. 8.8. The traps were found to lie between 0.15 and 0.63eV below the conduction band with densities in the range 0.17 to $7.1\times10^{14}\,cm^{-3}$. These results are summarised in fig. 8.9. The capacitance transients behaved exponentially giving a good fit to the function

$$C = A + B\exp(-t/\tau) \qquad 8.1$$

where A is an offset and B a scaling parameter (this is discussed in chapter 4). Transient for τ = 26msecs for the peak EP1 is given in fig. 8.10.

After a filling pulse at 80K the device capacitance under 2V reverse bias was scanned with temperature from 80-380K. Fig. 8.11 shows the capacitance-temperature scan. The important feature is the capacitance reduction with temperature from 95K to 190K. This probably corresponds to extended defects as discussed for CdS in section 5.2.2, and by Simoen et al [47]. Using Simoen's analysis for the determination of the dislocation density this gives a value of $10^{10}\,cm^{-3}$. In addition, some capacitance thresholds were observed at similar temperatures to the peaks seen in DLTS. These thresholds correspond to the temperatures at which the traps seen in DLTS freeze out.

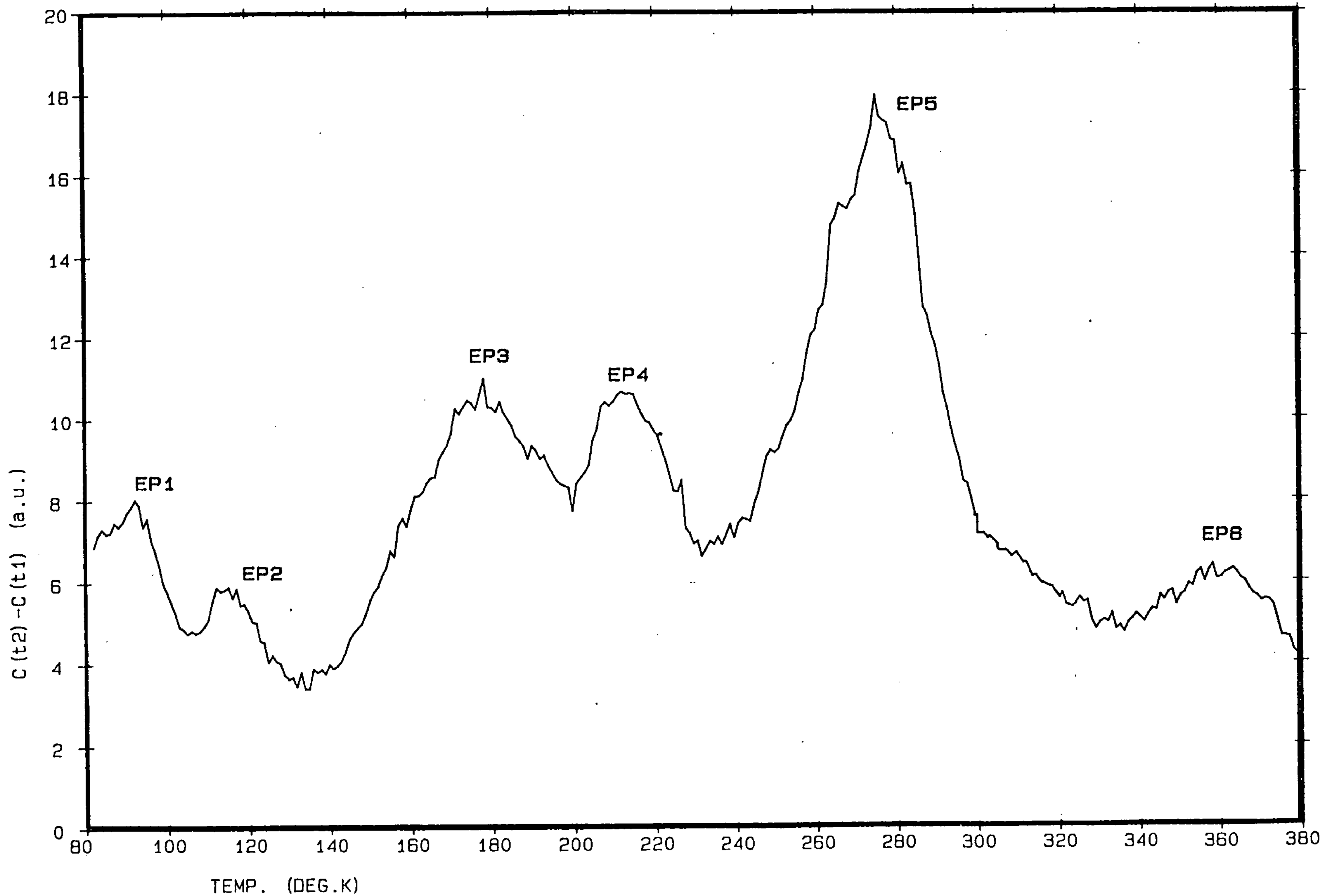


Figure 6.7 DLTS spectrum of nCdTe

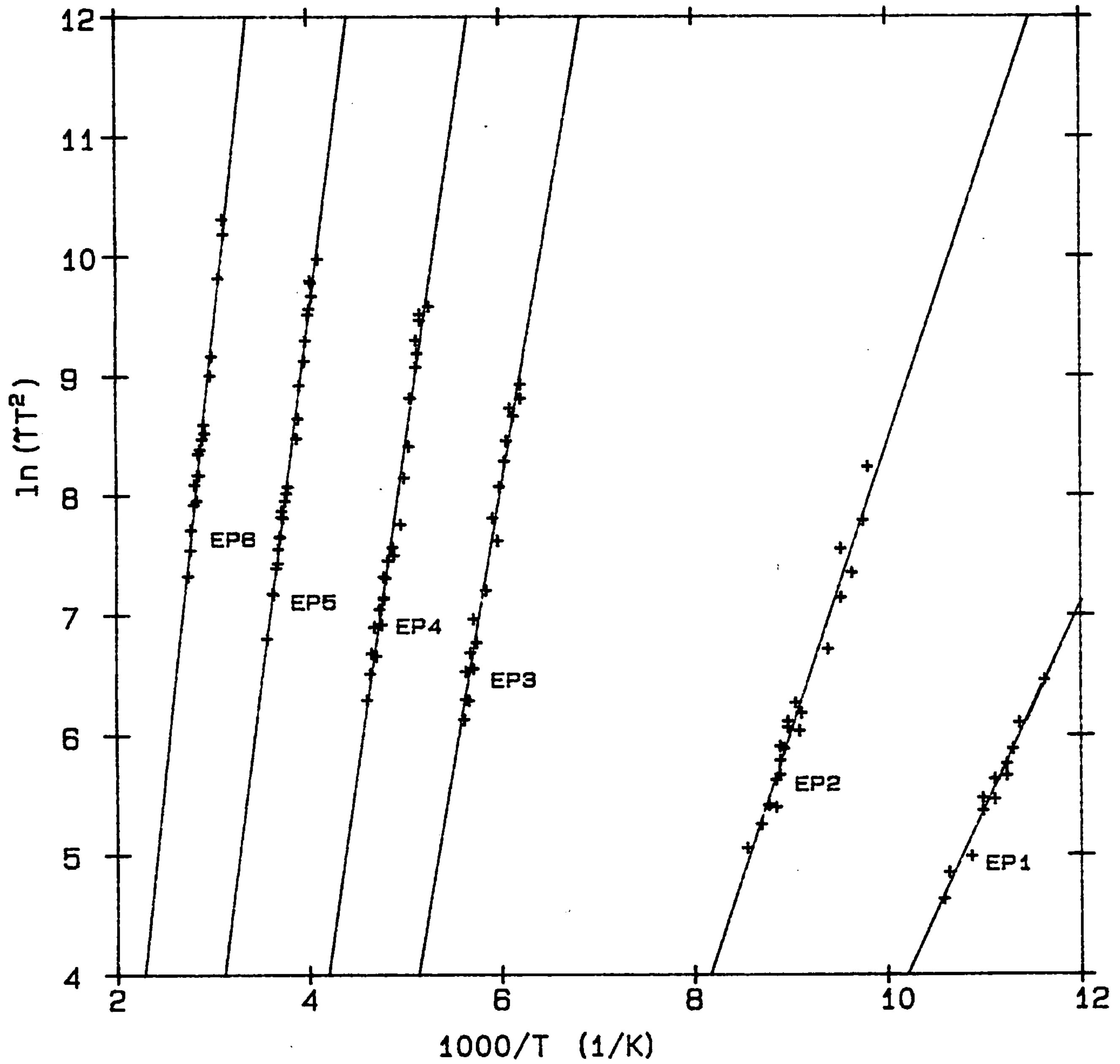
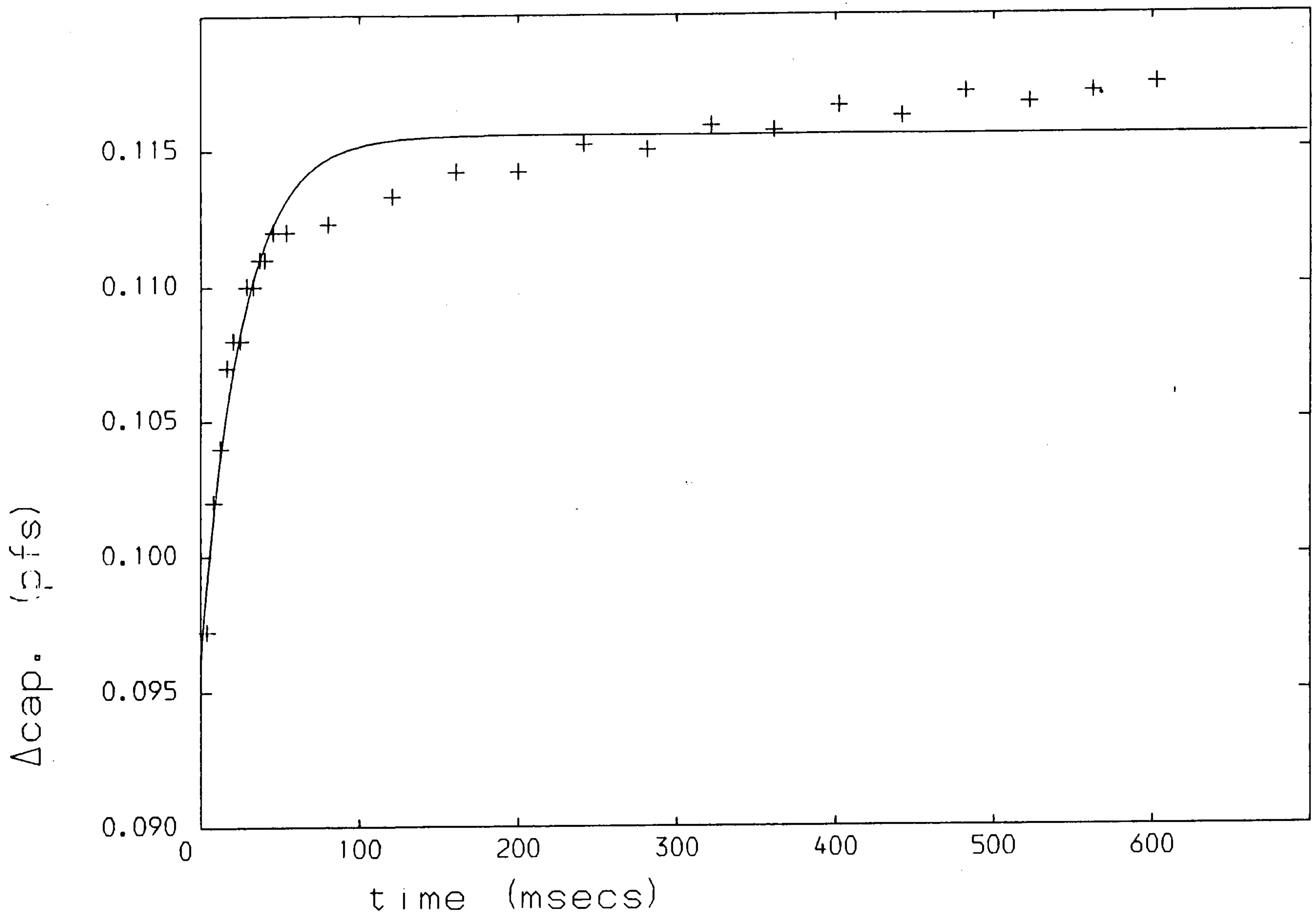


Figure 8.8 Arrhenius plots for the electron traps in nCdTe

	T-range/K	ΔE/eV	σ_n/cm^2	N_T/cm^{-3}	N_T/N_d
EP1	80 – 95	0.15 ± 0.01	$10^{-16\pm1}$	3.1×10^{14}	9.0×10^{-2}
EP2	100–120	0.21 ± 0.01	$10^{-15\pm1}$	1.7×10^{13}	5.4×10^{-3}
EP3	150–180	0.40 ± 0.02	$10^{-14\pm2}$	3.7×10^{14}	0.11
EP4	195–215	0.47 ± 0.01	$10^{-14\pm1}$	4.9×10^{14}	0.11
EP5	245–280	0.53 ± 0.01	$10^{-16\pm1}$	7.1×10^{14}	0.14
EP6	320–360	0.63 ± 0.02	$10^{-17\pm1}$	2.4×10^{14}	4.3×10^{-2}

Figure 8.9 Summary of the electron traps observed in nCdTe



FITTED PARAMETERS

P 1 = 0.116E00 P 2 = -0.194E-01 P 3 = 0.256E02

Figure 8.10 Capacitance transient due to electron emission from trap EP1 at 92K

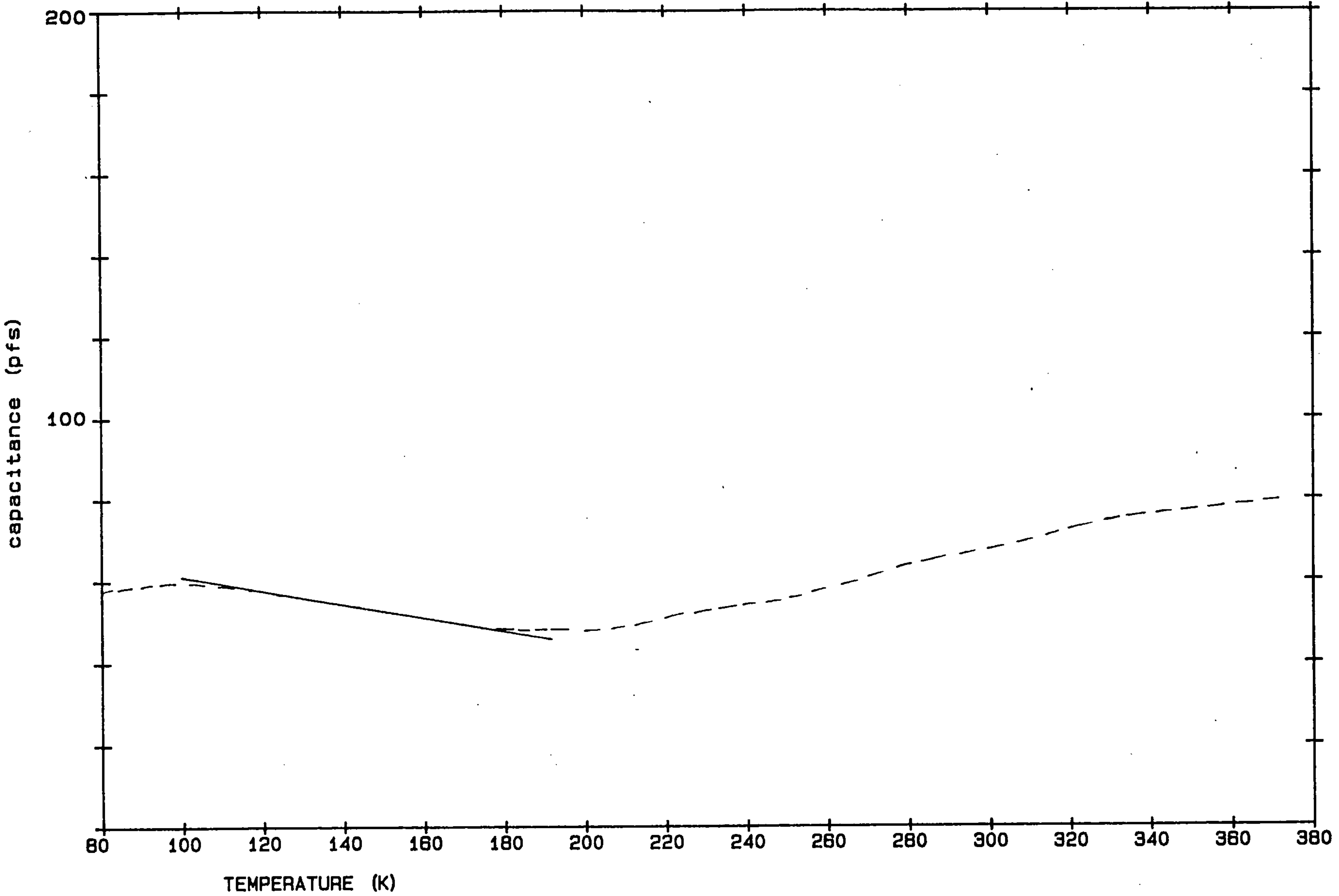


Figure 8.11 Capacitance-temperature scan for nCdTe

Optical DLTS was carried out using a pulsed, high intensity 'sweet spot' LED with peak output at 820nm. Over the temperature range 80-380K there were no peaks. However, one broad feature was observed whose peak could not be resolved since even for the shortest time constant available of ~4msec it extended below the 80K limit on the low temperature side of the spectrum (see fig. 8.12).

8.3.4 Discussion of Results

DLTS and ODLTS have been used to investigate the deep level parameters in Cd-annealed CdTe prepared by the Piper-Polich technique. The free carrier concentration was found to be invariant with temperature over the range 80-380K; this has been reported for CdTe grown by the Bridgman and travelling heater method (THM) [21] and in the Clark-Woods grown material [48]. This means that the shallow donor levels were completely ionised at liquid nitrogen temperature. Subsequent heating to 380K did not uncover further levels that would contribute to the free carrier density.

Six electron traps were observed using DLTS; their activation energies, capture cross-sections and densities have been given in fig. 8.9. Comparison of this data with other published data based on DLTS is indicated in fig. 8.13. The level EP1 at 0.15eV has not been previously reported. EP2 at 0.21eV has been reported by Verity et al [21,26] on as-grown (Bridgman) and In/Cd annealed material, and by Sitter et al on epitaxial CdTe [23-25]. The capture

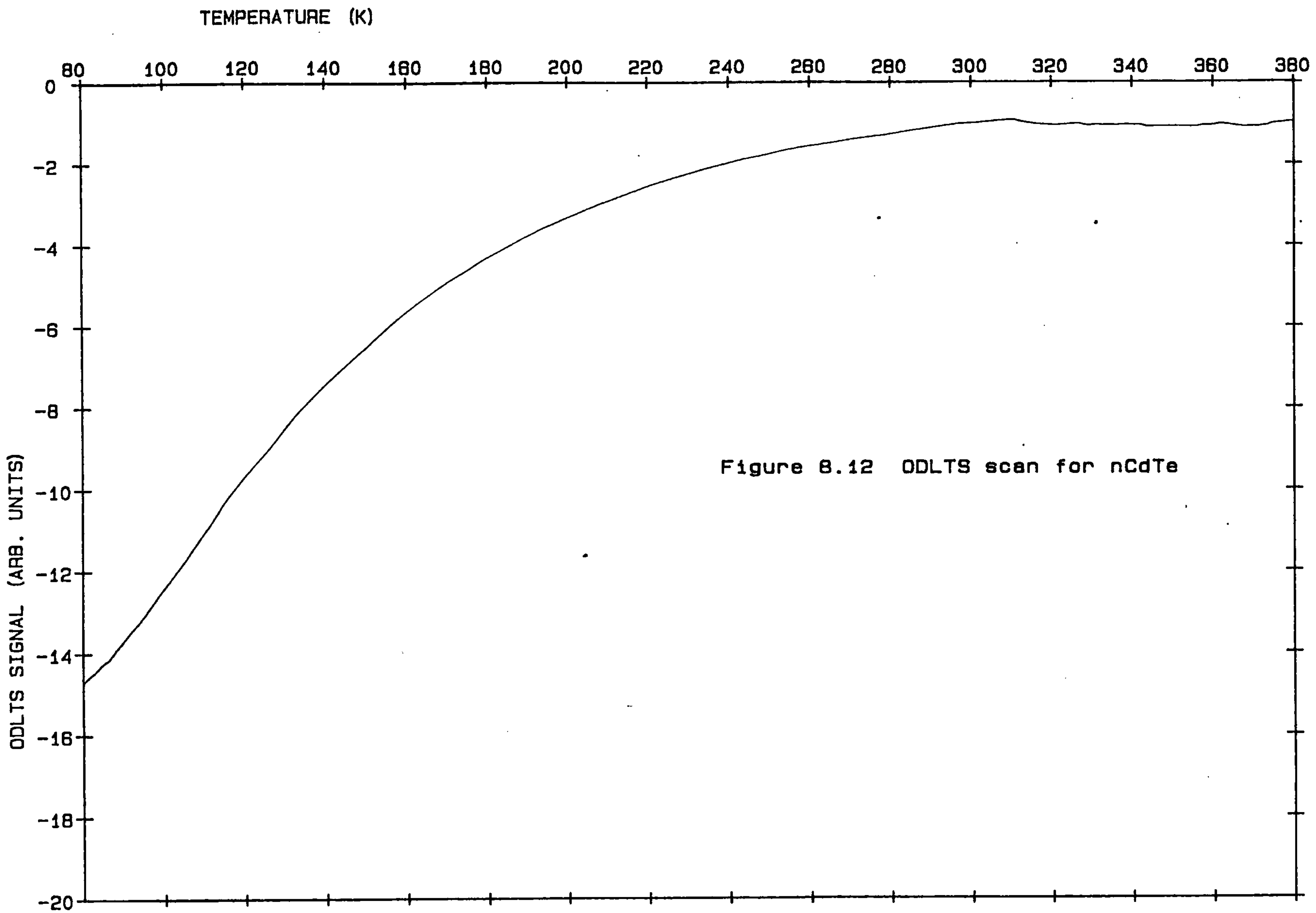


Figure 8.12 ODLTS scan for nCdTe

Figure 8.13 Summary of the reported DLTS data on nCdTe

cross-section reported by Verity et al is in good agreement with the value given in fig. 8.13. It must be pointed out that they found this trap disappeared in their Bridgman grown material after annealing in Cd vapour. A level with a similar activation energy has been reported by Isett and Raychaudhuri [18], however, they found this trap had a very small capture cross-section of 10^{-23} cm . Therefore, it is likely that the respective DLTS responses came from different levels. EP3 was also observed by Verity et al [21,26] but only in Bridgman material annealed in Cd vapour. This was not observed in their as-grown material nor in that grown by the THM method. Electron trap EP4 correlates with defects introduced by long anneal times as shown by Takebe et al (6hr anneal at 700C) [19,20] and Verity et al (40hr anneal at 800C) [21,26]. However, that quoted by Takebe et al has a capture cross-section two orders of magnitude less than that for EP4 so it is not clear whether these traps are identical. The value given by Verity et al is within the experimental error. The levels EP5 and EP6 have activation energies and capture cross-sections 0.52eV, 10^{-16} cm^2 and 0.63eV, 10^{-17} cm^2 respectively. These values are in good agreement with those for two levels observed by Isett and Raychaudhuri [18] at 0.52 and 0.63eV. EP6 has been reported by Sitter et al [23-25] on epitaxial CdTe - 0.64eV, $1.5 \times 10^{-17} cm^2$.

Optical DLTS has indicated the presence of a hole trap with a thermal emission rate at 80K that was faster than that available from the experimental rate window. This is shown in the ODLTS spectrum by the downward trend towards 80K indicating a peak below the low temperature limit of the

experiment.

The capacitance-temperature scan showed a reduction in capacitance between 95K and 190K. Such a phenomenon is thought to be due to extended defects [47]. Indeed a dislocation density of $10^{10}cm^{-2}$ was determined; Durose et al [49,50] have reported on the high density of dislocations in the CdTe grown in Durham. These can undergo polygonisation during the growth or any annealing process, thereby, creating subgrain boundaries. These types of defects may form electrically active deep states [51]. In addition, tellurium precipitates have been characterised in CdTe [51]; these can aggregate at extended defects and perhaps produce deep trapping centres. However, it is not clear which of the levels seen by DLTS, if any, may have arisen from dislocations.

Many electron traps have been observed in CdTe using DLTS [18-26]. The DLTS signature of a particular sample has been shown to depend upon the growth technique and conditions, and on post-growth treatment. Five levels shown in this work correspond with levels reported by others but not previously found together in the same sample and a new level, EP1, observed at 0.15eV below the conduction band. Identification of these levels is not directly possible by DLTS. The trap EP4 appears to be induced by long, high temperture anneals in Cd implying that it may be due to a tellurium vacancy or cadmium interstitial or to states associated with extended defects.

8.4 Zinc Sulphide

8.4.1 Introduction

Zinc sulphide exhibits a blue luminescence centre resulting from optical transitions between deep levels in the band gap and shallow states near the band edges. Consequently, the potential use of ZnS as a blue LED has motivated much interest. Indeed, such devices have been produced : Schottky barrier LED [eg 53], MIS LED [eg 54]. One of the main problems has been to produce low resistivity material since ZnS has such a large band gap (3.7eV at room temperature). Thomas et al [55] have reported semiconducting ZnS by annealing the material in molten Zn containing 1%Ga and 0.5%Al. This is the method used in the present work to produce material suitable for the study of deep level defects by DLTS, ODLTS and DLOS.

8.4.2 Material Growth and Device Preparation

Insulating ZnS was grown using the same method as for CdTe based on the Piper-Polich technique [46]. The charge material was vacuum sublimed ZnS. Growth over 48hrs was carried out at about 1500C with slow cooling (24hrs) to reduce cracking of the crystal boule. The boules so obtained were about 3cm in length and 1cm in diameter and typically contained a few grains.

The oriented material (hexagonal) was cut into 4x4x2mm dice suitable for device making. The dice were annealed in liquid Zn containg 1%Ga and 0.5%Al at 850C for 12hrs. This

treatment resulted in resitivities of the order of 1kΩcm. Ohmic contacts were made to the material by annealing In/10%Cd onto a surface for 2mins at 320C in vacuum. Gold provided a Schottky barrier on the opposite surface by evaporation. Capacitance-voltage measurements at 78K and 310K gave values for the free carrier concentrations - $5\times10^{15}cm^{-3}$ and $5\times10^{16}cm^{-3}$ respectively (see fig. 8.14 for $1/C^2$ vs V plots).

8.4.3 DLTS and ODLTS

DLTS was carried out over the temperature range 80-400K using a -6V steady state reverse bias. The samples were given 0V pulses of width 10msecs to ensure complete trap refilling. The DLTS spectrum is shown in fig. 8.15; two peaks denoted EZ1 and EZ2 were clearly visible at about 110K and 210K respectively. Analysis of the plot of $\ln(\tau T^2)$ against 1000/T shown in fig. 8.16 gave the activation energies and capture cross-sections : EZ1 - 0.25eV, $9\times10^{-16}cm^2$ and EZ2 - 0.5eV, $2\times10^{-14}cm^2$. These results, including the trap densities, are summarised in fig. 8.17.

ODLTS was carried out in order to investigate the deep acceptor states. Using the Ar laser system described in chapter 4 for a scan over the temperature range 80-400K no ODLTS features were observed. The operating wavelength of the laser was only suitable for hole traps at a depth greater than 1eV above the valence band. The problem then arises of thermal emission of holes not being possible due to the temperature limitations of the system.

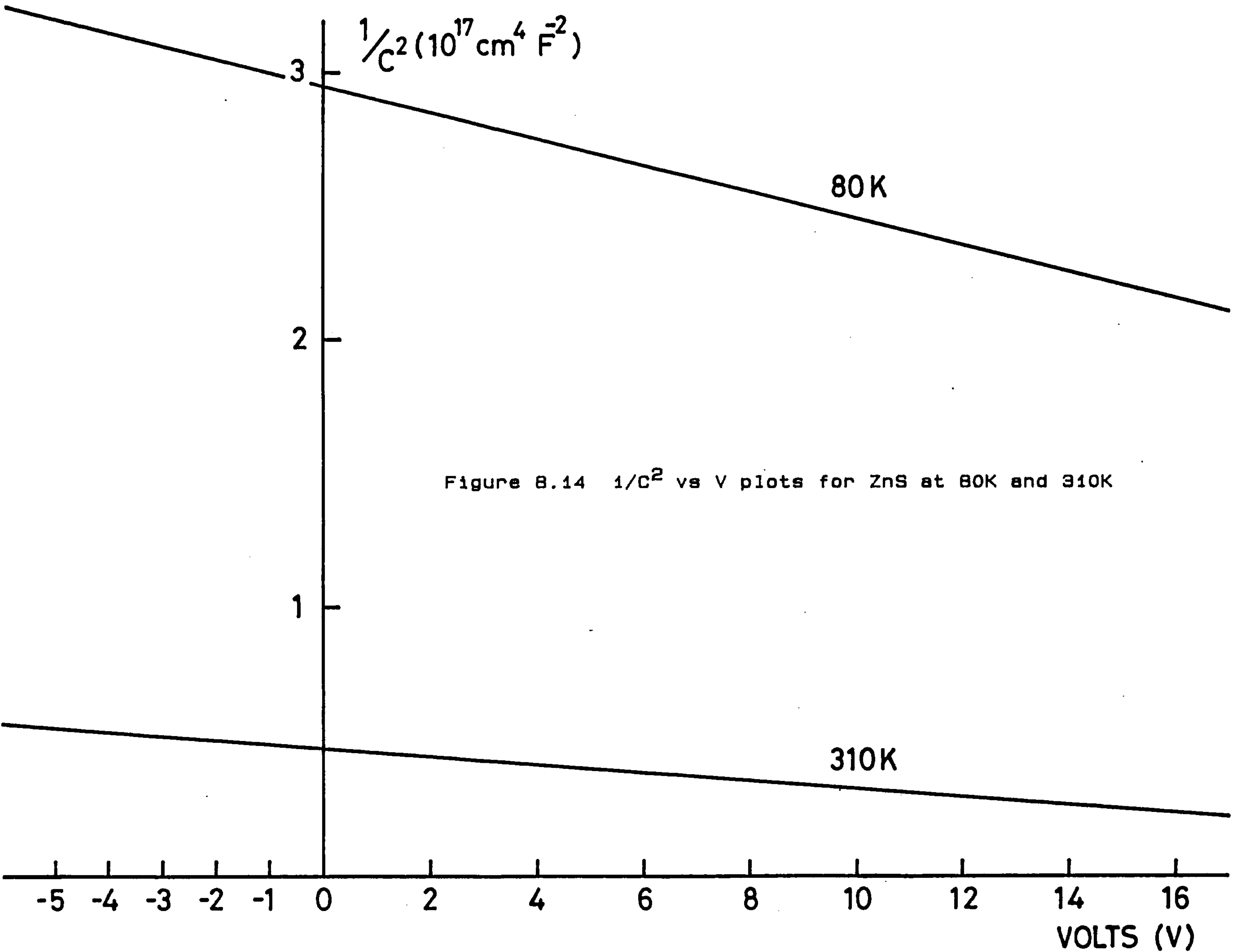


Figure 8.14 $1/C^2$ vs V plots for ZnS at 80K and 310K

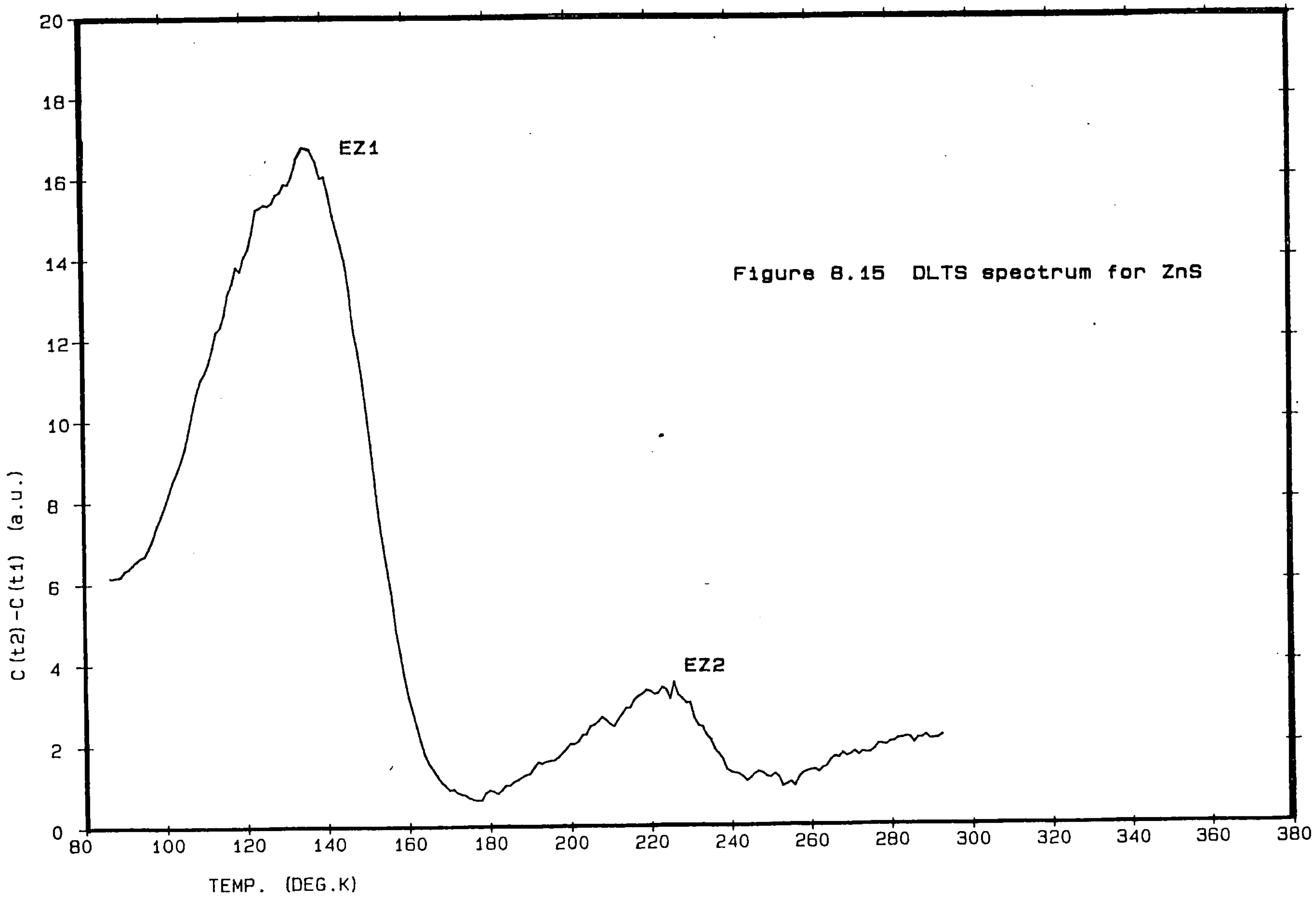


Figure 8.15 DLTS spectrum for ZnS

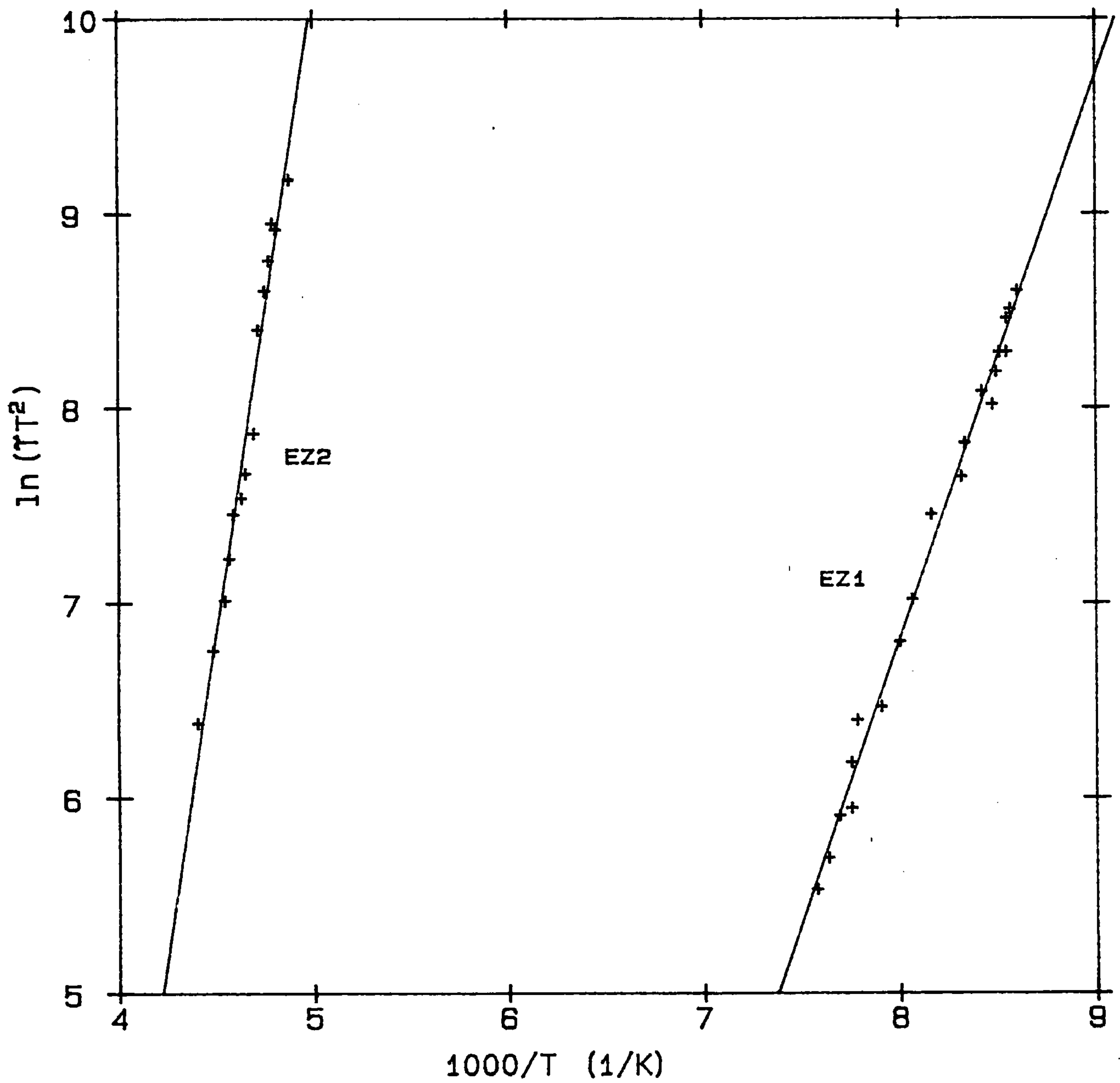


Figure 8.16 Arrhenius plots for the electron traps in ZnS

	Temp.range	ΔE / eV	σ_n / cm^2	N_T	N_T / N_d
EZ1	110–130	0·25±0·01	$10^{-15\pm1}$	$1\cdot6 \times 10^{15}$	0·33
EZ2	200–230	0·50±0·03	$10^{-14\pm1}$	$5\cdot2 \times 10^{14}$	$5\cdot2 \times 10^{-2}$

Figure 8.17 Summary of the electron traps observed in ZnS

Fig. 8.18 shows a capacitance-temperature scan over the range 80-380K. There were thresholds at 100K and 200K corresponding approximately in temperature with the DLTS peaks due to EZ1 and EZ2. From 300K the capacitance suddenly rose rapidly as a response to some deep trapping centre releasing its carrier.

8.3.4 DLOS

Electrical DLOS [56] was carried out over the optical energy range 0.7 to 2.6eV at room temperature. The samples were pulsed to zero bias from a steady state -5V with a pulse width of 20msec and a repetition period of 1sec. Fig. 8.19 shows the energy dependency of the electron capture cross-section over this range. Four thresholds in the DLOS spectrum were observed. The DLOS data in the threshold regions were fitted to the function

$$\sigma(h\upsilon) = \frac{P1(h\upsilon - P2)}{h\upsilon(h\upsilon + P3)^2} \qquad 8.2$$

using a nonlinear least squares method as described in section 4.7 in chapter 4. This is the Chantre function for the energy dependence of the capture cross-section [56]. The theoretical fits to the data are given in figs 8.20-23. These gave threshold energies of 1.25, 1.37, 1.89 and 2.19 eV corresponding to depths below the conduction band edge. The room temperature band gap of ZnS is 3.68eV [57] so the energy thresholds above the valence band were 2.43, 2.31, 1.79 and 1.49 eV.

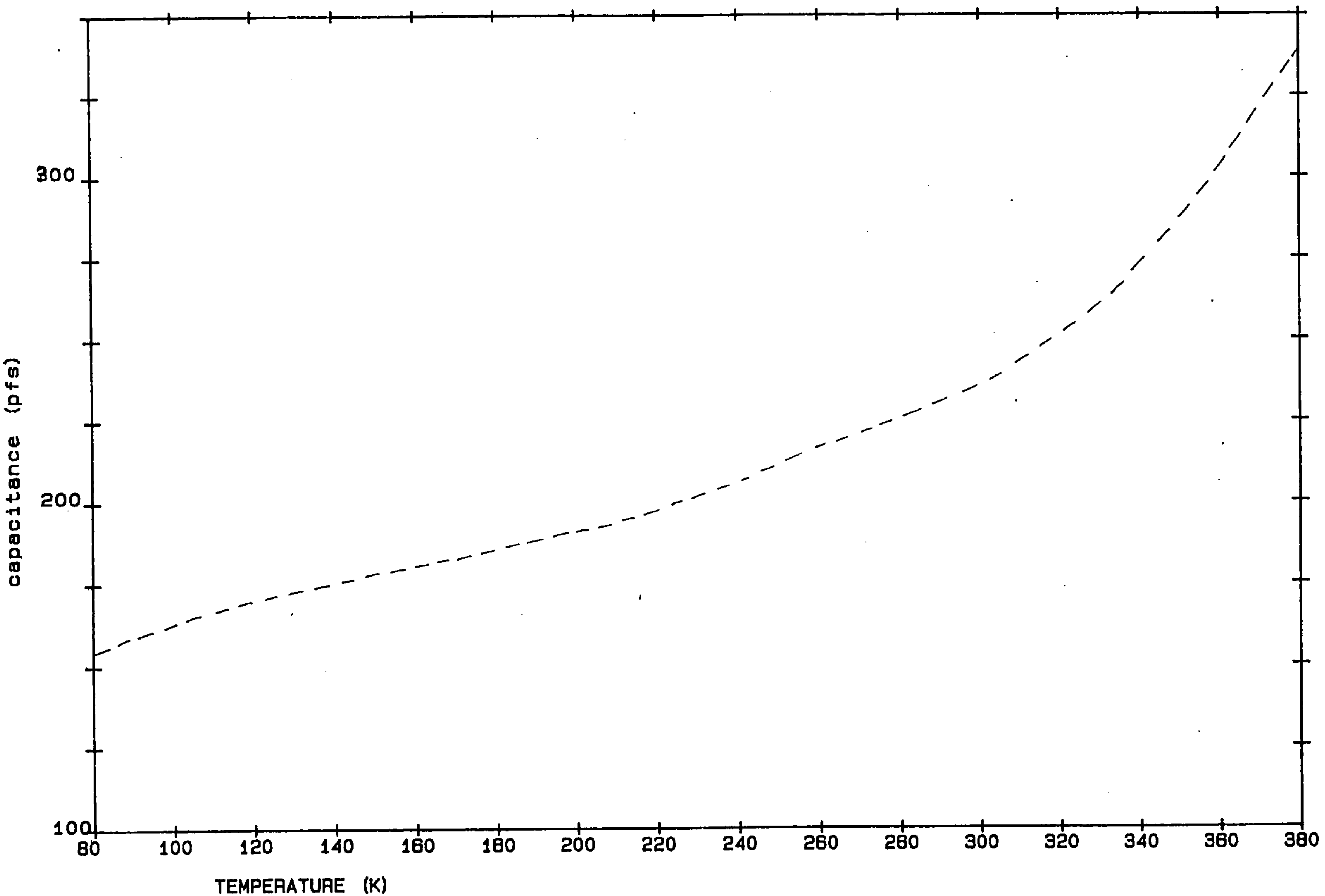


Figure 8.18 Capacitance-temperature scan for ZnS

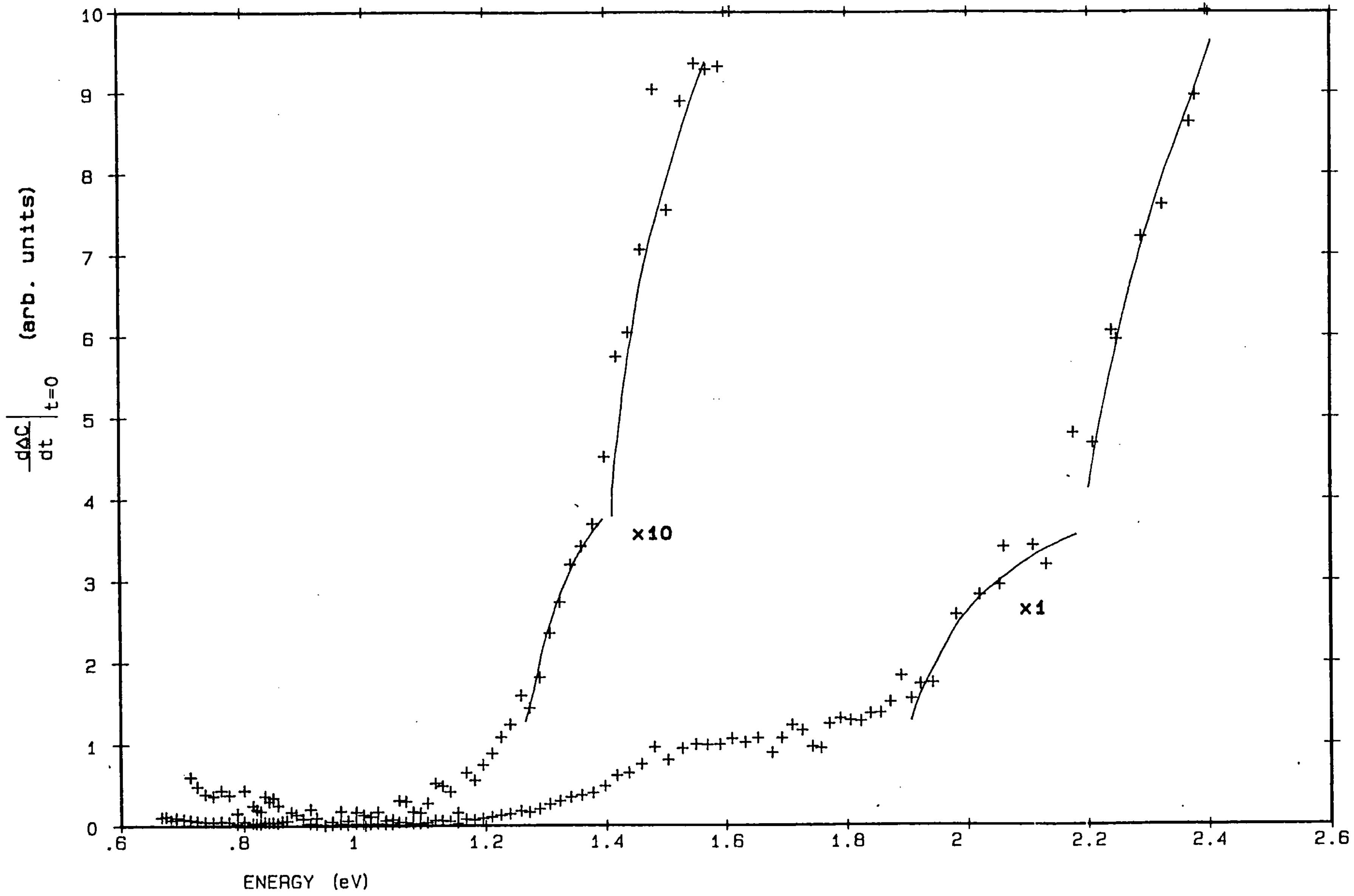
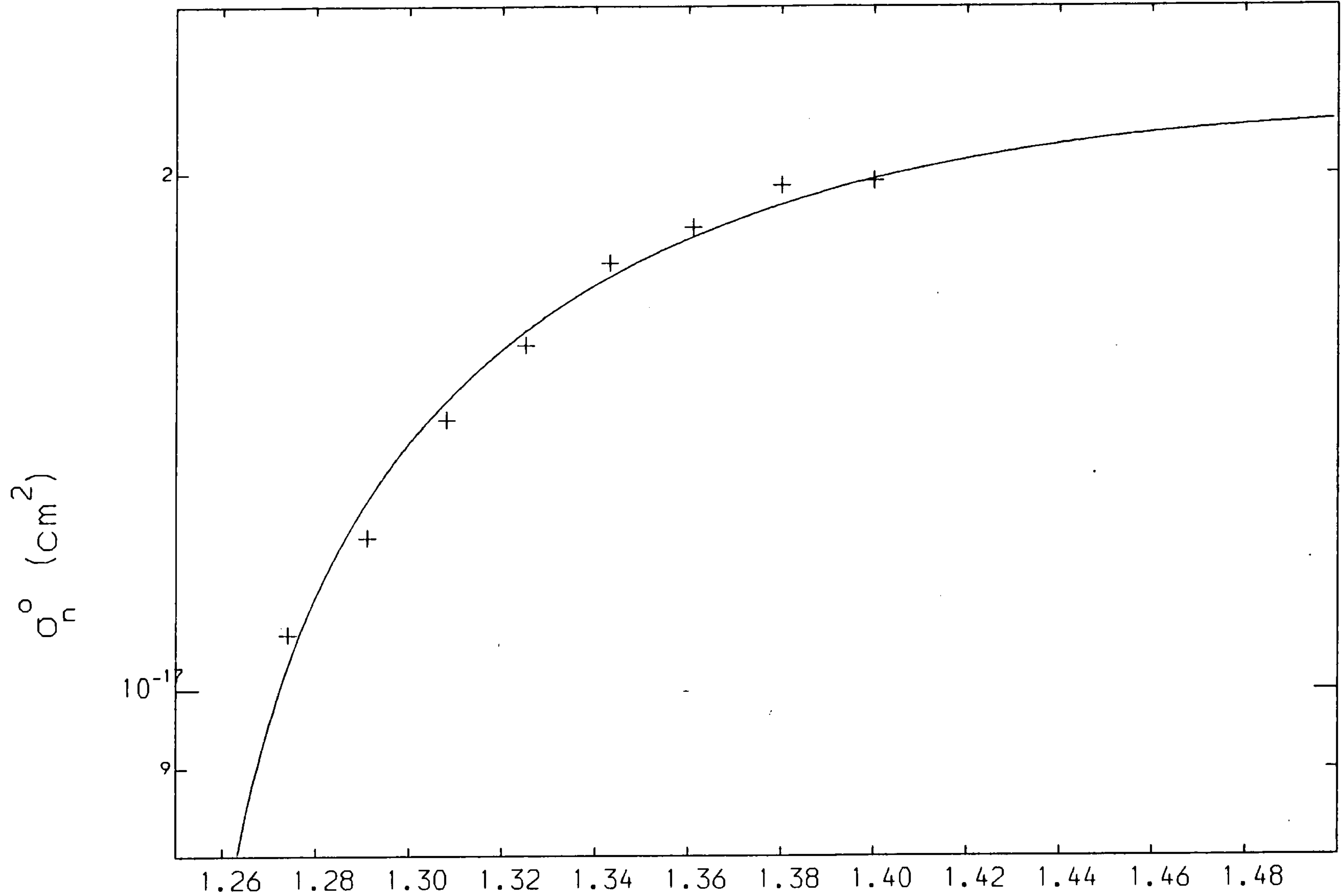


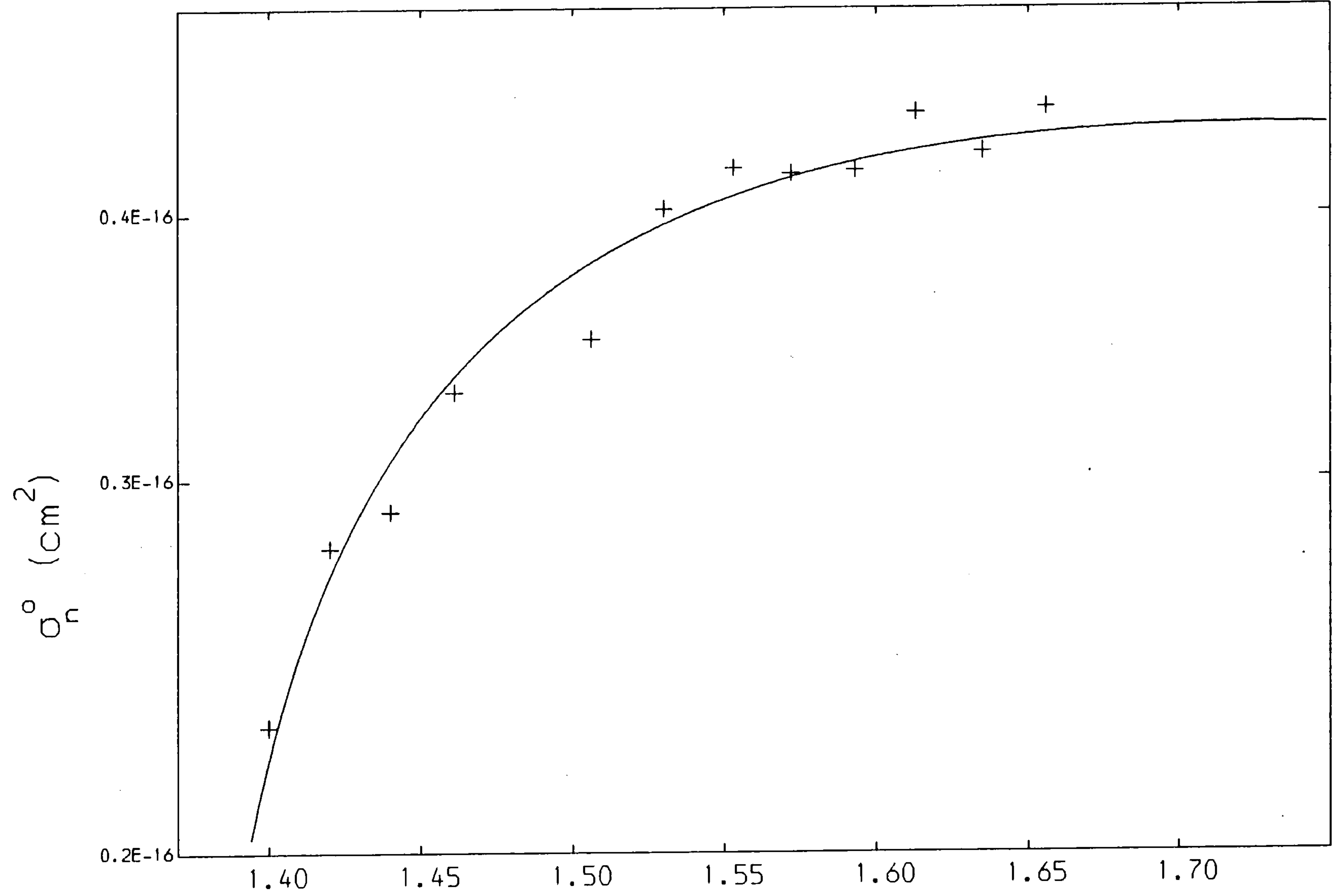
Figure 8.19 DLOS scan for ZnS at 295K



FITTED PARAMETERS

P 1 = 0.240E-15 P 2 = 0.125E01 P 3 = 0.434E00

Figure 8.20 Theoretical (——) and experimental (++++) DLOS curves showing a threshold at 1.25eV



FITTED PARAMETERS

P 1 = 0.772E-15 P 2 = 0.137E01 P 3 = 0.742E00

Figure 8.21 Theoretical (——) and experimental (++++) DLOS curves showing a threshold at 1.37eV

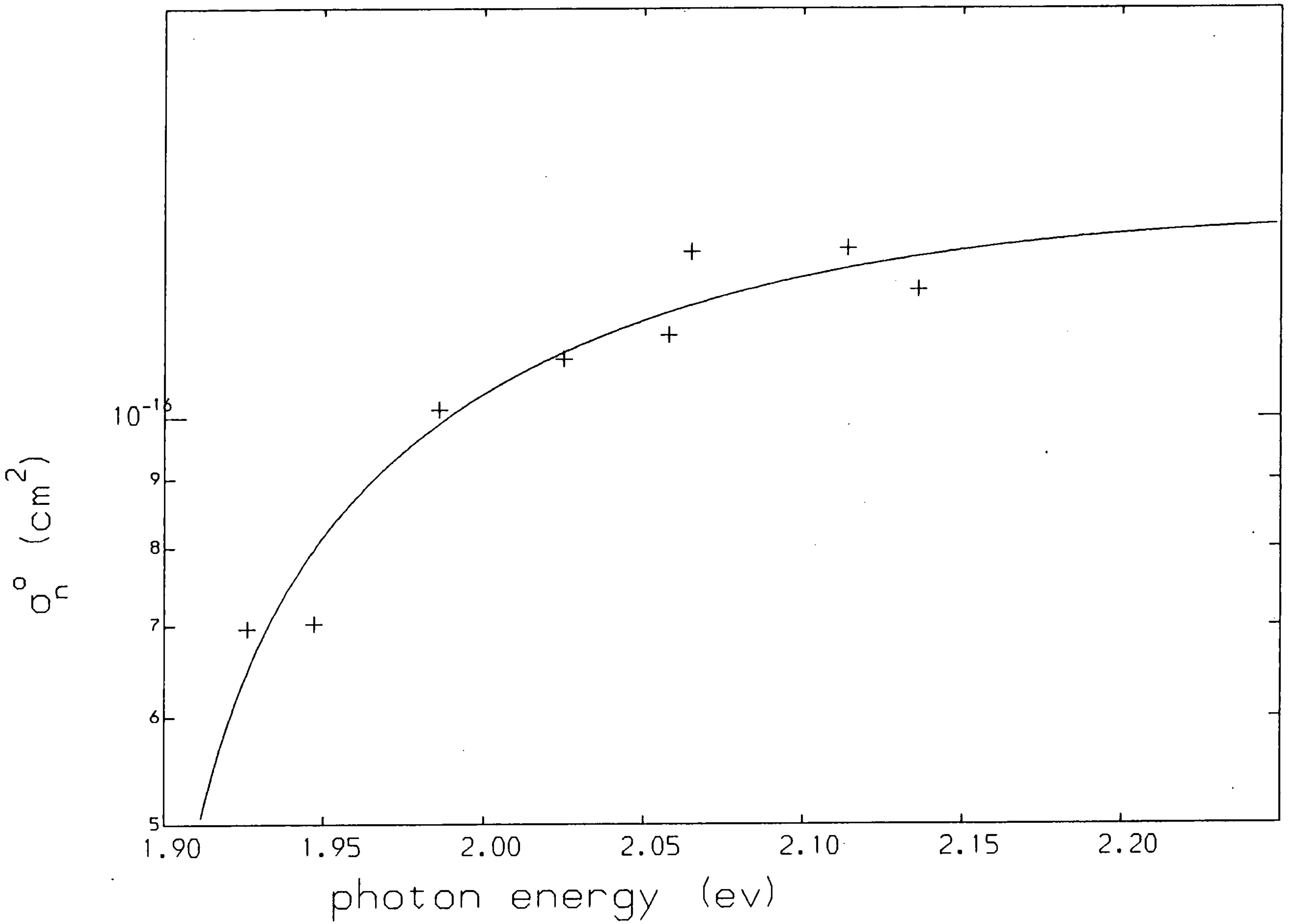


Figure 8.22 Theoretical (——) and experimental (++++) DLOS curves showing a threshold at 1.89eV

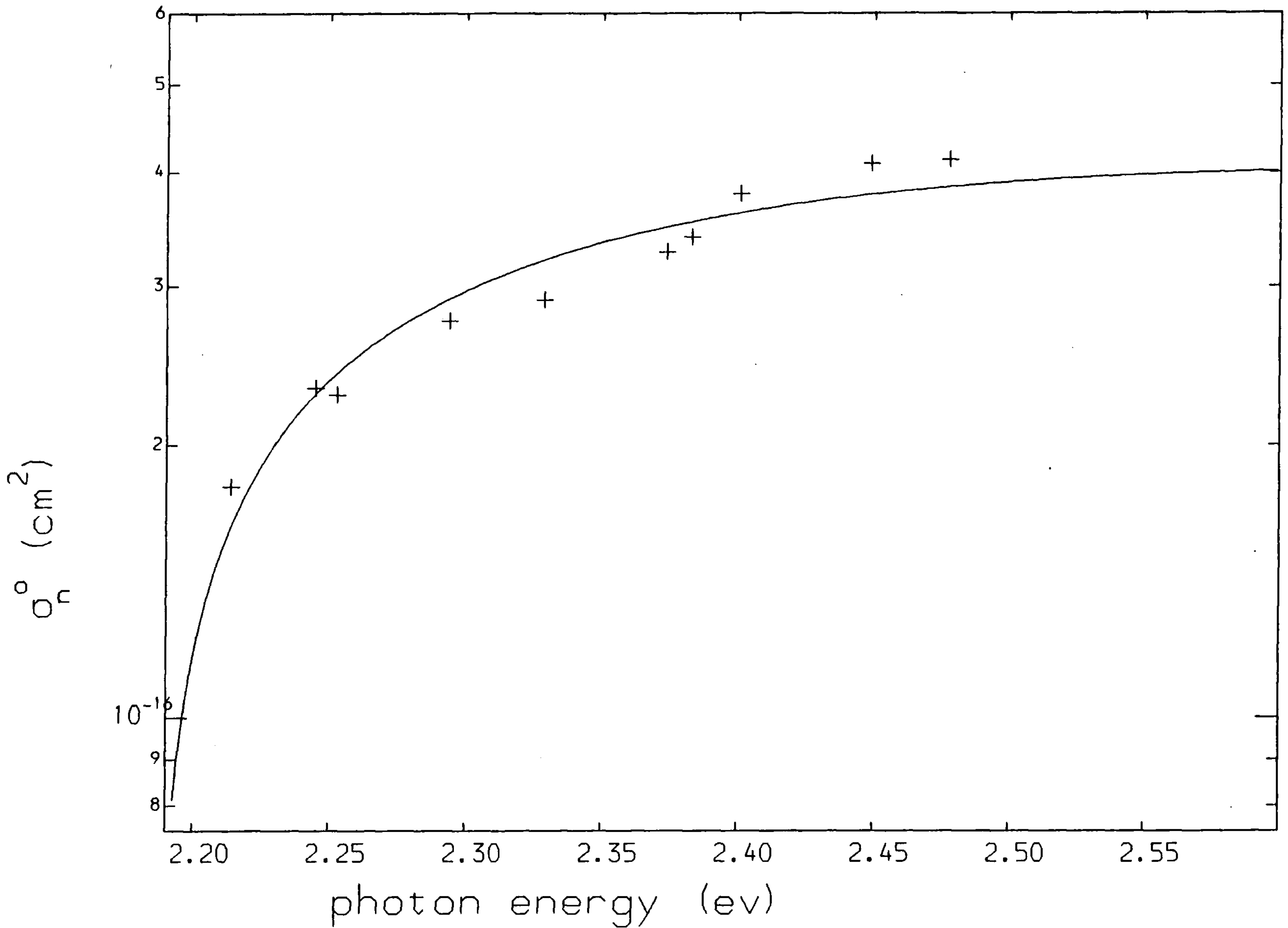


Figure 8.23 Theoretical (——) and experimental (++++) DLOS curves showing a threshold at 2.19eV

8.4.5 Discussion of Results

Much of the work presented on low resistivity ZnS has been based on photoluminescence measurements [58,59], with reference to the blue luminescence centres. The deep levels of interest are at least 1.1eV away from the band edges to give this luminescence band. This is outside the 'energy window' of DLTS and ODLTS. The data presented here indicate the presence of two previously unreported electron traps denoted EZ1 and EZ2 sited at 0.25eV and 0.5eV below the conduction band edge. The capture cross-sections suggest EZ1 is neutral and EZ2 is attracting (possibly with a single positive charge) [36]. DLTS gives no indication as to their identification; they may be due to native defects such as sulphur vacancies or zinc interstials, or to an impurity such as copper.

Copper is known to be a residual contaminant in ZnS, indeed, in the material studied here its concentration increases by an order of magnitude during growth to a few ppm [55]. The impurity centres compensate the shallow donor levels, thereby, reducing the resisitivity of the material. By doping with the group III impurities Thomas et al [58] suggested that they formed complexes with the copper so that the density of the compensating acceptor states were reduced. The types of impurity complexes are thought to be: (Cu^{+}_{Zn} - Al^{3+}_{Zn}), (Cu^{+}_{Zn} - Ga^{3+}_{Zn}); and in addition the group III's may complex with each other: (Ga^{+}_{Zn} - Al^{3+}_{Zn}). These centres are thought to give rise to a blue luminescence [58].

DLOS showed the presence of four deep traps at 1.49, 1.79, 2.31 and 2.43 eV above the valence band edge. As a result of their depth from the band edges these traps could not be observed in DLTS nor in ODLTS. Thomas et al [58] reported two defect states in similarly doped material using photoluminescence. These two blue luminescence bands had energies 2.588 and 2.522eV. The DLOS scan covered 0.7eV to 2.6eV below the conduction band and the results gave no indication of two levels with the same energies as those seen by Thomas et al [58]. Nor were two traps seen with these exact energies above the valence band. However, the levels at 2.43 and 2.31eV above the valence band may be the same as the centres seen by Thomas et al and the difference may be accounted for in a Stokes shift, that is, the optical depth of a centre from the conduction band plus its depth from the valence band is greater than the band gap; so emission and capture occur with the emission of lattice phonons (see section 2.4.4 in chapter 2). If this is the case then the centres observed by Thomas et al are deep donor levels and the luminesence bands arise from electron emission to shallow acceptor states. Thomas et al identified these centres as the impurity complexes mentioned above.

Taguchi and Yokagawa [59] in their studies on low resistivity, iodine doped ZnS have indicated that one of the blue luminescence bands occurs between a deep acceptor state (0.76eV) and a donor level at 0.22eV. The precise assignment of the transition was speculative but they have reported the 0.22eV level based on temperature dependent luminescent intensity. Allowing for the experimental error this may

correspond to EZ1. They reported a second donor level at 0.17eV but this was not observed in the DLTS spectrum.

8.5 Summary

DLTS and ODLTS have been used to characterise the deep electron and hole traps in n-CdTe, ZnS:Al,Ga, CdSe and CdSe:Cu and DLOS to probe deep into the wide band gap of ZnS:Al,Ga. All these materials showed the presence of deep trapping states.

DLTS on n-CdTe grown by the Piper-Polich technique has not previously been reported although many investigations have been carried out on material grown by other techniques. Six electron traps were observed, one of which was characteristic of only the Piper-Polich material. From ODLTS there was no indication of any deep acceptor states within the thermal window of the technique.

Low resistivity ZnS was obtained by doping with gallium and aluminium. This provided suitable material for using space charge techniques for the determination of its deep levels. Two deep donor levels were observed in DLTS one of which is thought to take part in the blue luminescence observed for this type of material. Again there was no indication of any hole traps within the thermal window of ODLTS. DLOS was used to probe further into the band gap than could be achieved by DLTS and ODLTS. These results showed the presence of four traps - two deep donor levels previously reported by Thomas et al [58] which give rise to blue

luminescence bands; and a further two, unreported levels which lie in the infrared energy range.

The defect levels in cadmium selenide have been thoroughly investigated using DLTS and ODLTS. These results show two sensitising centres one due to a native defect and the other due to a deep copper level, and a class I recombination centre. Several other defect states were characterised.

DLTS and ODLTS have proved invaluable techniques for the characterisation of deep levels in II-VI semiconductors. The work presented here is not intended to be a comprehensive study of all the deep level defect states that may exist in each of these materials. However, the results do extend the information available.

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CHAPTER 9

SUMMARY AND CONCLUSION

9.1 The Experimental Techniques

The work presented in this thesis has been concerned with the investigation of electrically and optically active deep level defect centres in some of the II-VI semiconductors. The importance of such a study stems from the behaviour of these defect states as, for example, recombination centres or trapping levels, which have a major effect on the properties of the material.

The principal techniques used were based on space charge, capacitance transient measurements, namely, deep level transient spectroscopy (DLTS), optical DLTS (ODLTS) and deep level optical spectroscopy (DLOS). The same basic instrumentation was used throughout these experiments. The capacitance transients were obtained by perturbing the steady state space charge capacitance with an electrical or optical pulse. The subsequent capacitance decay reflected the emission of trapped carriers from deep levels. The transient was digitised using a sampling DVM and data stored on floppy disc for later analysis. All the experiments were carried out under computer control.

DLTS and ODLTS gave information concerning the thermal

behaviour of the deep levels - activation energy, capture cross-section and density. The limitations were the time constants (minimum of ~4msec) and the temperature window (maximum range 80-450K) which controlled the energy range of the states that could be observed. DLOS gave the spectral dependence of the optical capture cross-section for electrons of a deep defect state. Thresholds in a DLOS spectrum corresponded to the optical depths of levels from the conduction band. Combining the information from these measurements gave the defect signature of the material under investigation.

9.2 Single Crystal CdS

Single crystal CdS has been shown to contain several dominant deep defect states. Four electron traps were characterised using DLTS with activation energies 0.29eV, 0.41eV, 0.61eV and 0.74eV below the conduction band; these were denoted E1-4. E1 and E2 were found consistently throughout the material studied. The density of E2 was shown to increase linearly with the free carrier concentration. Such a relation suggested that the level has its origin in associated native-impurity point defects formed during the growth of the material, as discussed in chapter 5.

The traps E3 and E4 were only observed in samples that had been annealed in Cd or S vapour. Using SEM and EBIC, these samples were shown to contain electrically active subgrain boundaries that extended to the surface. The dislocation density was about $10^{10}cm^{-2}$. The results

suggested that the states E3 and E4 were in some way connected with these extended defects.

An important property of E3 was that it decayed in the dark over a period of about 100hr and that the rate increased with temperature such that the level was not visible in DLTS after heating to 380K for 3hr in the dark. The thermal activation energy was found to be 0.25eV for the decay. Subsequently, the state could be reintroduced by illuminating the sample with a photon energy >1.1eV. If again the sample was maintained in the dark the level again decayed; this process of decay and photoinduction could be repeated indefinitely.

Copper is a substitutional impurity in CdS and produces two deep acceptor states that arise from a crytal field splitting of the Cu d^9 state. Using ODLTS and DLOS, these levels were found to be 0.35eV (excited state) and 1.1eV (ground state) above the valence band. The main conclusions from this study of undoped and copper doped CdS/Au Schottky devices and CdS/Cu_2S heterojunctions were: the states were present in unintentionally doped CdS, the copper being a residual impurity from the growth; and copper diffused into the CdS during the optimising heat treatment of the heterojunction.

Tellurium is an isoelectronic, substitutional impurity in CdS, occupying S sites in the lattice. It is one of the few isoelectronic elements that in low concentrations can introduce deep defect states in CdS and ZnS. Using DLTS,

ODLTS and DLOS the deep centres in Te doped CdS were investigated. In addition to the usual levels observed in CdS, a further centre was detected at 0.21eV above the valence band. Using photoluminescence, other workers have shown this defect state to be an important luminescence centre in CdS. It is thought to be an exciton, binding an electron with an energy of 0.2eV. The formation or annihilation of this exciton gives rise to the characteristic excitation and emission bands. It is also thought to behave as a recombination centre by capturing a free electron, thereby, giving an emission band.

9.3 Single Crystal (ZnCd)S

The defect states in $Zn_xCd_{1-x}S$ have been investigated using DLTS, ODLTS, DLOS and PHCAP. The study was essentially in three parts - the first of these was concerned with the effect of the introduction of Zn on the dominant electron trap E2 observed in CdS. DLTS showed the presence of a level similar to E2 but it shifted in energy as the Zn concentration was increased. The DLTS peaks were broader than that observed for E2 in CdS; this was thought to be due to a statistical distribution of Cd and Zn atoms around the defect site which would cause localised fluctuations in the band gap. The change of activation energy with band gap indicated that the level was probably pinned to the valence band. Consequently, a relationship similar to the compostion dependence of the band gap was obtained, this was found to be

$$E(x) = 0.41 + 0.68x + 2.98x^2 \qquad 9.1$$

so that the activation energy could be determined for any composition. This gave an emission rate equation

$$e_n(x) = N_c V_{th}\ \sigma_n\ \exp[-(0.41+0.68x+2.98x^2)/kT] \qquad 9.2$$

showing that for a given temperature the emission rate decreases with increasing x.

The second part of the investigation examined the effect of composition on the copper levels H1 (0.35eV) and H2 (1.1eV) observed in CdS. Using ODLTS and DLOS it was found that the activation energies were independent of composition. A further point stemmed from the fact that these two levels arose from the crystal field splitting of the Cu d^9 state giving a ground state (1.1eV) and an excited state (0.35eV). The degree of splitting was also found to independent of composition. The reason for these two observations was explained in terms of the symmetry of the defect site. Assuming that the defect was a substitutional impurity, then it was surrounded by 4 S nearest neighbours. These effectively shielded the copper from the compositional change so that the symmetry of the defect site would be little changed. In addition, there would be a negligible perturbation on the bonding of copper with its nearest neighbours. Consequently, the defect levels would be little affected by the change of composition.

The final part of this investigation looked at the deep levels induced during the optimising heat treatment of the $Zn_xCd_{1-x}S/Cu_2S$ solar cell. It is widely accepted that for a

composition of about x=0.2 the ternary compound gives a better lattice and electron affinity match to Cu_2S than does CdS. In principle this should improve the open circuit voltage and short circuit current, thereby, giving a solar cell with a higher efficiency. However, the current collection has been found to decrease and so, there has been no significant improvement. One of the contributory factors was thought to be deep recombination centres in $Zn_xCd_{1-x}S$. Using DLOS and PHCAP, a deep level at about 1.2eV below the conduction band was detected. It appeared to be an artefact of the processing of this heterojunction since it was not observed in CdS/Au, $Zn_xCd_{1-x}S$/Au Scottky devices nor in the CdS/Cu_2S solar cell. It was considered to be a recombination centre which could reduce the current collection efficiency during the operation of the solar cell.

9.4 Polycrystalline CdS Films

The advantage that CdS has over most other semiconducting materials is that it can be deposited over a wide area using low technology with little material wastage. Consequently, it has found a potential use as a solar cell material in such devices as CdS/Cu_2S and CdS/CdTe. The techniques used for CdS deposition in this investigation were silk screen printing and evaporation. The primary concern was the deep level defect states in the material that could be detrimental to the operation of any subsequent device.

The silk screen printing process required an annealing procedure to convert the powdery film into a polycrystalline

film. A $CdCl_2$ flux was incorporated in the CdS in order to reduce the required sintering temperature. The films were investigated using SEM and RHEED so that structural information could be fed back into the film processing to obtain better layers. CdS/Au and CdS/Cu_2S devices were prepared on these films for electrical measurements (current-voltage and capacitance-voltage) and for DLTS and ODLTS to determine the deep levels in these films.

It was found that the defect signature of the CdS layer was sensitive to the device processing as was shown by the DLTS results on the Schottky devices. After annealing at 640C for 1hr, 2 electron traps were observed at 0.16eV and 0.48eV below the conduction band. After an anneal at 670-700C these traps were found to disappear and a level at 0.13eV was detected. For the heterojunction prepared on CdS annealed at 670C, two further defect levels were observed in addition to the 0.13eV level. One of these could not be resolved; the other had an activation energy of 1.1eV. These results showed the significant effect that the processing of CdS has on the defect signature of the material and emphasises the difficulty of their control.

The dominant electron trapping centres in evaporated CdS were investigated using DLTS. The presence or absence of defect states in this material was shown to be dependent upon the type of substrate used. For this study, CdS was evaporated onto SnO_x or Ag coated glass giving oriented CdS grains and layers about 20μ thick. DLTS scans for films on Ag showed the presence of 3 electron traps at 0.48eV, 0.98eV

and the third, poorly resolved. The latter unresolved trap was also detected in CdS on SnO_x, whereas, the 0.48eV and 0.98eV centres were not. This showed that the defect signature was influenced by the type of substrate and that the two levels at 0.48eV and 0.98eV were associated with Ag impurity.

The incorporation of Ag into the CdS film is thought to inhibit the indiffusion of copper during the optimising heat treatment of the CdS/Cu_2S solar cell. This maintains the stoichiometry of the Cu_2S layer during the lifetime of the device and so, using Ag has solved the problems of degradation and reproducibility which were encoutered with other substrates.

9.5 Single Crystal CdSe, CdTe, ZnS

Apart from those materials mentioned above several other II-VI compounds were investigated, namely, CdSe, CdTe and ZnS. These semiconductors have several potential applications that can be affected by crystalline imperfections. In an effort to discover which defects were present, DLTS and ODLTS were used to characterise the electron and hole trapping centres in these compounds, and DLOS was used to probe deep into the wide band gap of ZnS to detect states not accessible by the other techniques.

From DLTS and ODLTS, undoped and copper doped CdSe showed the presence of several defect states. Two sensitising centres were observed: a level at 0.64eV above

the valence was detected in both doped and undoped material and was thought to be due to a native defect; the other at 0.95eV above the valence band which had a cross-section ratio $\sigma(p)/\sigma(n)=10^4$, was only detectd in copper doped CdSe thus identifying its origin in a copper associated defect. A level at 0.9eV below the conduction band was found to have a cross-section ratio $\sigma(p)/\sigma(n)=1$ indicating it behaves as a class I recombination centre. This defect state was observed in both doped and undoped CdSe suggesting it originated from a native defect. Several other centres were characterised using DLTS and ODLTS - a level at 0.22eV above the valence band found in the doped material only, and thought to be a copper impurity centre; an electron trap at 0.45eV which was common to undoped and doped CdSe; and a level at 0.16eV below the conduction band in undoped CdSe only.

The defect states in n-type CdTe grown by the Piper-Polich technique were investigated using DLTS. Six deep electron traps were observed and these results were compared with those obtained by other workers using CdTe grown by alternative methods. Five of these levels (0.21eV, 0.40eV, 0.47eV, 0.53eV, 0.63eV) have been characterised by others but not all in the same material. The remaining level at 0.15eV was not previously reported. The important conclusion was that the defect signature for CdTe was very much dependent upon the growth technique, growth conditions and post-growth annealing treatments.

Low resistivity ZnS obtained by doping with gallium and aluminium was investigated using DLTS, ODLTS and DLOS. DLTS

showed two electron trapping centres at 0.25eV and 0.50eV. In iodine doped ZnS, the 0.25eV level is thought to emit its carrier into an iodine associated state at 0.76eV above the valence band giving a blue luminescence band. There are no previous reports of the 0.50eV level. ODLTS gave no indication of deep hole traps. The DLOS spectrum at room temperature had 4 thresholds at 1.25eV, 1.37eV, 1.89eV and 2.19eV below the conduction band. The first two are thought to give rise to blue luminescence bands and have been identified as possible complex centres such as (Cu^{+}_{Zn}-Al^{3+}_{Zn}), (Cu^{+}_{Zn}-Ga^{3+}_{Zn}) or (Ga^{+}_{Zn}-Al^{3+}_{Zn}). The remaining levels at 1.89eV and 2.19eV have not been reported previously.

9.6 Conclusion

Space charge, capacitance transient measurements, namely DLTS, ODLTS and DLOS, have proved useful for the investigation of deep level defect states in II-VI semiconductors. DLTS and ODLTS are thermal scanning techniques that provided the thermal activation energy and capture cross-section for a particular defect state. An electrical DLOS spectrum gives the photon energy dependence of the optical capture cross-section for electrons for a trapping centre. Combining this information provided the defect signature for the material under investigation. The main drawback is that they are unable to identify, with certainty, the origin of a particular defect state. It would be useful to correlate other techniques such as EPR and ODMR with those used in this work to gain a more complete picture of the behaviour of deep defect states.