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THE DESIGN AND CONSTRUCTION OF A  
SWITCHING VOLTAGE REGULATOR

A.S.WAHAB

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for the degree of Master of Science, in the  
University of Durham



13. APR. 1984

To my Parents, with very much love

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## ABSTRACT

The work presented in this thesis is concerned with a method of converting DC Voltage to another higher DC Voltage. The circuit used VMOS switches in a "flying capacitor" technique to generate regulated 6V from single cell of about 1.5 V .

The computer simulation gave efficiencies of 80.3% and 62% at 2 and 27 mA respectively with peak to peak ripple about 5% when the output capacitor equal to 10 or 20  $\mu\text{F}$  and these results were confirmed by the experimental measurements.

## ACKNOWLEDGEMENTS

I would like to take this opportunity to thank my supervisor, Dr. B.J. Stanier, for his helpfulness and guidance throughout both my work and preparation of this thesis.

## INTRODUCTION

The series pass element in a conventional series regulator operates as a variable resistance which drops an unregulated input voltage down to a fixed output voltage. This element, usually a transistor, must be able to absorb the voltage difference between the input and output at the load current. The power generated can become excessive, particularly when the input voltage is not well regulated and the difference between the input and output voltages is large.

Switching regulators, on the other hand, are capable of high efficiency operation even with large differences between the input and output voltages. The efficiency is, in fact, negligibly affected by the voltage difference since this type of regulator acts as a continuously-variable power converter. Switching regulators are, therefore, useful in battery-power equipment. They are frequently the most economical solution in commercial and industrial applications where the increased efficiency reduces the cost of the series pass transistors and simplifies heat sinking.

One of the disadvantages of switching regulators is that they are more complex than linear regulators, but this is often a substitution of electrical complexity for the thermal and mechanical complexity of high power linear regulators. Another disadvantage is higher output ripple.

Most switching regulators share the property of storing energy in an inductor then releasing it into a filter capacitor and load.

This thesis is concerned with an experimental technique designated the flying-capacitors technique. It uses VMOS switches to generate a regulated output voltage, nominally 6 V, from an



unregulated voltage of about 1.5 V .

Chapter one is concerned with the principle of operation of the series and the switching regulator and also mentions some commercial switching regulator IC circuits. The using of power field-effect transistors (VMOS) as switches is explained in chapter two.

The third chapter deals with computer simulation of the circuit using the Princeton Circuit Analysis Program (PCAP). In chapter five the experimental results are presented and compared with the computer results. General conclusions follow at the end of the thesis.

## 1.1 Introduction

A dc power supply is usually regulated by some type of feedback circuit that senses any change in the dc output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

This chapter will demonstrate the principle of operation of the series and the switching regulator circuits. The last part considers some commercial switching regulator circuits that are now available.

## 1.2 Regulated power supplies

An ideal regulated power supply is an electronic circuit design to provide a predetermined dc voltage  $V_o$  which is independent of the current  $I_L$  drawn from  $V_o$ , of the temperature and also of any variation in the ac line voltage.

Fortunately it is easy to construct a stable power supply by some type of feedback circuit that senses any change in the dc output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

In Figure (1.1), the output voltage is sampled and a high-gain differential amplifier compares a portion of this voltage with a reference voltage. The output of the amplifier is then used to modulate the control element.

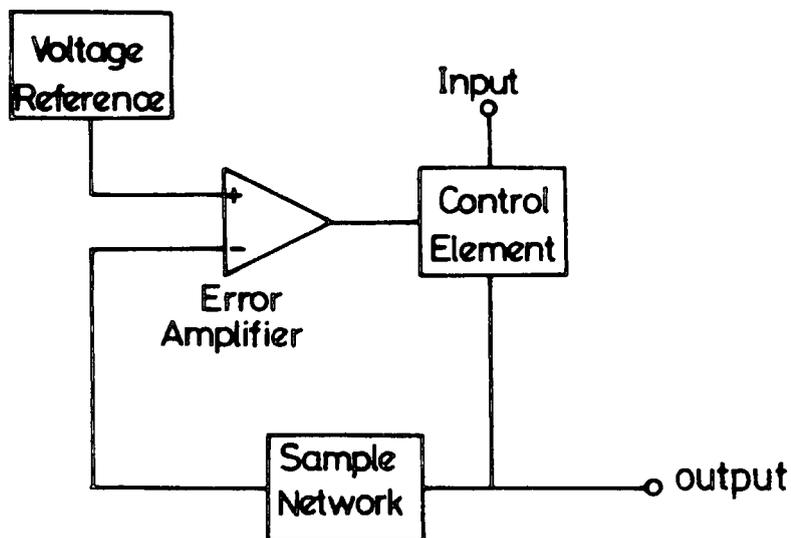


FIG. 1-1 Block diagram of linear system.

In Figure (1.2) if we assume that the voltage gain of the error amplifier and the control element ( $Q_1$ ), is  $A_V$ ; then

$$V_O = A_V V_i = A_V (V_{REF} - \beta V_O) \quad \dots\dots\dots (1-1)$$

where the feedback is

$$\beta = \frac{R_2}{R_1 + R_2} \quad \dots\dots\dots (1-2)$$

From equation (1-1) it follows that

$$V_O = V_{REF} \frac{A_V}{1 + \beta A_V} \quad \dots\dots\dots (1-3)$$

The output voltage  $V_O$  can be changed by varying the feedback factor ( $\beta$ ).

The emitter follower  $Q_1$  is used to provide current gain because the current delivered by the error amplifier usually is not sufficient.

Also the control element  $Q_1$  must absorb the difference between the unregulated input voltage  $V_{IN}$  and the regulated output voltage  $V_O$ .

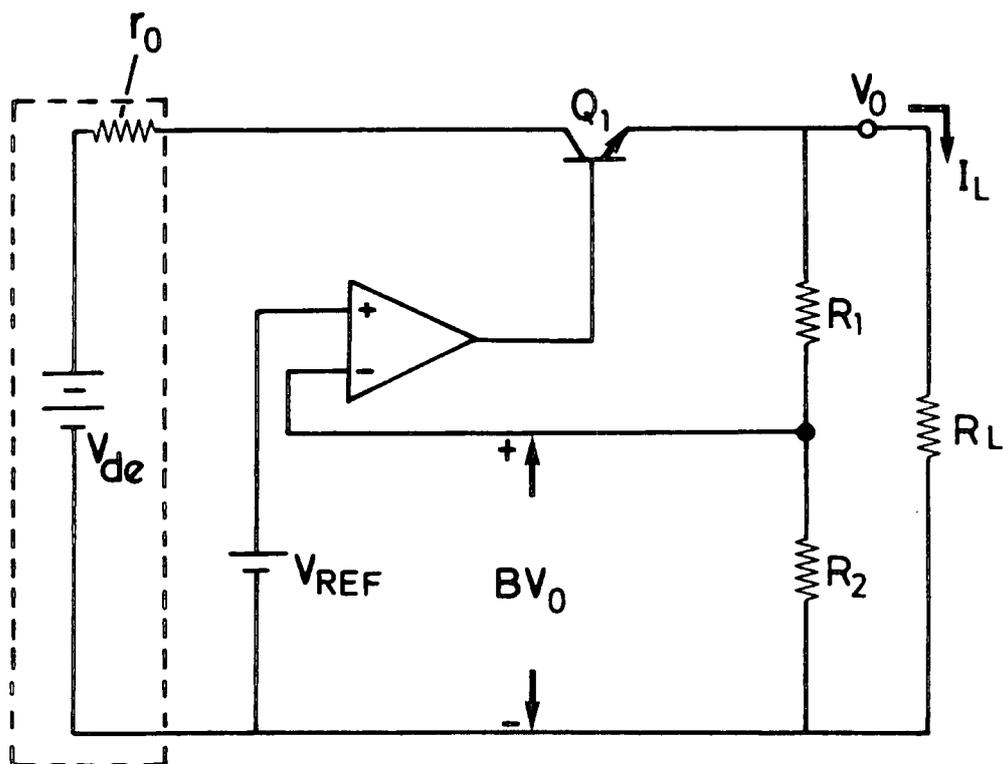


FIG.1-2. Circuit diagram of linear regulator.

This kind of regulator is called a linear regulator or (series regulator) since the control element is operated in the linear region. Linear regulators provide excellent regulation and reduction of ripple factor and so are widely used but they have three drawbacks.

- 1) They are relatively inefficient in that the control element (the pass transistor  $Q_1$ ) is operated in the active region and must pass the full current taken by the load.
- 2) The input-voltage magnitude must be greater than the output voltage magnitude. The greater the input-out differential for a given current, the greater the losses.
- 3) In the linear regulator the input and the output voltage have to be the same polarity.

All these difficulties can be avoided by using a switching regulator (sometimes called a periodic energy-transfer regulator), in which the control element (pass transistor) is operated only at cut-off or

at saturation. Cut-off and saturation modes are efficient modes of operation. In the cut-off mode, there is a large voltage across the transistor but little current through it, in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, most of the input power is transferred to the output, and the efficiency is high.

Most switching regulators share the property of storing energy in an inductor, then releasing it into a filter capacitor and load. In a switching regulator whose output is at a lower voltage than the unregulated input, the current drawn from the unregulated supply may be less than the output current delivered to the load. In fact, the unregulated supply voltage can be much larger than the regulated output voltage. For example consider a regulator provides +5 volts and up to 5 amps from an unregulated source of 25 volts. A conventional linear regulator will dissipate 100 watts and will require 5 amp input current. A switching regulator requires less than 2 amps input current. To put it in other terms, the linear regulator is 20% efficient where the switching regulator is about 70% efficient.

This makes the whole electronic system easier to keep cool, reduces the running cost of the system in terms of the cost of electricity and may simplify the system design to the level where it no longer needs to be fan-cooled.

With switching regulators we can generate output voltage greater than the unregulated input voltage, and it is even possible to generate output of polarity opposite to that of the unregulated input.

Regulation is achieved by controlling the duty cycle that controls the average current transfer to the load.

$$V_{\text{out}} = V_{\text{in}} \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = V_{\text{in}} \frac{t_{\text{on}}}{T} \quad \dots\dots\dots (1-4)$$

If  $V_{in}$  increases, the control circuit will cause a corresponding reduction in the duty cycle and thereby maintain a constant  $V_{out}$  and vice versa.

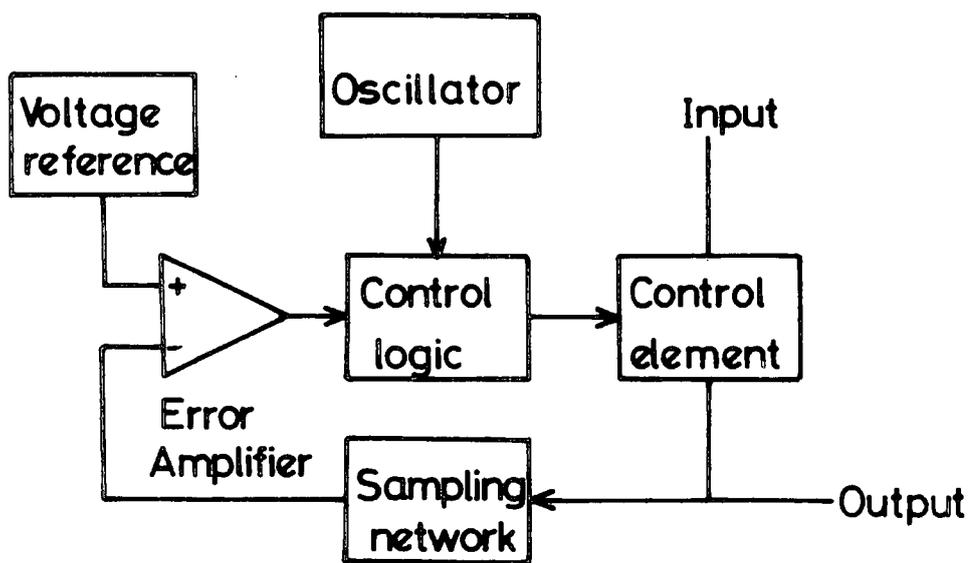


FIG. 1-3 Block diagram of switching regulator.

### 1.3 Consideration of some practical switching regulator I.C.S circuits

As we mentioned in the past, the simple series regulator circuit suffers from the disadvantages that its output voltage can never be greater than the input and must be of the same polarity. These and other problems can be avoided by using a switching regulator circuit. This section considers some commercial integrated circuits that are now available.

The TL497A 14-pin I-C device contains most of the components on its chip which are required to make a switching regulator of any of three basic types : step-down, step-up and inverter. The maximum permissible output current is 500 mA, although higher output currents can be obtained by using the device to control an external power

transistor. The only difference between the TL497 and the more recent TL497A is that the latter has a Schottky diode rather than a conventional diode to provide faster and more efficient switching.

The chip contains an internal 1.22 V precision reference voltage source which provides one input to a comparator. The other input to the comparator is provided by a fraction of the voltage from the output of the circuit. The output from the comparator varies according to which of these comparator input voltages is the greater and the comparator output is used to switch the internal transistor of the device which functions as the transistor in a basic regulator circuit.

The switching transistor is turned ON during the charging portion and turned OFF during the discharge portion and any subsequent standby period after the charge/discharge cycle of the timing capacitor  $c_t$ . The ON time therefore is always constant. The frequency and OFF time varying according to load requirement.

The absolute maximum input voltage of 15 V to the TL497A should never be exceeded or the device may be damaged, indeed it is wise to limit the input voltage to about 13 V to allow a margin of safety. The absolute maximum permissible output voltage is 35 V, but a limit of 30 V is probably wise.

The output voltage is programmed by the resistor  $R_1$  and  $R_2$  in accordance with  $V_{out} = (1 + R_1/R_2) \times 1.22 \text{ v}$

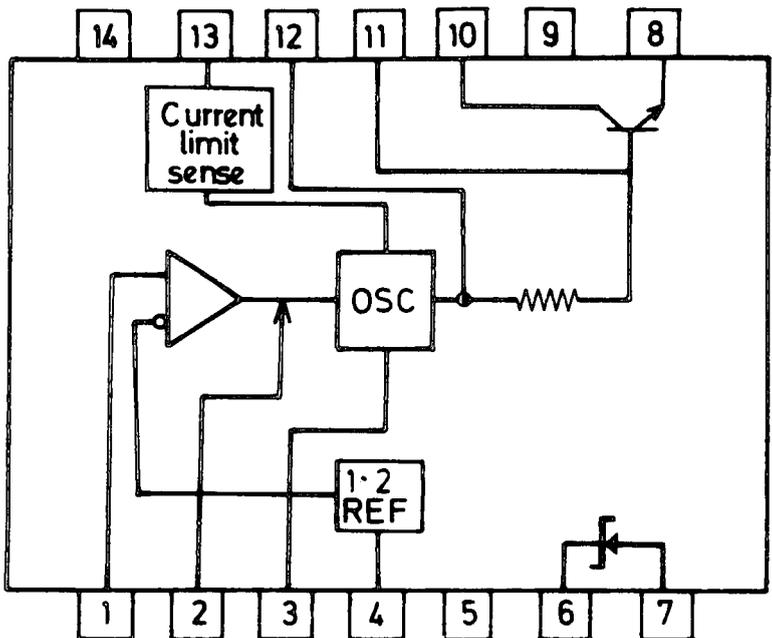


FIG.1 -4. Block diagram of the TL 497A

The  $\mu$ A78S40 device can perform the same functions as the TL 497A but there are important differences between the two devices. The  $\mu$ A 78S40 can provide output currents of up to 1.5A without the use of external transistors whereas the TL 497A device is limited to 0.5 maximum, although like the TL 497A an external transistor can be added when more current is required. The  $\mu$ A 78S40 can operate from a lower standby current (typically 2.3 mA) than the TL 497A (typically 6 mA).

A further advantage of the  $\mu$ A 78S40 device is the wider operating voltage range of 2.5 V to 40 V at the input as opposed to the 4.5 V to 15 V of the TL 497A. The absolute maximum output voltage of the  $\mu$ A 78S40 is quoted as 40 V which is a little higher than 35 V quoted for the TL 497A.

The internal reference voltage source 1.3 V for the  $\mu$ A 78S40 and 1.22 V for the TL 497A. Since this voltage source is used as

one input to a comparator against which a fraction of the output voltage is compared, so the output voltage

$$V_{\text{out}} = (1 + R_1/R_2) \times 1.3 \quad \text{v}$$

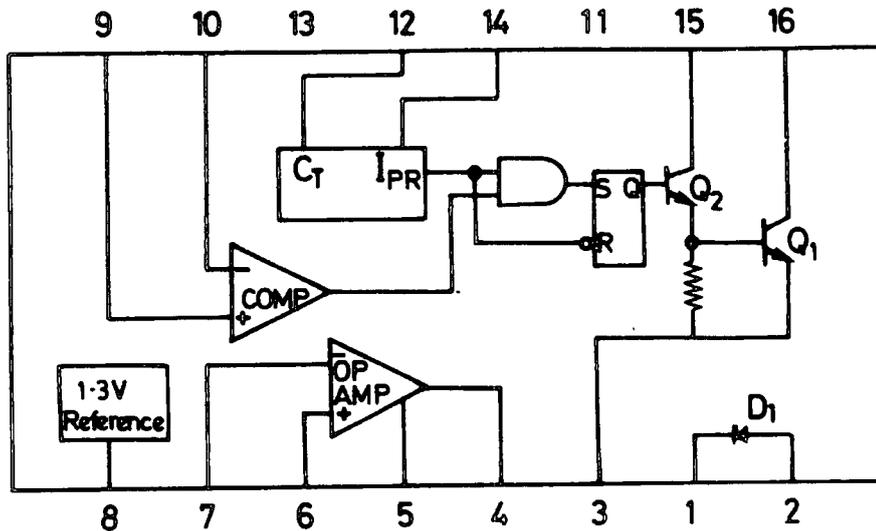


FIG.1-5. Block diagram of the 78S40

The SH1605 offers a way of constructing very simple switching regulator circuits providing output of up to 5 A without the use of any other active device. The output voltage can be adjusted over the range 3 V to 30 V, but the SH1605 has been designed for step-down switching regulator circuit only. It is manufactured in a TO-3 type of metal package with 8 pins. This case must be bolted to a suitable heat sink. The device can provide power efficiencies of about 70 percent. The variation of the output voltage over the output current range and over the input voltage is about 50 mv.

The SH1605 is not a monolithic circuit, but a hybrid device containing more than one chip. This inevitably means it carries a higher price tag than a typical monolithic device, but it does offer a very convenient way of making a very simple, high output current switching regulator circuit.

The TL496 is a device containing not only a switching regulator, but also a series regulator in a miniature 8-pin d.i.l package. It has been specifically designed for operation from one or two cells of about 1.5 V each with or without mains power. It is especially suitable for applications such as calculators and toys which required about 9 V at a current of up to about 80 mA and which are more conveniently operated from single cell or two cells than from a 9 V battery.

The switching regulator circuit is used to convert the battery voltage up to a value of about 8.5 V (depend on the circuit), whereas the series regulator is used only with a mains input to provide a regulated output of about 9 or 10 V.

If a two cell circuit is to be employed, the total input voltage should be between 2.3 and 3.0 V and if one cell is used, the voltage should be in the range 1.1 to 1.5 V.

Optimum efficiency is obtained with an inductor of about 40  $\mu\text{H}$  to 50  $\mu\text{H}$ , but it should have a low dc resistance (less than  $0.15\Omega$ ) to obtain high conversion efficiency in the battery powered mode. The single cell circuit will provide an output of about 40 mA at 7.2 V, whereas the two cell circuit will provide about 80 mA at 8.6 V.

Efficiency of up to about 56 percent were measured <sup>5</sup> with two-cell operation, but naturally the current taken from the cells is considerably greater than the output current owing to the higher output voltage.

The silicon general SG3524 is similar to 1524, 2524 and 3524 devices available from various manufacturers under type numbers such as SG1524 (RCA), LM1524 (National Semiconductor), etc. These devices have been designed for use in pulse width modulated circuits in which the switching frequency is held constant while the duty cycle is varied. It is claimed that this type of circuitry allows greater design flexibility

in the selection of components than in frequency modulated regulators such as the TL497 where the frequency changes during circuit operation. However this flexibility tends to be obtained at the expense of circuit complexity.

The ICL 7660 contains all the necessary circuitry to complete a dc voltage conversion. It uses MOS switches in a "flying capacitor" technique to generate a negative dc output voltage equal in magnitude to the positive supply. It operates from 1.5 V to 10 V. It is ideally suited for providing low current. This convenient chip comes in an 8 pins package and requires just two external components (capacitors). By stacking several ICL 7660 we can generate a negative output voltage equal to a multiple of the supply voltage.

## 2.1 Field-Effect Transistors

Field-effect transistors (FETs) are transistors with properties quite different from bipolar transistors. FETs work by controlling a current with an electric field produced by an applied voltage rather than with a base current. The result is that the control electrode (the gate) draws virtually no current, except for leakage. The resulting high input impedance (which can be greater than  $10^{14}\Omega$ ) is essential in many applications, and in any case, it makes circuit design simple.

## 2.2 FET-characteristics

There are two fundamental varieties of FETs namely

1. Junction FET (JFET)
2. Metal-oxide semiconductor FET (MOSFET)

### JFET

The JFET is a conducting semiconductor bar, with the ends labelled drain (D) and source (S). A gate region is diffused between drain and source. A voltage applied to the gate controls the conductivity of the bar, or "channel". FET are nearly symmetrical, but the gate-drain capacitance is designed to be less than the gate source capacitance, for instance thus making the drain the preferred output terminal.

### MOSFET

In the JFET the gate forms a diode junction with the drain-source channel, this limits the performance because there is leakage current (as much as a nanoampere or so at ordinary temperatures and considerably more at large drain voltages), and if the gate becomes forward-biased with respect to either source or drain, regular diode conduction occurs, with drastic reduction of the input impedance. In the MOSFET, the gate region is separated from the conducting channel by a thin layer of  $\text{SiO}_2$

(glass) grown onto the channel. The gate is truly insulated from the source-drain circuit (input resistance  $\sim 10^{14}\Omega$ ), and it affects the source-drain current only by its electric field. With MOSFETs the gate can go either polarity relative to the source without gate current flowing, since it is electrically insulated from the source-drain circuit. This often simplifies circuit design. It also allows the construction of two varieties of MOSFET, the depletion and enhancement types.

Depletion-mode MOSFETs conduct with the gate tied to the source (or forward-biased) and are cut-off with the gate back biased a few volts (just like JFETs). Enhancement-mode MOSFET are cut off with the gate tied to the source (or back-biased) and conduct only when the gate is forward biased.

### 2.3 The FET as a switch

Figure (2.1) shows the region of the FET characteristic curves for small drain source voltage. The  $I_D$  versus  $V_{DS}$  curves are approximately straight lines for  $V_{DS}$  smaller than  $V_{GS} - V_T$ , where ( $V_T$ ) is the threshold voltage and sometimes given as the gate-source voltage corresponding to drain current of  $10\ \mu\text{A}$ . The curves pass through the origin and extend into both positive and negative quadrants. These properties make FET quite suitable for switching applications. The FET as a switch is shown in Figure (2.2). To turn the FET ON the gate has to be positive and to turn OFF the gate should be made negative.

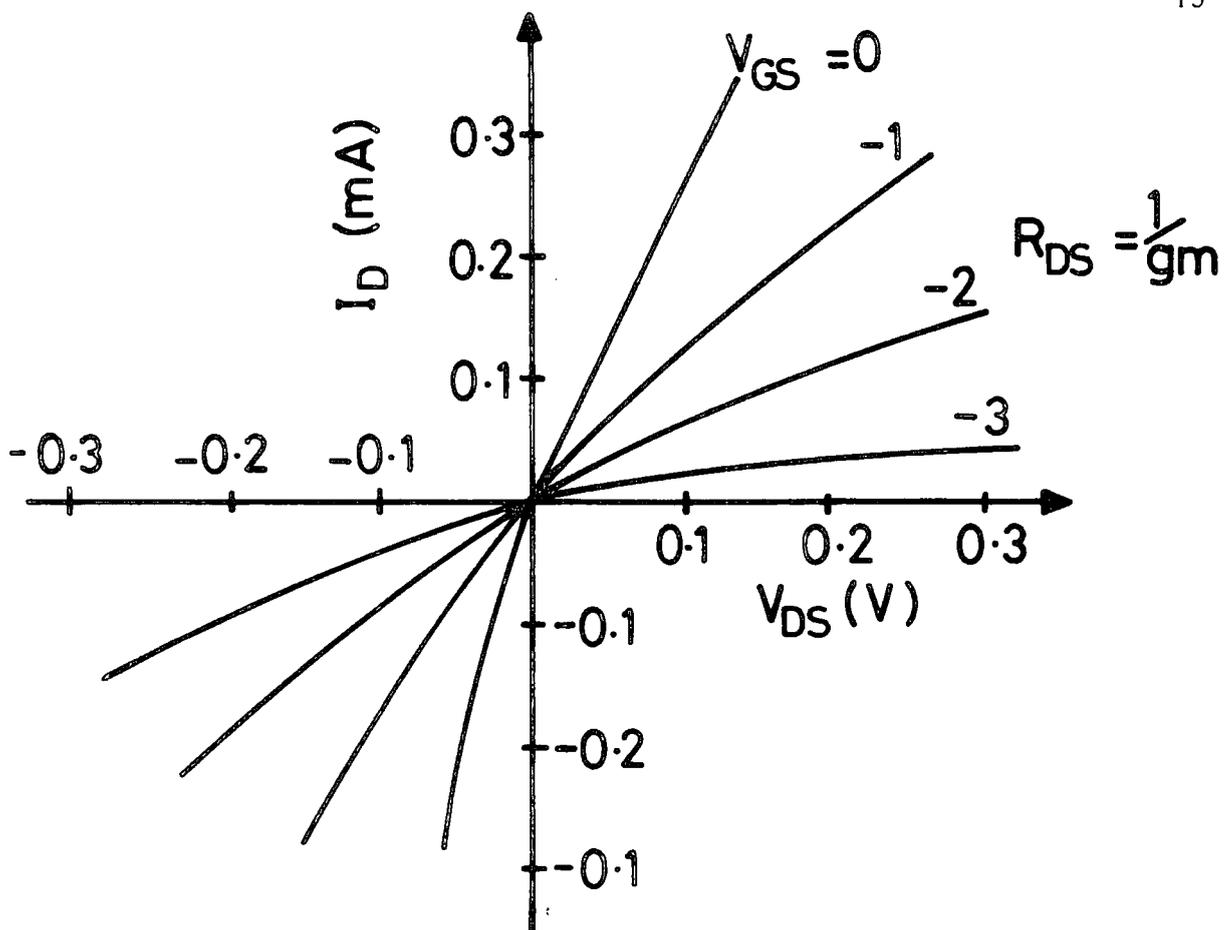


FIG. 2-1

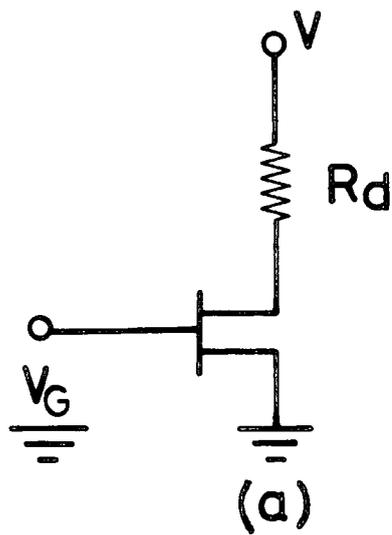
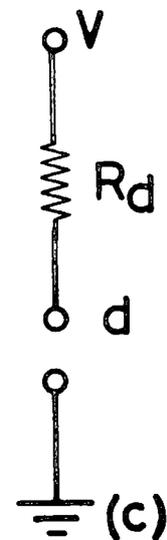
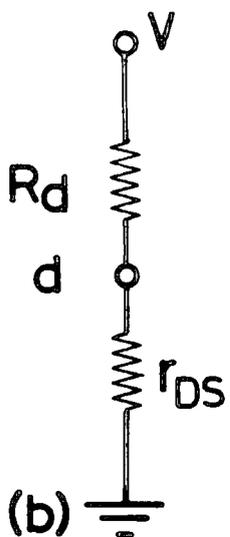


FIG. 2-2 Operation of the FET as a switch.



## 2.4 Power Field-Effect Transistor (VMOS)

The VMOS is a new type of enhancement MOSFET, fabricated so that the current flows vertically. Hence this transistor is designated VMOS. This construction distinguishes the VMOS from the low-power MOSFET, where the carriers flow horizontally from source to drain. Among the advantages of VMOS are -

1. Thermal runaway is not possible because the current becomes limited as the device heats up (no hot spots develop and secondary breakdown does not occur).
2. The ON resistance is very low and has a positive temperature coefficient. This makes it easy to parallel MOSFETs. Additionally, paralleling MOSFETs result in reduction of effective ON-resistance.
3. Being voltage-controlled, FETs offer very high input impedance, so they require very low drive current. This can greatly simplify the circuitry needed to control them.
4. Power FETs have extremely low noise figures.
5. The VMOS breakdown voltage between drain and source is high.
6. Being majority carrier devices FETs do not have minority-carrier delay time. Consequently bandwidths and switching times are 10 to 100 times faster than bipolar transistor of comparable size.
7. The temperature stability of MOSFET electrical parameters is generally superior to that of similar bipolar device.

## 2.5 The reasons for using VMOS transistors in the dc-to-dc convertor

In theory a dc-to-dc convertor can approach 100% efficiency if certain conditions are met.

1. The drive circuit consumes minimal power.
2. The switches have extremely low ON resistance and very high OFF resistance.
3. The equivalent series resistance of the capacitor is very low and the parallel leakage resistance is very high.

The ON resistance of VMOS transistors is very low, the OFF resistance is very high and VMOS transistors are also very fast. They are therefore nearly ideal switches and suitable for this application.

### 3.1 Introduction

Nearly all electronic circuits, from simple transistor and op-amp circuits up to elaborate digital and microprocessor systems require one or more sources of stable dc voltage. Batteries with a flat discharge curve are the most desirable but also the most expensive.

This chapter is concerned with the design of a converter of DC voltage to another higher DC voltage without the use of an inductor.

### 3.2 General Description

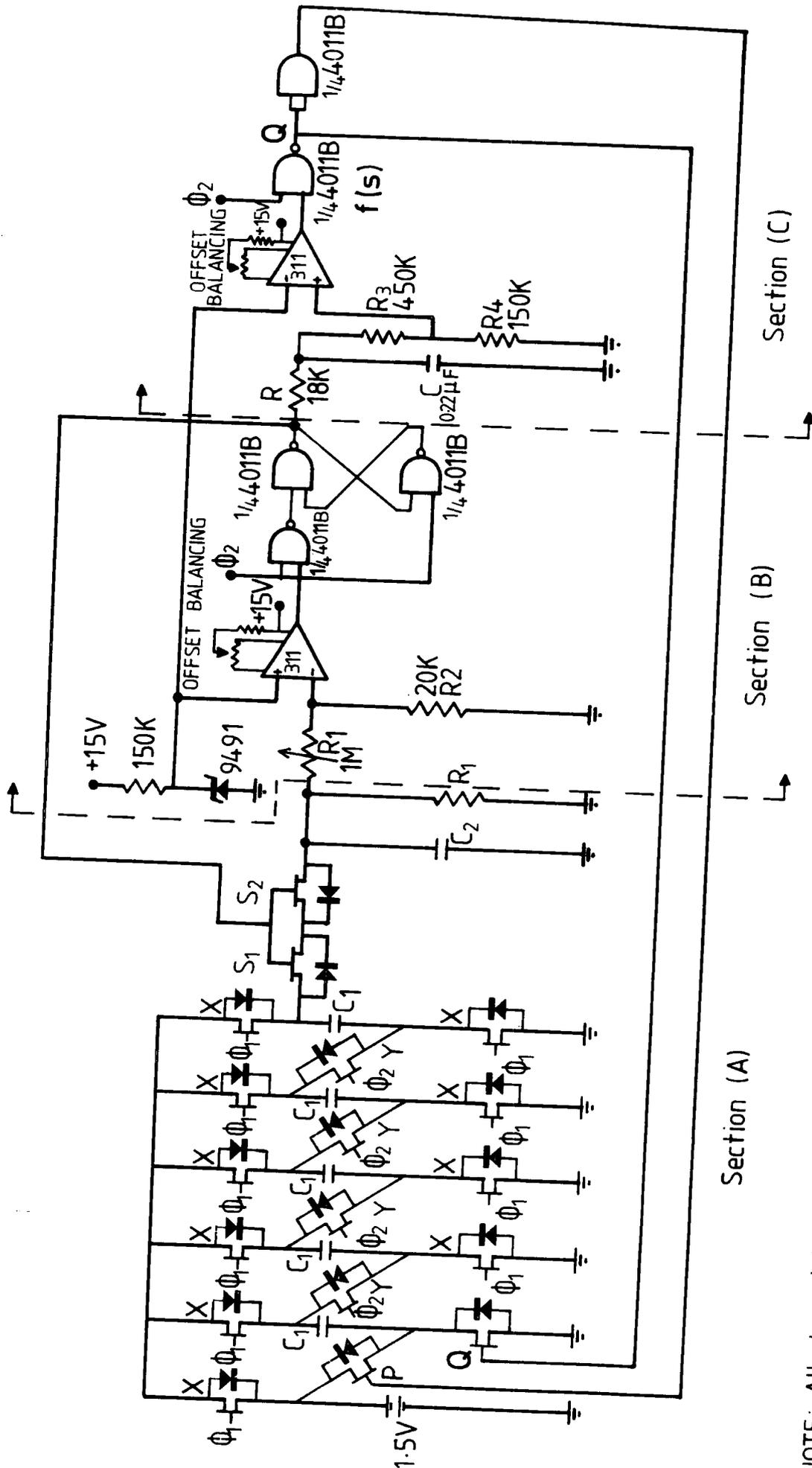
The operation of the circuit in Figure (3.1) is divided to three sections. In section(A), for half cycle of operation the capacitors ( $C_1$ ) are placed in a parallel position and each capacitor ( $C_1$ ) is charged to the battery voltage of about 1.5 V. During the second half cycle of operation the capacitors ( $C_1$ ) are connected in series and at the same time they are connected via the two switches  $S_1$  and  $S_2$  to charge ( $C_2$ ) to 6 V.

In section (B), the 1.22 V reference voltage source is compared with a fraction of output voltage of the circuit. The output from the comparator indicates which of these voltages is the greater and its output is used to modulate the ON time of  $S_1$  and  $S_2$  by an RS flip-flop.

In section (C), an R-C circuit is used to average the Q-output voltage of the RS flip-flop and is compared with the same 1.22 V reference. The output of the comparator is then used to connect the battery voltage in series with the capacitors ( $C_1$ ) if the voltage on the capacitors ( $C_1$ ) alone are not enough to maintain the output voltage at 6 V.

### 3.3 Circuit Design

In section (A) of Figure (3.1), all the switches are N-channel VMOS transistors. The diode across the drain-source is an internal



NOTE: All transistors are VMOS 1VN 5000 ANE

FIG (3-1)

diode. When the source is made positive with respect to the drain, the diode conducts with a forward current rating equal to the drain current rating of the VMOS transistor. In the reverse direction, the diode has a breakdown voltage equivalent to the drain-source breakdown of the VMOS transistor.

The polarity of the (X) VMOS switches used to connect the capacitors ( $C_1$ ) to the 1.5 V source is chosen so that the internal diode is always reverse biased during the second half cycle of operation ( $\phi_2$ ). The polarity of the (Y) VMOS switches used to connect the capacitors ( $C_1$ ) in series is chosen to prevent the internal diodes from conducting during the first half cycle of operation ( $\phi_1$ ). To be able to charge output capacitor ( $C_2$ ) to 6 V, two VMOS transistors ( $S_1$  and  $S_2$ ) are connected back to back so that one of the internal diodes always remains reversed biased.

The ON resistance of a VMOS transistor was measured and found to be  $2.2 \Omega$  when  $V_{GS}$  and  $I_D$  were 9V and 1.5 mA. It was  $1.8 \Omega$  when  $V_{GS}$  and  $I_D$  were 15 V and 1.5 mA.

Zero gate voltage drain current ( $I_{DSS}$ ) of a typical VMOS transistor was experimentally found to be 27 nA when  $V_{DS}$  was 1.5 V and 320 nA when  $V_{DS}$  was 9V.

Tantalum capacitors were used in the circuit because of their low leakage current. Manufacture data sheets give leakage current of 12 nA and 120 nA for the 1  $\mu$ F and 10  $\mu$ F capacitors. The experimental measured values were 8 nA and 40 nA.

In section B, the sample current in the resistive divider  $R_1$  and  $R_2$  needs to be much greater than the input bias current. The input bias current of the (311) comparator is 100 nA, so the sample current was made 10  $\mu$ A.

$$\text{Therefore } R_1 + R_2 = 600 \text{ K } \Omega$$

$$R_2 = (R_1 + R_2) \frac{V_{REF}}{V_{out}}$$

$$R_2 = 120 \text{ K}\Omega \text{ and } R_1 = 480 \text{ K}\Omega$$

$R_1$  was made  $1 \text{ M}\Omega$  preset for adjusting the output voltage.

The reference circuit consists of a low current bandgap device (9491) in series with a resistor. The 9491 is a stable 1.22 V temperature compensated bandgap voltage reference featuring low temperature drift, low noise and good regulation over a wide operating range of 50  $\mu\text{A}$  to 5 mA.

The reference current is chosen to be about 100  $\mu\text{A}$ , which requires R to be 150 K $\Omega$ .

The (311) comparator has an open collector output. By supplying an external "pull-up" resistor connected to the 15 V supply voltage the output will swing from the supply voltage to ground. Since the output transistor operates as a saturated switch, the resistor value is not at all critical, with values typically between a few hundred ohms and a few thousand ohms. Smaller values yield improved switching speed and noise immunity at the expense of increased power dissipation. The value of the pull-up resistor is chosen to be 1.2 k $\Omega$ .

The output of the comparator is used to modulate the ON time of  $S_1$  and  $S_2$  by the RS flip-flop as shown in Figure (3.2). The set input of the flip-flop is connected to the output of the NAND gate whose inputs are the  $\phi_2$  clock and the output of the comparator. The reset input of the flip-flop also connected to  $\phi_2$  clock.

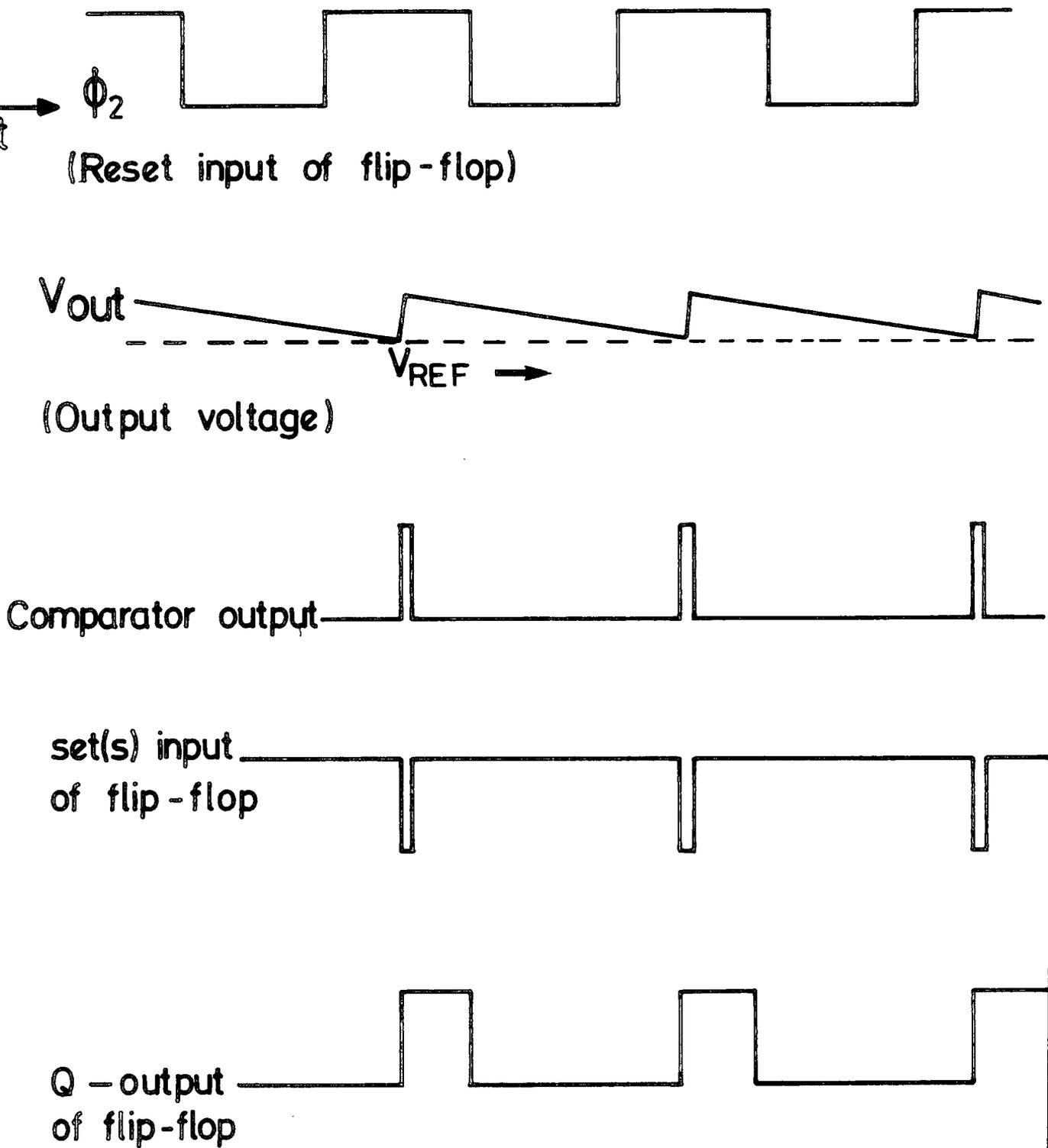


FIG. 3-2

The gates used in Figure (3.1) are CMOS Logic because they can drive VMOS transistors without any interface components. CMOS offers very low power consumption with high noise immunity 45% of supply voltage. CMOS devices operate from supply voltages between 3 to 18 V dc. The ON resistance of the VMOS transistor decreases when the drive voltage increases. When the ON resistance of the VMOS switch decreases, the power losses also decrease and the efficiency will increase. Therefore the drive voltages of the circuit ( $\phi_1$  and  $\phi_2$ ) should be as high as possible in order to get highest efficiency.

In section (C), the output of the comparator is used with  $\phi_1$  and  $\phi_2$  to control the two switches P and Q as shown in Table (3.1).

$\phi_1$	$\phi_2$	f(s)	P	Q
0	0	0	X	X
0	0	1	X	X
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	X	X
1	1	1	X	X

Table (3.1)

X means don't care

$$P = \phi_2 f(s)$$

$$Q = \bar{\phi}_2 + \bar{f}(s) = \overline{\phi_2 f(s)}$$

$$Q = \bar{P}$$

The RC filter is shown in Figure (3.3). The time constant CR was chosen to be much greater than the switching period. To avoid excessive loading of the output,  $(R_3 + R_4)$  is made much larger than R.

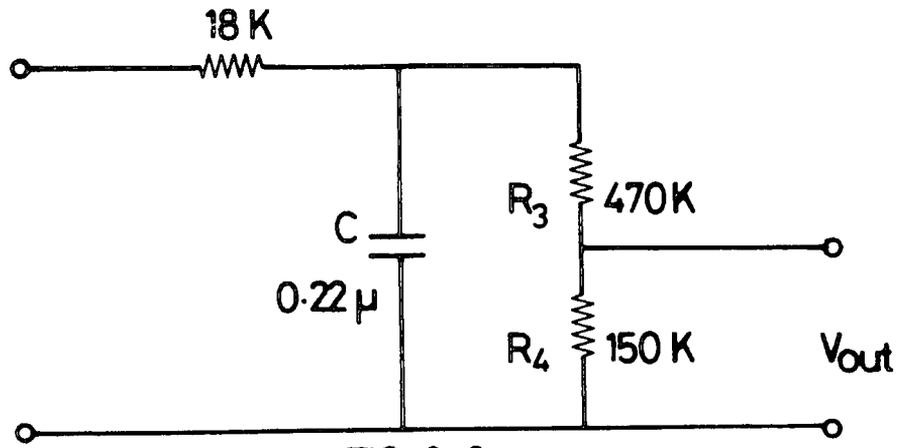


FIG. 3-3

3.4 Clock Generator

Non overlapping clock waveforms are necessary to avoid switches X and Y conducting simultaneously. A clock generator was built to produce various clock frequencies between 1 and 200 KHZ. Figure (3.4) shows the clock waveforms at frequency 10 KHZ.

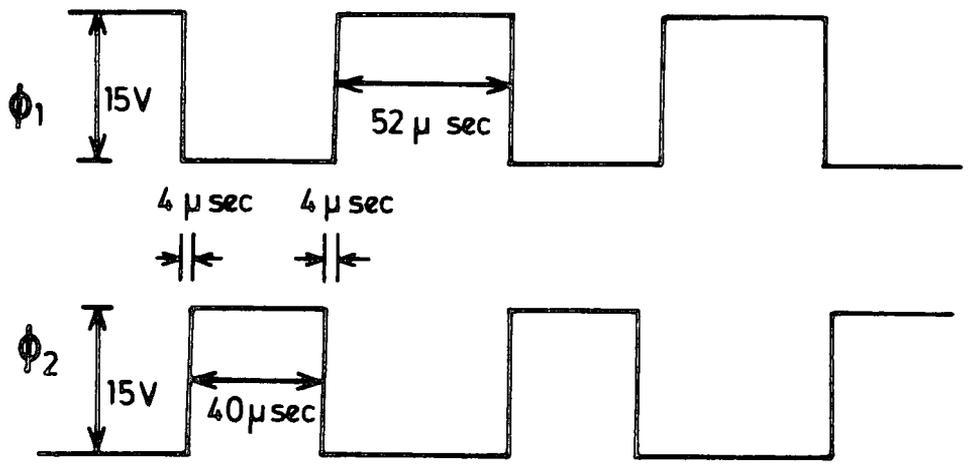


FIG. 3-4

#### 4.1 Introduction

This chapter deals with the Princeton Circuit Analysis Program (PCAP) used to model the circuit and to study the effect of changing the switching frequency,  $C_1$  and  $C_2$ , the ON resistance of the switches and the load resistance  $R_L$ . In each case the efficiency, the output voltage, the input current and the ripple is determined. The relation between the input current and the output current for varying load is also examined.

The other part of the chapter explains the models for the VMOS transistor and the capacitor, the PCAP program and a sample of calculations for each of the input current, the output current, the power input, the efficiency and the ripple.

#### 4.2 Sample of the calculations

For example let us take

$$\begin{aligned} \text{Frequency} &= 5 \text{ KHz} & C_1 &= 10 \mu\text{F} & C_2 &= 10 \mu\text{F} & R_L &= 1 \text{ K } \Omega \\ R_{\text{switching}} &= 2.5 \Omega \end{aligned}$$

To verify that the input current waveform from the PCAP program is an exponential, it is best to plot the logarithm of input current against time, Figure (4.1). The linear relation between them proves that the waveform is an exponential decay with the time, Figure (4.2).

The equation for the exponential is

$$f(t) = A e^{-t/RC}$$

where

$A$  = the maximum value of the exponential

At  $t = RC$ , the value of input current is 37% of its maximum value therefore at this time the current is 100.9 mA.

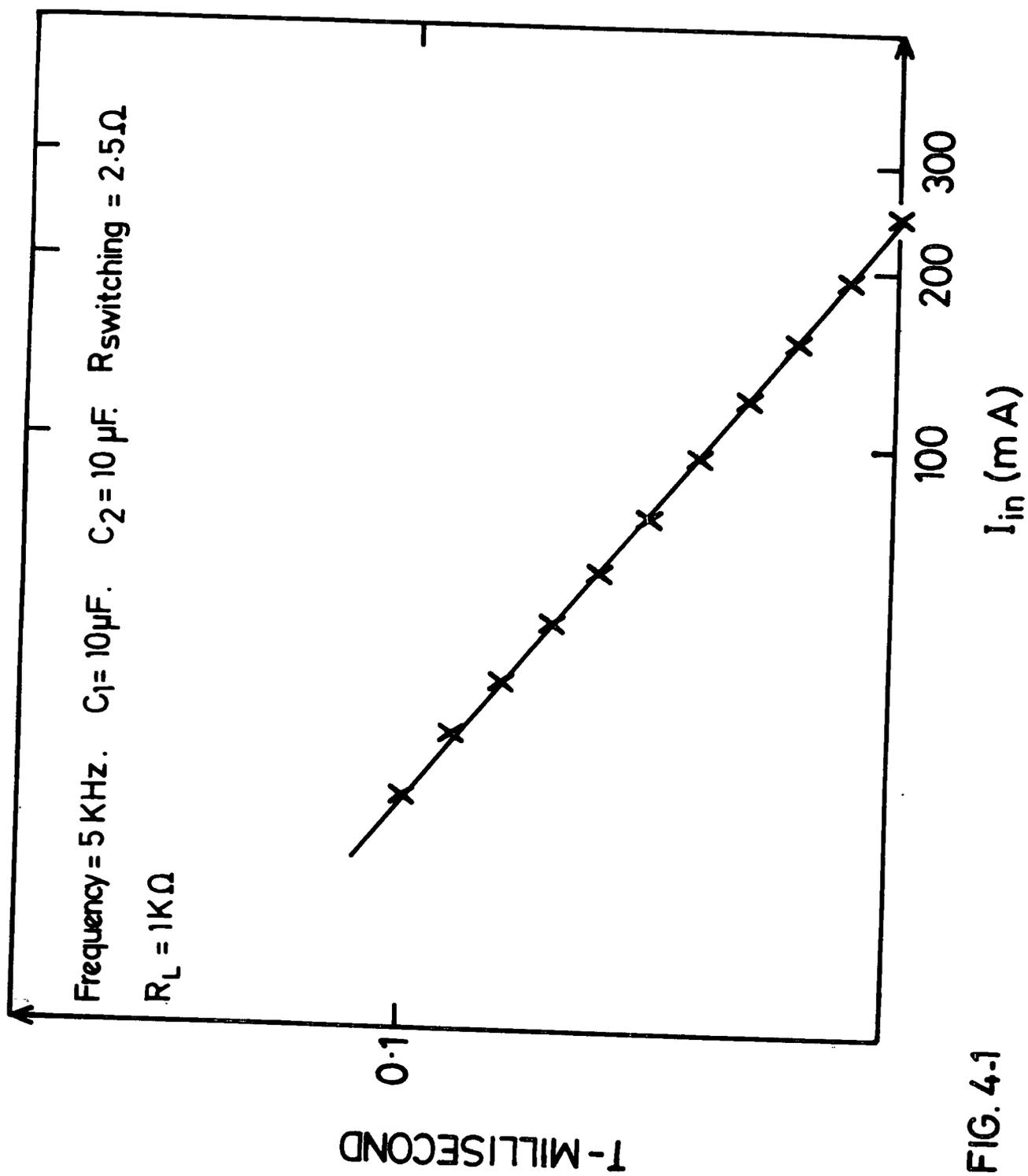


FIG. 4-1

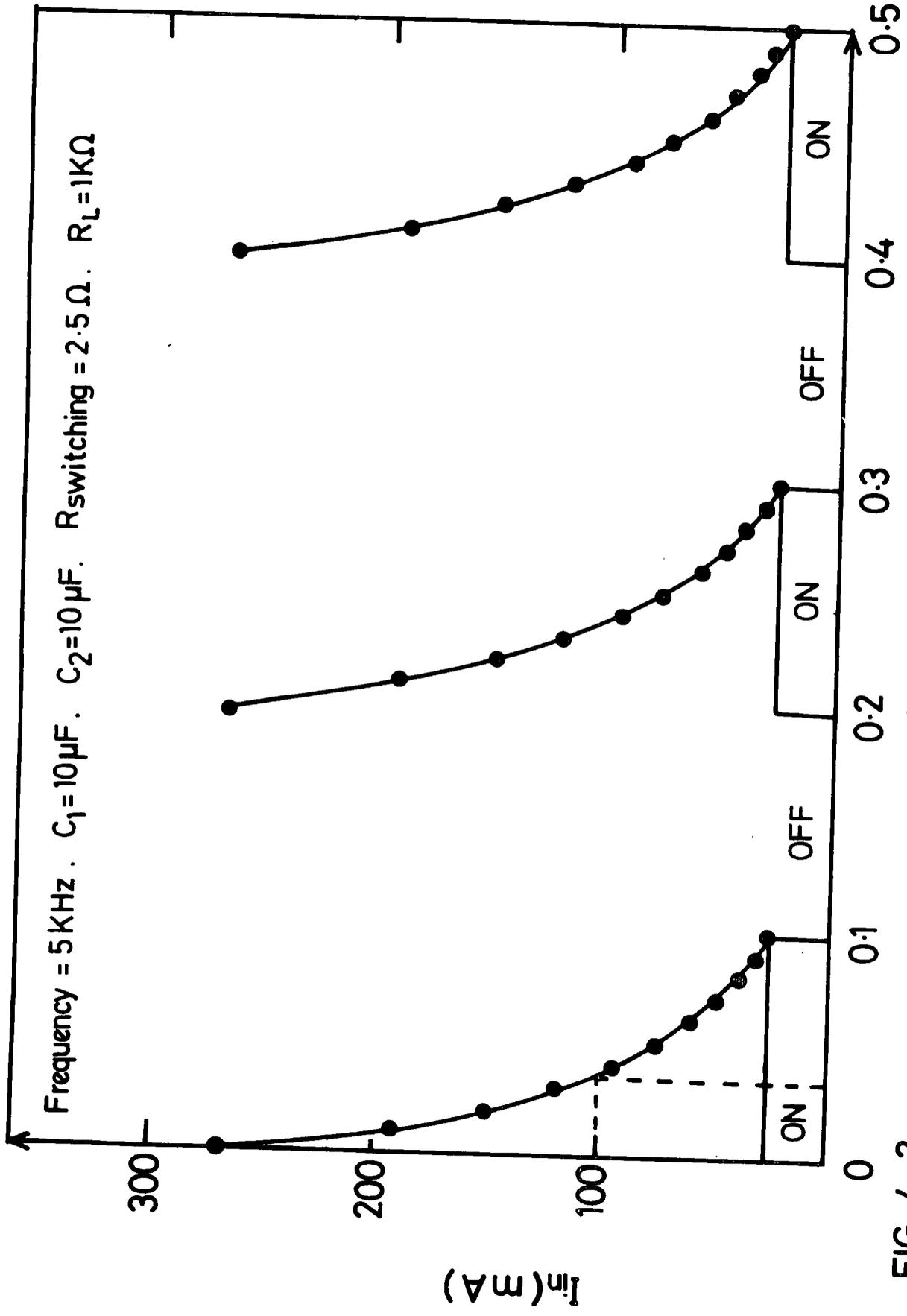


FIG. 4-2  
T - MILLISECOND

From Figure (4-2), the time constant (RC) was found to be 42  $\mu$ sec.

$$I_{in(average)} = 0.5 \left( \frac{1}{10^{-4}} \int_0^{10^{-4}} 272.85 e^{-t/42 \times 10^{-6}} dt \right)$$

$$= 52.4 \text{ mA}$$

This has been multiplied by 0.5 because the circuit draws current from the power only during one half cycle of operation.  $V$  is constant and from  $P = V.I$ , so if the current waveform is exponential the power waveform must be exponential.

$$P_{in(average)} = 0.5 \left( \frac{1}{10^{-4}} \int_0^{10^{-4}} 409.47 e^{-t/42 \times 10^{-6}} dt \right)$$

$$= 78.7 \text{ mw}$$

This has been multiplied by 0.5 because the circuit consumes power only during one half cycle of operation. The output current is shown in Figure (4-4). This is approximately a sawtooth waveform so

$$I_{out(average)} = \frac{I_{max} + I_{min}}{2}$$

$$= 7.9 \text{ mA}$$

The load resistance  $R_L$  is constant and so the average power output

$$P_{out(average)} = \frac{P_{max} + P_{min}}{2}$$

$$= 62 \text{ mw}$$

Then the efficiency will be

$$= \frac{P_{out}}{P_{in}} \times 100$$

$$= 78.6\%$$

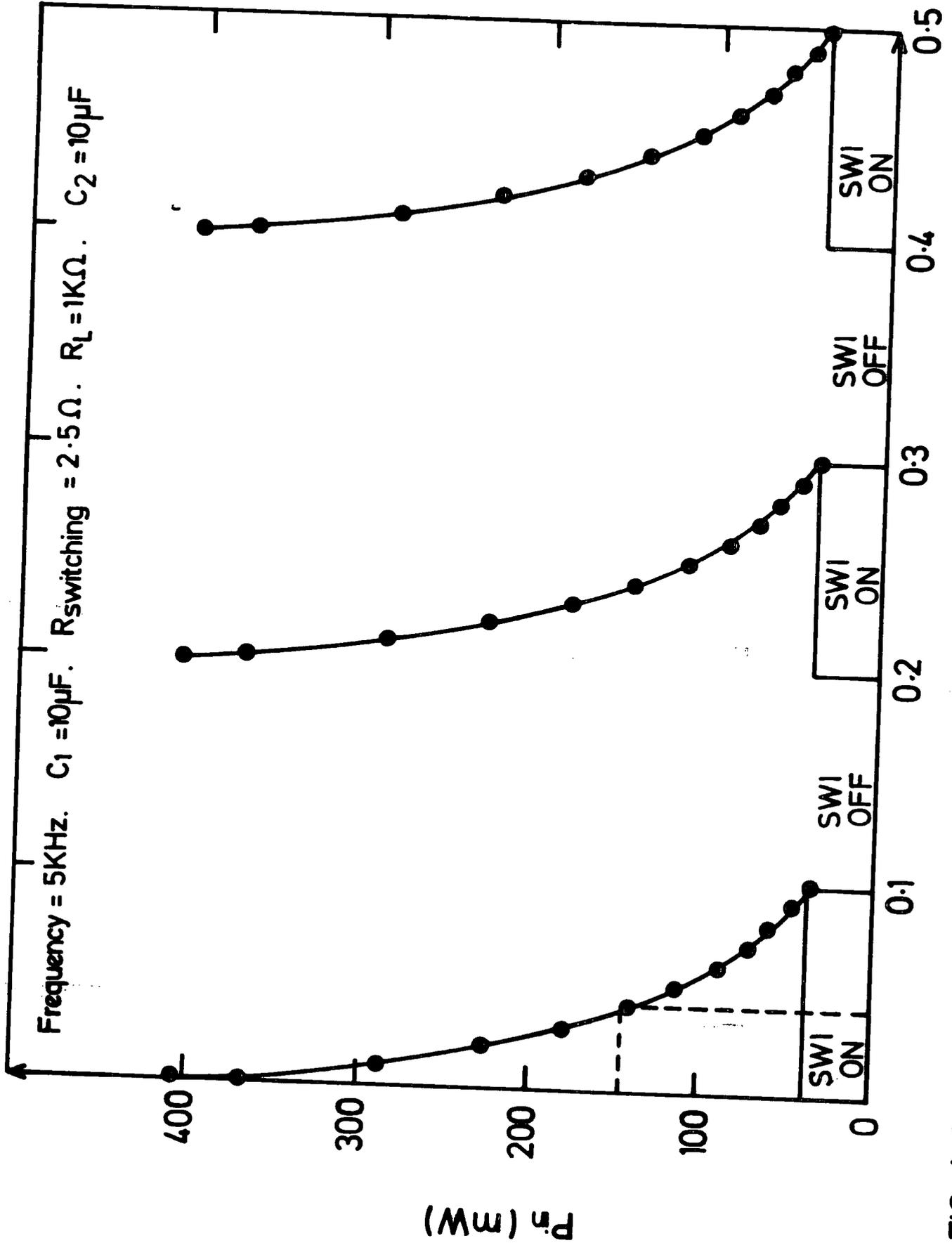


FIG. 4-3 T - MILLISECOND

FIG. 4-3

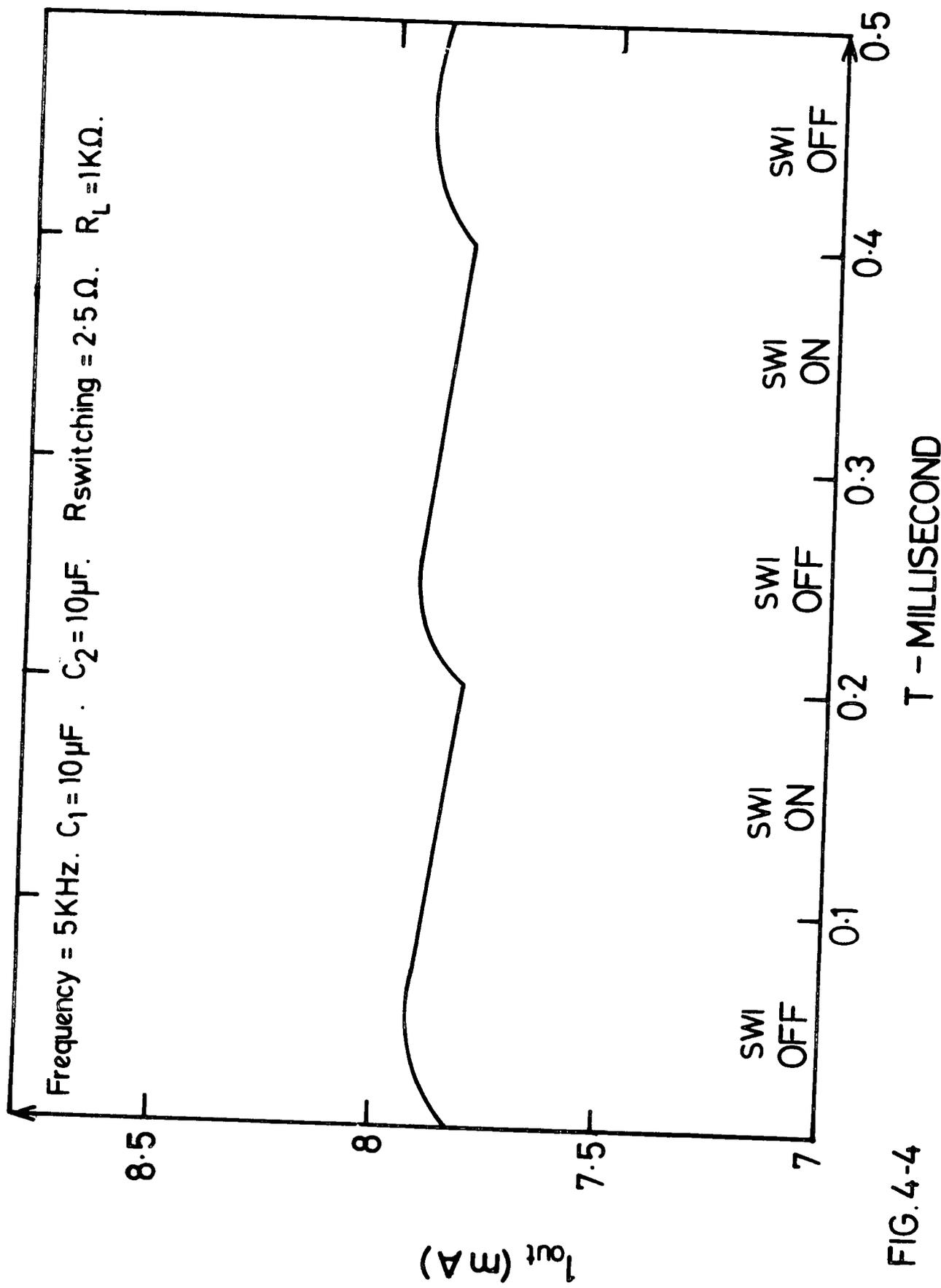
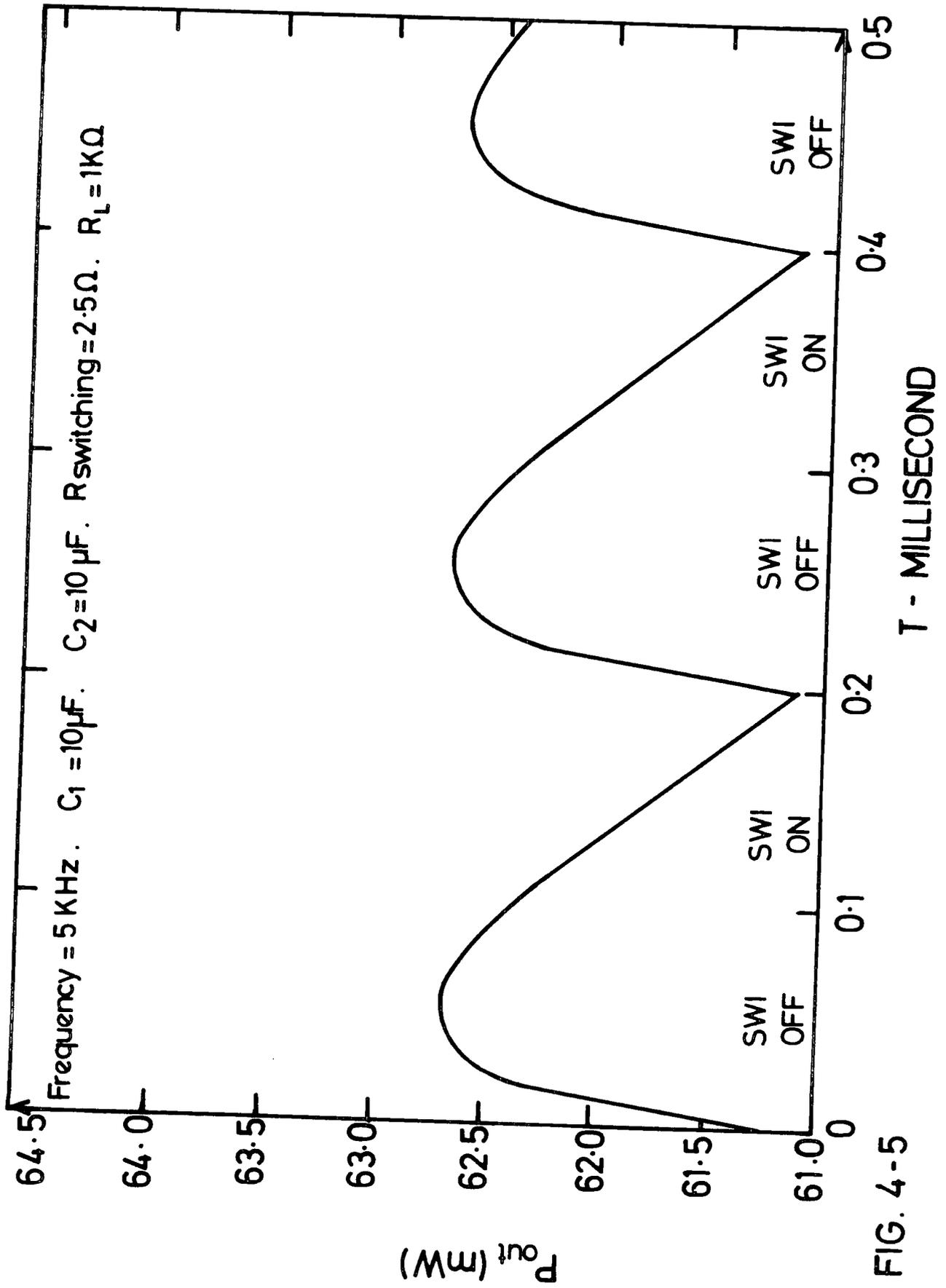


FIG. 4-4



The ripple voltage is

$$V_{\text{ripple(peak-peak)}} = (I_{\text{max}} - I_{\text{min}}) \cdot R_L$$

$$= 0.1 \text{ v}$$

Then the % ripple will be

$$\% \text{ ripple} = \frac{V_{\text{ripple(peak-peak)}}}{V_{\text{out}}} \times 100\%$$

$$= 1.26\%$$

#### 4.3 The effect of varying the switching frequency on the circuit

This section explains the effect of the switching frequency on the circuit in four different cases.

Case 1 Figures (4-6,7,8) show the following

1. The ripple decrease with increasing switching frequency and with increasing output capacitor ( $C_2$ ).
2. The efficiency increases as switching frequency increases.
3. Below 10 KHz the output voltage increases with increasing switching frequency. Above 10 KHz the output voltage is not substantially affected by increasing switching frequency.
4. Below 10 KHz the input current increases as the switching frequency increases and above 10 KHz the input current decreases with increasing switching frequency.
5. The efficiency, the output voltage and the input current are not substantially affected by the value of the output capacitor ( $C_2$ ).

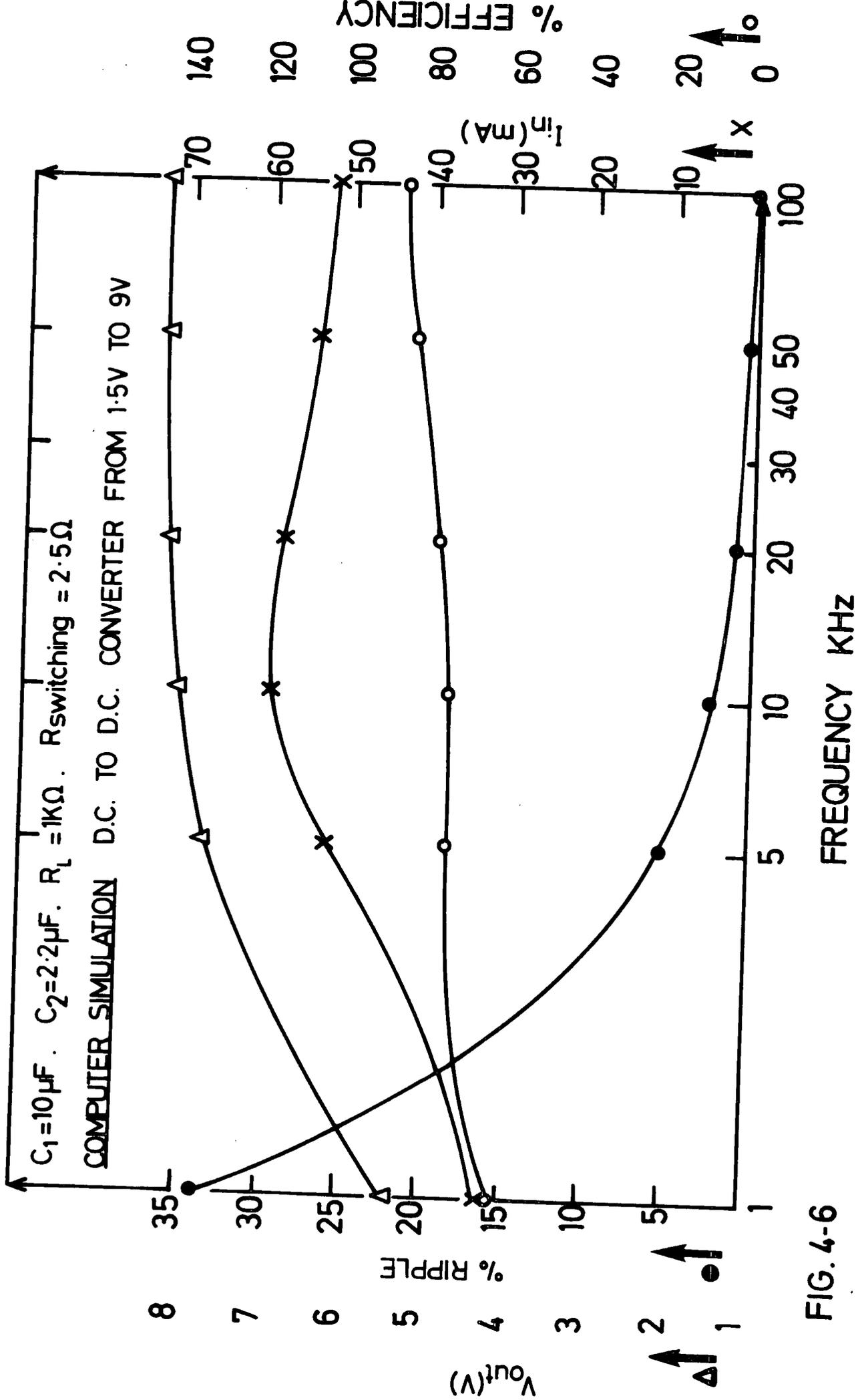


FIG. 4-6

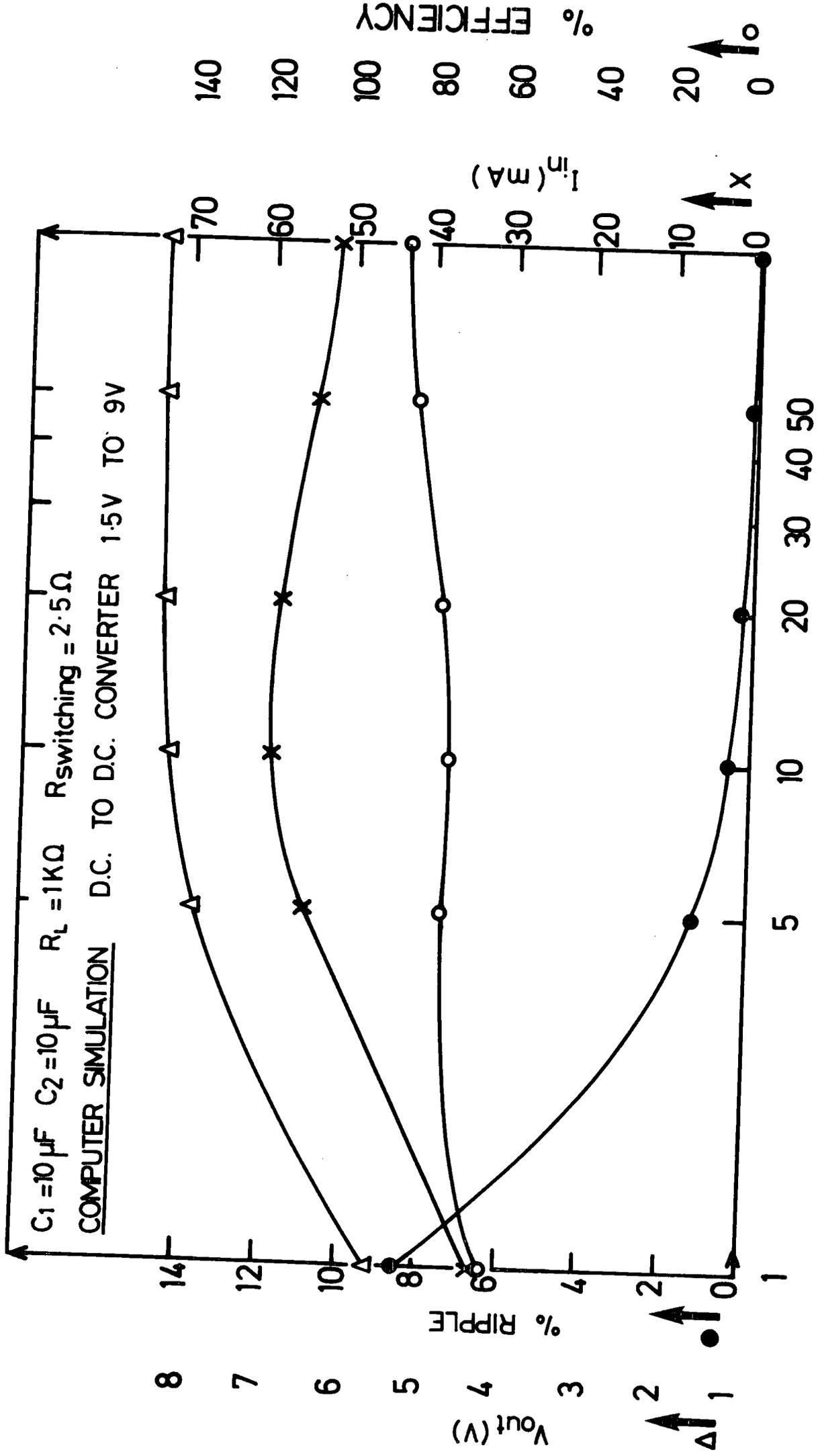


FIG. 4-7.

FREQUENCY KHz

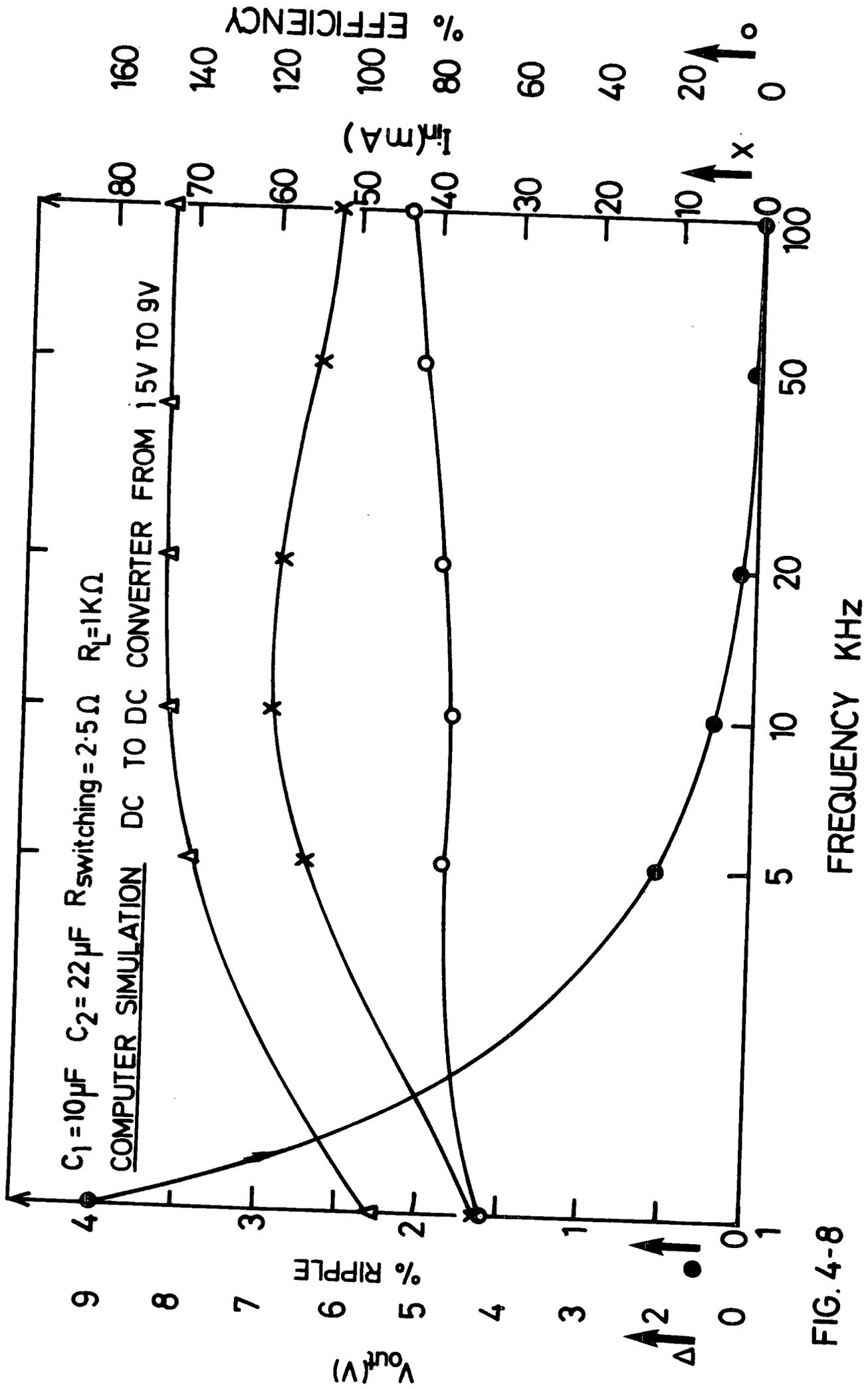


FIG. 4-8

Case 2 Figures (4-9,10,11) show the following

1. Similar to Figures (4-6,7,8), the ripple in Figures (4-9,10,11) decreases with increasing switching frequency and with increasing output capacitor ( $C_2$ ).
2. Below 20 KHz the efficiency increases with increasing switching frequency. Above 20 KHz the efficiency slightly decreases with increasing switching frequency. This is different from case (1). The efficiency in Figures (4-9,10,11) are less than the efficiency in Figures (4-6,7,8).
3. In Figures (4-9,10,11), the output voltage always increases with increasing switching frequency unlike the case shown in Figures (4-6,7,8). For same switching frequency the output voltage in Figures (4-9,10,11) are always less than the output voltage in Figures (4-6,7,8).
4. In Figures (4-9,10,11), the input current always increases with increasing switching frequency unlike the case shown in Figure (4-6,7,8).
5. As in Figures (4-6,7,8), the efficiency, the output voltage and the input current in Figures (4-9,10,11) are not substantially affected by the value of the output capacitor ( $C_2$ ).

Case 3 Comparison of Figures (4-12,13,14) with Figures (4-6,7,8) shows that -

1. The efficiency in Figures (4-12,13,14) is less than the efficiency in Figures (4-6,7,8).
2. The output voltage in Figures (4-12,13,14) is less than the output voltage in Figures (4-6,7,8).

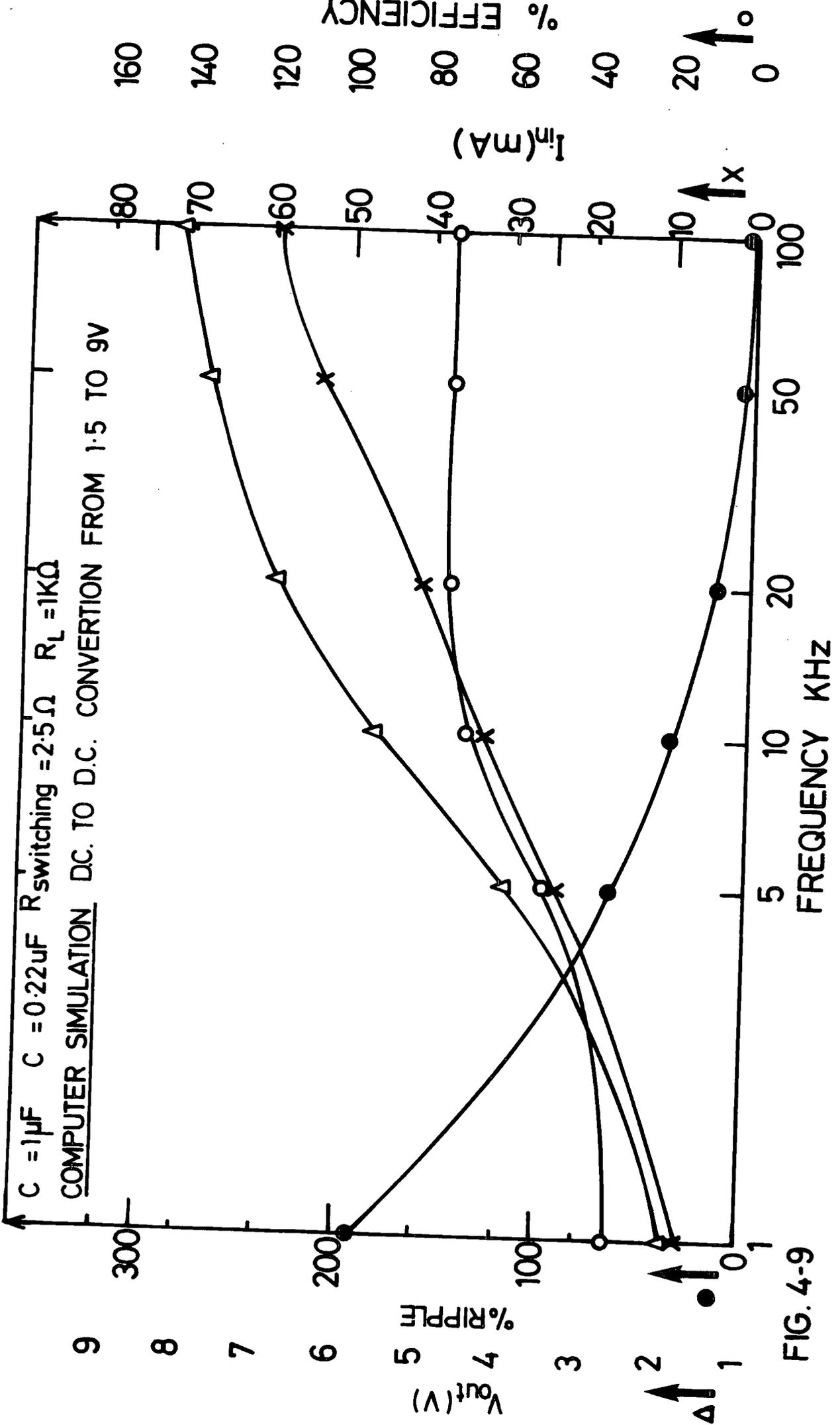


FIG. 4-9

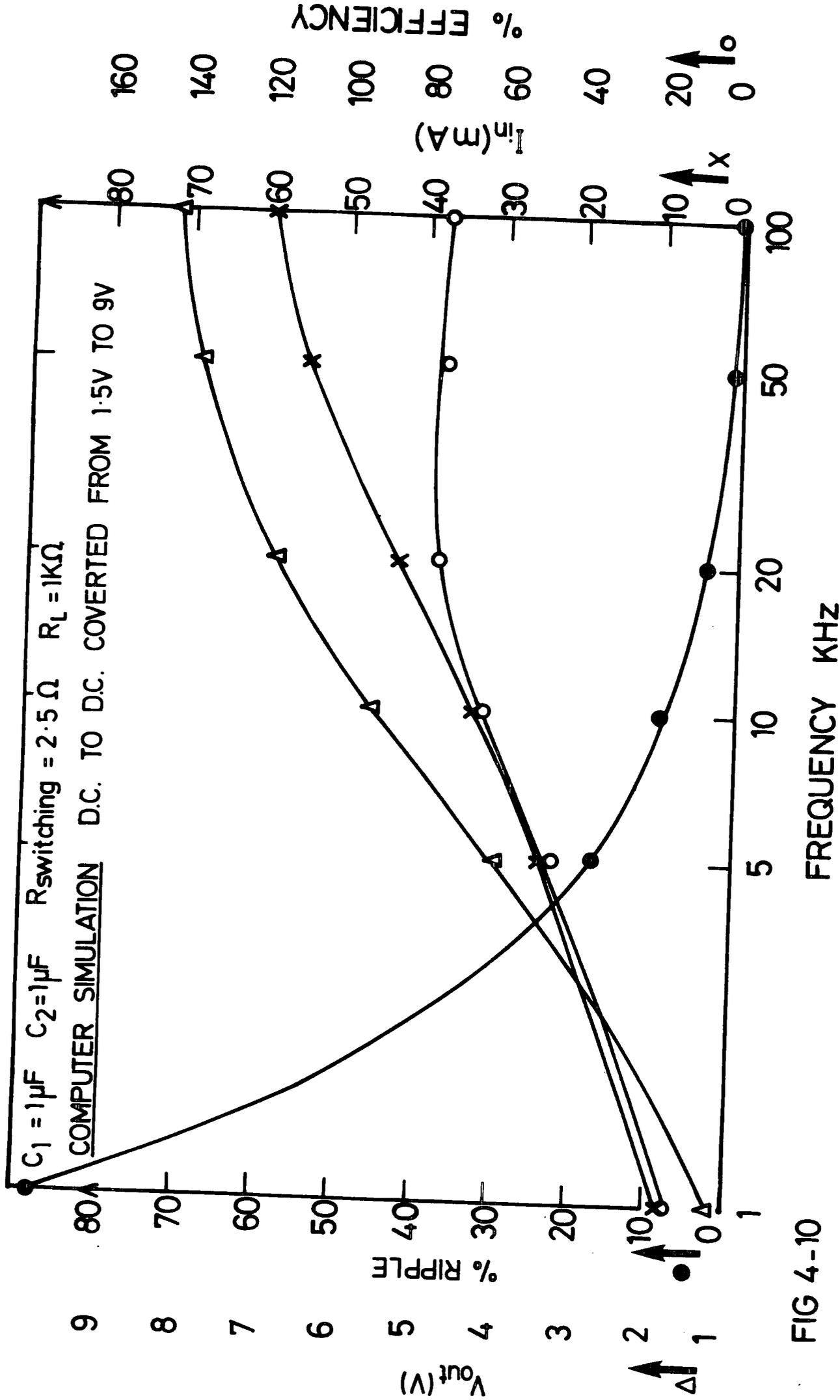


FIG 4-10

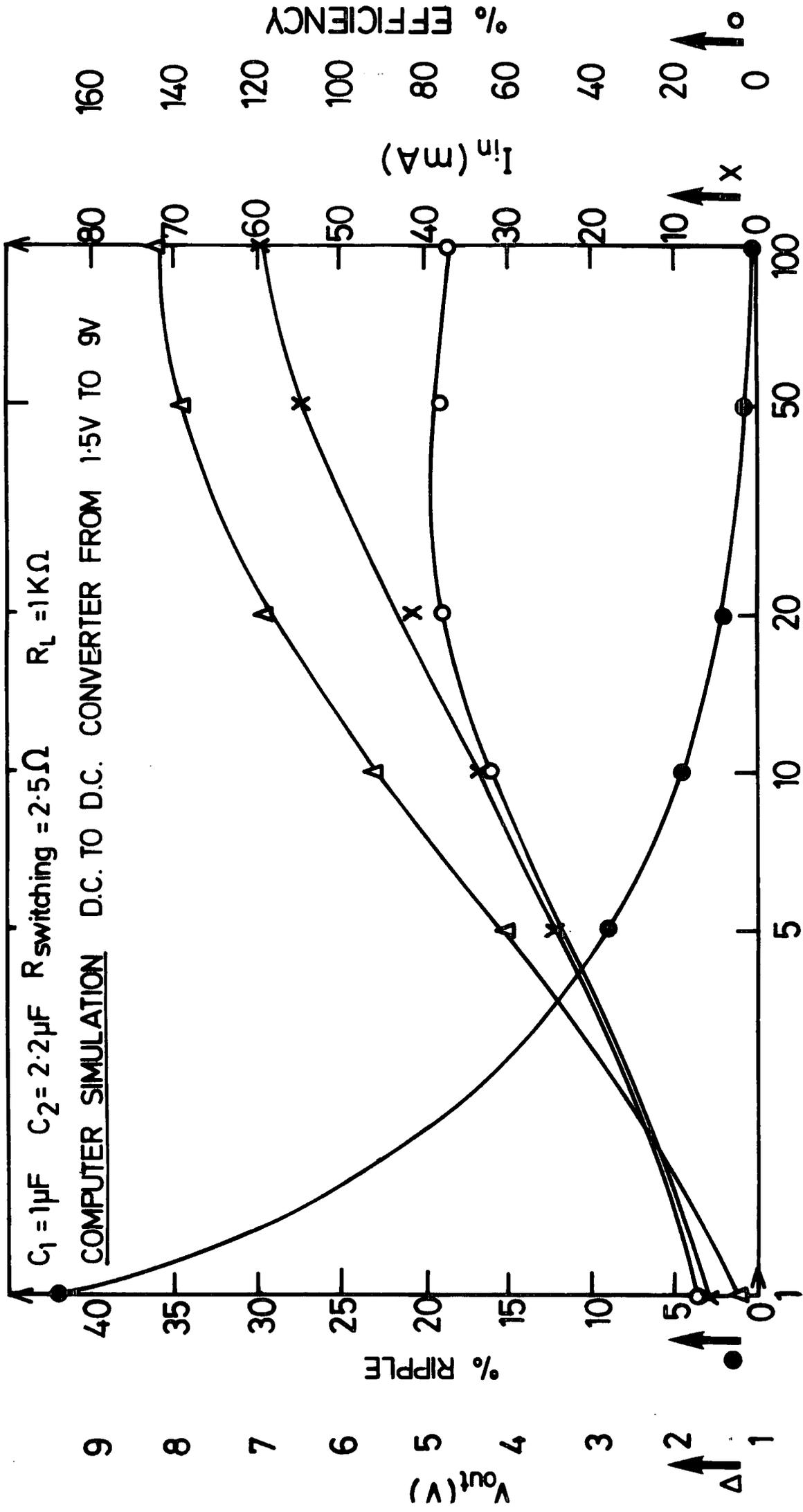


FIG. 4-11

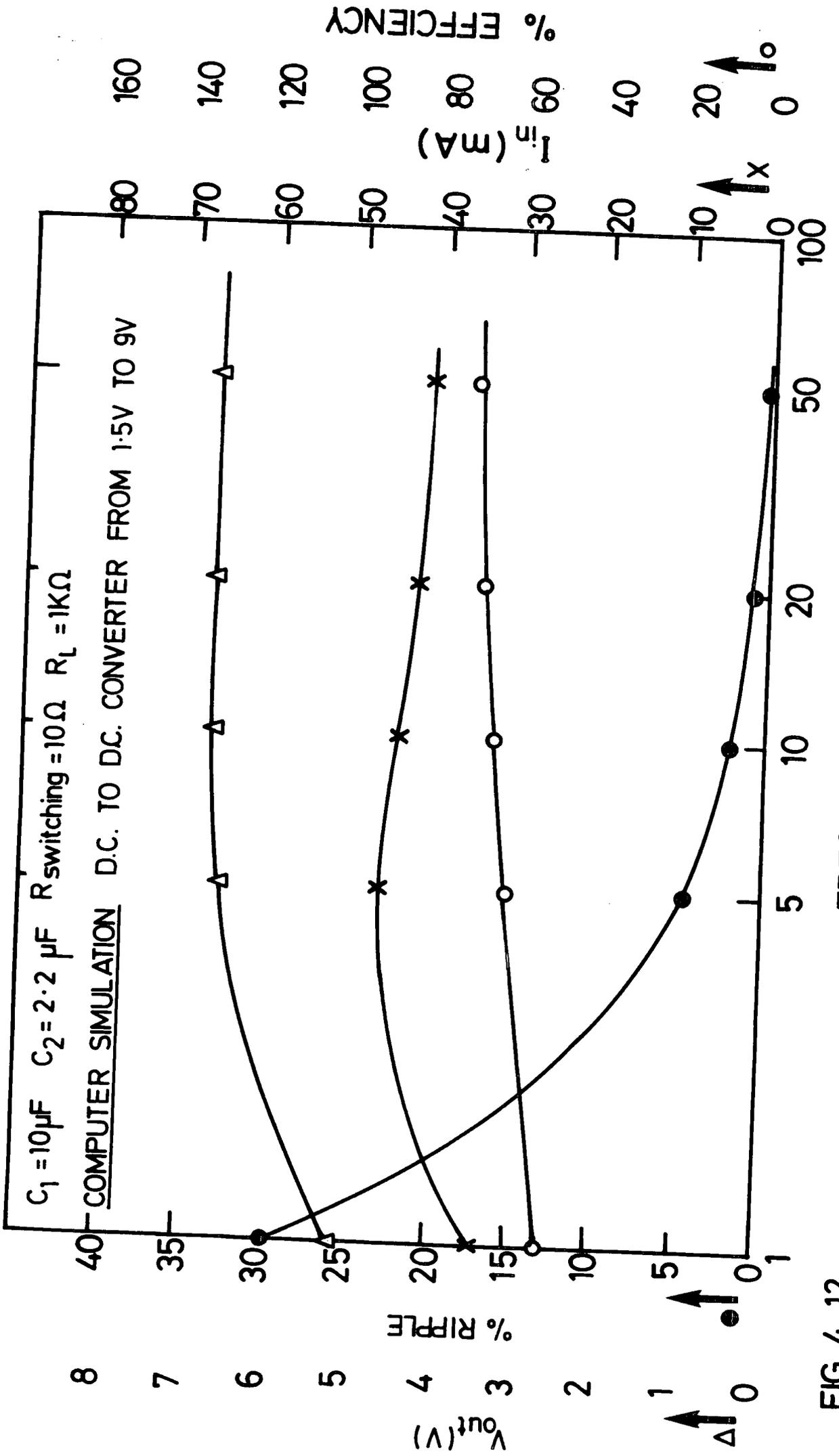


FIG. 4-12

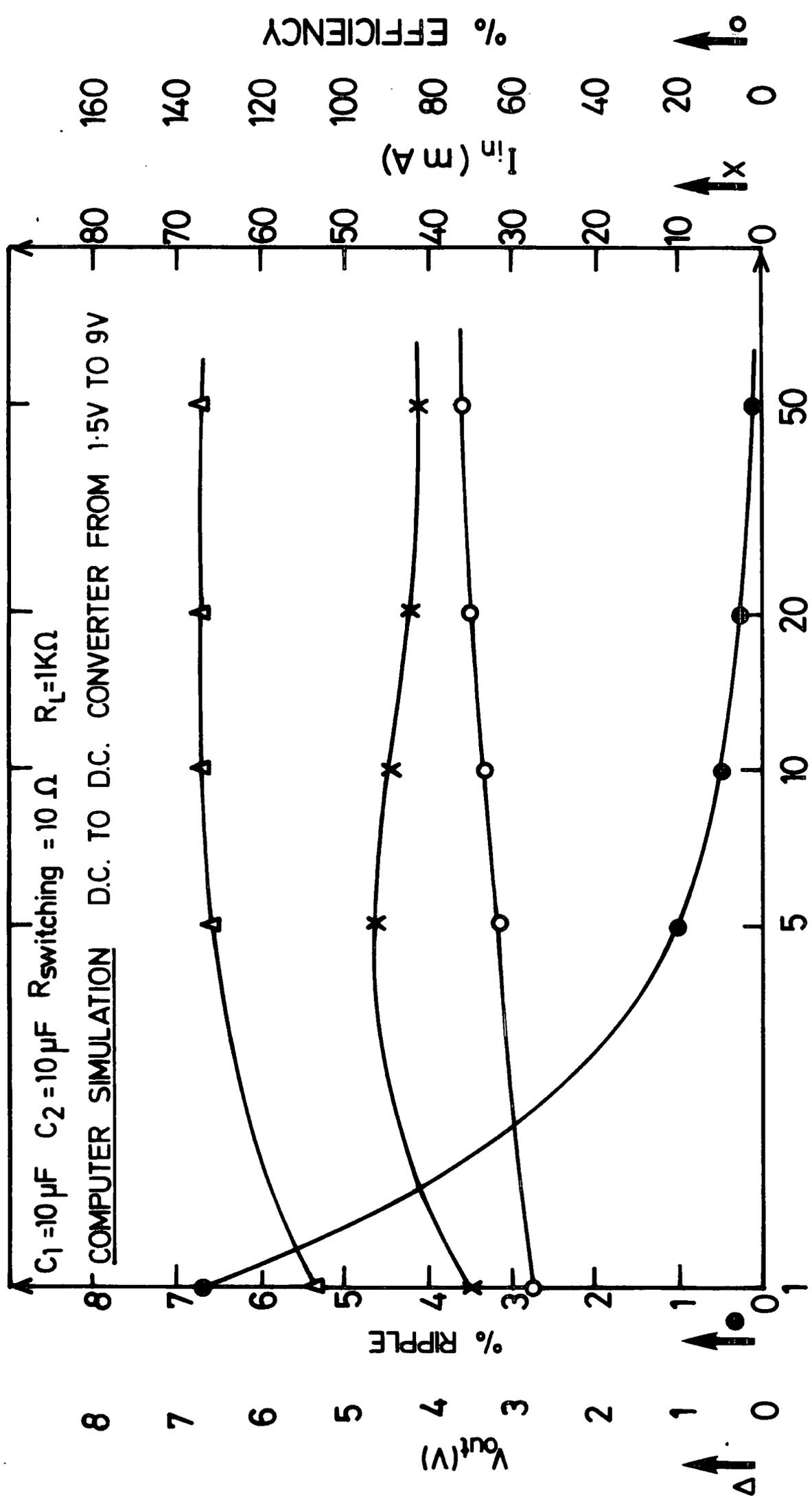


FIG. 4-13

FREQUENCY KHZ

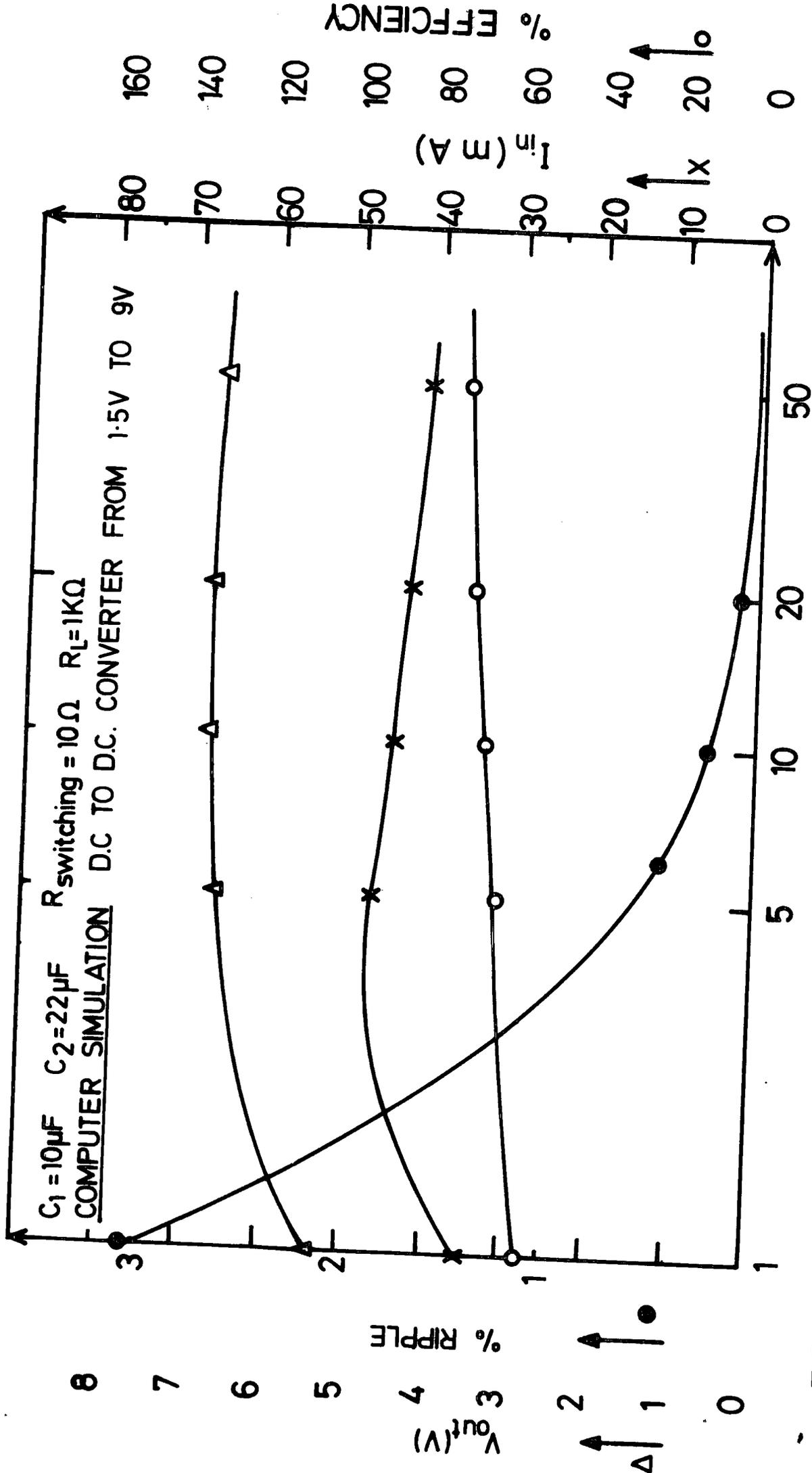


FIG.4-14

Case 4 Comparison of Figures (4-15,16,17) with Figures (4-9,10,11) gives that -

1. The efficiency in Figures (4-15,16,17) is less than the efficiency in Figures (4-9,10,11).
2. The efficiency in Figures (4-15,16,17) increases with increasing switching frequency. This is different from Figures (4-9,10,11).
3. The output voltage in Figures (4-15,16,17) is less than the output voltage in Figures (4-6,7,8).

#### 4.4 The effect of varying the ON resistance of the switch on the circuit

Figure (4.18) shows the following:-

1. The ON resistance of the switch has no effect on the ripple.
2. The output voltage decreases with increasing ON resistance of the switch.
3. The efficiency decreases with increasing ON resistance of the switch.
4. The input current also decreases with increasing ON resistance of the switch.

#### 4.5 The effect of the output current on the circuit

Figure (4.19) shows the following:-

1. The ripple increases with increasing output current.
2. The relation between the input current and the output current is linear.
3. The output voltage decreases with increasing output current.
4. The efficiency decrease with increasing output current.

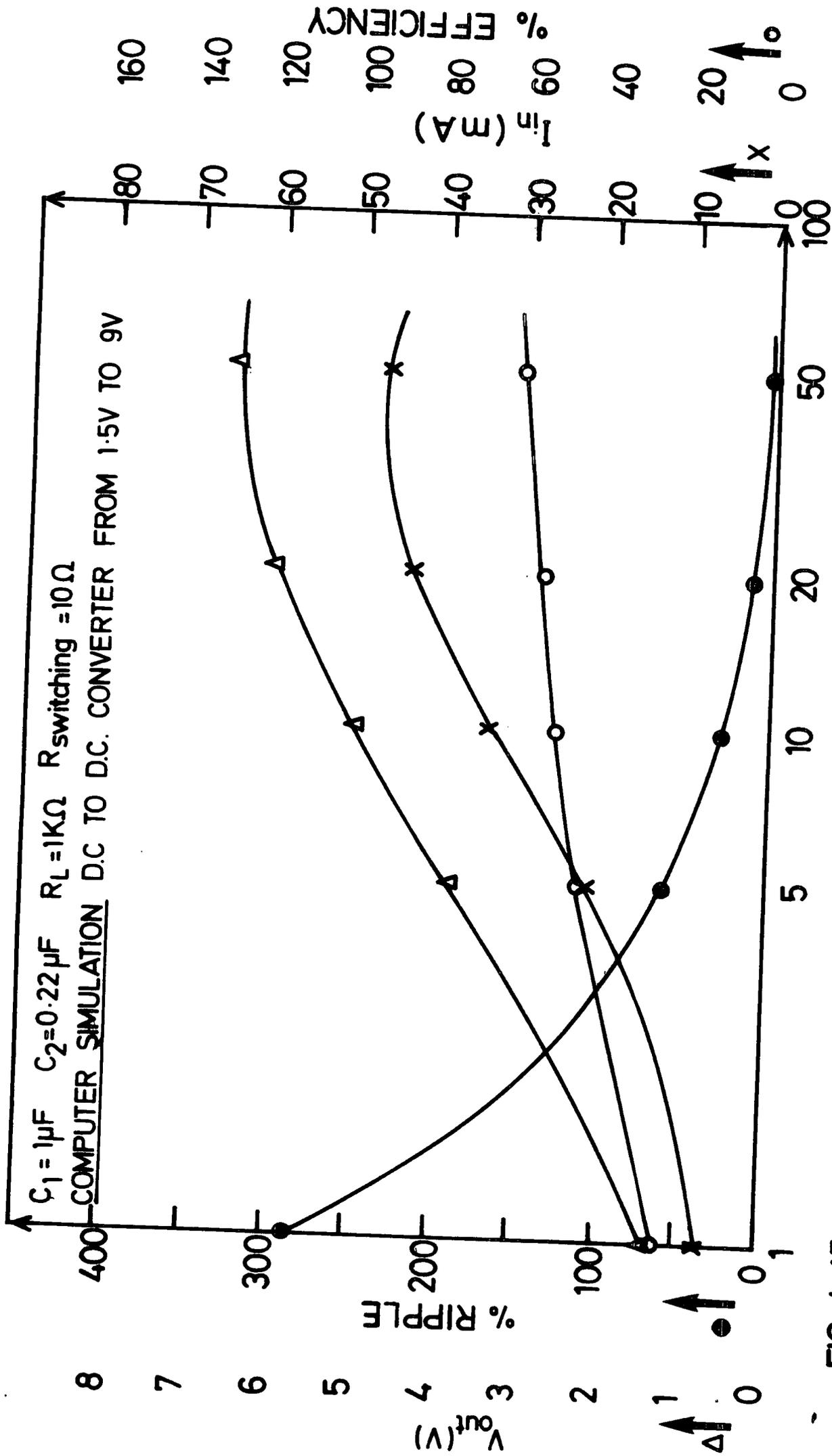


FIG. 4-15

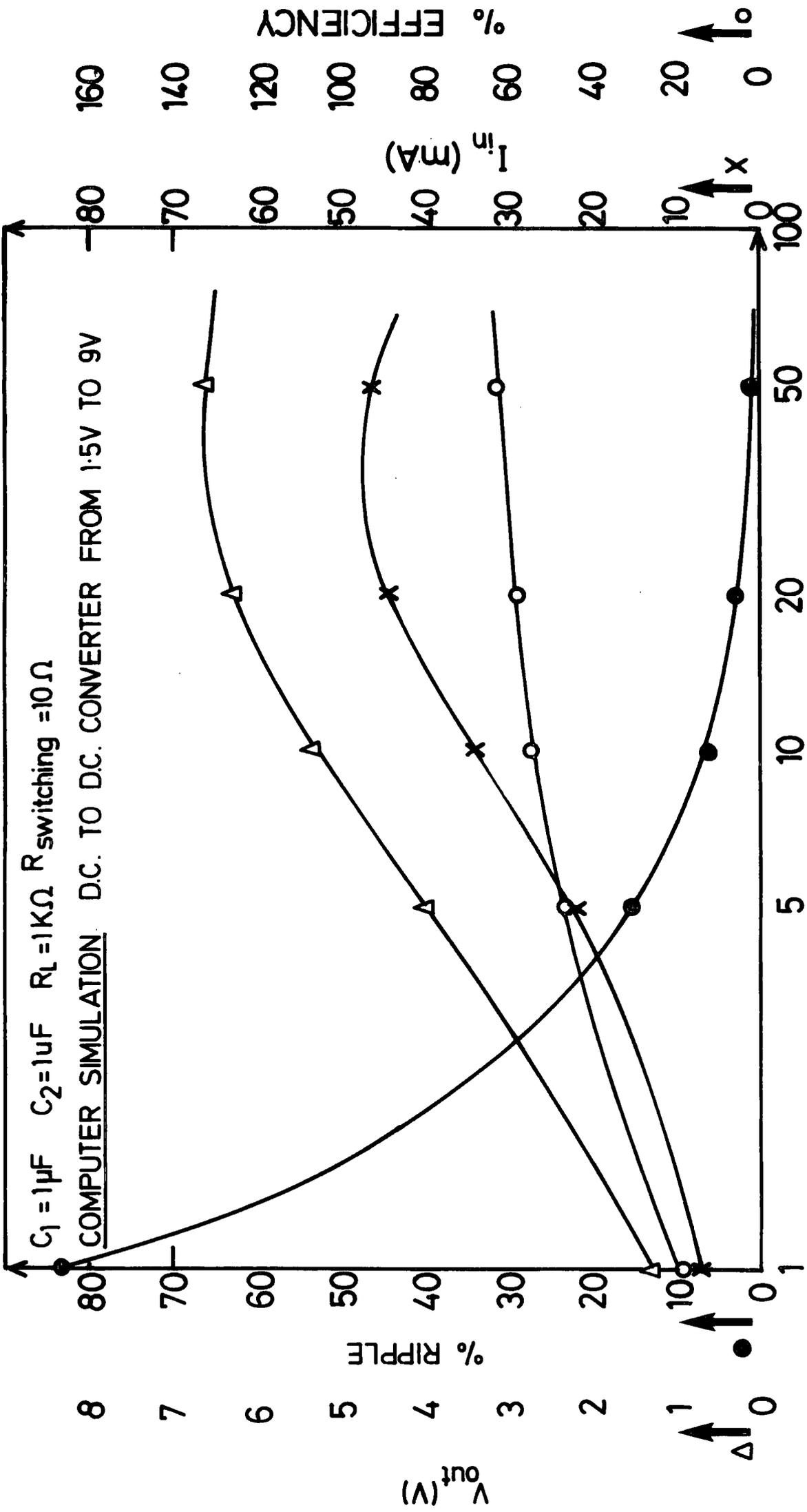


FIG. 4-16 FREQUENCY KHZ

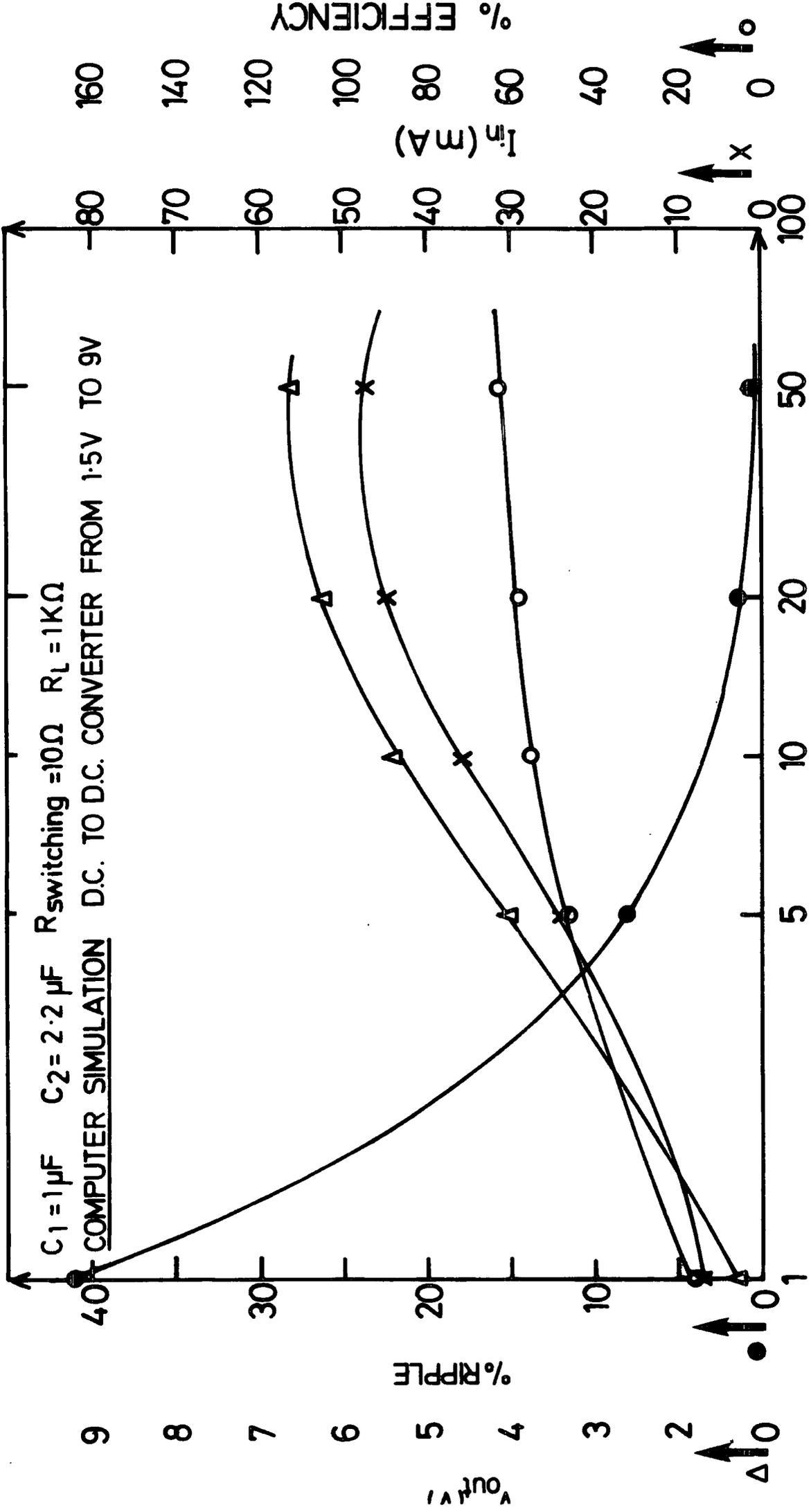


FIG. 4-17

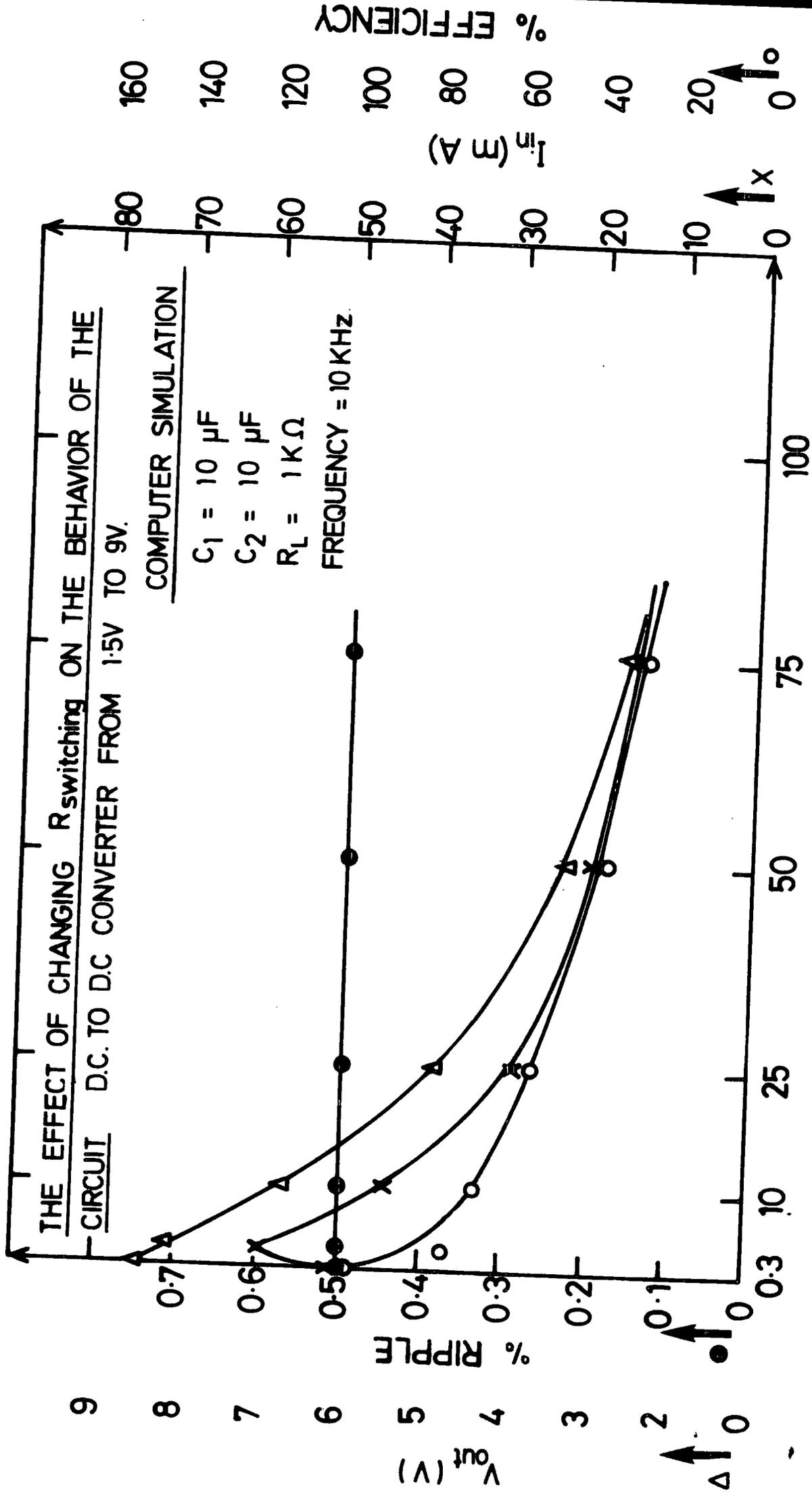


FIG. 4-18

$R_{switching} (\Omega)$

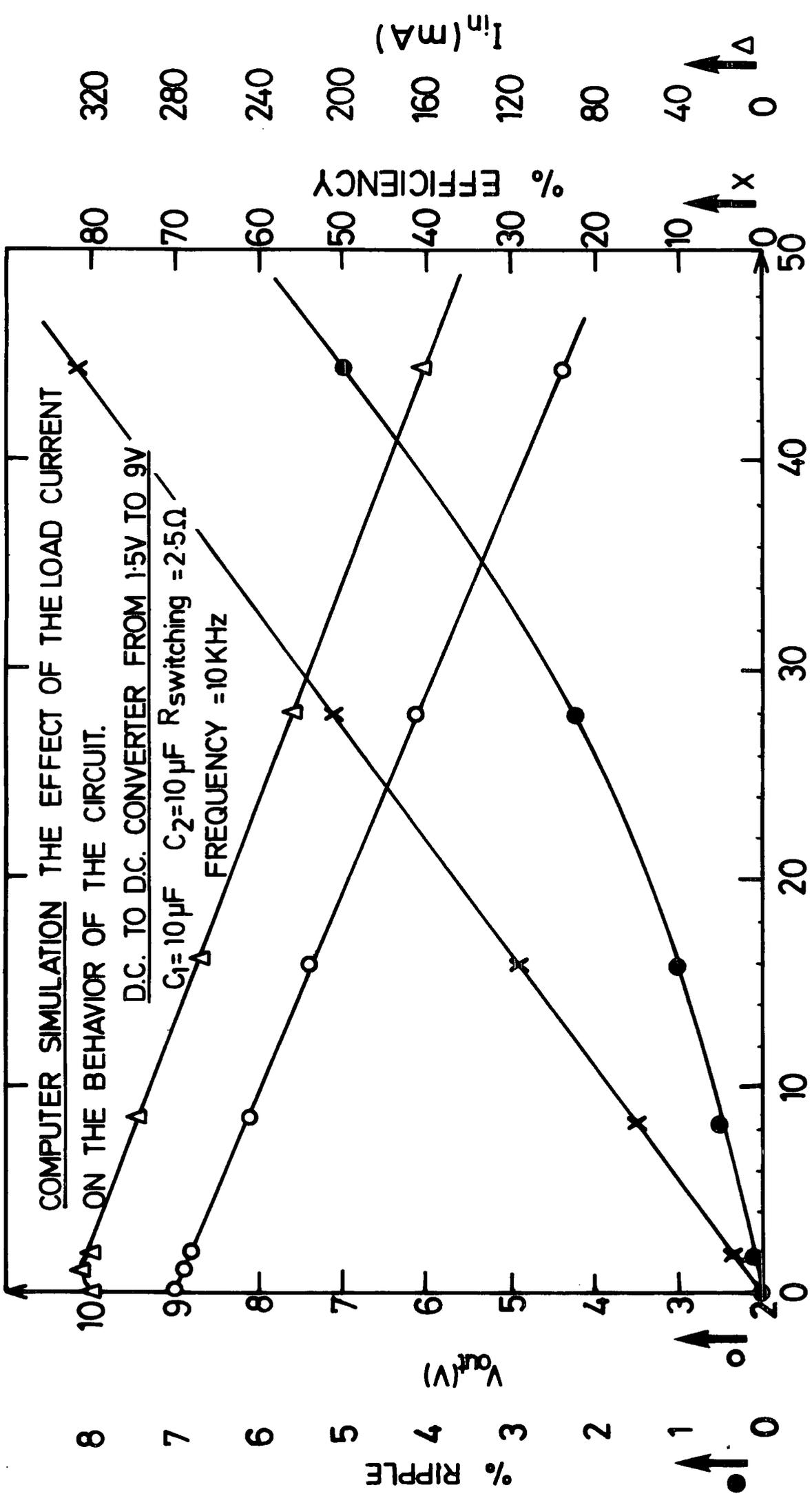


FIG. 4-19  $I_L$  (mA)

#### 4.6 Low-Frequency Model for the FET

In general, the drain current of any type of FET can be written in the following form

$$i_D = f_1(V_{GS}, V_{DS}) + f_2(V_{DS}) \quad \dots\dots\dots (4-1)$$

where  $f_1$  is a nonlinear function of  $V_{GS}$ ,  $V_{DS}$  and the parameters of the FET and  $f_2$  is a nonlinear function of  $V_{DS}$  and the FET's parameters.

Equation (4-1) can be represented by the model of Figure (4.20). The generator whose current is  $i(V_{GS}, V_{DS})$  represents the effect of  $f_1$ , that is

$$i(V_{GS}, V_{DS}) = f_1(V_{GS}, V_{DS}) \quad \dots\dots\dots (4-2)$$

The nonlinear resistance  $r_D$  represents the effect of  $f_2$ . In this case

$$r_D = \frac{V_{DS}}{f_2(V_{DS})} \quad \dots\dots\dots (4-3)$$

The diodes  $D_1$  and  $D_2$  are added to Figure (4-20) to model the isolation of the FET from the substrate. In the VMOS transistor the substrate is connected to the source and the substrate-drain diode  $D_1$  of Figure (4-20) is reverse biased. Thus  $D_1$ ,  $D_2$  and the substrate lead will be omitted from the model.

**Cutoff Region Model :** In the cutoff region, the drain current is extremely small. So the FET can be accurately modelled by an open circuit. However in PCAP a branch cannot be a perfect short circuit or perfect open circuit. So  $R_D$  was made equal to  $10^7\Omega$  as shown in Figure (4-21a).

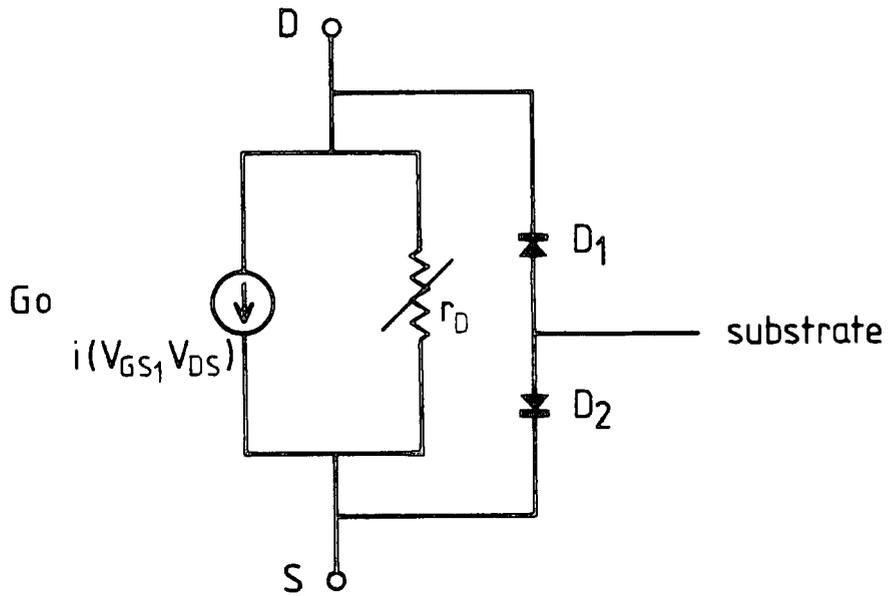


FIG (4-20), A general low frequency model for the FET

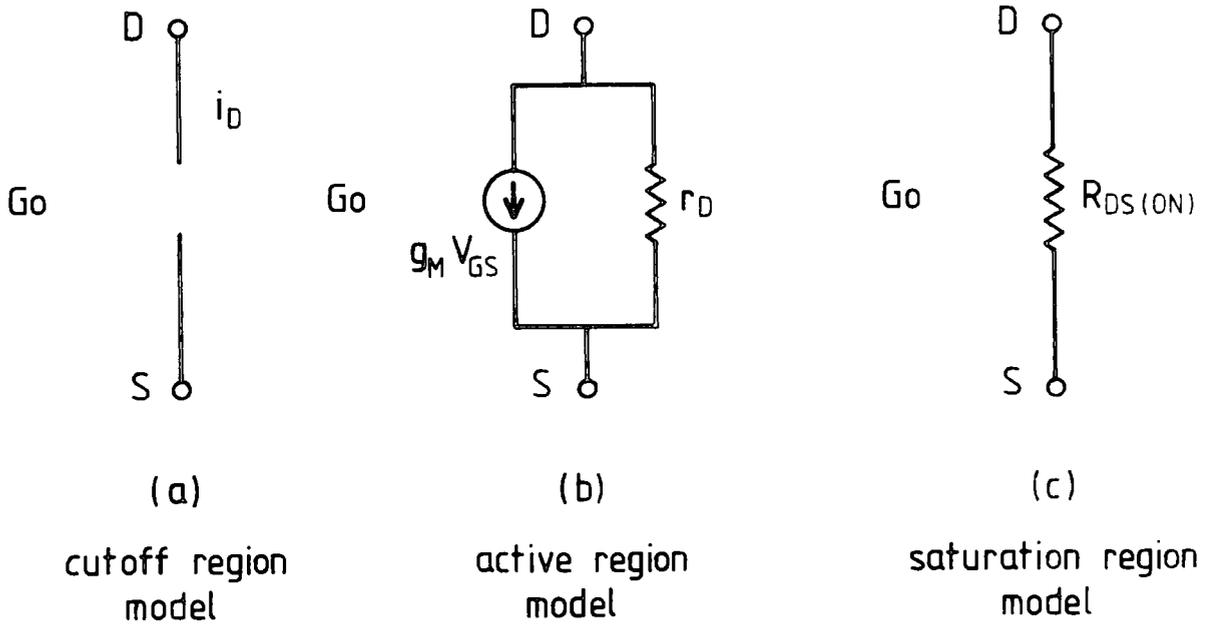


FIG (4-21)

Active Region : The active region model for the FET is shown in Figure (4-21b). Where

$$r_D = \left. \frac{V_{DS}}{i_D} \right|_{V_{GS} = \text{constant}}$$

and

$$g_M = \left. \frac{i_D}{V_{GS}} \right|_{V_{DS} = \text{constant}}$$

The values of  $r_D$  and  $g_M$  are obtained by appropriately averaging the parameter values over the active region.

Saturation Region : In the saturation region the FET can be approximated by a single resistance  $r_{DS(ON)}$  as shown in Figure (4-21c).

#### 4.7 High-Frequency Model for the FET

An accurate high-frequency model for enhancement and depletion MOSFET's can be obtained from the general model of Figure (4-20) by adding appropriate nonlinear capacitances. Let us start by considering the capacitance between gate and source, gate and drain, and drain and source. In general,  $C_{GS}$  and  $C_{GD}$  are nonlinear since the dimensions of the channel vary with the terminal voltages of the devices. For instance, if the induced channel's dimensions increase, then the overlap capacitance would increase. This tends to increase  $C_{GD}$  and  $C_{GS}$ .

In general,  $C_{DS}$  can usually be considered to be a linear capacitor since it is not substantially changed by the change in the channel's dimensions. The nonlinear junction capacitances of the diodes of Figure (4-20) which isolate the FET from the substrate must also be included. The model that results when all these capacitances are added is shown in Figure (4-22).

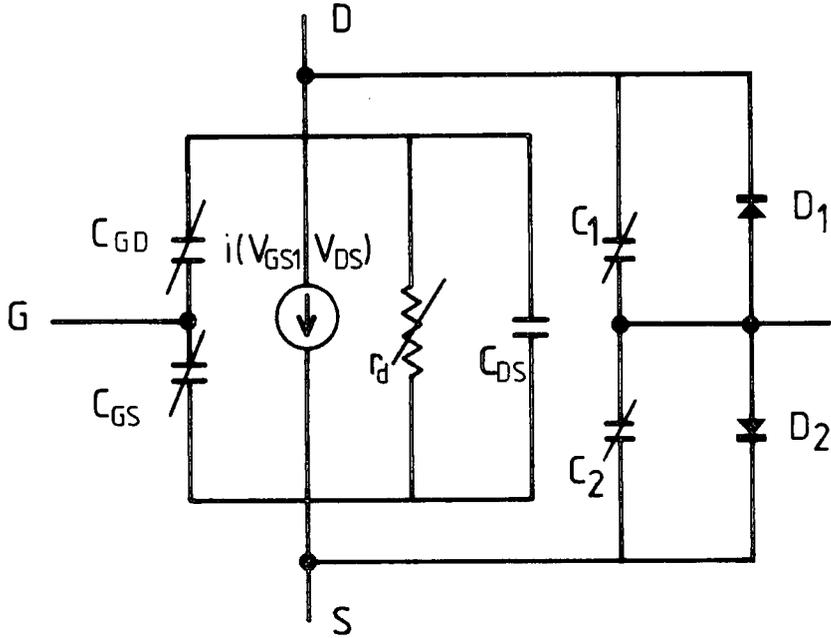
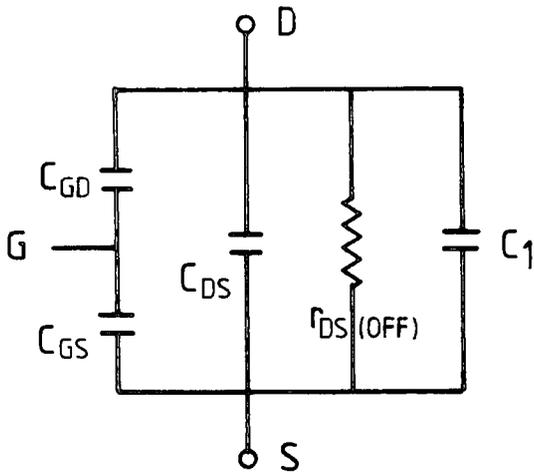
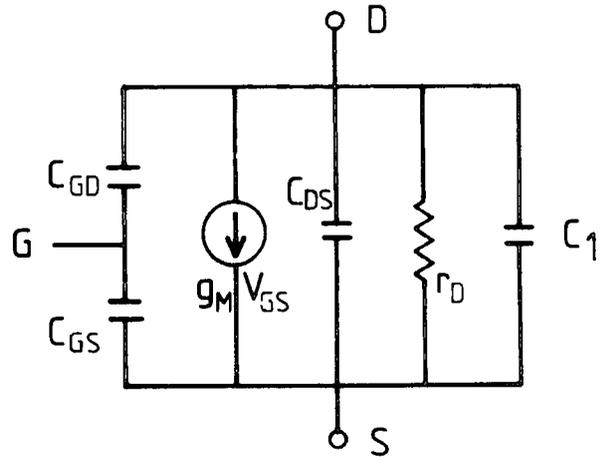


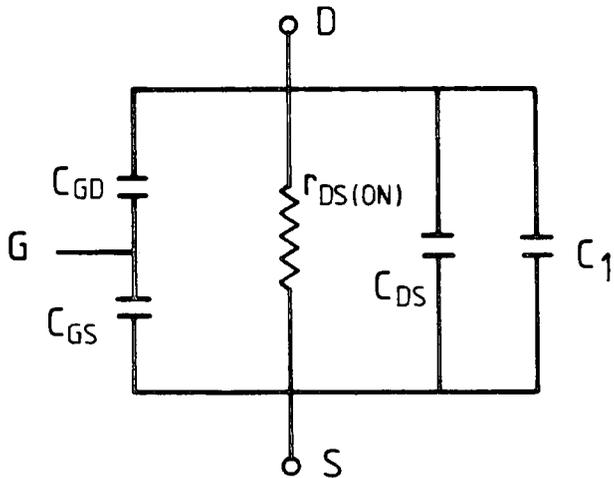
FIG (4 - 22) High - Frequency Model For The FET



(a) cutoff region model



(b) Active region model



(c) Saturation region model

FIG (4 - 23) Approximate High - Frequency Model For FET

The nonlinear high-frequency model Figure (4-22) can be approximated by three linear models which represent the behaviour in the saturation, active and cutoff region respectively. Such models are shown in Figure (4-23).

Note

Neither the high frequency nor the active region models are considered in this particular program.

4.8 Model of a capacitor

A model of a capacitor is shown in Figure (4-24). Besides possessing the property of capacitance there will also be small quantities of series resistance and shunt resistance which represent the loss component and the leakage in the capacitor. Both of them prevent the capacitance from being completely effective. The capacitor model used in the PCAP program just consists of the capacitance and the shunt resistance. The series resistance was neglected because it was experimentally found to be much smaller than the ON resistance of the VMOS transistor

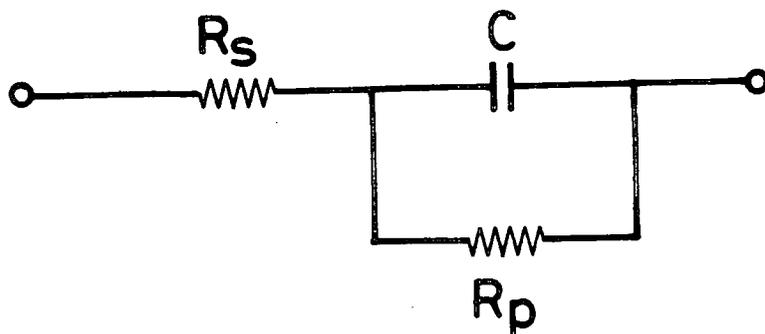


FIG. 4-24

#### 4.9 The aim of the PCAP program

The Princeton Circuit Analysis Program (PCAP) has evolved from the ECAP program developed by IBM. The objective of the PCAP is to help in the analysis of electric and electronic circuits. PCAP is used by supplying information about the simulated circuit to the computer and then requesting information about the performance of the simulated circuit from the computer in a systematic, simple, and natural way. Three types of analysis are possible with PCAP : DC ANALYSIS, AC ANALYSIS and TRANSIENT ANALYSIS. DC and AC ANALYSIS can be used to analyze large networks of linear circuit elements with constant sources (DC) or sources which are phasors (AC). TRANSIENT ANALYSIS, in addition to linear problems, can be used to study a wide class of nonlinear problems.

In any PCAP problem :

- (a) A node voltage is the voltage measured at a node with respect to the reference node, which is electrical ground. Nodes may be numbered in any order using consecutive numbers beginning with zero. PCAP always assumes that node (0) is the reference node (electrical ground). The maximum number of nodes that may be used is 40, not including node (0).
- (b) Branches may be numbered in any order using consecutive numbers beginning with one. The B statements (which contain the branch descriptions) must each contain one, and only one, passive element and must be entered sequentially on the coding sheet. The maximum number used is 150.
- (c) In all PCAP analysis there must be at least one path, through the branches of the circuit, between every node and ground; that is, there can be no "floating" node. The branches which were added as

dummy branches, are connected to the reference node to assure that nodes have paths to ground. A dummy branch is a branch which has no effect on the circuit performance but is added for the sake of the PCAP analysis.

(d) The branch current  $i_b$  is considered positive when it flows through the branch from node  $n_i$  to node  $n_f$  (from the "initial" node to the "final" node). With this choice for the positive current direction, the branch voltage is defined to be

$$e_b = e_{ni} - e_{nf}$$

Note that the positive directions for  $e_b$  and  $i_b$  are not independent : once the positive direction for  $i_b$  has been chosen the positive direction for  $e_b$  is determined as above, and conversely. Note also that the positive directions assigned for  $e_b$  and  $i_b$  have nothing to do with the actual polarities of these quantities. In a given problem  $e_b$  and  $i_b$  could both be positive, they could both be negative, or they could have opposite signs.

(e) The constant voltage source is specified as a positive quantity if the positive terminal of the source is connected to the initial node and the negative terminal to the final node.

(f) The TAB output format is intended to provide a compact table of a limited number of output variables versus a parameter (or frequency, or time). For the DC and AC ANALYSIS Programs, it can be used for the initial solution as well as when a parameter is being varied over a range of values. For the DC and TR programs, the table of data contains a maximum of 8 columns in addition to the column for the independent variable (either a parameter or time). If more than 8 columns are requested, up to 10 columns will be printed with reduced accuracy.

For AC program, where each variable (except average power) has both a magnitude and a phase angle, 10 columns of data (i.e. five complex variables) are possible in addition to the column for the independent variable (either frequency or a parameter).

(g) EXECUTE : specifies that the circuit has been completely described and that the analysis is now to be performed.

The program used the same basic rules with the following additions :

1. In the transient analysis, the instantaneous branch power loss is defined to be

$$P_b(t) = e_b(t) \cdot i_b(t)$$

Note that  $P_b(t)$  can be positive (when the branch is absorbing power from the external network connected to node  $n_i$  and  $n_f$ ) or negative (when the branch is supplying power to the external network).

2. First, second, and fourth order numerical integration routines are available. They can be obtained by including \*ORDER = K (\* in column 1), where K is the desired order. The second order routine is the default option.

3. Time step : is the time between successive solutions.

4. Final time : is the total time over which solution is to be obtained.

5. Output Interval : is the number of time steps between tabulated or plotted points.

Both the "Time step" and "Final Time" cards are required. If the final time is not specified the program will compute one time step and stop. It may sometimes be necessary to determine an

optimum time step by trial and error. The MODIFY card can be used advantageously for this purpose. In order for the numerical integration to converge to a reasonably accurate solution the time step should be about 0.1, the smallest time constant in the system for a second-order routine. It can be one-half to one-fourth the smallest characteristic time for the fourth-order routine. The maximum number of TIME STEPS cannot exceed 3050 unless the limitation is removed by a \*NOLIM card (\* in column 1).

6. E-cards:- Time varying source may be specified with E-cards (voltage sources) or I-cards (current sources). These cards are not numbered sequentially, the number b following the initial E or I is the number of the branch containing the time varying source. Such a branch must not contain a fixed E or I specification although it may contain both a time-varying  $E(t)$  and a time varying  $I(t)$ . There are various types of Time-varying sources. The one used in this program is called "Periodic Piecewise Linear Functions" and the first entry for this type of function is  $P(T_K)$ , and this is followed by a series of numbers. The quantity  $T_K$  is the desired time interval between specified points and for proper operation  $T_K$  should be specified as an integral multiple of the Time step. The series of numbers is a table of values for the function at equally spaced intervals of  $T_K$  seconds starting at  $t = 0$ . There may be up to 101 tabulated values but the last entry must be the same as the first. When the last entry is reached the program repeats the function. The maximum number of time-varying sources that may be used is 10.

7. S-card:- is used when the current in one branch, the controlling (From) branch causes a parameter in the other branch, the controlled (To) branch, to change from one value to another when the controlling current changes sign. The parameter to be switched in the controlled

branch must be given a pair of values rather than a single value (otherwise the parameter will not change value). The first of these is the value taken by the parameter when the switch is in its initially specified state (either ON or OFF) and the second is the value taken when the switch change state. The maximum number of S-cards is 100 and the maximum number of branches affected by all switches is 200.

### List of the Program

DC to DC converter

C Effect of varying frequency on the circuit

Transient Analysis

\* No limit

\* Order = 4

$B_1$	N(1,0), R = 1E-3, E = 1.5
$B_2$	N(1,2), R = (2.5, 1E7)
$B_3$	N(2,0), C = 10E-6
$B_4$	N(2,0), R = 3E7
$B_5$	N(1,3), R = (2.5, 1E7)
$B_6$	N(3,4), C = 10E-6
$B_7$	N(3,4), R = 3E7
$B_8$	N(4,0), R = (2.5, 1E7)
$B_9$	N(1,5), R = (2.5, 1E7)
$B_{10}$	N(5,6), C = 10E-6
$B_{11}$	N(5,6), R = 3E7
$B_{12}$	N(6,0), R = (2.5, 1E7)
$B_{13}$	N(1,7), R = (2.5, 1E7)
$B_{14}$	N(7,8), C = 10E-6
$B_{15}$	N(7,8), R = 3E7
$B_{16}$	N(8,0), R = (2.5, 1E7)
$B_{17}$	N(1,9), R = (2.5, 1E7)

$B_{18}$        $N(9,10)$ ,  $C = 10E-6$   
 $B_{19}$        $N(9,10)$ ,  $R = 3E7$   
 $B_{20}$        $N(10,0)$ ,  $R = (2.5,1E7)$   
 $B_{21}$        $N(1,11)$ ,  $R = (2.5,1E7)$   
 $B_{22}$        $N(11,12)$ ,  $C = 10E-6$   
 $B_{23}$        $N(11,12)$ ,  $R = 3E7$   
 $B_{24}$        $N(12,0)$ ,  $R = (2.5,1E7)$   
 $B_{25}$        $N(2,4)$ ,  $R = (1E7,2.5)$   
 $B_{26}$        $N(3,6)$ ,  $R = (1E7,2.5)$   
 $B_{27}$        $N(5,8)$ ,  $R = (1E7, 2.5)$   
 $B_{28}$        $N(7,10)$ ,  $R = (1E7, 2.5)$   
 $B_{29}$        $N(9,12)$ ,  $R = (1E7,2.5)$   
 $B_{30}$        $N(11,13)$ ,  $R = (1E7,2.5)$   
 $B_{31}$        $N(13,0)$ ,  $C = 10E-6$   
 $B_{32}$        $N(13,0)$ ,  $R = 4.5 E7$   
 $B_{33}$        $N(13,0)$ ,  $R = 1.0 E3$   
 $B_{34}$        $N(0,14)$ ,  $R = 50$   
 $E_{34}$        $P(5E-5)$ , 8, -8, 8  
 $B_{35}$        $N(14,0)$ ,  $R = 1E7$   
 $B_{36}$        $N(0,15)$ ,  $R = 50$   
 $E_{36}$        $P(5E-5)$ , -8, 8, -8  
 $B_{37}$        $N(15,0)$ ,  $R = 1E7$   
 $S_1$        $B = 34$ , (2,5,8,9,12,13,16,17,20,21,24), ON  
 $S_2$        $B = 36$ , (25,26,27,28,29,30), OFF

Time step =  $5E-6$

Output Interval = 1

Final Time =  $1E-1$

TAB, BV(1,33), I(1,33), P(1,33)

Ex

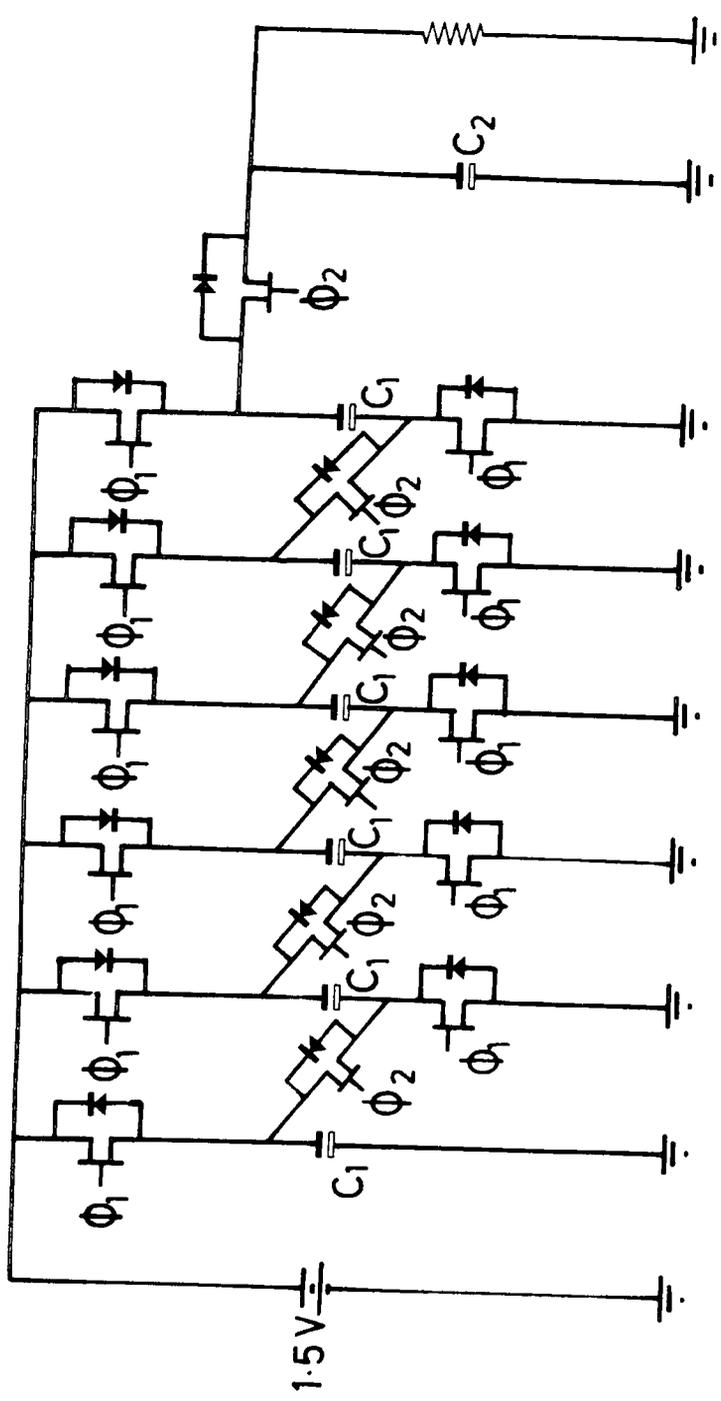


FIG 4-25

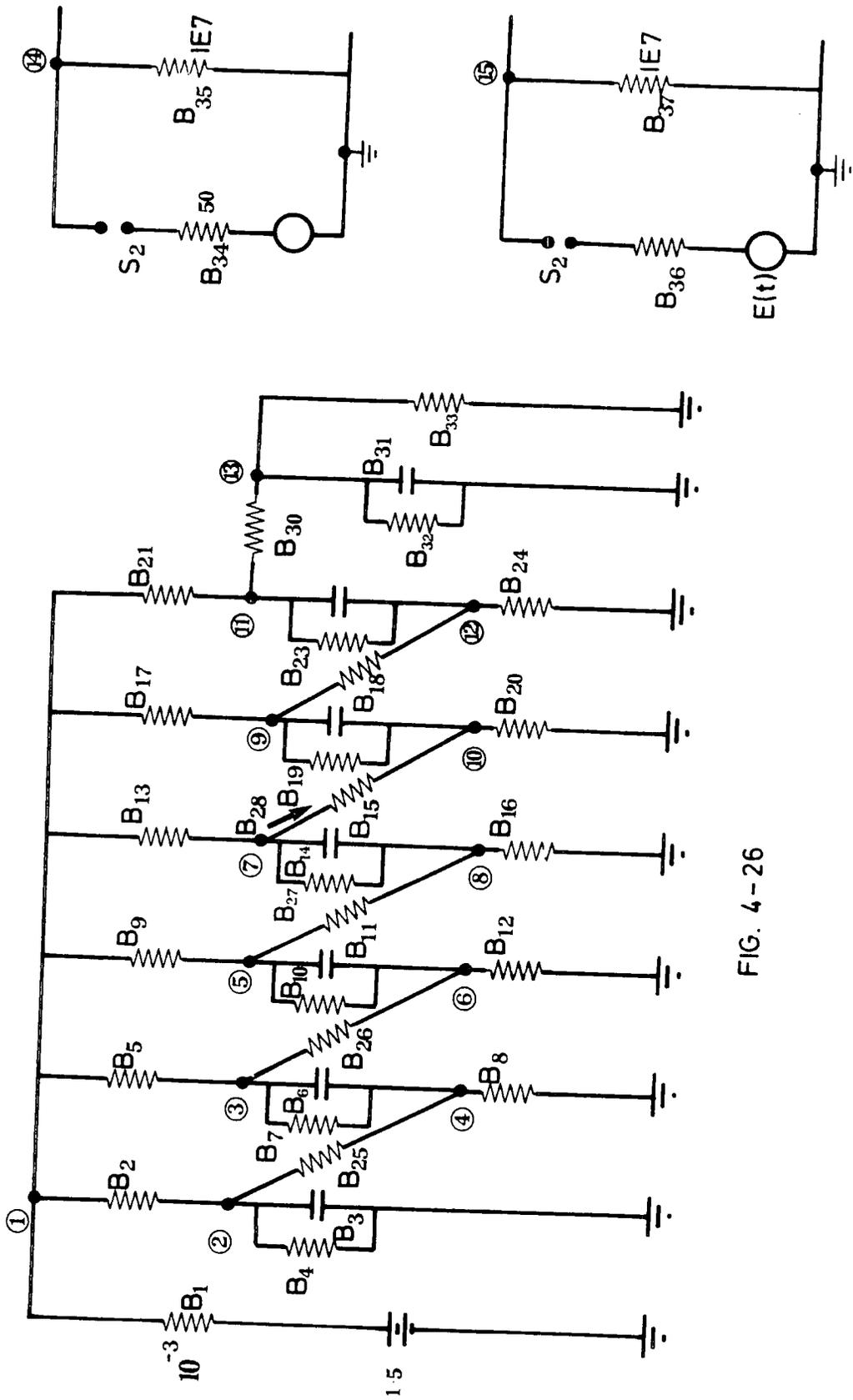


FIG. 4-26

## 5.1 Introduction

This chapter is concerned with the experimental measurements of output voltage, input current, efficiency and output ripple for various switching frequency, drive clocks and load resistance.

The experimental results are not strictly comparable with the computer simulation results due to the difference between the two circuits (The output voltage is unregulated in the computer simulation circuit and regulated in the other).

## 5.2 The effect of the switching frequency on the circuit

This section explains the effect of the switching frequency on the circuit in three different cases and the experimental results are compared with the computer simulation.

Case 1 Figures (5-1, 2,3) show the following -

1. Over a range of switching frequency from 5 to 100 KHz the efficiency is fairly constant. Above 100 KHz the efficiency begins to decrease because of a portion of input power is lost during the transition as switches are turned OFF and ON and losses increase with increasing switching frequency. Below 5 KHz the efficiency increases with increasing switching frequency and this result agrees with the computer simulation results.
2. The efficiency and the input current are not substantially affected by the value of the output capacitor ( $C_2$ ). The computer simulation shows the same effect.
3. The ripple decreases with increasing switching frequency and with increasing output capacitor value ( $C_2$ ). This is similar to the computer simulation.

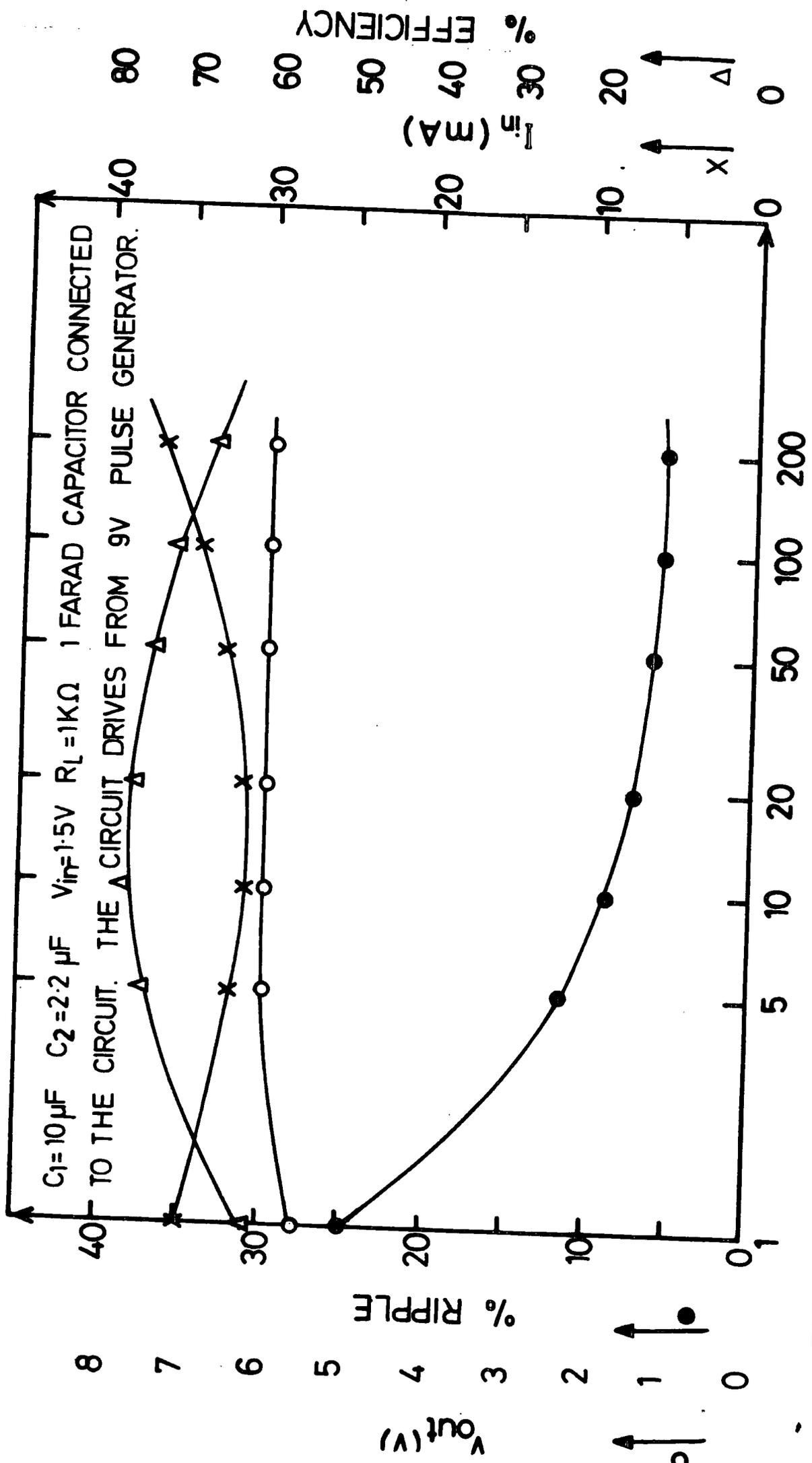


FIG. 5-1

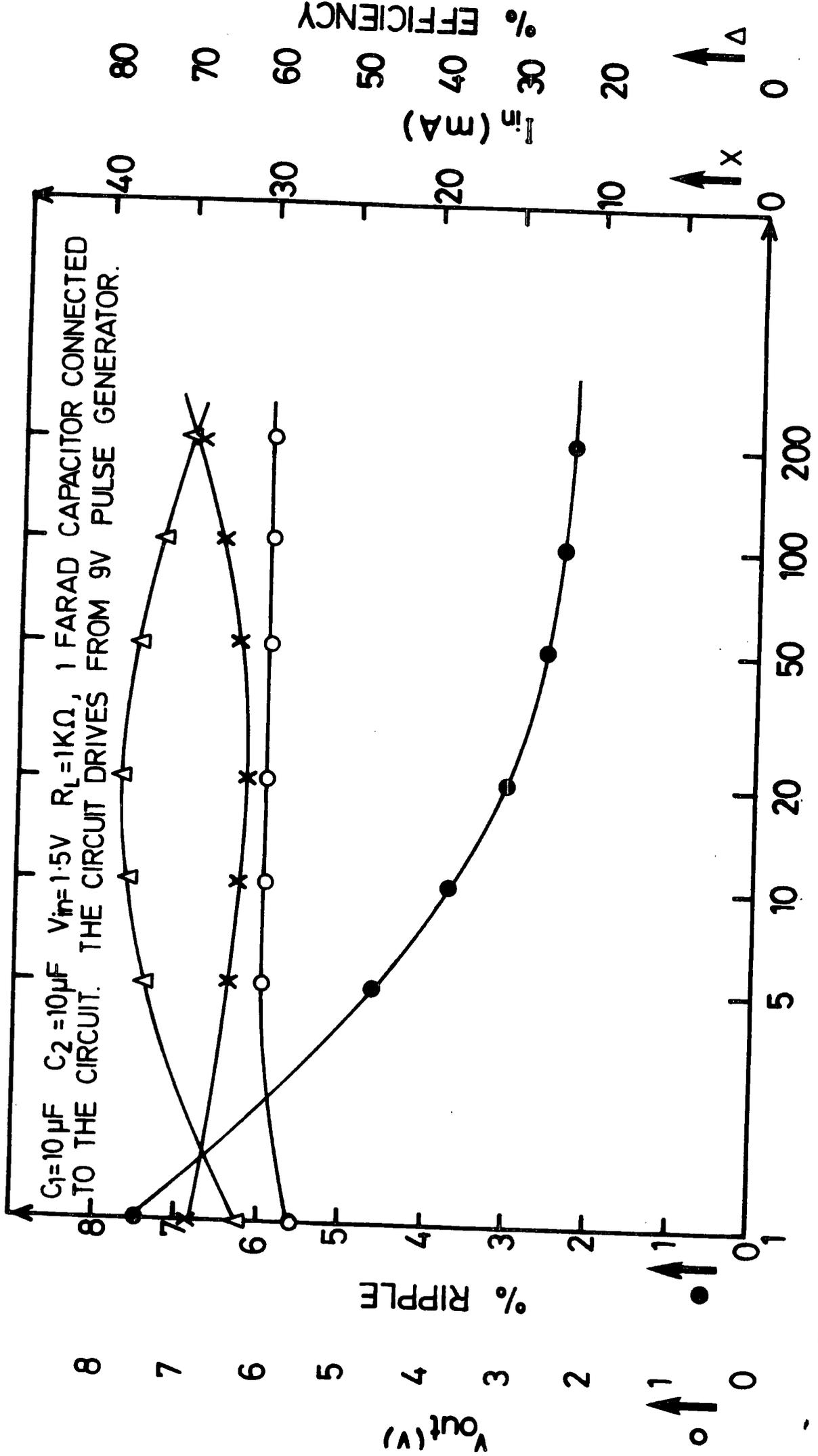


FIG. 5-2

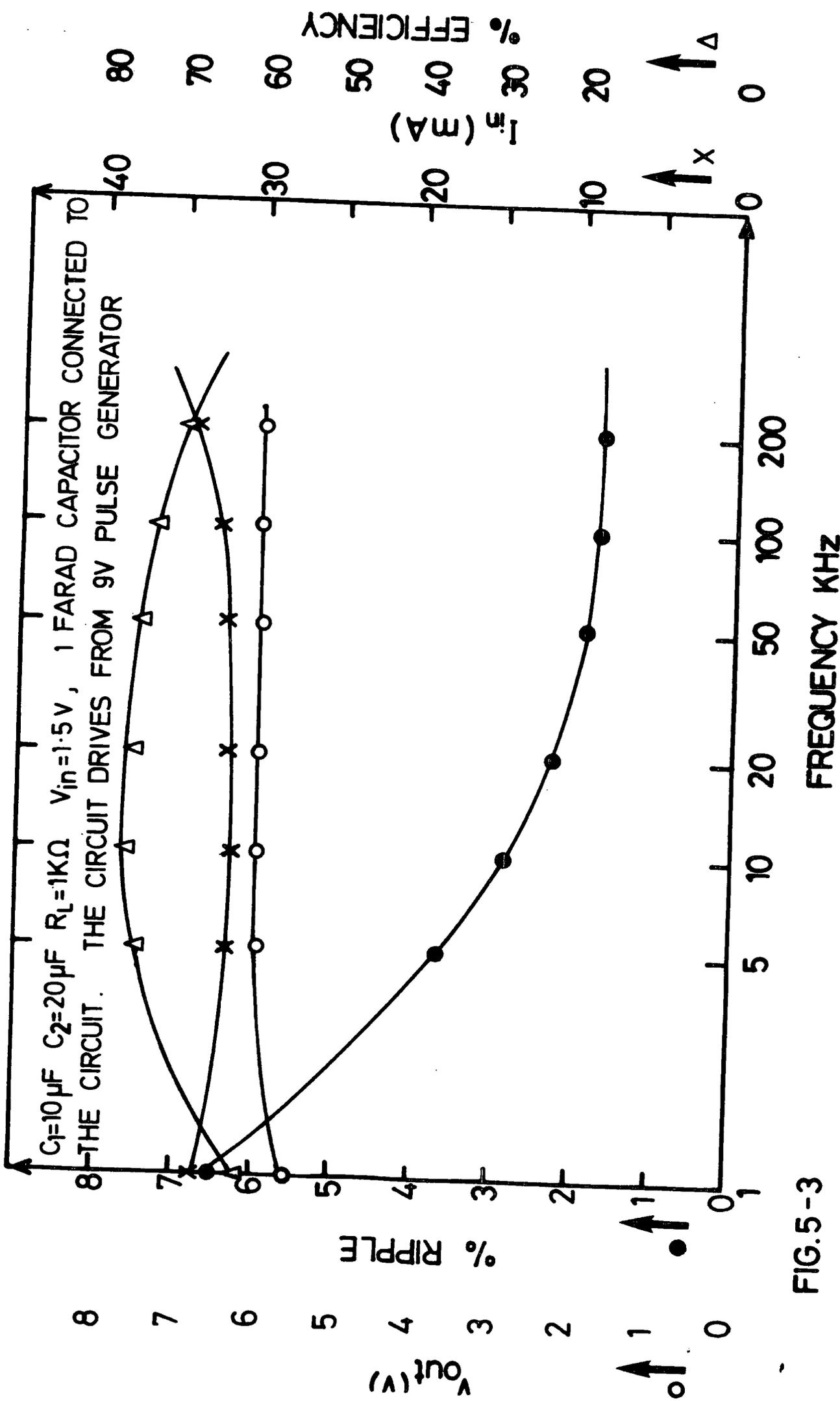


FIG.5-3

4. The relation between the input current and the switching frequency is opposite to the relation between the efficiency and the switching frequency. This is expected because the output voltage is constant.

5. Between 5 and 200 KHz the output remains fixed at 6 V. However at 1 KHz the output voltage is less than 6 V which agrees with the computer simulation.

Case 2. Figures (5-4, 5,6) show the following -

1. The efficiency and the input current are fairly constant over a range of switching frequency from 10 to 100 KHz. Below 10 KHz the efficiency increases while the input current decreases with increasing switching frequency. This is similar to the computer simulation results. Above 100 KHz the efficiency decreases and the input current increases as the switching losses increase.

2. The efficiencies in Figures (5-4, 5,6) are less than the efficiencies in Figures (5-1,2,3). This again agrees with the computer simulation.

3. Similar to Figure (5-1,2,3), the efficiency and the input current in Figures (5-4,5,6) are not substantially affected by output capacitor value ( $C_2$ ). The computer simulation shows the same effect.

4. Similar to Figures (5-1,2,3), the ripple in Figures (5-4,5,6) decreases with increasing switching frequency and with increasing output capacitor ( $C_2$ ).

5. Between 20 and 200 KHz the output voltage remains fixed at 6 V. Below 20 KHz the output voltage is less than 6 V and decreases with decreasing switching frequency. This again agrees with the computer simulation.

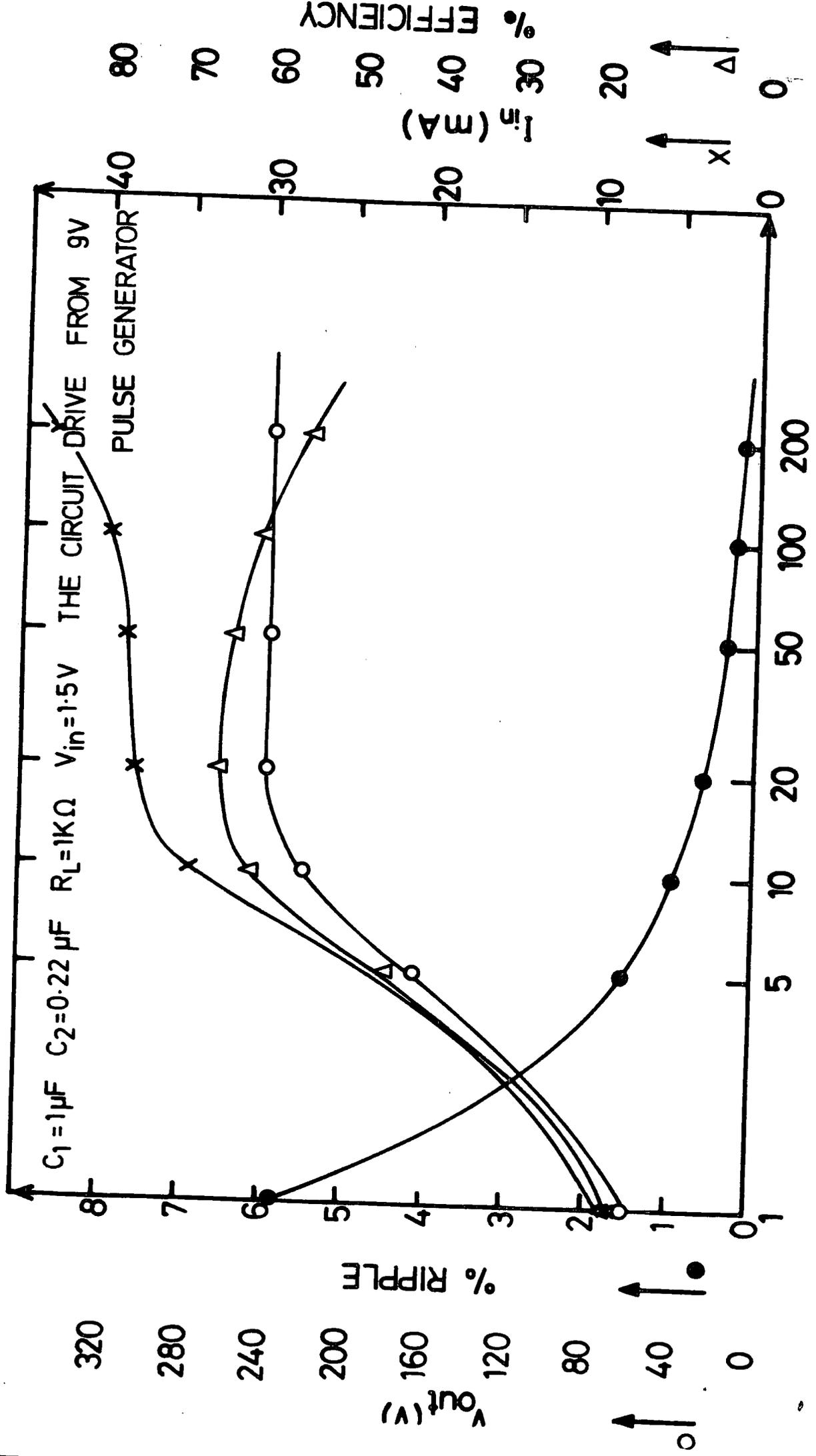


FIG. 5-4

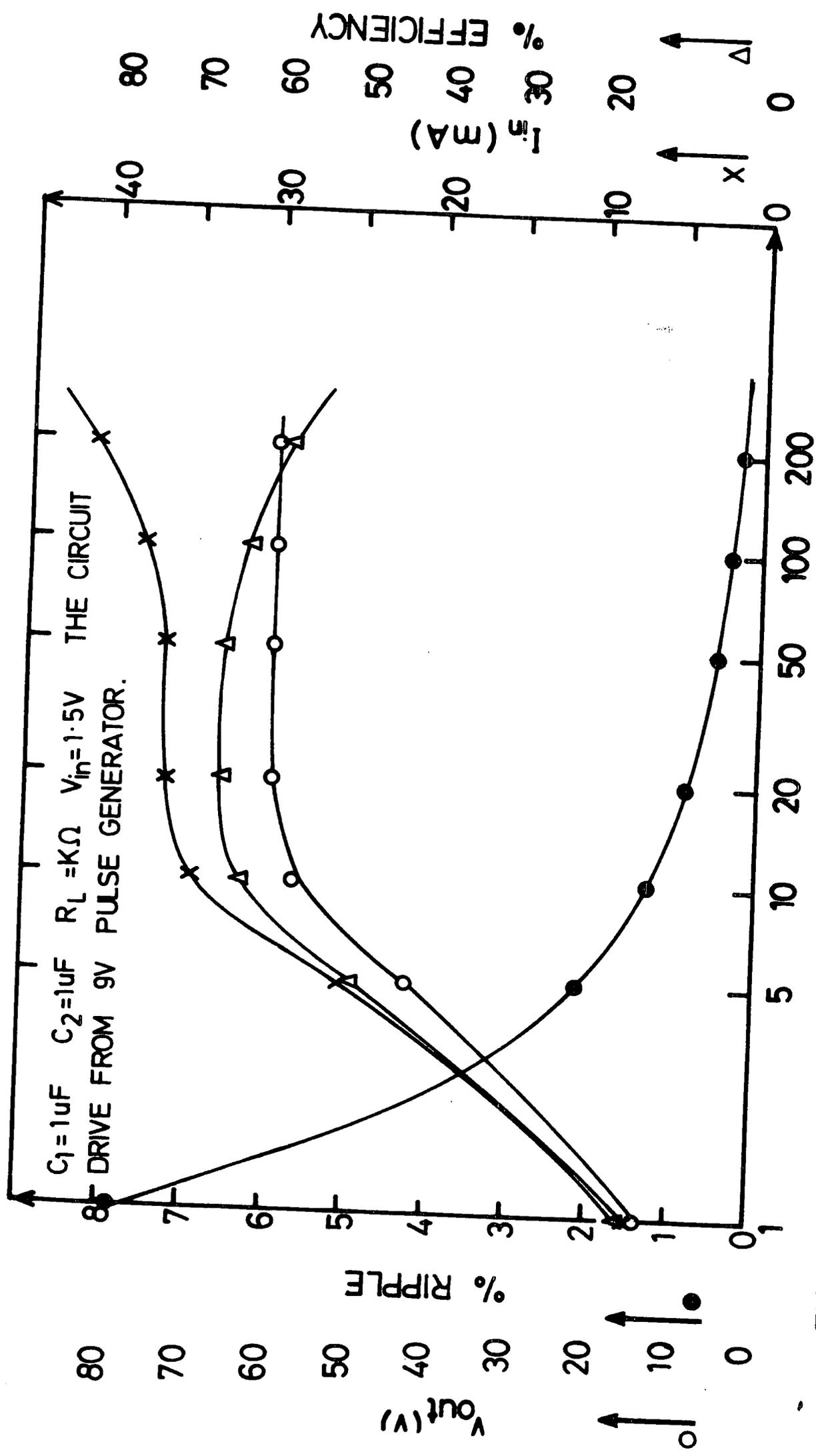


FIG. 5-5

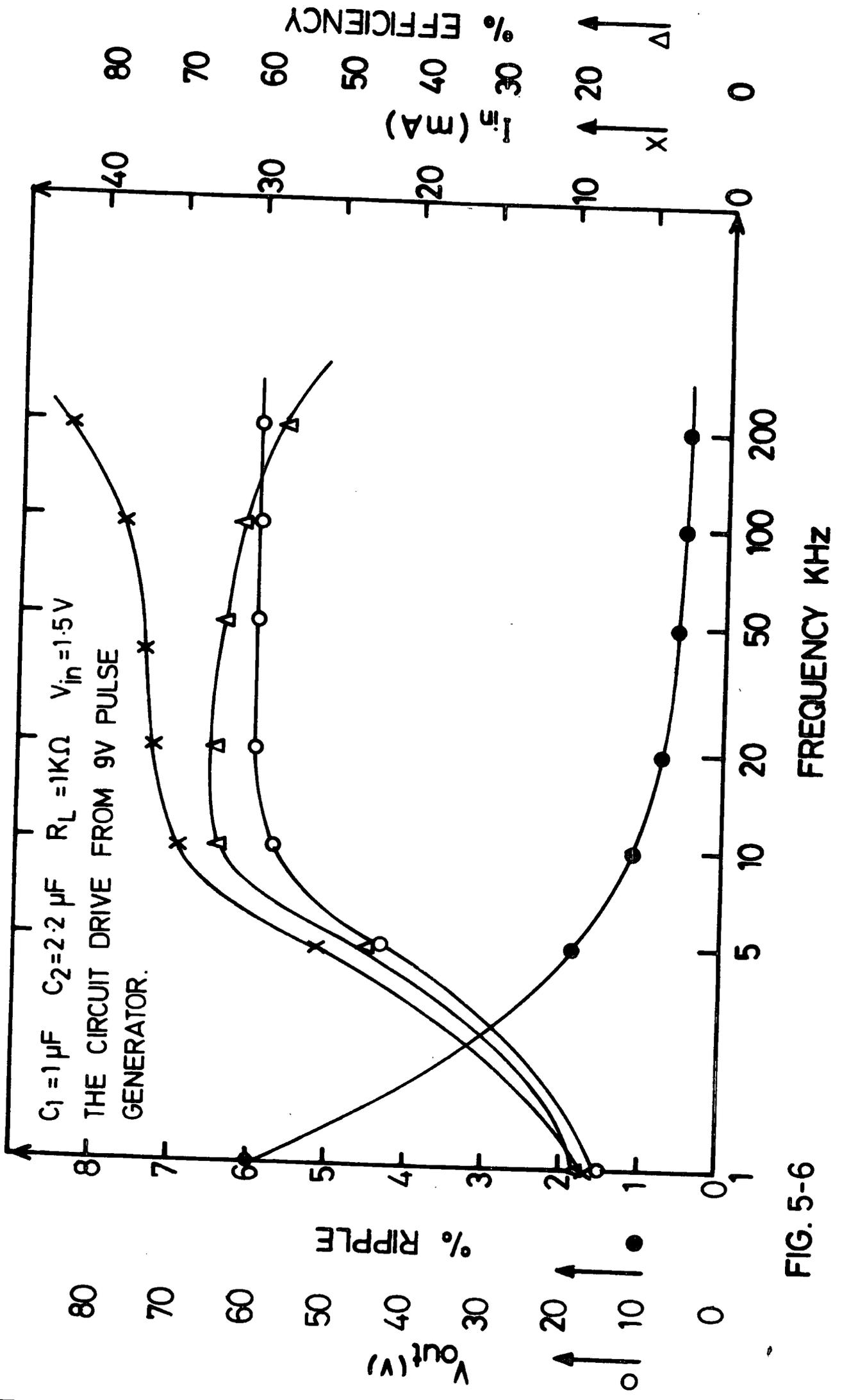


FIG. 5-6

Case 3 Figures (5-7,8,9) and Figures (5-1,2,3) are similar except the output voltage in Figures (5-8,9) at 1 KHz is 6 V.

### 5.3 The effect of the load current on the circuit

This section demonstrates the effect of the load current on the circuit in two different cases.

Case 1 Figures (5-10,11,12) show the following -

1. Regulation at 6 V is maintained for load currents up to 10.5 mA. Above 10.5 mA the output voltage falls.
2. The input current increases with increasing output current in a linear relation as predicted by the computer simulation.
3. Below 3 mA, the efficiency decreases with decreasing load current. Above 3 mA the efficiency decreases with increasing load current. Maximum efficiency is 78% at 3 mA.
4. Over the regulated part of output voltage, the ripple has no regular relation with load current and the value is higher than the value at an unregulated output voltage. This is due to the switching in the stabilizer. For unregulated output voltage the ripple increases with increasing load current. This again agreed with the computer simulation.
5. The efficiency, the output voltage and the input current are not substantially affected by output capacitor value ( $C_2$ ). The computer simulation shows the same effect.

Case 2 Comparing Figures (5-10,11,12) with Figures (5-13,14) we can see that -

1. In Figures (5-13,14), regulation at 6 V is maintained for load currents up to 23 mA. Above 23 mA the output voltage falls. This is because of the circuit being driven from 15 V clock waveform and ON

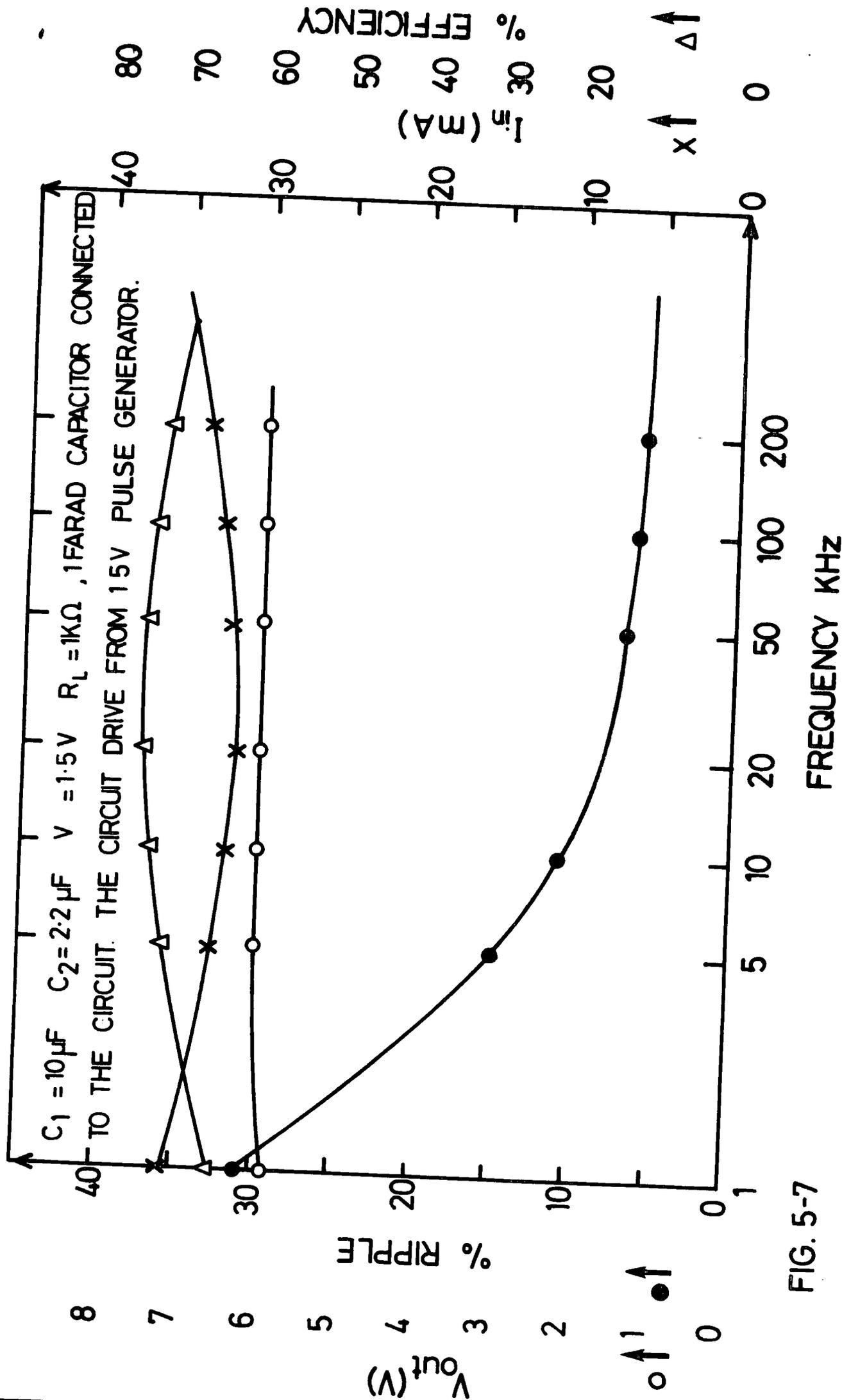


FIG. 5-7

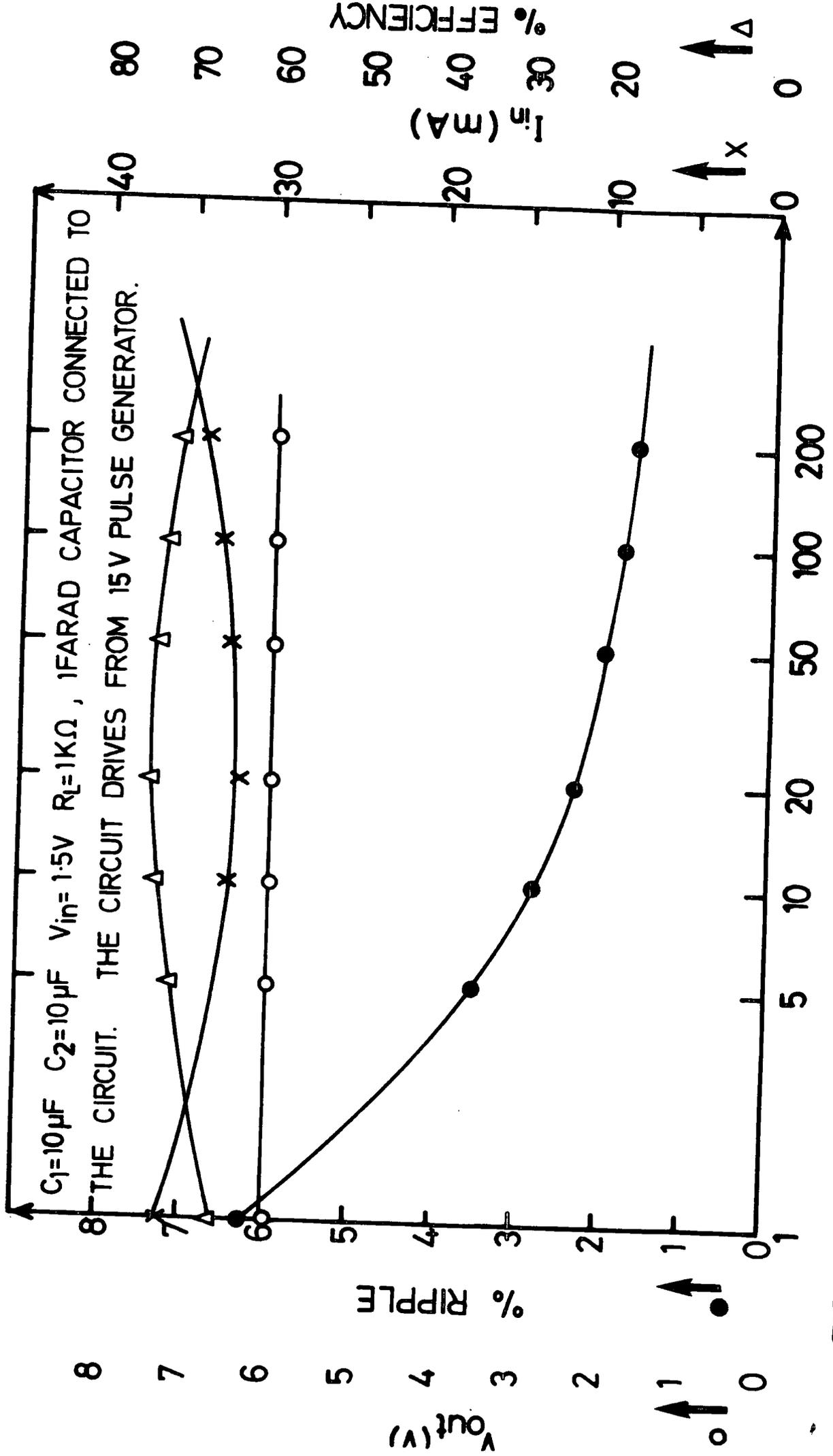


FIG. 5-8

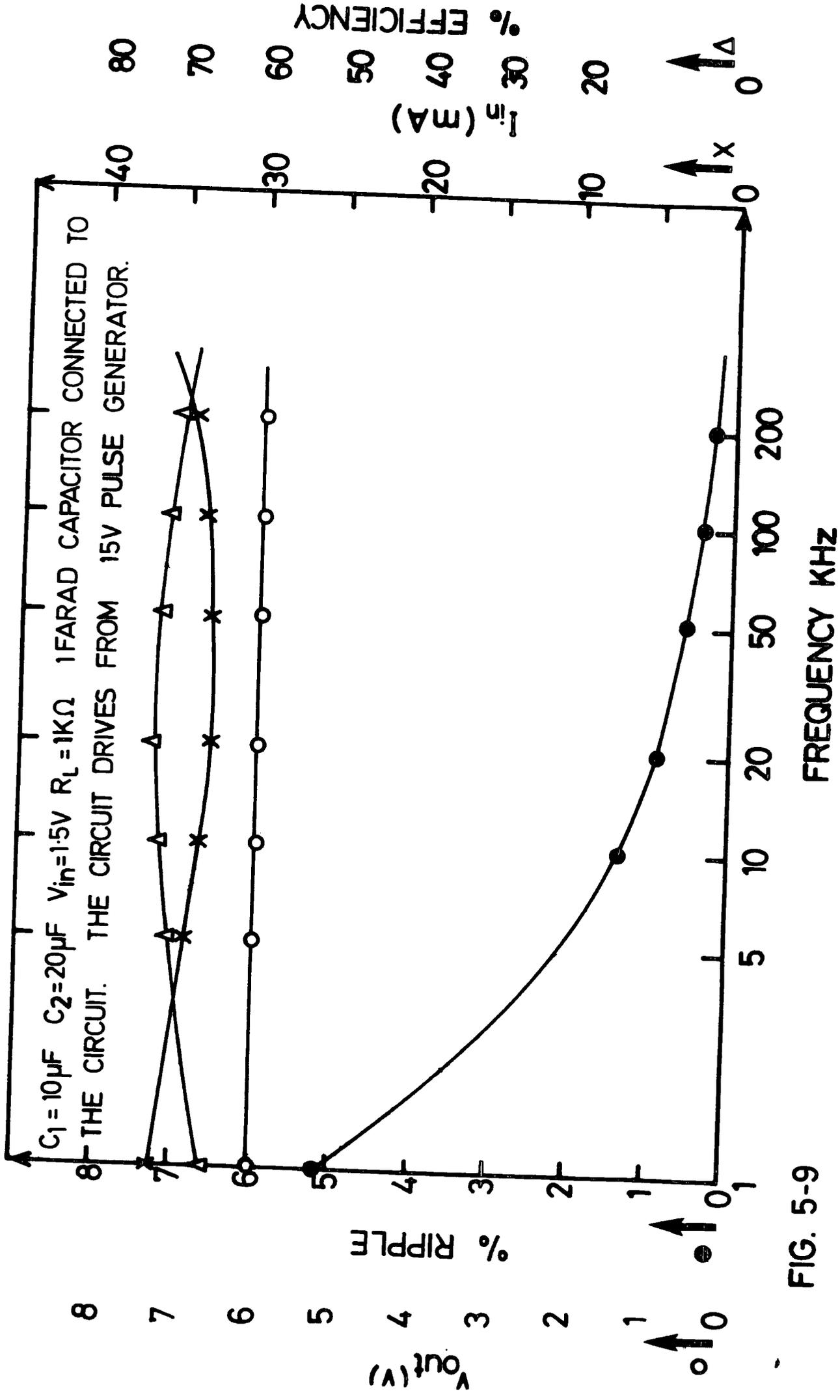


FIG. 5-9

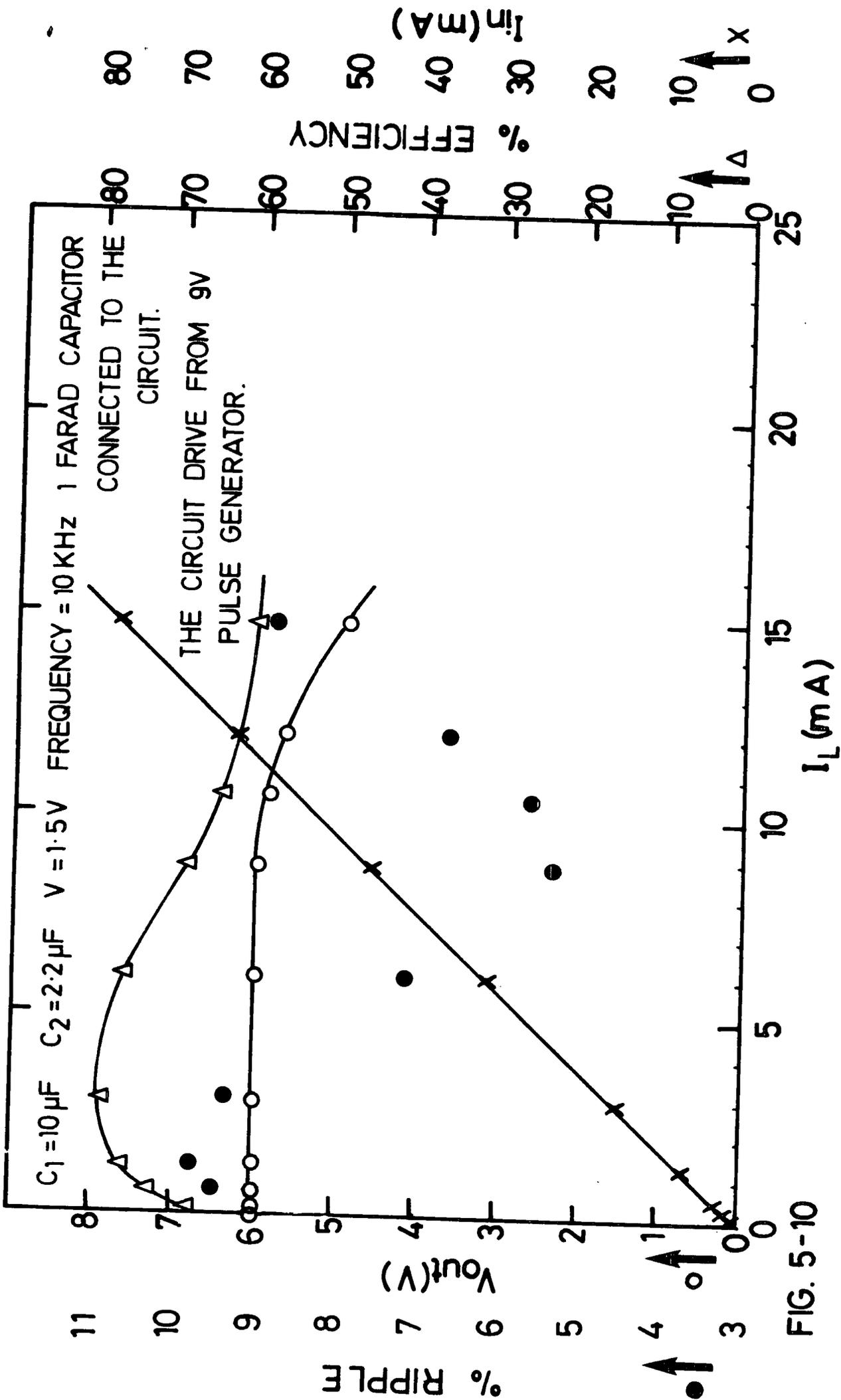


FIG. 5-10

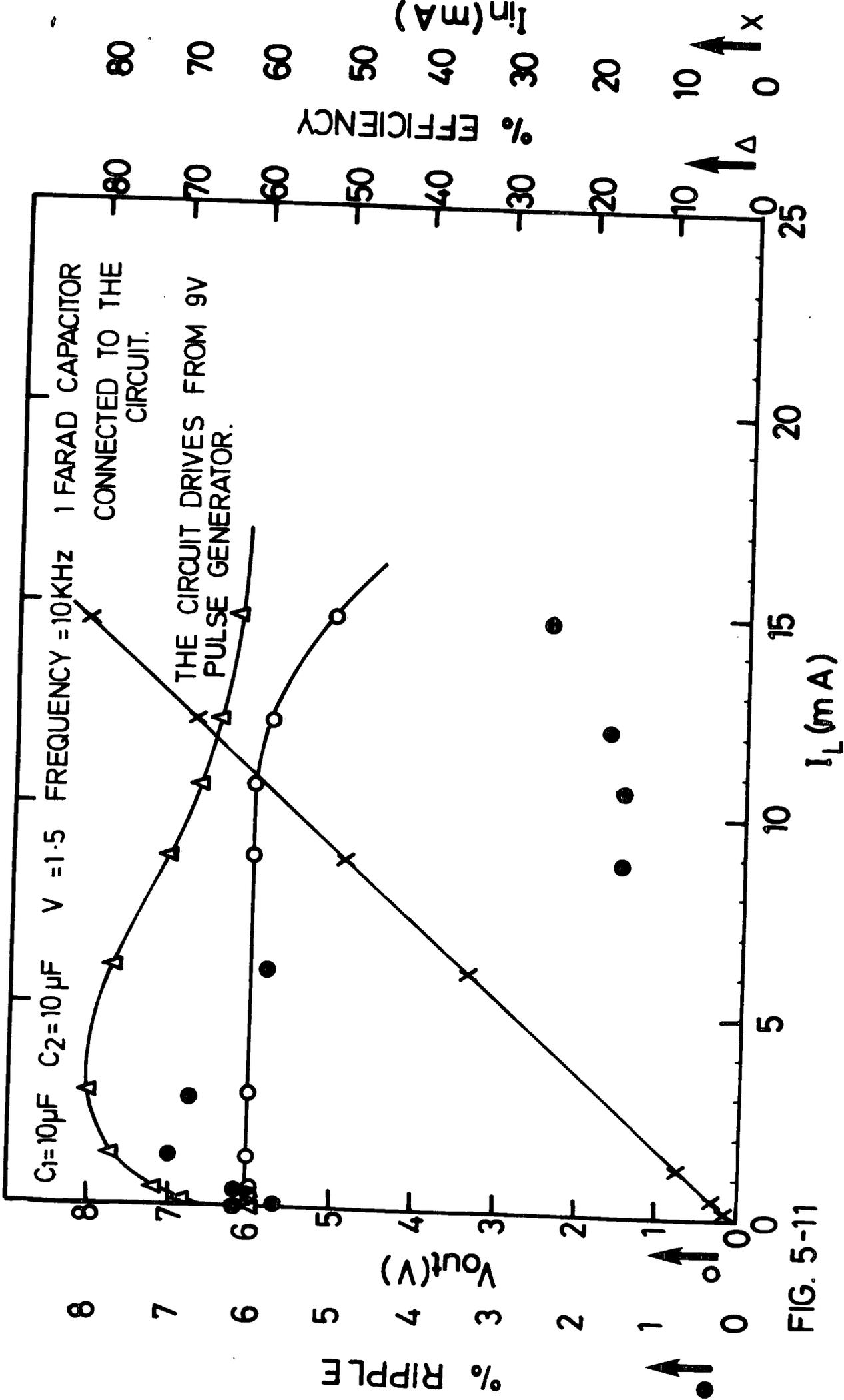


FIG. 5-11

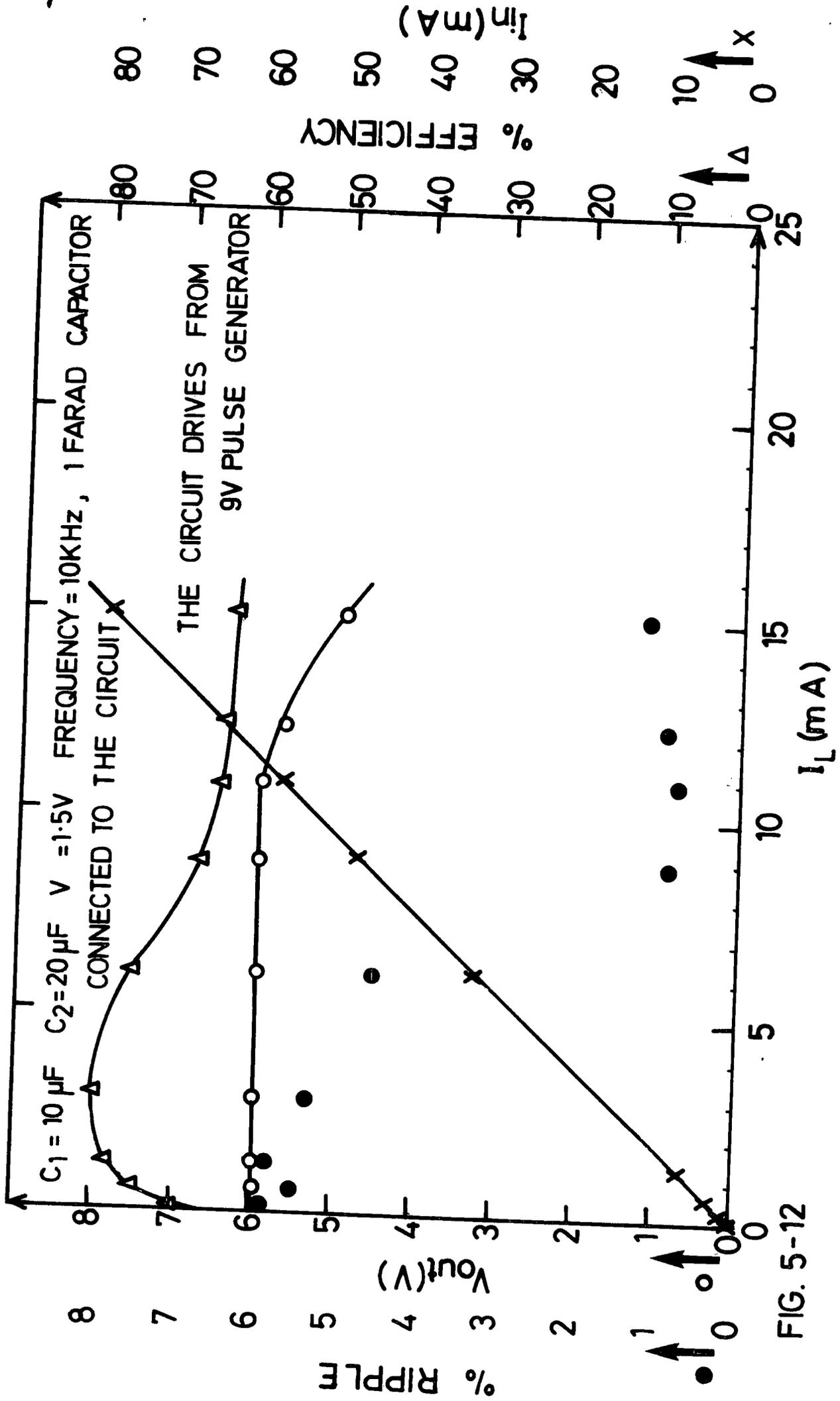


FIG. 5-12

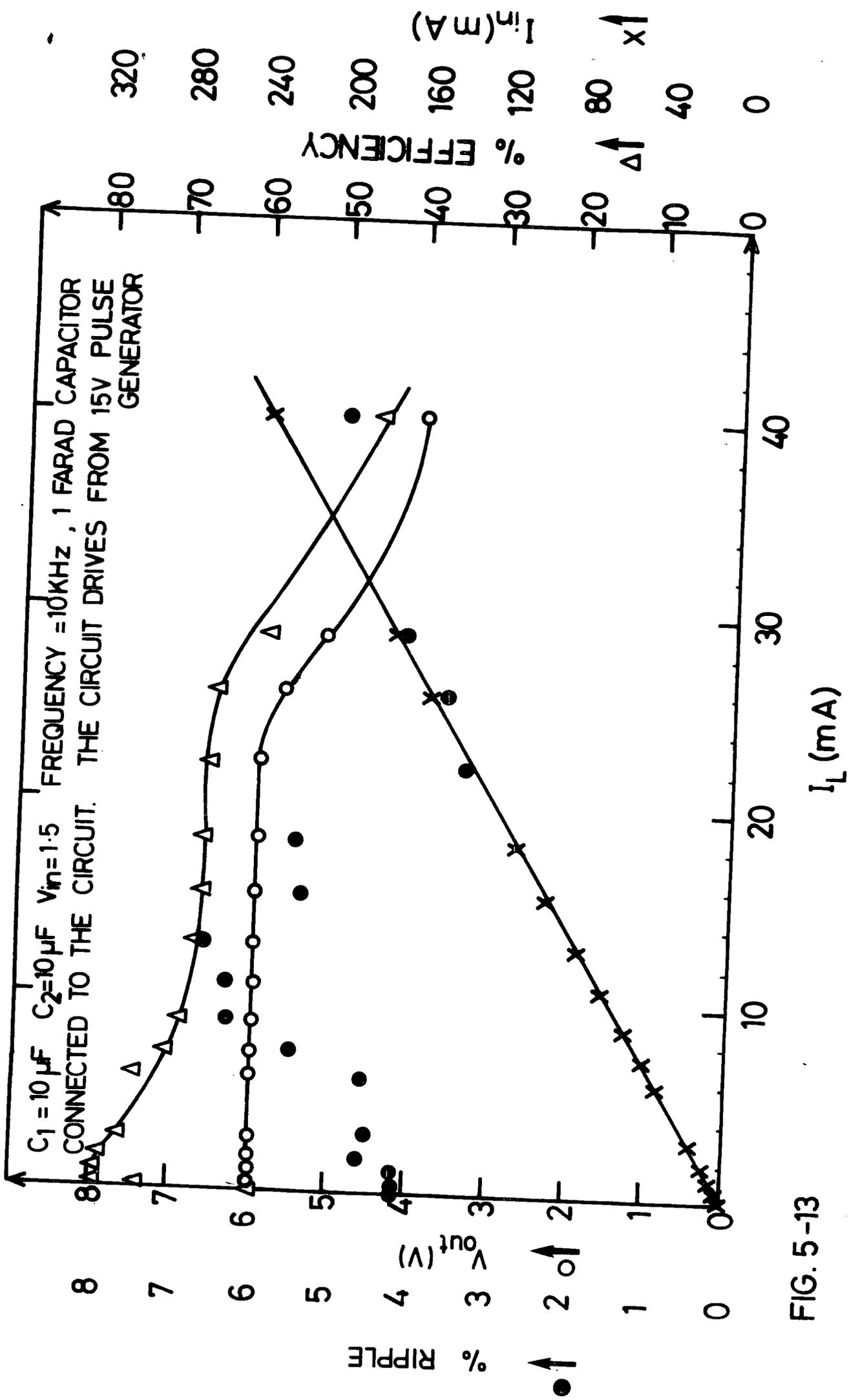


FIG. 5-13

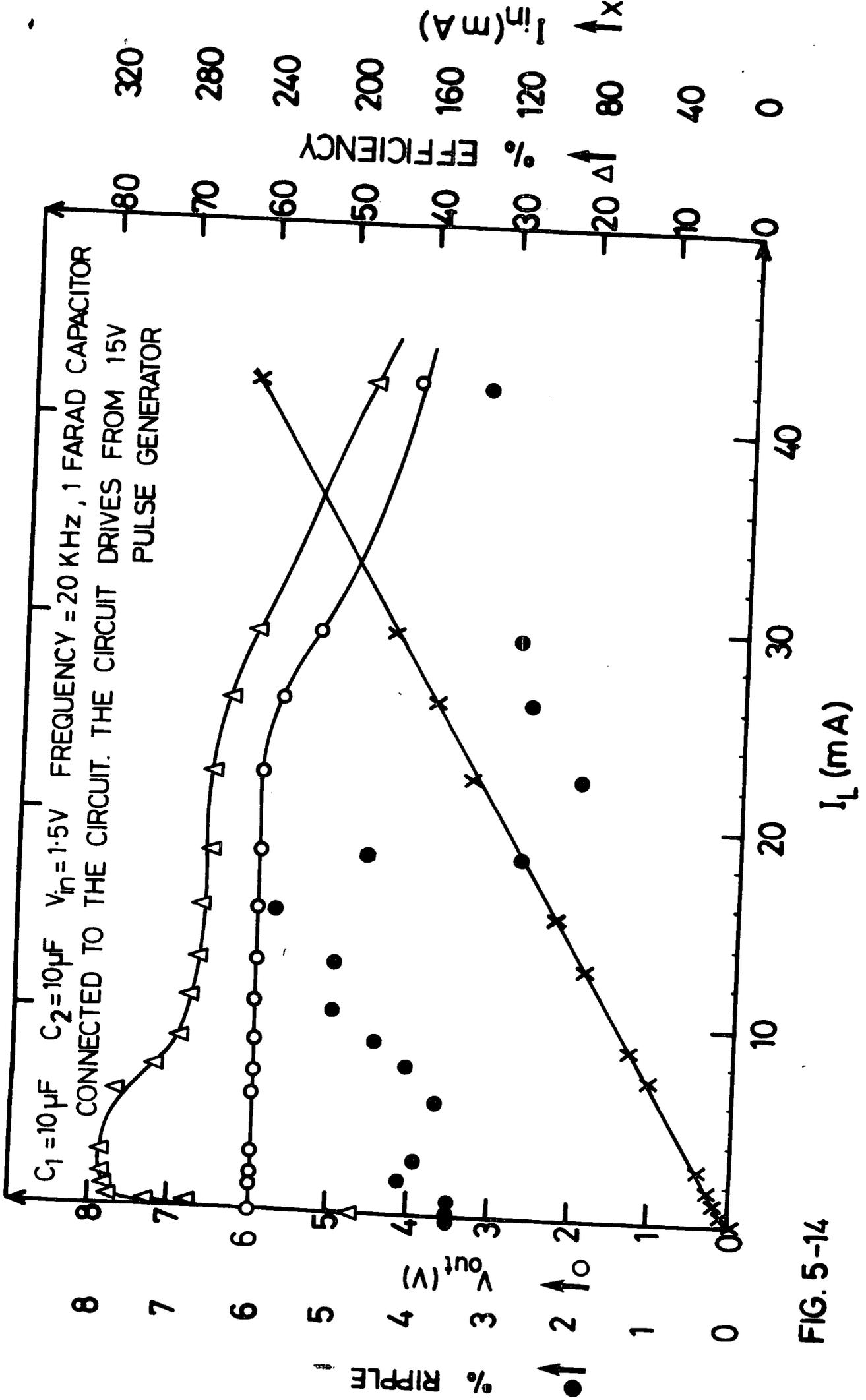


FIG. 5-14

resistance of VMOS transistor decreases when the driving voltage increases.

2. Maximum efficiency is about 80% at 2 mA and at 26 mA the efficiency is 67%. The computer simulation gives an efficiency of 80.3% at 2 mA.

#### 5.4 Measuring the average input current

The input current drawn by the converter has a pulse waveform. To reduce the error in measuring the average of this waveform a high value (1 Farad) capacitor was connected across the input terminals as shown in Figure (5-15). The leakage current of the capacitor was experimentally found to be  $10\ \mu\text{A}$  and this was neglected as being negligible compared with the input current.

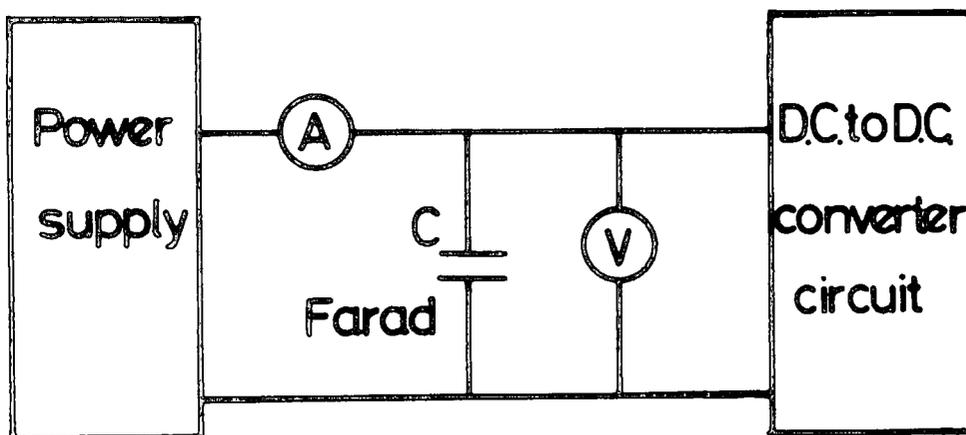


FIG. 5-15.

## CONCLUSIONS

The work presented in this thesis was concerned with a method of conversion DC Voltage to another higher DC Voltage. The circuit used VMOS switches in a flying capacitors technique to generate regulated 6 volts from single cell about 1.5 V.

The computer simulation gave efficiencies of 80.3% and 62% at 2 and 27 mA respectively and these results were confirmed by the experimental measurements.

The computer simulation showed that the efficiency is significantly affected by the ON resistance of the switches. For example at a load resistance of 1 K $\Omega$ , the efficiency was 97.7% when ON resistance of switch was 0.3  $\Omega$  and it fell to 74.4% when the ON resistance was 2.5  $\Omega$ . The ON resistance of a VMOS transistor can be reduced by increasing the driving voltage. Further reduction could be achieved by increasing the width/length ratio of the channel, and some other parameter (oxide capacitance, carrier mobility).

Since a VMOS transistor operates as a switch the power dissipated in it is low so the transistor does not need a heat sink but it does need to stand high peak currents when the ON resistance is low. For example, if the ON resistance is 0.3  $\Omega$  and the supply voltage is 1.5 V, the transistor has to stand a peak current of 5 amp. In theory a dc-to-dc convertor can approach 100% efficiency if certain conditions are met.

1. The drive circuit and the control circuit consume minimal power.

2. The equivalent series resistance of capacitor is very low and parallel leakage resistance is very high.
3. The switches have extremely low ON resistance and very high OFF resistance.

Since the VMOS transistor has very high input resistance (which can be greater than  $10^{14} \Omega$ ) and operated at low drain-source voltage these make the gate leakage very low and simplify the driving circuit.

The object of this project was to investigate the flying capacitor technique itself and no attempt was made to minimize the power consumption of the drive and control circuits.

In a practical application it would be necessary to reduce this power consumption overhead and the use of MOS circuitry should enable the loss to be kept to about a 1 mW. This would then have little effect on the overall efficiency.

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