Cadmium telluride for solar cells

G. R. Awan

Dedicated to my parents

" Thy Lord hath decreed, that ye worship none save Him, and (that ye show) kindness to parents. If one of them or both of them attain old age with thee, say not "Fie" unto them nor repulse them, but speak unto them a gracious word".

(Qura'n XVII : 23)

CADMIUM TELLURIDE FOR SOLAR CELLS

by

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CONTENTS

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ABSTRACT

Cadmium telluride is an attractive material for solar cell applications because of its near optimum bandgap and high absorption coefficient. This thesis presents the results of a study into the use of CdTe for solar cells. Three types of cell have been investigated, namely; CdS/CdTe devices fabricated by the vacuum evaporation of CdS onto either: (a) single crystal p-CdTe substrates or (b) p-CdTe thin films, and (c) p-Cu_2Te/n-CdTe devices made by a chemiplating process onto single crystal n-CdTe.

The effects of substrate polishing and preparation on the performance of CdS/CdTe bulk crystal cells have been investigated together with the problems of doping and contacting to p-type CdTe. These studies have shown that the best results are obtained with devices that have been prepared on pad polished, phosphorus doped substrates using carbon contacts (efficiency = 7.2%). The influence of deposition conditions on the electrical and structural properties of thin CdS and CdTe layers, and their effect on CdS/CdTe device efficiency were also studied, and optimum growth conditions established. In the third group of Cu_2Te/CdTe solar cells a number of structural and electrical aspects such as the phase of Cu_2Te, and the influence of dopants, substrate resistivity and preparation and ageing on cell efficiency have been examined.

As secondary objectives, an investigation into the epitaxial growth of CdS on CdTe, and the characterisation of as-grown and doped CdTe have been carried out. It has been shown that epitaxy is possible on the {111} and {221} faces of CdTe. The characterisation of CdTe has revealed the presence of dominant levels at energies above the valence band of 0.50 eV in the as-grown crystals; 0.53, 0.71 and 0.84 eV in Te-annealed single crystals; and 0.35 eV in Cu doped CdTe thin films.

CHAPTER 1

INTRODUCTION

1.1 Terrestrial Solar Cells

The rapid growth in the world population together with the development of a more advanced technological age has resulted in an increased demand for energy. At present the energy needs are satisfied mainly by fossil fuels and in the more developed countries in part by nuclear power. Conventional fossil fuels such as coal, oil and gas are finite and will run out in the foreseeable future since these fuels are being consumed much faster than they are being produced. Geological formation of these fuels takes 600 million years while modern rates of consumption are measurable in centuries. Although new reserves are continually being discovered, the most readily accessible and cheapest supplies are being steadily depleted.

The future viability of nuclear power is also in question. Already serious shortages are being predicted in the supply of relatively inexpensive uranium-235 within the next two decades. The development of breeder reactors that can consume the more plentiful uranium-238 (and thorium) should, in principle, give an energy supply hundreds of times greater than all the fossil fuels combined, but of course, reserves are still finite and depletion is again the end result. Moreover, both fossil fuel and nuclear power generation inject an undesirable level of pollution into the environment. The recent disasters at Chernobyl and Three Mile Island, and the reports of leakages in nuclear power and reprocessing plants in the Western world have very clearly pointed out the dangers accompanying nuclear energy. Public anxiety over safety may well prevent the full exploitation of nuclear power.

This situation in conjunction with the substantial increase in the price of oil during the 1970's has produced a general public awareness that alternative renewable, cheap, clean and reliable energy sources must be explored to supplement, and eventually supplant conventional fossil fuel and nuclear resources. Among the potential alternatives, solar energy, especially the direct conversion of sunlight into electricity is very attractive. Despite its disadvantage of having low flux density with large diurnal and temporal variations, solar energy (fuel) is clean, free, renewable, dependable, predictable and importantly is distributed more evenly and equably around the populated World than any other energy source. For example, seventy percent of the World's known crude oil reserves are in the Middle East and North America[1]. In addition to its democratic distribution, solar fuel is immune to trade embargo and does not require any infrastructure for its delivery, and no foreign exchange. Of course, solar power technology will doubtless be subject to trade embargo and involve nominal foreign exchange. But it would not require recurrent expenditure on the same scale as in the case of fossil fuels and nuclear energy.

Clearly, photovoltaics hold considerable promise to provide a reasonable proportion of the World's energy needs. The direct conversion of solar energy into electricity via photovoltaic devices called solar cells is already an established field of science and technology. The self-contained nature and ideal modular flexibility of photovoltaic systems permits their effective use for different applications. Commercial applications include remote microwave repeater stations, navigational aids, railway signals, telecommunications, cathodic protection of bridges and pipelines, and electrification of villages in which petrol or diesel engines cannot be fuelled or serviced.

Major developing applications include water pumping, remote lighting, and residential and commercial electricity. One of the recent uses of solar energy is to provide educational classrooms in remote areas where teachers are not available. A very successful television classroom system has been established in the Ivory Coast[2] where 20,000 remote television classrooms are educating the children. Such services provided through photovoltaic power can improve rural community life, restrain outmigration to the cities, and thus reduce the expenditures involved in urbanization.

Third World developing countries find a special interest in solar energy. With their rural and agro-industrial base they need stand-alone, fuel free and reliable systems for electrification of remote villages where the extension of a central grid would be very expensive. Moreover, almost all the developing countries are situated in the sunbelt of the World. By the end of the present century 40% of the World population will live in the villages of Third World countries, and thus distributed generation of electricity will be necessary. It is in such decentralised power generation that photovoltaic systems offer their greatest potential.

1.2 The Photovoltaic Effect

The photovoltaic effect is the creation of an electromotive force by the absorption of light (or any ionizing radiation such as x-rays, γ-rays) in an inhomogeneous system. It is to be distinguished from any thermoelectric effect caused by localized heating and the Dember effect[3] which results from non-uniform illumination in a homogeneous photoconductive material. When an ionizing radiation such as light is incident on the surface of a photoconductor, it produces electron-hole pairs which diffuse to the non-illuminated region and are responsible for the Dember voltage which can be measured by a suitable contact geometry.

The essential conditions for a photovoltaic effect to exist are; (1) the absorption of light and generation of electron-hole pairs, (2) the separation of the electrons and holes across an internal electric field created by some inhomogeneity in the system (i.e. a p-n junction),(3) and the collection of charge carriers for transmission to external circuit. The discovery of the photovoltaic effect is not as recent as is commonly supposed, although the most significant advances have been made since the 1950's. The effect was first reported in the 19th century when Becquerel[4] in 1839 observed that when two electrodes were immersed in a liquid electrolyte and one was exposed to light a potential difference developed between the electrodes. A similar effect was observed by Adams and Day[5] in 1877, shortly after the discovery of photoconductivity in selenium by Smith[6] in 1873. Adams and Day investigated the effect of light on the currents flowing in a selenium sample with platinum contacts, and discovered that the action of light incident on the positively biased end of the sample was to reduce the current whilst light falling on the negatively biased end caused an increase. They also observed that an E.M.F. could be developed across the sample when both the contacts were illuminated. The existence of an E.M.F. was confirmed by Fritts[7] who produced a selenium cell with a transparent gold counter-electrode. Minchin[8] developed the first thin film cell by oxidizing chemically a tin foil to give a tin-tinoxide cell. He named these cells "impulsion cells" since they needed to be flicked with the finger in order to make them work. Minchin was probably the first person to suggest the photovoltaic conversion of sunlight.

Further work in the 1930's on selenium[9] and Cu-Cu0[10,11] pioneered the way to the successful development of the exposure meter in photography. In 1954 Reynolds et al[12] discovered the photovoltaic effect in Cu/CdS single crystal junction and this work led to the

development of the Cu_2S/CdS thin film solar cell in the 1960's[13-15]. However, in April 1954 Chapin et al[16] made a significant discovery which is normally recognised as the start of the modern history of solar cells. They produced a 6% efficient p-n junction cell on single crystal silicon. This device was commercialised the following year and the first silicon solar cells rode in Russian and American space satellites.

In the 1970's the potential of solar cells for terrestrial applications was also realised and research activity in this field expanded quite rapidly. Continued efforts during the last fifteen years to fabricate high efficiency solar cells have succeeded in producing single crystal Si and GaAs solar cells with efficiencies in excess of 20% and 25% respectively. However, the high cost GaAs and Si single crystals made these cells too expensive for wide terrestrial applications. Therefore, many different materials have been investigated for low-cost solar cell production and consequently, amorphous silicon, copper indium diselenide and cadmium telluride have emerged as leading candidates for low cost thin film solar cells. Devices with more than 10% efficiency have been fabricated from these materials.

1.3 The Present Work

Cadmium telluride is a strong contender for terrestrial low cost solar cells and CdTe based solar cells with efficiencies in excess of 10% have been produced by a number of different techniques. However, there is still ample scope for research on many aspects of the material before photovoltaic devices from CdTe become commercially viable for wide use. The primary motivation behind the present study was an investigation of the potential of CdTe for solar cells both from the material and device fabrication point of view.

This thesis begins with a general discussion of the terrestrial use of solar cells and of their historical background. Chapter 2 describes

the general characteristics of solar cell devices, the specification of a good solar cell material and the role of CdTe in solar cells. The third Chapter gives a brief review of the principles of operation of photovoltaic and related devices with reference to current transport mechanisms. The details of the experimental work (crystal growth, materials analysis, RHEED, SEM and other diagnostic techniques) are outlined in Chapter 4 and 5.

The bulk of the original experimental results are presented in Chapters 6 to 10. The results of measurements of the electrical properties of bulk single crystal CdTe using Space Charge Limited current and DLTS techniques are given in Chapter 6. Chapter 7 describes the findings of an investigation of bulk CdTe/CdS heterojunction devices, and includes studies of the use of different contact materials (such as carbon and gold) with p-CdTe, the effect of heat treatment and ageing on device performance and the measurement of minority carrier diffusion length. The experimental results of parallel studies in CdTe/Cu_2Te heterojunction solar cells are reported in Chapter 9. Chapter 8 details the electrical and optical properties of vacuum evaporated CdS and CdTe thin films and their use for fabricating CdS/CdTe heterojunctions including the optimisation of the device fabrication process.

Studies of the epitaxial growth of cadmium sulphide on single crystal cadmium telluride substrates are described in Chapter 10.

The thesis concludes with a summary of the main objectives achieved during the course of this work and some suggestions for the future work in this field, with particular emphasis on the thin film CdS/CdTe solar cells.

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CHAPTER 2

SOLAR CELLS AND MATERIALS

2.1 The Solar Cell

2.1.1 Components of a Solar Cell

A solar cell makes use of the photovoltaic effect[1]; namely the absorption of light in a photosensitive material to create positive and negative charges (EH pairs) which can be separated by a built-in-field to develop a photovoltage and photocurrent, so allowing power to be delivered to an external load. In essence a solar cell is a diode that produces useful electricity from the absorption of solar radiation. In order for a photovoltaic effect to occur the light must be absorbed to produce electron-hole pairs. The internal field in the diode then separates the positive and negative charge carriers and in so doing generates an e.m.f.

A solar cell has two active parts, the absorber and the junction, and two passive parts, the converter-collector and the electrodes (a generalized configuration of a solar cell is given in Fig 2.1. The absorber, sometimes known as emitter absorbs the incident light, generating minority carriers, a proportion of which diffuse to the junction. The magnitude and the sign of the diffusion current is determined by the minority carrier density at the absorber-junction interface. The essential parameters of the absorber-generator are its energy gap (i.e. the threshold energy for the production of electron-hole pairs) and its absorption coefficient. The energy gap will determine the maximum efficiency that can be achieved with a given absorber, since it will fix the portion of the incident solar spectrum that can be absorbed. The absorber is generally chosen to be a p-type material because of the large diffusion lengths for minority electrons.

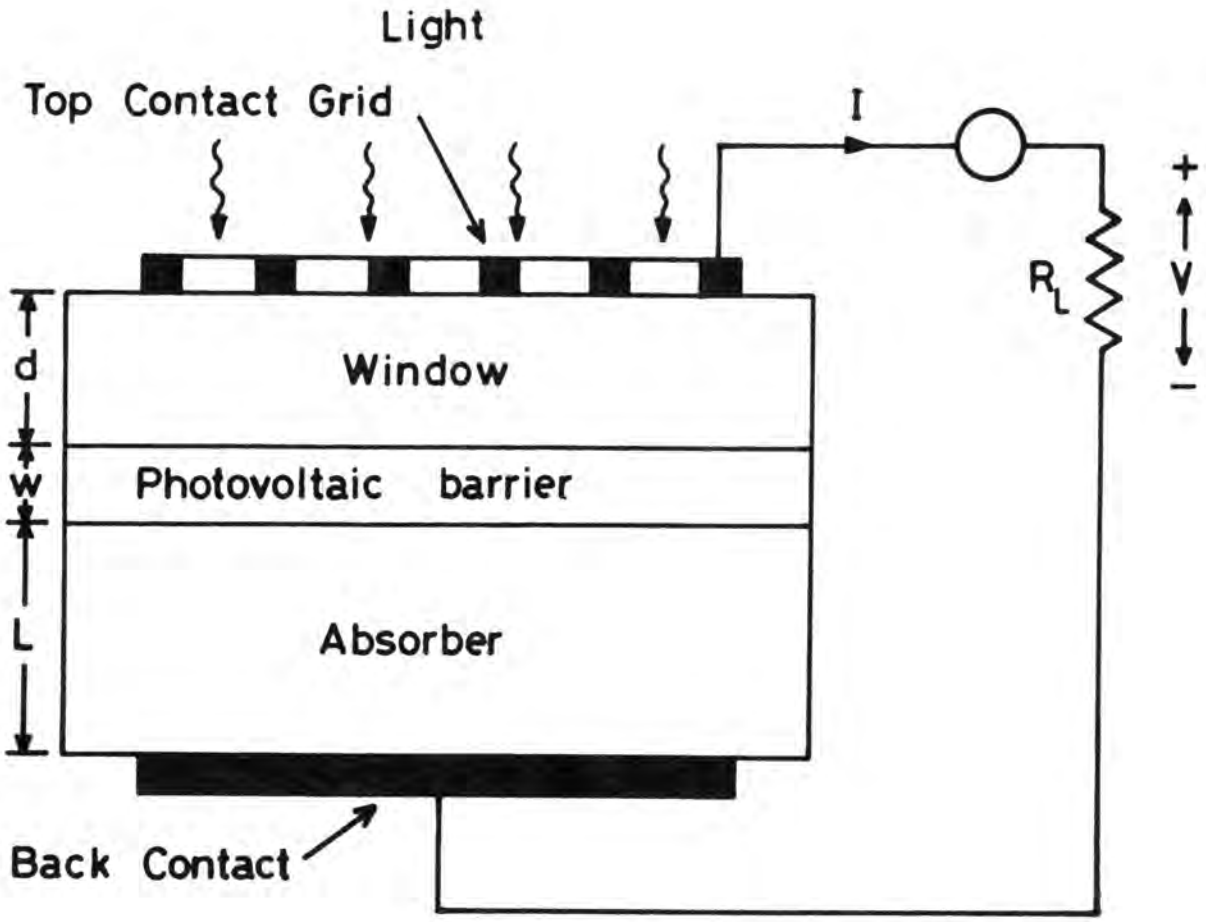

Fig. 2.1: A generalized configuration of a solar cell

The junction is the space charge region in which the minority carriers from the emitter are separated from the majority carriers and supplied to the collector for transmission to the external circuit. The junction provides almost all the voltage drop of the cell. The junction may be described as abrupt or graded, depending on whether the impurity concentration gradient across the junction changes from p to n abruptly or gradually. The three most common types of junction or barrier are:

(1) Homojunctions, i.e. p-n junction within the same semiconductor material.

(2) Heterojunctions, p-n junctions between two different semiconductors; and

(3) Schottky barriers, a metal/semiconductor junction.

The semiconductor layer on the other side of the junction interface from the absorber is called the collector-converter. The primary role of the collector is to collect the minority carriers and convert them into majority carriers. This requires that the collector be of opposite conductivity type so that the minority carriers swept across the junction become majority carriers, thus preventing their recombination before completing the external circuit.

As already mentioned, the junction in a solar cell may be a homojunction, a heterojunction or a Schottky barrier. The properties of the junction are strongly influenced by the properties of the semiconductors forming the junction. For example, the electron affinity which is defined as the energy required to raise an electron from the conduction band edge to the vacuum level, and the lattice parameters of the two materials (in heterojunctions) strongly affect the solar cell performance. In the case of a p-type absorber solar cell, if the electron affinity of the collector-converter is greater than that of the absorber generator, it causes a reduction in the final achievable open circuit voltage with a consequent reduction in the maximum obtainable

efficiency of the device. Conversely, if the electron affinity is smaller for the collector-converter than that of the absorber-generator, the resulting spike in the conduction band reduces the current, again leading to an overall decrease in efficiency.

Similarly, good lattice matching is also desirable since the dislocations at the metallurgical junction between the absorber and collector will act as recombination sites for the generated carriers. So an ideal collector-converter is the same material as the generator but with opposite conductivity.

The fourth non-functional part of a solar cell which affects device performance is provided by the metal electrodes to the absorber and collector. For an efficient performance of a cell good quality contacts (i.e. low resistance ohmic contacts) are necessary.

2.1.2 Classification of Photovoltaic Devices

There are two commonly used systems for the classification of photovoltaic devices. The first is based on the macro- and microstructure (i.e. degree of perfection) of the material used to fabricate the devices, while the second is based on the type of junction formed. According to the first scheme, PV devices are classified as:

(1) Single crystal: In these devices the materials used for their fabrication have the highest order of crystallinity or perfection and are primarily single crystal silicon devices, although some single crystal (Si or GaAs) thin film devices are also included[2]. Because of their high crystal perfection these types tend to have the highest efficiency of any solar cell. They are also the most expensive because of the time and energy intensive methods needed to produce such high quality materials. Single crystal solar cells are presently used in both non-concentrator and concentrator systems.

(2) Polycrystalline: This class of solar device includes primarily thin film devices, but some bulk types also. It is always less energy

intensive and time consuming to produce polycrystalline materials. Many different techniques have been developed to produce polycrystalline thin films for photovoltaic devices, of which the most important include thermal evaporation[3], sputtering[4], screen printing[5], ion-beam deposition and spraying[6,7]. Although less expensive to produce, these polycrystalline devices sacrifice efficiency and possibly stability[8] because of the inherent imperfections. A particular problem is recombination at grain boundaries.

(3) Amorphous: These materials have no long range order, and have different electro-optical properties from single crystal and polycrystalline materials. Although amorphous materials have entered the research field only relatively recently, they have already demonstrated great promise and have been utilised in the manufacture of cells for low power applications such as calculators, watches, etc.

Under the second scheme based on the type of the electronic junctions, solar cells are classified as:

(a) Homojunction; A solar cell in which the p-n junction is formed between two regions of the same semiconductor having different types of conductivity. The best known examples are the standard p-n junction silicon and gallium arsenide solar cells. Homojunctions generally exhibit a high efficiency, but particularly in a direct bandgap material, with a high absorption coefficient, they suffer from front surface recombination which reduces the overall efficiency of the solar cell.

(b) Heterojunctions; In these devices the junction is formed between two different semiconductors, one with p-type and the other with n-type conductivity. Generally, the two semiconductors are chosen to have widely differing bandgap energies. The difference in the bandgaps between the two materials leads to the "window effect" when the device is illuminated from the side with the large bandgap E_g, i.e. the photons

with energies less than the bandgap of the window layer are transmitted into the narrow gap material where they are absorbed, preferably near the junction. Examples are CdS/CdTe and Cu_2S/CdS heterojunction solar cells. Heterojunctions, unlike homojunctions, can be fabricated from a large variety of pairs of semiconductors.

One problem is lattice mismatch in these devices, which can have deleterious effects on the open circuit voltage and possibly on the short circuit current. When the two semiconductors in a heterojunction have a good lattice match reducing the density of interface states, the heterojunction may exhibit the optimum properties of a homojunction constructed from the small bandgap material without the problem of front surface recombination losses.

(c) Buried homojunction; This consists of a p-n homojunction with an additional surface layer of a semiconductor with a large bandgap that acts as a window for the p-n junction. Thus the high recombination loss normally experienced at the front surface of the p-n homojunction is replaced by the interface with the large bandgap semiconductor which may provide improved properties. In principle, buried homojunctions combine the positive aspects of both homojunctions and heterojunctions.

(d) Schottky barriers; These devices consist of metal-semiconductor (MS) junctions. The Schottky barrier cells have the advantage of ease of preparation. Variations of this structure include metal-insulator-semiconductor (MIS) and semiconductor-insulator-semiconductor devices. The insulation layer is often an oxide and is found to reduce the forward current, which increases the open circuit voltage.

2.1.3 Solar Cell Parameters

The performance parameters of a solar cell are derived from the output characteristic. Usually four main parameters are used as figures of merit.

(1) Short circuit current (SCC, I_{sc}): This is the photocurrent output of a solar cell when the load impedance is much smaller than the device impedance, or it may be defined as the photocurrent flowing through the junction at zero applied bias. In ideal conditions (i.e. when the series and shunt resistance effects are negligible) it is equal to the light generated current I_L and is proportional to the incident photon flux with energy greater than or equal to the energy gap of the absorber.

In essence, the short circuit current is determined by the spectrum of the light source and the spectral response of the device. The spectral response in turn depends on the optical absorption coefficient α, the junction depth, the width of the depletion region, the lifetimes and mobilities on both sides of the junction, the presence or absence of electric fields in both the semicondctors on either side of the junction, and the surface recombination velocity[9]. The energy contained in sunlight is distributed over a wide range of wavelengths, and efficient conversion requires an equally wide spectral response. In wider energy gap absorber materials less sunlight is absorbed and hence they lead to smaller short circuit currents than narrow bandgap materials.

(2) Open circuit voltage (OCV or V_{oc}): The open circuit voltage is the output voltage of the device under illumination when the load impedance is much greater than the device impedance, i.e. it is the voltage across the terminals of an illuminated solar cell at zero current flowing through the junction. The open circuit voltage of a p-n junction solar cell is directly related to the bandgap of the semiconductor through the barrier height at the junction; it is often expressed in terms of the short circuit current I_{sc}, the reverse saturation current I_o and the ideality factor A as[10]:

$$V_{oc} = \frac{A\,kT}{2} \ln\left(\frac{I_{sc}}{I_o} + 1\right) \qquad 2.1$$

It might appear from equation (2.1) that high values of A are desirable in obtaining high V_{oc} but this is not so. With large values of A, I_o increases and consequently the open circuit voltage is reduced. In contrast in an ideal junction, A is equal to unity and V_{oc} attains its highest value. The dark current I_o is mainly determined by the energy gap of the material and the temperature ; I_o decreases and V_{oc} increases with increasing energy gap or decreasing temperature. There is thus a trade-off between high V_{oc} with a large bandgap absorber and the high I_{sc} obtained from narrow gap material.

(3) Fill factor (FF): Mathematically the fill factor is the ratio of the maximum electrical power output to the product of V_{oc} and I_{sc}. It describes the rectangularity or squareness of the photovoltaic output characteristics. The fill factor is mainly determined by the value of A, the series resistance R_s and the shunt resistances R_{sh}. The series resistance is the total internal resistance of the device which arises from the contact resistances to the front and back surfaces, the resistance of the base and window layers. The shunt resistance is the internal resistance in parallel with the p-n junction and is caused by the surface leakage along the edges of the cell, by diffusion spikes along dislocations or grain boundaries, or possibly by fine metallic bridges along microcracks, grain boundaries, or crystal defects such as stacking faults after contact metallization has been applied. A high shunt resistance and low values of A and R_s are required for a high fill factor. High values of fill factor correspond to high rectangularity of the output characteristics, while small values result in softening of the characteristics.

(4) Efficiency: This parameter describes the overall performance of a solar cell. The three parameters, I_{sc}, V_{oc}, and FF, determine the efficiency of a cell, which can be expressed as[11]:

$$\eta = \frac{I_{sc} V_{oc}}{P_{inc} \times \text{Area}} \times FF \qquad 2.2$$

where P_{inc} is the incident radiation power density, usually expressed in mW/cm^2.

2.2 Choice of Materials

2.2.1 Solar Spectrum

The solar spectrum dictates the range of solar materials which can be used for photovoltaic device fabrication. The solar radiation from the sun can be approximated by that of a black body at a temperature of 5900 K. This black body spectrum is modified by the variations in temperature across the sun's disk, the effect of the solar atmosphere, and the Fraunhofer absorption lines.

In outer space, 98% of the total energy radiated by the sun lies in the wavelength range 0.25 to 3.0 μm. The intensity of the solar radiation incident on the top of the earth's atmosphere is called the solar constant and is defined as the rate at which energy is received on a unit area surface, perpendicular to the sun's direction, in free space at the earth's mean distance from the sun ; its most recently accepted value is 1.353 KW m^{-2} [12]. The actual solar radiation in free space at the mean distance of the earth from the sun differs from this value by ± 3.35% because of changes in the earth-sun distance throughout the year[12].

The intensity and spectral distribution of solar radiation arriving at the earth's surface is affected by scattering and absorption within

the earth's atmosphere, and this in turn depends on the composition of the atmosphere as well as the path length of the radiation traversed by the radiation through it. There are three principal mechanisms which modify the solar spectrum at the surface of the earth.

(a) absorption by atmospheric gases, particularly ozone which absorbs strongly in the ultraviolet;

(b) absorption by water vapour which occurs in the infrared;

(c) scattering by aerosols.

The effect of the atmospheric attenuation on solar irradiance is described by a parameter known as the air mass number which is equal to the secant of the angle between the sun's direction and the normal to the earth's surface. Conventionally, solar cell performance is often measured in terms of certain standard conditions of illumination, in particular AM0,AM1 and AM2. AM0 (air mass zero) corresponds to the solar irradiance at the top of the earth's atmosphere. AM1 is the irradiance at sea level under a standard atmosphere (dust free, 2 cm precipitable water) when the sun is at the zenith and AM2, which is a typical average irradiance at the earth's surface corresponds to the condition when the angle between the sun and the zenith is 60°. Fig 2.2 shows the different solar spectra.

2.2.2 Properties of Optimum Solar Cell Materials

The following properties, some of which are interrelated are important for consideration for the choice of a solar material.

(1) Energy gap: The energy gap of an absorber material places an upper limit on the wavelength of the incident radiation. Thus the smaller the energy gap, the larger the portion of the solar spectrum which is potentially utilized, and therefore the greater the short circuit current. However, the maximum photovoltage attainable is correspondingly small (Sec.2.1.3). On the other hand, a large energy gap can give rise to high V_{oc} with lower leakage across the junction,but with a lower I_{sc}. Therefore, as discussed in section 2.1.3 a judicious

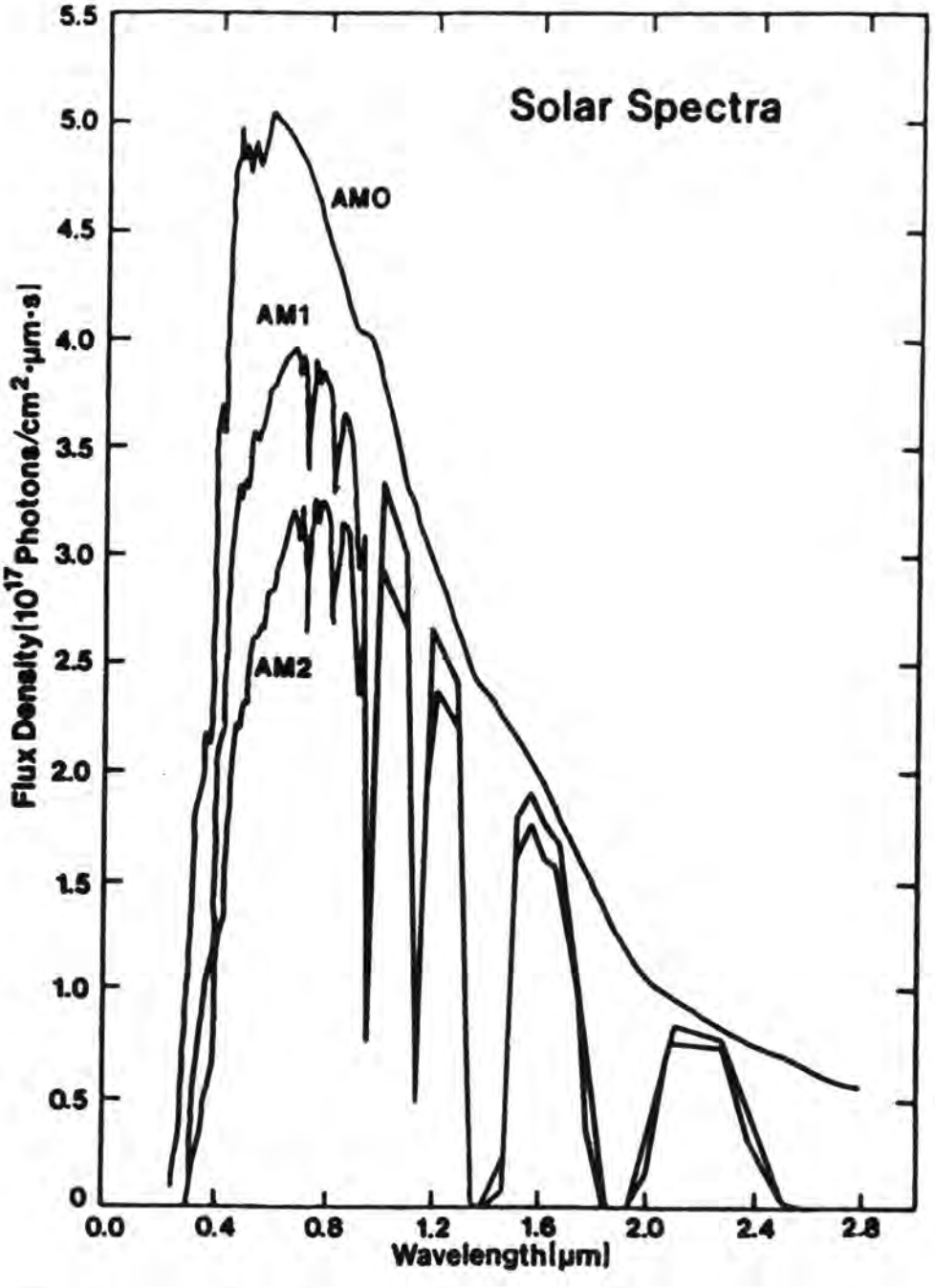

Fig. 2.2 : Spectral distribution of solar radiation under different conditions (Ref. 18)

compromise has to be made to optimise the spectral response of the device. Moreover, the solar spectrum is not smooth but has a great deal of structure due to the various atmospheric absorption bands[13]. As a result there have been a number of studies attempting to match the energy gap to the solar spectrum[14-17]. Figure (2.3) represents a relation between the energy gap E_g and efficiency η for ideal and non-ideal homojunctions under AMO conditions. For ideal solar cells the optimum energy gap is between 1.5-1.6 eV and for more realistic devices it is between 1.3-1.4 eV[18].

Recently, similar studies for heterojunction devices have been reported[15]. Figure 2.4 shows the maximum achievable efficiency as a function of absorber energy gap for different window materials. The window is a large bandgap semiconductor that does not absorb any significant proportion of the incident-photons. Together with the active absorber, the window collector forms the junction which yields the photovoltaic effect. These results relate to AM1 conditions and do not include refinements such as grain size[16,17,19] or lattice matching between the absorber and window layer[20,21], which can further affect the performance. The optimum value of the energy gap for terrestrial applications is 1.5 eV[14].

(2) Absorption coefficient: A high absorption coefficient, α is important from both technological and economic considerations. In general absorber-generators should have large absorption coefficients associated with interband transitions[22]. Since the necessary absorber thickness is of the order of $1/\alpha$[23], large absorption coefficient permits the absorber layer to be thin (i.e. incident photons are absorbed near the surface) and hence less material is necessary for device fabrication. In principle, a direct bandgap material is more desirable, since the absorption coefficient is larger. For example, all photons will be absorbed in 2 μm of GaAs, and 5 μm of CdTe, but

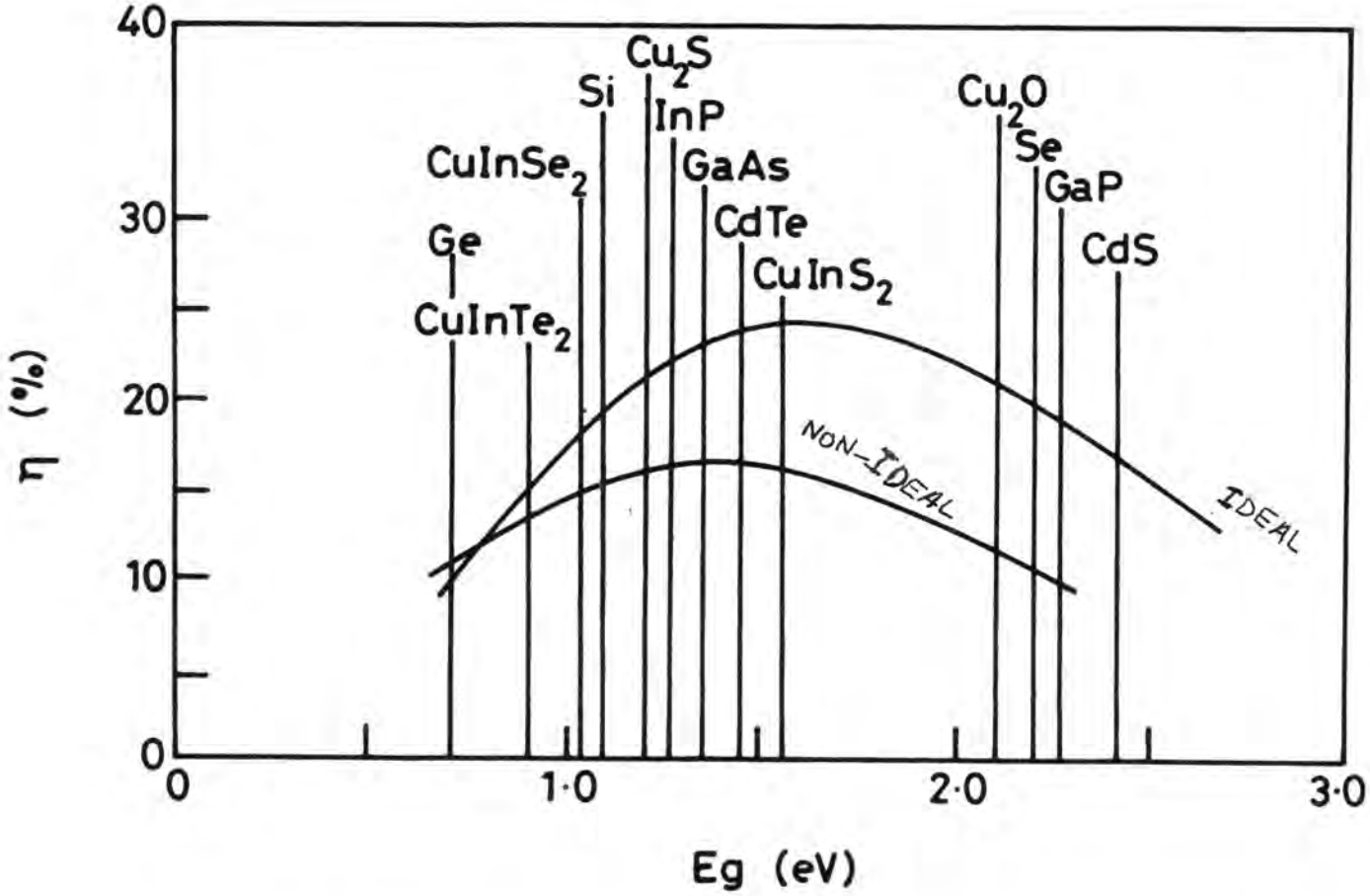

Fig. 2.3 : Relationship between the energy gap Eg and efficiency η for ideal and non-ideal homojunction solar cells under AMO conditions. (ref 18)

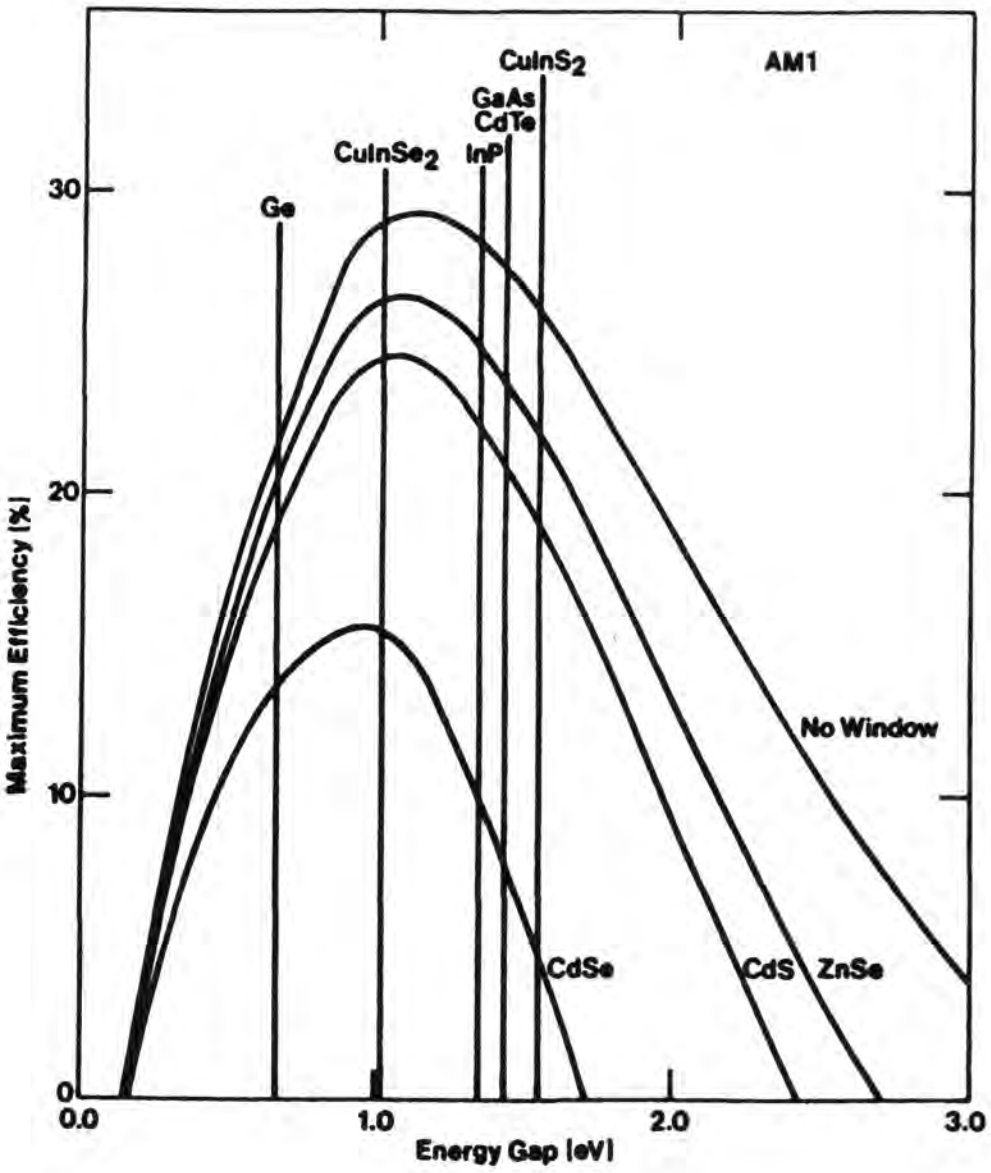

Fig. 2.4 : Theoretical efficiencies of heterojunction solar cells as a function of energy gap. Results are calculated for various absorber levels and window materials (ref. 18)

about 100 μm is required for Si which has an indirect bandgap. Figure 2.5 represents the absorption coefficients as a function of photon energy for several solar cell materials.

(3) Diffusion length: An essential requirement for the successful operation of a solar cell is that the photogenerated carriers must be able to move across that absorption region to the junction. The charge carriers that recombine before arriving at the junction are lost to the photovoltaic effect and cannot contribute to the photocurrent. Diffusion is the mechanism by which the minority carriers move to the edge of the depletion region and therefore the minority carrier diffusion length is a most important material parameter. In general the diffusion length should also be of the order of $1/\alpha$[23]. The diffusion length depends on various factors such as:

(i) The impurity and defect concentration[24-27].

(ii) The crystallinity of the material[28].

(iii) The crystal orientation[29].

(iv) The stoichiometry[30].

(4) Minority carrier lifetime: Another important material property that is fundamental in determining the effectiveness of a semiconductor as a solar material is the minority carrier lifetime. Large values of lifetimes are usually desirable for efficient devices.

One factor which seriously reduces lifetime is the presence of a high density of localised states and in particular of the "killer" centres located at the middle of the bandgap. For example, it has been found that for 10% efficient CdTe solar cells the lifetimes should be longer than 10^{-7} sec. Shorter lifetimes have been found in the material due to the presence of "killer" centres.

(5) Doping: Impurity concentration levels can have a profound effect on absorption, diffusion length and energy bandgap[31]. It is desirable to obtain a large photovoltage and this requires high levels

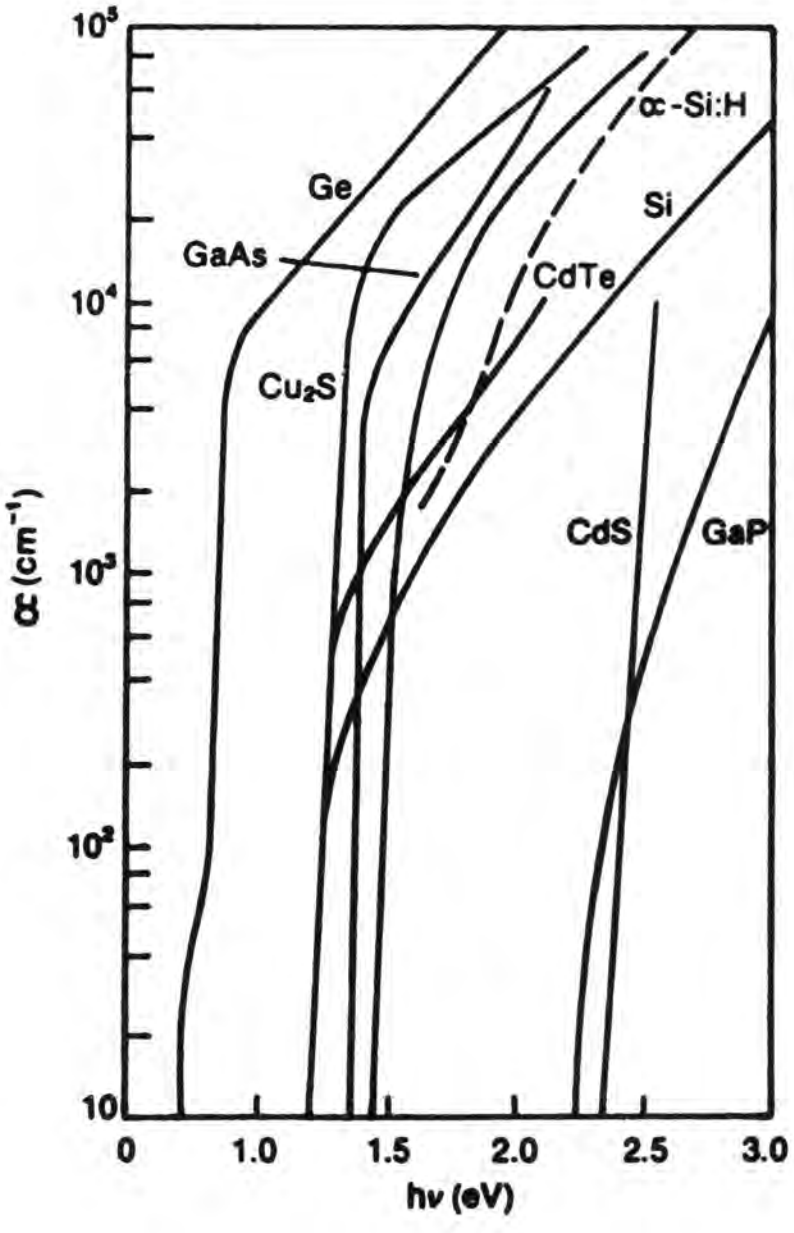

Fig. 2.5 : Optical absorption coefficients as a function of photon energy for several solar cell materials (Ref. 18)

of doping. On the other hand long lifetimes are also necessary and these are reduced by doping too heavily. It is also important that the series resistance of the cell be very small to reduce ohmic losses in the device itself. These conflicting requirements necessitate that the doping level can be controlled for optimum performance.

(6) Surface recombination and density of localized states: In photovoltaic devices surface recombination can seriously limit their performance. High surface recombination arises from a number of causes including the presence of surface states associated with dangling bonds, native oxide layers, chemical residues, etc. In an illuminated solar cell, carrier generation is highest at the surface and decreases exponentially with depth into the material. Thus surface recombination is a critical parameter, especially in the direct bandgap materials. Its effects can be reduced by various techniques for surface preparation or through passivation of the photovoltaic material surface.

A high density of localized states results in extremely poor diffusion lengths. It is also difficult to dope materials effectively to form the necessary junctions and obtain reasonable minority carrier lifetimes if the localized defect state density is high. This is especially critical for amorphous materials.

Densities of these states have been reduced by alloying and complexing[32,33]. With amorphous Si, fabrication in a hydrogen discharge has been found to reduce the density of localized states considerably[34] and recently a glow discharge Si:H:F alloy has been shown to reduce such states even more[35].

2.3 CdTe Based Cells

2.3.1 Cadmium Telluride as an Absorber

Cadmium telluride is the only II-VI compound that can at present be prepared with a reasonably high conductivity in both n and p type forms, and consequently shows promise for making homojunction solar cells. It

is, however, generally difficult to obtain a very high p-type conductivity ($p>10^{17}$ cm^{-3}) probably because of self-compensation and this has introduced a number of difficulties.

CdTe has a direct bandgap of 1.47 eV which is near the optimum (1.5 eV) for photovoltaic conversion of solar energy[14]. Among the most promising absorber materials CdTe has the largest bandgap. Its potential in heterojunction solar cells therefore depends on whether the OCV developed in such a cell under solar illumination is sufficiently larger than the OCV achieved with cells made from smaller bandgap semiconductors to offset the decrease in SCC, which is an inevitable consequence of its larger bandgap.

The optical absorption coefficient of CdTe has been recently redetermined[36,37]; it rises rapidly to values in excess of 10^4 cm^{-1}. The high absorption coefficient of CdTe implies that photons with energies above 1.47 eV are absorbed within a few micrometers of the CdTe surface, and in principle, therefore less material is required for device fabrication, with a potential saving in the cost of the device. Conversely, silicon with an indirect bandgap of 1.11 eV requires a layer twenty microns thick to absorb the same proportion of the light. When used in a heterojunction with a suitable window CdTe with its high absorption coefficient has the special advantage that the photocarriers are generated near the junction, where charge separation and collection occurs. The requirement for large diffusion lengths (which are generally difficult to achieve in polycrystalline films) in the bulk is then relaxed so that the viability of low cost thin film solar cells is enhanced.

Because of its low sublimation temperature, CdTe is amenable to easy processing to form good quality films using inexpensive techniques such as thermal evaporation, although films produced by conventional evaporation methods are found to have a high resistivity.

Despite all these attributes the full potential of CdTe for photovoltaic applications has not yet been exploited because of inherent problems associated with the material. These include:

(1) Minority carrier lifetime: For efficient photovoltaic devices long lifetimes of minority carriers are desirable. Bell et al[38] have shown that lifetimes of 10^{-7} sec in CdTe are essential to obtain a 10% efficient solar cell. However, minority carrier lifetimes in n-CdTe are generally less than 10^{-8} sec, and lifetimes are even shorter in p-CdTe[39,40]. Theoretically, lifetimes greater than 10 μs should be achievable in CdTe, even when doped to low resistivity (10^{18} cm^{-3}). Low minority carrier lifetimes are believed to be due to the presence of "killer" centres near the middle of the bandgap. Bell et al[38] have also shown that lifetimes are affected by the chemical nature of the dopant (higher lifetimes were observed for iodine doped material than for Cl-doped material), and these authors have suggested that to achieve long lifetimes it will be necessary to find a natural compensation process to minimize the effect of the defect states responsible for the short lifetimes. The search to find a suitable dopant to satisfy this requirement is still continuing.

(2) High resistivity: The real promise of CdTe for low cost solar cells is attributable to its amenability to inexpensive thin film fabrication techniques. But the problem with the CdTe films grown by thermal evaporation methods is their high resistivity. Attempts to dope the films by adding acceptor impurities to the charge have not in general been successful in producing low resistivity films. This difficulty in preparing low resistivity p-type films makes cheap CdTe homojunction cells unlikely.

(3) Ohmic contacts: Low resistance ohmic contacts to the semiconductor layers are one of the basic requirements for the production of a high efficiency solar cell. It has, however, been

difficult to make low resistance contacts to p-CdTe. The work function of CdTe is 5.9 eV[41]. Theoretically a barrier free contact to a p-type semiconductor is obtained when the work function of the metal ϕ_m, used for the contact is greater than the work function of the semiconductor. Unfortunately, none of the commonly available metals has a work function large enough to match the work function of p-CdTe, and so it is always difficult to make ohmic contacts to p-CdTe. The second possibility is to produce a tunneling contact through a narrow Schottky barrier and this needs the surface of CdTe under the contact to be heavily doped p-type which is not easily achieved because of limited solubility of common acceptor impurities.

A number of different attempts to make ohmic contacts to p-CdTe have been reported in the literature and Ponpon[42] has recently published a review. Evaporated Au and Pt contacts followed by firing at 200°C in hydrogen have been used to make low resistance ohmic contacts to p-CdTe[43]. Evaporated gold contacts on As^+ implanted CdTe surfaces also proved to be successful[44]. Contacts with a resistivity of 0.15 Ω-cm^2 were obtained by heating layers of nickel deposited on a dichromate etched surface at 200°C[45]. According to the authors, the thin tellurium layer left behind by the etching constitutes a diffusion source of Te atoms which form a heavily p-type doped zone between the nickel and the bulk CdTe. Unfortunately, the resistance of contacts made with Ni, Pt and Au was found to increase with time.

High work function HgTe (5.9 eV) deposited in a close-spacing isothermal deposition process on p-type CdTe surface etched in bromine-in-methanol has been found to give low resistivity contacts[41]. Here HgTe was first deposited on the sample surface and then covered with electroless gold. Recently, screen printed and painted[46] carbon contacts have been successfully used in the production of high efficiency CdS/CdTe solar cells.

In the present study gold and carbon contacts have been used in solar cells employing thin films and bulk crystals of CdTe. The preparational details are given in Section 4.6.1.

2.3.2 Cadmium Sulphide as the Window Layer

There are many good reasons for using CdS as a window layer in CdTe based solar cells. It is a II-VI compound with a direct bandgap of 2.4 eV, which is high enough to form a wide gap window, and will therefore transmit most of the incident solar spectrum. Although the minimum temperature at which cadmium sulphide melts is 1475°C (and that is accompanied by an equilibrium vapour pressure of ∿ 4 atmospheres[47]), it does sublime at a much lower temperature of 700°C at atmospheric pressure, and hence it can be readily evaporated to form thin films. However, there is a relatively large lattice mismatch between CdS and CdTe, and moreover, CdS generally crystallizes in the hexagonal wurtzite structure whereas CdTe is cubic. Consequently, CdS deposited on CdTe is usually polycrystalline, although epitaxial growth on CdTe, is possible[48,49] as will be discussed in Chapter 10 in this thesis.

CdS can be doped n-type only but it may be made highly conducting. It is therefore feasible to displace the region of maximum photocarrier generation away from the surface where the recombination velocity is very high into the region of maximum carrier collection. In addition, since the electron affinities of both CdS and CdTe are approximately 4.5 eV[50], the conduction bands of the two materials join smoothly at the interface[51-53]. Thus CdS is a natural choice as a window material in n-CdS/p-CdTe heterojunctions. Another important factor is that CdS is relatively inexpensive. CdS has been widely and successfully used as a window material in other systems, of which the best known is the CdS/Cu_2S heterojunction. Thin film cells of Cu_2S/CdS with active areas of 1 cm^2 and efficiencies up to 9% have often been reported[54], and

high efficiencies of 17% with InP/CdS[55], and 12% with $CuInSe_2$/CdS[56] single crystal type cells have been claimed.

The low sublimation temperature of CdS enables thin films of good quality to be relatively easily produced, using inexpensive techniques such as evaporation, r.f. sputtering etc. This is an important consideration from an economic point of view and is to be contrasted with the difficulty in preparing good thin films of Si or GaAs by similar techniques.

2.3.3 Copper Telluride

One of the most interesting CdTe based solar cells developed in the 1960's was the Cu_2Te/CdTe heterojunctions[57]. Layers of copper telluride were produced by dipping CdTe thin films and single crystal substrates in a warm (<100°C) aqueous solution of cuprous ions. This produced a displacement reaction analogous to that used in the fabrication of Cu_2S/CdS devices. This simple production process makes the Cu_2Te/CdTe heterojunction an attractive candidate for a potential thin film cell.

Although the properties of Cu_2Te are much less well understood than those of copper sulphide[58], it is known to be a semiconductor with a bandgap of 1.04 eV[59], and is believed to be indirect[56]. In natural form it is found as Rickardite (Cu_3Te) and Weissite (Cu_2Te)[60]. The structural properties have been studied by Nowonty[61] who found cuprous telluride (Cu_2Te) to have a hexagonal structure with lattice constants, c = 7.27 Å and a = 4.23 Å. For tellurium rich samples the values of c and a were found to be 7.24 and 4.19 Å respectively. The atom-to-atom distances in Cu_2Te were estimated to be Cu-Cu = 2.23 Å, Te-Te = 2.82 Å and Cu-Te = 2.67 Å. It is therefore reasonable to suppose that cuprous telluride has phases which are closely analogous to those of cuprous sulphide[58].

Cusano's[57] study of the spectral response of Cu_2Te/CdTe heterojunction indicated that cuprous telluride was opto-electronically inactive and simply produced a low resistance ohmic contact to p-type CdTe in the n-CdTe/p-CdTe/Cu_2Te p-n homojunction. Cu_2Te solar cells have also been studied by Bernard et al[62] who investigated the properties of copper telluride with different tellurium to copper ratios using previously obtained data[63,64]. Junction studies again revealed that the cell was probably a cadmium telluride p-n homojunction with the copper telluride acting as a semi-transparent conducting electrode. Cu_2Te films were found to degrade with time and this was associated with the presence of moisture, absorbed oxygen, and the diffusion of copper[57,65-67].

2.4 Review of CdTe Solar Cells

The history of CdTe solar cells dates back to the 1960's when Vodakov et al[68] and Naumov and Nikolaeva[69] reported efficiencies of 4 and 6 percent respectively for their homojunction cells. However, other early studies of cadmium telluride revealed that an economical CdTe homojunction terrestrial cell was not feasible, because minority carrier lifetimes in CdTe were less than 10^{-8} sec[39,40,70]. Nevertheless, Barbe et al[71] produced a shallow homojunction cell on an n-type substrate with an efficiency of 13.4% under AM1 illumination. Several alternative CdTe heterojunction cells have been fabricated and investigated during the last two decades in attempts to produce an efficient cell.

In 1963 Cusano[57] produced CdTe/Cu_2Te thin film and single crystal heterojunctions with efficiencies of 6 and 7.5% respectively. The cells were fabricated by treating CdTe films and single crystals in a warm aqueous solution of cuprous chloride to form copper telluride. Similar

devices were prepared by Leburn[72] and Bernard et al[62] using flash evaporation of Cu_2Te although this was never fully investigated.

A year later Muller and Zuleeg[73] reported preliminary results with a CdS/CdTe cell. This device had an Al/CdS/CdTe/Au structure and was fabricated by vapour deposition of 1 μm thick CdS and 500 Å thick CdTe layers. This was followed by Dutton and Muller[74] who reported cells formed by evaporating ∿ 100 Å of either Te or CdTe onto ∿ 1 μm thick films of CdS. Spectral sensitivity studies, however, revealed the presence of a CdS_xTe_{1-x} graded region in addition to CdTe, indicating that these devices were not ideal heterojunctions. In 1971, Bonnet and Rabenhorst[75] produced CdS/CdTe heterodiodes with graded bandgaps by co-evaporation of CdS and CdTe onto glass substrates maintained at 180°C.

In the early 1970's there were several reports of the fabrication and evaluation of CdS/CdTe thin film diode arrays[76-78]. The arrays which were investigated for potential applications to optoelectronics, had a layered structure of n-SnO_2/n-CdS/p-CdTe/metal. Short circuit currents of 15 mA/cm^2 and open circuit voltages of 0.3V were measured under 100 mW/cm^2 illumination. The spectral sensitivity of the photovoltage was consistent with the known cut-off wavelengths for CdS and CdTe.

In 1972 Bonnet and Rabenhorst[79] published the details of an all thin film CdS/CdTe heterojunction cell fabricated on a molybdenum foil substrate. A layer of CdTe 10-20 μm thick was first evaporated onto the Mo substrate using a high temperature reactor, then a layer of CdS was vacuum evaporated at a substrate temperature of 180°C. Difficulties were experienced in trying to obtain an ohmic contact to the p-type CdTe, and it was found necessary to deposit a thin layer of Cu onto the Mo substrate before evaporating the CdTe layer.

Two years later Fahrenbruch et al[80] reported on calculations of the photovoltaic conversion efficiencies of II-VI compounds, in which they estimated an efficiency of 17% for CdTe/CdS cells. Fahrenbruch et al then fabricated CdS/CdTe devices by close-space vapour transport of CdTe in H_2 onto single crystals of CdS. The highest efficiency achieved was 4.0 percent with an open circuit voltage of 0.61 V, a short circuit current of 14 mA/cm^2 and a fill factor of 36% under 80 mW/cm^2 illumination. Indium and Ni were used to make ohmic contacts to CdS and CdTe respectively.

In 1975 Yamaguchi et al[48] produced a single crystal CdTe/CdS cell with an efficiency of 4.5%, an open circuit voltage of 0.55V, a short circuit current of 14 mA/cm^2 and a fill factor of 47%. The cells were fabricated by vapour deposition of In-doped CdS on P-doped CdTe substrates in a H_2 atmosphere at a substrate temperature of 400 to 500°C. The CdS layer was about 30 μm thick with a resistivity of 0.1 Ω-cm. SEM studies of the junction indicated the diffusion of indium into the CdTe to form an n-CdS/n-CdTe/p-CdTe junction. After further development, Yamaguchi et al[49] obtained an active area efficiency of 12% in cells fabricated by epitaxial growth of CdS on (111) P-doped CdTe grown by the Bridgeman technique. The basic structure was In-Ga/CdS/CdTe/Ni. Careful analysis of this cell indicated that it was actually a buried homojunction with an n-CdS/n-CdTe/p-CdTe structure. Bube et al[81] have also produced 7.9% efficient devices using the same approach.

Spray pyrolysis has been used to put down "windows" of CdS and ZnCdS on CdTe wafers[82] to produce CdS/CdTe and ZnCdS/CdTe heterojunctions. These cells have exhibited OCV values of 0.74 V and 0.80 V respectively, and efficiencies of 6.0 and 7.8%.

Solar cells fabricated using close-space vapour transport of CdTe onto CdS have produced efficiencies of up to 4% with an open circuit voltage of 0.61 V and a quantum efficiency of 0.85[83]. Tyan and Perez-Albuerne[84] described a thin film heterojunction fabricated by the close-space sublimation technique. The cells had typical values of open circuit voltage of ∿ 750 mV, short circuit current 17 mA/cm^2, fill factor ∿ 62% and efficiency 10.5% under simulated AM2 illumination. Basol et al[85] have investigated electrodeposited CdS/CdTe thin film cells. The efficiency achieved was 8% for small area (0.02 cm^2) devices under 80 mW/cm^2 illumination and for large area (4.2 cm^2) devices it was 7%.

The use of a larger bandgap window in place of CdS should in principle result in more efficient cells. One such possibility is to replace the CdS by indium tin oxide (ITO) and preliminary work on the resultant heterojunction has shown higher values of OCV as expected[81]. In 1982 indium tin oxide/CdTe solar cells fabricated by electron beam evaporation of ITO onto p-type single crystals and thin films of CdTe deposited on single crystal CdTe substrates, were reported[86]. A solar efficiency of 10.5% (referred to the active area) was achieved with OCV = 0.85 V, and SCC = 20 mA/cm^2 for single crystal CdTe substrate cells and of 5.5% for the thin film ITO/CdTe structures.

Recently, screen printing has emerged as a very successful technique for producing efficient CdS/CdTe thick film cells. Nakayama et al[87] produced an 8.1% efficient cell using a CdS/CdTe/Cu_2Te structure which was operated in the back-wall mode. In this cell, transparent indium tin oxide was first deposited on glass before the sequential screen printing of a 20-30 μm thick n-CdS film with 0.2 Ω-cm

resistivity. This was followed by a 10 μm n-CdTe layer of about the same resistivity. The structure was then dipped into a cuprous chloride solution to grow a Cu_2Te layer to form a CdS/CdTe/Cu_2Te device. Microprobe analysis of similar cells produced on single crystals substantiated the formation of a homojunction with n-CdS/n-CdTe/p-CdTe/$(p^+)Cu_2Te$ heteroface structure. A screen printed CdS/CdTe device is being extensively researched in Japan and recently a cell with an active area efficiency of 12.8% was reported by Matsumoto et al[88].

Other wide gap semiconductors have also been studied as possible window materials for CdTe solar cells. For example, ZnO/CdTe cells prepared by spray pyrolysis have shown an efficiency of 8.8%[89], and ZnSe/CdTe cells have also been considered but so far the efficiencies achieved have been low, 1 and 2%[83].

Solar cells based on CdTe have demonstrated very good potential during the last two decades of research but the efficiencies achieved are still well below the theoretical maximum of 17%. Much research therefore still remains to be carried out before the full potential of the material can be realized.

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CHAPTER 3

REVIEW OF THE PRINCIPLES OF DEVICE OPERATION

3.1 Introduction

Although the experimental aspects of fabrication and characterisation of CdTe based solar cells are the major concerns of this thesis, the underlying principles and theory still retain their relevance. This Chapter is therefore primarily devoted to a review of the fundamental physics of solar cells. In essence, a solar cell is a p-n junction or a Schottky barrier device in which the incident light is absorbed to produce electrical energy. In both types of device the junction and material properties govern the final behaviour of the cell. It is thus appropriate to describe, in the first part of this chapter, the characteristics of a p-n junction together with current transport mechanisms both in the dark and under illumination.

Characterisation of the materials used was also carried out during this work. The main techniques used for electrical characterisation included space charge limited current (SCLC) analysis, steady state photocapacitance and deep level transient spectroscopy (DLTS). Schottky barrier structures as well as heterojunctions were used to provide suitable structures for the space charge region based measurements. The second part of this chapter therefore describes an overview of the relevant theory of Schottky barrier devices, and background theory of crystal imperfections.

3.2 P-n Junction Characteristics

Solar cells may be either homojunctions or heterojunctions, but in both cases it is the p-n junction that provides the means for separating the positive and negative charge carriers liberated by the absorption of

light. The separated charges generate an electromotive force (EMF) which then drives an electric current through an external circuit to produce useful power. The efficiency of the photovoltaic conversion process is closely related to the quality of the p-n junction and the diode characteristics. Thus, in this section some of the basic current transport mechanisms in both ideal and real devices will be discussed.

3.2.1 Dark Current Mechanisms in p-n Homojunctions

The ideal dark current-voltage characteristics for a homojunction are well described in the literature. Hovel[1] has discussed many of the cases relating to solar cells. Three mechanisms are generally thought to contribute to the dark current in forward-biased junctions. They are illustrated in Fig 3.1 and include: (1) injection current; (2) space charge region recombination current; and (3) tunneling through localized states.

(1) Injection current: The injection current component (Fig 3.1) consists of electrons injected from the n-side conduction band over the potential barrier to the p-side where they diffuse (and drift, if there is an electric field) away from the junction. Eventually they recombine with holes either in the bulk or at a surface. There is also analogous current due to hole injection from the p-side valence band into the n-side. The injected current is described by the Shockley diffusion model[2] which is based on the following assumptions: (a) the built-in potential and applied voltages are supported by a dipole layer with abrupt boundaries while outside the boundaries the semiconductor is neutral; (b) the Boltzmann approximation is valid; (c) the injected minority carrier densities are small compared with the majority carrier densities; and (d) no generation or recombination currents exist in the depletion layer, and the electron and hole currents are constant through the depletion region.

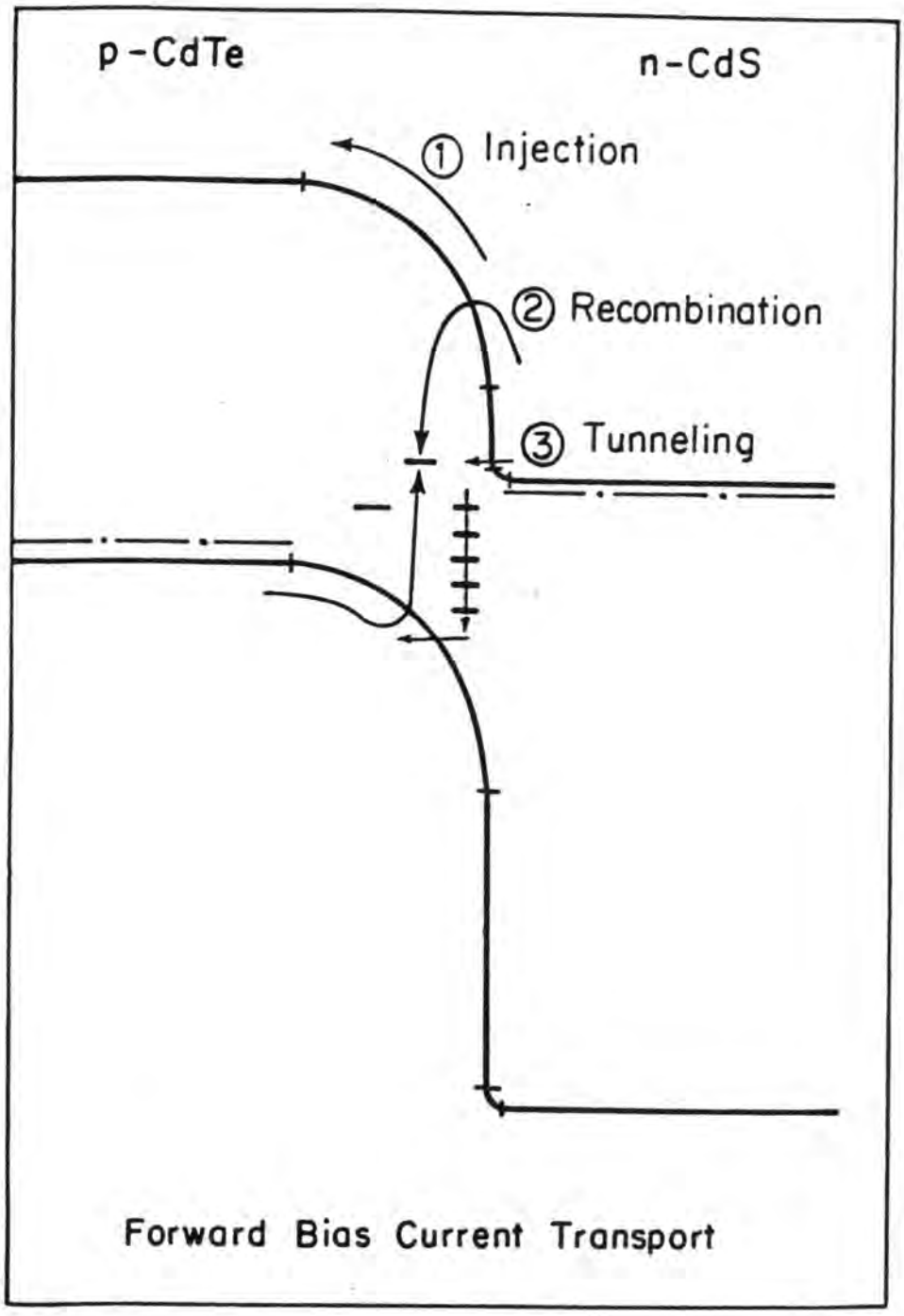

Fig. 3.1 : Current transport mechanisms in forward biased p-n CdS/CdTe heterojunction (Ref. 4)

Neglecting the surface recombination, i.e. the junction is far from the surface, the diode current is expressed by the Shockley diode equation[2]:

$$J = J_o \left[\exp \frac{qV}{AkT} - 1 \right] \tag{3.1}$$

where

$$J_o = q \left[\frac{n_p D_n}{L_n} + \frac{p_n D_p}{L_p} \right] \tag{3.2}$$

and q is the charge of an electron; A, the diode factor is equal to unity (ideal case); V is the voltage across the ideal junction; n_p is the electron concentration in the p-region; p_n is the hole concentration in the n-region; and D_n, L_n and D_p, L_p are the minority carrier diffusion coefficients and diffusion lengths in the n and p regions respectively. The equilibrium minority carrier concentrations are given by:

$$n_p = n^2_i/P_p = n^2_i/N_A \tag{3.3}$$

$$p_n = n^2_i/n_n = n^2_i/N_D \tag{3.4}$$

where N_A and N_D are ionized acceptor and donor densities respectively, and n_i the intrinsic carrier concentration

$$n^2_i = N_v N_c \exp(-E_g/kT) \tag{3.5}$$

N_c and N_v are the effective densities of the states for the conduction and valence bands respectively, and E_g is the semiconductor bandgap. The diffusion constant is related to the carrier mobility and is expressed by the Einstein relation.

$$D = (kT/q)\,\mu \tag{3.6}$$

where μ is the carrier mobility. Substituting this expression into equation 3.2, the reverse saturation current J_o is given by:

$$J_o = (kT)\,(n^2_i)\,(\mu_n/N_A L_n + \mu_p/N_D L_p) \tag{3.7}$$

from which it can be seen that J_o depends directly on the temperature and carrier mobilities, but inversely with the donor and acceptor densities and the minority carrier diffusion lengths. Generally speaking for solar cell considerations, J_o should be small.

(2) Space charge region recombination current: When a p-n junction is forward biased, electrons from the n-side and holes from the p-side are injected across the junction space charge region into the p and n sides respectively. However, at the same time some of these carriers recombine in the depletion region, resulting in an increase in the dark current through the device. This "space charge region recombination current" was first described by Sah et al[(3)]. They assumed: (i) the doping levels were the same on opposite sides of the junction; (ii) only single-level recombination centres located in the vicinity of the middle of the bandgap are important; and (iii) the recombination rate is approximately constant within the space charge region.

The space charge region recombination current in the dark under forward bias is given by the relation[4].

$$J = \frac{q\, n_i\, W}{\sqrt{\tau_{po}\, \tau_{no}}} \left[\frac{2 \sinh (qV/2kT) f(b)}{q(V_b - V)/kT} \right] \tag{3.8}$$

where W is the depletion region width, τ_{po}, τ_{no} are the minority carrier lifetimes on the two sides of the junction, V is the voltage across the junction, V_b is the junction built-in voltage, and the factor f(b) is a function involving the trap level and the two lifetimes as follows:

$$f(b) = \int_0^\infty \frac{dx}{x^2 + 2bx + 1} \tag{3.9}$$

and

$$b = \exp(-qV/2kT) \cosh \left[(E_t - E_i)/kT + (\tfrac{1}{2}) \ln(\tau_{po}/\tau_{no}) \right] \tag{3.10}$$

where E_i is the intrinsic Fermi level.

The Sah et al (S-N-S) theory was extended by Choo[5] to asymmetric junctions where the trap levels are not located at mid-gap, doping levels on each side of the junction are unequal, and the lifetimes τ_{po},τ_{no} are also different. The derived dark current expression is essentially the same as equation 3.8, except the factor f(b) is smaller in magnitude than that obtained by Sah et al, i.e. the effect of junction asymmetries is to lower the recombination current below the value predicted by the S-N-S theory. The recombination current expressed by relation 3.8 can be simplified using the following assumptions.

(a) when $N_D >> N_A$ the depletion layer width W is given by:

$$W = (2\varepsilon/qN_A)^{\frac{1}{2}} (V_b - V)^{\frac{1}{2}}, \tag{3.11}$$

(b) for an applied voltage V >> 2kT/q (0.05 V at 300 K),

sinh (qV/2kT) simplifies to ½ exp (qV/2kT). Under these conditions, the recombination current is given by:

$$J = J_o \exp(qV/2kT) \tag{3.12}$$

where

$$J_o = J_{oo} \exp(-E_g/2kT) \tag{3.13}$$

and

$$J_{oo} = (kT)\ (2N_c N_v \epsilon/qN_A \tau_{po} \tau_{no})^{\frac{1}{2}}\ (V_b - V)^{-\frac{1}{2}}\ f(b) \tag{3.14}$$

where ϵ is the dielectric constant.

(3) Tunneling current: The third type of dark current for the homojunctions is a tunneling current caused by electrons or holes tunneling from the conduction or valence band into energy levels within the bandgap, followed by either tunneling the remainder of the way into the opposite band or by a tunneling-recombination mechanism. The tunneling current through localized states is given by the expression[4]:

$$J = J_o \exp(\alpha V) \tag{3.15}$$

where

$$J_o = B\ N_t \exp(-\alpha V_b) \tag{3.16}$$

and

$$\alpha = \frac{4}{3\hbar}\left[m^* \epsilon \left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{\frac{1}{2}} \tag{3.17}$$

where m^* is the effective mass and the term α is essentially temperature independent, but J_o varies through the slight temperature-dependence of V_b.

In homojunctions, the injection and space charge recombination currents are usually the major components of the dark current. Tunneling can be important for high conductivity (0.01 Ω-cm) Si devices. The major differences between the injection and space charge recombination currents lie in their voltage, temperature and bandgap

dependences. The injection and space charge currents vary as exp(qV/kT) and exp(qV/2kT) respectively. The bandgap dependence of J_o for the injection currents is expressed in the form, $\exp(-E_g/kT)$, compared to $\exp(-E_g/2kT)$ for the space charge recombination current, indicating that recombination becomes increasingly important relative to injection mechanism for large bandgap materials and at low temperatures. Further details of the dark current mechanisms in homojunctions can be found in the books of Hovel[1] and Sze[2].

3.2.2 Heterojunctions

A heterojunction is simply a junction formed between two dissimilar semiconductors. The heterojunction is referred to as isotype if the two semiconductors have the same type of conductivity, otherwise it is referred to as an anisotype. In 1951, Shockley proposed the abrupt heterojunction to be used as an efficient emitter-base junction in a bipolar transistor[6]. This was followed by Gubanov's theoretical work on heterojunctions[7]. Kroemer[8] later analysed a similar, although graded, heterojunction as a wide-gap emitter. Since then heterojunctions have been extensively studied for applications such as light-emitter diodes, photodetectors and solar cells. Heterojunctions have been reviewed by Milnes and Feucht[9], Sharma and Purohit[10], and Casey and Panish[11].

The injection current model for heterojunctions was first developed by Anderson[12,13] as an extension of the conventional model for homojunctions[2] with barrier heights evaluated in terms of the energy-band profile. When the effects of dipoles and interface states are negligible, the energy band profile of the n-CdS/p-CdTe heterojunction at thermal equilibrium and zero-bias is as shown in Fig 3.2(a) and (b) before and after the formation of an abrupt junction[4].

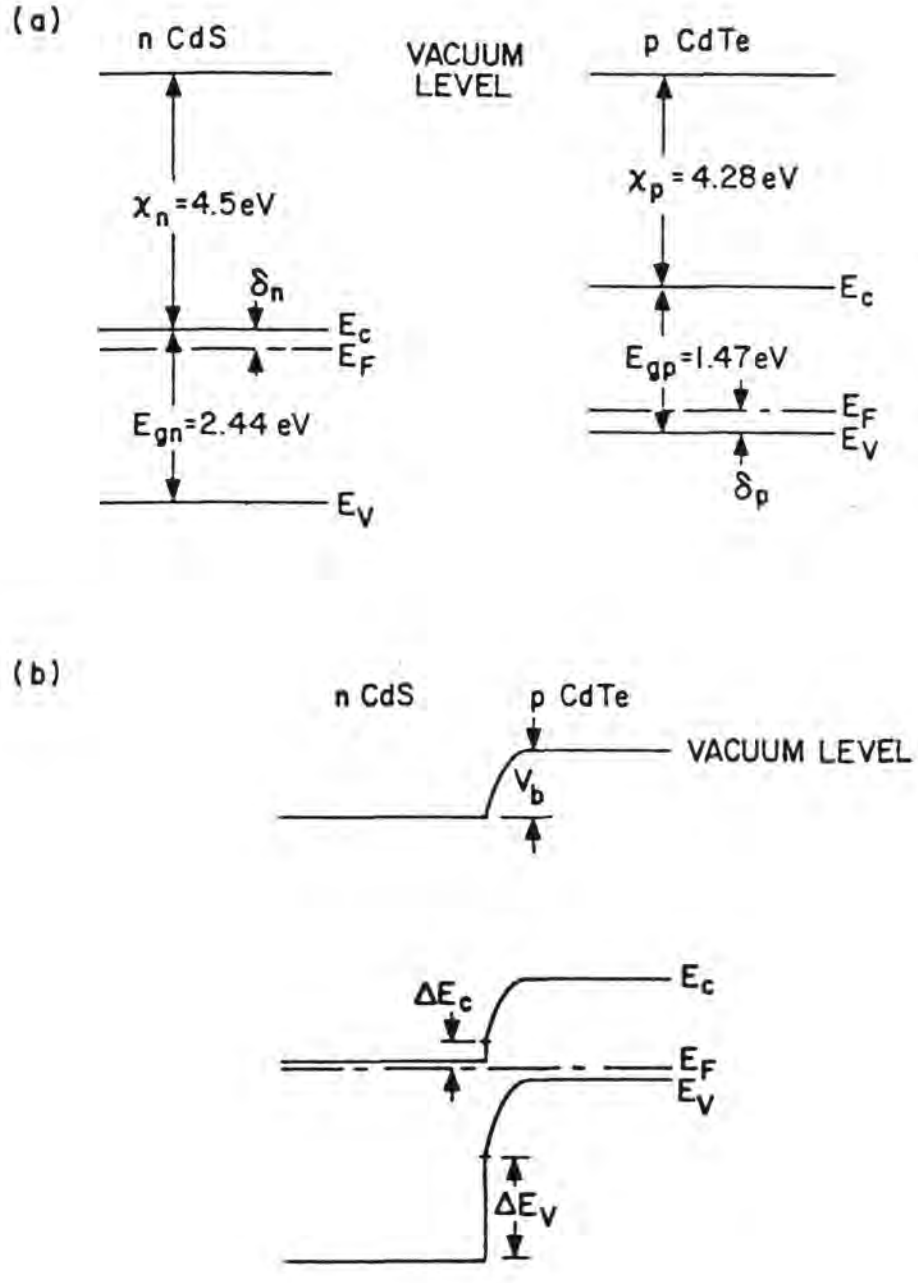

Fig. 3.2 : Equilibrium energy band diagram for the CdS/CdTe heterojunction (Ref. 4): (a) before; and (b) after the formation of an abrupt p-n junction.

Both the semiconductors are characterized by their electron affinities, bandgaps and work functions. In this (ideal) situation, the barrier height is given by:[1,4]

$$V_b = E_{gp} + \Delta E_c - \delta_n - \delta_p \tag{3.18}$$

where ΔE_c is the conduction band discontinuity at the hetero-interface, and δ_n and δ_p are the displacements of the Fermi level from the conduction band edge in the n(CdS) and p(CdTe) type materials, respectively. E_{gp} is the bandgap of p-type material. The discontinuities are given by:

$$\Delta E_c = \chi_p - \chi_n \tag{3.19}$$

$$\Delta E_v = (E_{gn} - E_{gp}) - \Delta E_c \tag{3.20}$$

where E_{gn} is the band gap of n-type material.

The current-voltage relationship takes the form[4,10]:

$$J = J_{oo} \exp(-qV_{bp}/kT) \left[\exp(qV_p/kT) - \exp(-qV_n/kT) \right] \tag{3.21}$$

where

$$J_{oo} = X\, q\, D_n\, N_D/L_n \tag{3.22}$$

and

$$V_{bp} = K_p\, V_b \text{ where } K_p = (1 + N_A\, \epsilon_p/N_D\, \epsilon_n)^{-1} \tag{3.23}$$

$$V_p = K_p V \tag{3.24}$$

$$V_n = K_n\, V \text{ where } K_n = 1 - K_p \tag{3.25}$$

V_{bp} is the portion of the built-in voltage on the p-side of the junction; V_p and V_n are the portions of the applied voltage appearing in the p and n-side of the junction; X is the transmission coefficient for electrons to pass the interface; D_n, L_n are the diffusion constant and

diffusion length respectively for electrons in the p-type semiconductor. The contribution to the current from the injection of holes into the wider bandgap semiconductor is negligible because of the large energy barrier to hole injection arising from ΔE_v. When the n-type (CdS) is highly doped with respect to the p-type semiconductor, the expression for the current-voltage simplifies as:

$$J = J_o \left[\exp (qV/kT) - 1 \right] \tag{3.26}$$

where

$$J_o = (XqN_D D_n / L_n) \exp(-qV_b/kT) \tag{3.27}$$

The energy band discontinuities and the appearance of interface states complicate the formulation of recombination current. Recombination can take place either through the interface states or in the space charge region and is affected by the band profile within the junction region. Dolega[14] proposed a recombination current model which is based on the assumption that the thermal emission of carriers takes place into a thin region at the junction where the recombination velocity is high due to the interface states. This model simply describes the heterojunction as two back-to-back Schottky diodes, having the boundary carrier concentrations dependent upon the applied bias. Similar treatments of the current transport assuming a metal-like thin layer of the recombination centres at the junction were developed by Oldham and Milnes[15] and Donnelly and Milnes[16]. Using Dolega's theory, Van Opdorp[17] derived an expression for the recombination current of the form[4,10]:

$$J = J_o \left[\exp (qV/AkT) - 1 \right] \tag{3.28}$$

where

$$J_o = J_{oo} \exp(-qV/AkT) \tag{3.29}$$

The diode factor A (which lies between 1 and 2) is a function of the imperfection densities in the two semiconductors and J_{oo} is a weak function of temperature. The recombination current within the depletion region can be approximated by the expression for the homojunctions given by equation 3.8.

The tunneling mechanism to describe the current-voltage characteristics of an abrupt heterojunction was first reported by Rediker et al[18]. The tunneling current for a heterojunction is essentially the same as for a homojunction except that: the number of states responsible for tunneling is much higher, due to interface states; an additional quantum mechanical reflection term must be included; and the tunneling energy barrier is modified by a distribution coefficient[4]. For $N_D >> N_A$, the tunneling current is represented by[1,9]:

$$J = J_o \exp(\alpha K_p V) \tag{3.30}$$

where

$$J_o = BXN_t \exp(-\alpha V_b) \tag{3.31}$$

$$\alpha = (4/3\hbar)(m^* \varepsilon_p / N_A)^{\frac{1}{2}} \tag{3.32}$$

Here ε_p and N_A are the dielectric constant and the doping densities respectively of the p-type semiconductor. The tunneling current may also be expressed as[4]:

$$J = J_{oo} \exp(\beta T) \exp(\alpha K_p V) \tag{3.33}$$

where

$$\beta = -\alpha \quad \partial E_{gp}/\partial T + \partial \Delta E_v/\partial T - \frac{\partial \delta n}{\partial T} - \partial \delta_p/\partial T \qquad (3.34)$$

In addition to the tunneling of carriers, a multi-step tunneling-recombination process has been proposed by Riben and Feucht [19,20]. The resultant current-voltage relation is similar to equation 3.33. If a number of tunneling steps are involved, the coefficient α is modified by the number of steps R so that α becomes[20,21]:

$$\alpha^* = \alpha/(R)^{\frac{1}{2}} \qquad (3.35)$$

Adirovich et al[21] used the model expressed by equations 3.33 and 3.35 to explain the behaviour of CdS/CdTe heterojunctions.

3.2.3 Non-ideal Diodes

The ideal behaviour of the p-n junctions discussed earlier is not generally seen experimentally. In real systems there are additional effects which may be lumped together in the form of a series resistance R_s and a shunt resistance R_{sh}, so that experimental behaviour may be approximated by the relation[22]:

$$J - (V-R_sJ)/R_{sh} = \sum_i J_{oi} \left[\exp\{\alpha_i(V-JR_s)\} - 1 \right] \qquad (3.36)$$

where the sum over i indicates various contributions to the diode current which can occur and α_i is written for q/A_ikT.

The series resistance of the diode arises from two major sources: (1) the resistance of the series components; and (2) of the electrodes

and contacts to the external circuit. Shunt resistance arises from the current leakage paths within the diode. Generally, the shunt resistance in "good" diodes is so large that its effects are negligible. In cases where its effects are significant, gross defects in the junction are usually the cause. The outer boundaries of a junction device inevitably permit some leakage of current, but even in single crystal diodes, some areas are found to have much higher leakage currents than average[23]. Surface damage during fabrication seems to play a significant role in reducing the shunt resistance in these areas[23,24].

In thin film devices the possibilities for current leakage are higher due to their structure[24]. Thin films usually have a columnar structure with a junction formed on each crystallite. Unless great care is taken in the deposition of the base film to ensure high packing density, and in the formation of the junction, leakage paths can exist down the grain boundaries. The presence of gross defects, such as pin holes in the outer junction layer of the device formed by sequential evaporation can also lead to shorting between the collecting grid and the base layer[24].

3.2.4 Junction Capacitance

The depletion width and capacitance of a p-n junction can be obtained by solving Poisson's equation for either side of the junction. An exact solution of the equation (which requires numerical techniques) is generally not necessary, since approximate analytical solutions are adequate for most cases of interest. It is common to assume that in the space charge region, all the donors and acceptors are ionized and for space charge computations, the free carrier density can be neglected.

Thus for a homojunction Poisson's equation can be written as[2,25]:

$$-\frac{\partial^2 V}{\partial x^2} = \rho/\epsilon\epsilon_o = \frac{q}{\epsilon\epsilon_o}\left[(p(x)-n(x) + N_D(x) - N_A(x)\right]$$

$$\cong \frac{q}{\epsilon_n\epsilon_o} N_D(x) \quad \text{for } 0 < x < x_n \tag{3.37}$$

$$\cong \frac{q}{\epsilon_p\epsilon_o} N_A \text{ for } -x_p < x < 0$$

In this case the origin has been taken as the junction plane, ρ is the charge density, ϵ_o is the permittivity of free space, x_n and x_p are the widths of the space charge region in the n and p materials respectively. The variation of $N_D(x)$ and $N_A(x)$ is generally assumed to be either a step function (abrupt junction) or a linear function of x (graded junction).

For heterojunctions the abrupt approximation is assumed to be valid, although some intermixing of the two materials on an atomic scale probably does occur. Assuming however, that the abrupt approximation applies, charge neutrality demands that

$$N_D x_n = N_A x_p \tag{3.38}$$

Using equations 3.37 and 3.38 the width of each space charge region, as a function of applied voltage can be written:

$$x_n = \left(\frac{2N_A\epsilon_n\epsilon_p(V_b-V)\epsilon_o}{q N_D(\epsilon_p N_A + \epsilon_n N_D)}\right)^{\frac{1}{2}} \tag{3.39}$$

$$x_p = \left(\frac{2N_D\epsilon_n\epsilon_p(V_b-V)\epsilon_o}{q N_A(\epsilon_n N_D + \epsilon_p N_A)}\right)^{\frac{1}{2}} \tag{3.40}$$

The total width, W of the depletion region therefore is given by:

$$W = x_n + x_p = \left(\frac{2\varepsilon_n\varepsilon_p(N_D^2 + N_A^2)(V_b - V)\varepsilon_o}{q\, N_D N_A(\varepsilon_n N_D + \varepsilon_p N_A)} \right)^{\frac{1}{2}} \tag{3.41}$$

The relative voltage supported in each side is given by:

$$\frac{V_{bn} - V_n}{V_{bp} - V_p} = \frac{N_A\, \varepsilon_p}{N_D\, \varepsilon_n} \tag{3.42}$$

where V_n and V_p are the voltage drops in the n and p material respectively, and $V_b = V_{bn} + V_{bp}$.

For an abrupt heterojunction with uniform doping, the capacitance per unit area (when dipole and interface state effects are negligible), is given by[4,9]:

$$C = \left[\frac{qN_D N_A \varepsilon_n \varepsilon_p}{2(\varepsilon_n N_D + \varepsilon_p N_A)(V_b - V)} \right]^{\frac{1}{2}} \tag{3.43}$$

If $N_D >> N_A$ then equation 3.43 takes the form:

$$C = \left[\frac{q\varepsilon_p N_A}{2(V_b - V)} \right]^{\frac{1}{2}} \tag{3.44}$$

The net acceptor density N_A can thus be obtained from the slope of a plot of C^{-2} vs V, and the built-in voltage V_b from the intercept on the voltage axis.

3.3 Light Current Mechanisms

3.3.1 Equivalent Circuit

When a diode is exposed to light of sufficient energy ($h\nu > E_g$) electron-hole pairs are generated. These carriers diffuse to the junction where they are separated to produce useful electrical energy. This can be modelled as a light dependent current generator connected in parallel with the diode. This is illustrated in the equivalent circuit of Fig 3.3 which includes series and shunt resistance components.

The general expression for the total current through the illuminated diode is given by the following equation which is a linear super position of the dark and light generated currents[26]

$$J - \frac{V-JR_s}{R_{sh}} = \sum_i J_{oi}\left[\exp\left\{\frac{q}{A_i kT}(V-JR_s)\right\} - 1\right] - J_L(V) \qquad (3.45)$$

where J_L is the light generated current. This is discussed in the following section, with reference only to the window-absorber heterojunction solar cells (Section 2.1.2). Under illumination, the dark current voltage characteristics are translated by the amount of light current. The dark and light current-voltage characteristics for an ideal case are given in Fig 3.4.

3.3.2 Generation and Collection of Photocarriers

Although the absorption of light takes place in both the absorber and the collector of a heterojunction solar cell, the analysis of photocarrier generation and collection is greatly simplified by assuming that the light is absorbed mainly in the absorber. In particular, for the CdS/CdTe cell the following assumptions are made[4]:

(1) light absorbed in the CdS (window layer) does not contribute to the photocurrent; (2) the CdTe layer is wider compared to the absorption length so that back surface effects can be neglected; (3)

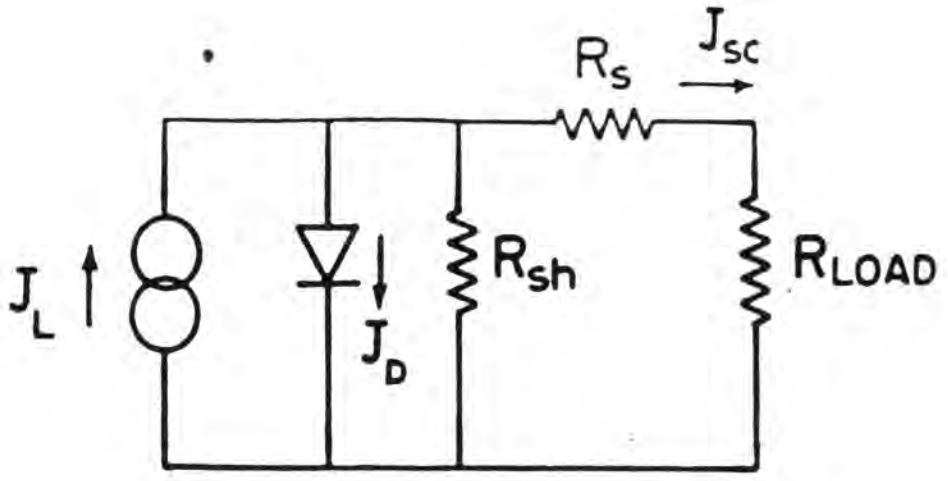

Fig. 3.3 : Equivalent circuit of a solar cell.

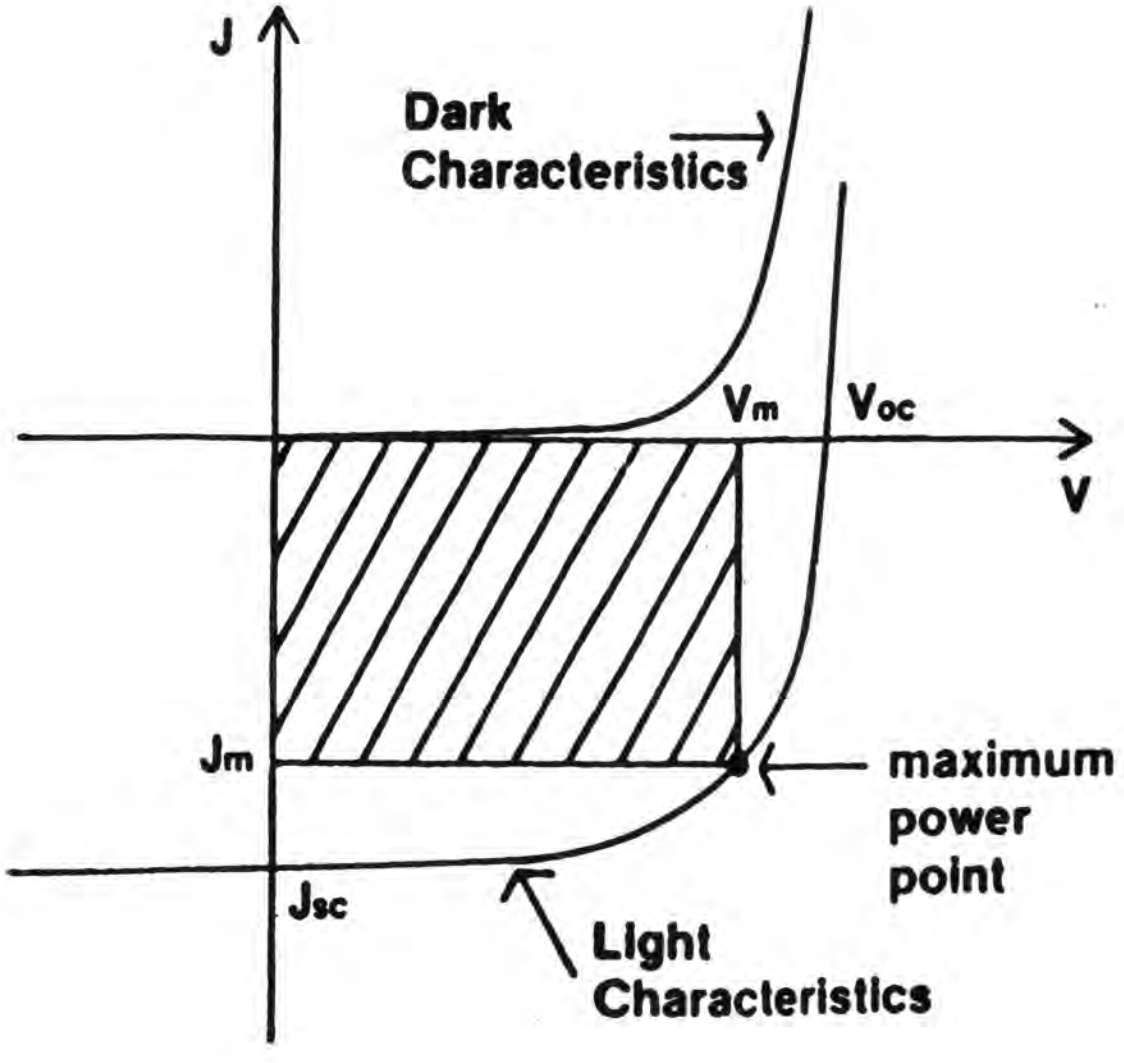

Fig. 3.4 : Typical dark and light J-V characteristics of an ideal solar cell

there are no electric fields outside the depletion region; and (4) the electric field is sufficiently strong in the depletion region to separate all carriers generated within it, or arriving at its boundaries[27]. The collection of photogenerated minority carriers in the CdTe (absorber) is evaluated by considering the contribution from two regions: (a) the depletion region, where the high junction field assists the carrier collection; and (b) the bulk, characterized by a constant minority carrier diffusion length. The collection of photogenerated carriers may thus be described as the product of two terms: a generation term representing the number of carriers generated by absorption of light; and a carrier collection term describing the fraction of carriers arriving at a specific boundary (i.e. crossing the junction).

If ϕ (λ) is the photon flux density incident on the CdTe and α (λ) is the optical absorption coefficient then the absorption of light in CdTe is described by the relation[4].

$$\phi(x) = \phi_o (\lambda) \exp[-\alpha(\lambda)x] \tag{3.46}$$

where $\phi(x)$ is the photon flux density at a distance x from the surface, $\phi_o(\lambda)$ is the photon flux entering the CdTe. The number of photons absorbed in the depletion region(width W) is $\phi_o[1-\exp(-\alpha W)]$ and the total generation of carriers in this region is therefore:

$$G_W = a_o \phi_o [1-\exp(-\alpha W)] \tag{3.47}$$

where a_o is the quantum efficiency for the absorbed light to produce electron-hole pairs (the ratio of the number of charge carriers generated to the number of photons absorbed), and G_W is the number of carriers generated in the depletion region. Since the bulk of the

absorber semiconductor is assumed to be thick enough to absorb all the photons reaching it, then the total photocarriers generated in the bulk, G_B is :

$$G_B = a_o \phi_o \exp(-\alpha W) \tag{3.48}$$

Assuming total carrier collection, the photocurrent reaching the junction interface from the depletion region is directly proportional to the number of photons absorbed and is given by:

$$J_W = qG_W = q\, a_o \phi_o [1-\exp(-\alpha W)] \tag{3.49}$$

The photocurrent due to the diffusion of photogenerated carriers (from the bulk) to the edge of the depletion region is[4,16]:

$$J_B = q\, G_B (1 + 1/_{\alpha L})^{-1} \tag{3.50}$$

$$J_B = q\, a_o \phi_o (1 + 1/_{\alpha L})^{-1} \exp(-\alpha W) \tag{3.51}$$

where L is the minority carrier diffusion length in the bulk CdTe. The total photocurrent to the junction interface, J_I, is therefore the sum of J_W and J_B, i.e.

$$J_I = q\, a_o \phi_o [1-(1 + \alpha L)^{-1} \exp(-\alpha W)] \tag{3.52}$$

The recombination current J_R due to interface states can be expressed as:

$$J_R = q\, S n_I \tag{3.53}$$

where S is the recombination velocity and n_I is the density of minority carriers at the interface. Conservation of currents at the interface leads to the relation:

$$J_I = J_R + J_L \tag{3.54}$$

where J_L is the current which enters the collector (CdS). The light current J_L may be expressed as[4]:

$$J_L = q\, n_I\, \mu_e E_I \tag{3.55}$$

where μ_e is the electron mobility in the junction region and E_I is the electric field at the junction interface. Using equations 3.53-3.55, J_L can be written:

$$J_L = \left(1 + S/\mu_e E_I \right)^{-1} J_I \tag{3.56}$$

and substituting for J_I from equation 3.52, the photogenerated current reaching the CdS is:

$$J_L = q\, a_o\, \phi_o (1 + S/\mu_e E_I)^{-1} \left[1 - (1 + \alpha L)^{-1} \exp(-\alpha W) \right] \tag{3.57}$$

Equation 3.57 may be written as:

$$J_L = q a_o \phi_o h(V) g(V) \tag{3.58}$$

where $h(V) = (1 + S/\mu_e E_I)^{-1}$ (3.59)

and $g(V) = [1 - (1 + \alpha L)^{-1} \exp(-\alpha W)]$ (3.60)

The term g(V) represents the fraction of photogenerated minority carriers reaching the junction, and h(V) is the fraction of minority carriers that safely pass through the junction upon reaching it. The product of h(V) and g(V) is called the collection function H(V) i.e.

$$H(V) = h(V) g(V) \tag{3.61}$$

3.3.3 Spectral Response and Quantum Efficiency

As described in Chapter 2, a solar cell is characterized by "external" or performance parameters such as its short circuit current, open circuit voltage etc. In addition, some "internal" quantities also exist of which the principal ones are the spectral response and the quantum efficiency.

The spectral response is the photocurrent collected at each wavelength relative to the number of photons incident on the surface of the device. The quantum efficiency (also known as internal spectral response) is the ratio of the number of collected carriers to the number of photons which enter the cell[28]. Both the spectral response (in mA mW^{-1}) and quantum efficiency express the solar cell's ability to convert light into electrical current and are a function of the wavelength of the incident light. The quantum efficiency gives a more physical insight into the actual behaviour of the cell while spectral response expresses conversion performance in units that can be measured, and which are of more interest to the user.

By definition, the quantum efficiency (spectral response corrected for reflection loss is:

$$Q(\lambda) = J_L/q\phi_o \tag{3.62}$$

where ϕ_o is the photon flux entering the cell. The relation between incident photon flux ϕ_s and the photon flux entering the cell ϕ_o is given by:

$$\phi_o = \phi_s\ (1-R) \tag{3.63}$$

where R is the overall reflection loss. So substituting for J_L from equation 3.58 the quantum efficiency can be expressed as:

$$Q(\lambda) = a_o\ H(V) \tag{3.64}$$

where a_o is the quantum efficiency of the absorbed light to produce electron-hole pairs, and is equal to unity. Thus $Q(\lambda)$ for the CdS/CdTe solar cell becomes:

$$Q(\lambda) = (1 + S/\mu_e E_I)^{-1} [1-(1 + \alpha L)^{-1} \exp(- \alpha W)] \quad (3.65)$$

For CdS/CdTe heterojunction cells, the short wavelength cut-off of the spectral response is defined by the sharp absorption edge of the window material (CdS) and the shape of the long wavelength edge by the collection of charge carriers from the CdTe, given by the collection function H(V). The quantum efficiency is voltage dependent through the variation of the electric field at the junction and the width of the depletion region with applied bias.

3.4 Rectifying Metal-Semiconductor Contacts

3.4.1 Schottky Barriers

Because of their simple structure and relative ease of fabrication, Schottky devices were used in the present study as a means of characterizing the materials. It is therefore essential to give a brief description of Schottky devices and their electrical characteristics. The earliest studies on metal-semiconductor (MS) rectifying systems are generally attributed to Braun[29], who in the 19th century observed that the total resistance of a metal-semiconductor contact depended on the polarity of the applied voltage and the surface conditions. This was followed by the development of the point-contact rectifier in 1904[30]. However, it was not until after the introduction of the band theory of solids[31] by Wilson in 1931, that Schottky was able to offer an explanation for the effect. He suggested that there would be a barrier (i.e. the Schottky barrier) at the contact due to stable space charges in the semiconductor[32]. In the Schottky model the density of charged impurities in the barrier region is assumed to be constant, so that the

electric field increases linearly and the potential quadratically as the metal is approached. The basic theory and the theoretical development of rectifying MS contacts have been fully reviewed by Henisch[33].

When an intimate contact is made between a semiconductor of work function ϕ_s and a metal of work function ϕ_m, a readjustment of charges takes place to establish thermal equilibrium. For a metal contact to an n-type semiconductor with $\phi_m > \phi_s$, a transfer of electrons from the semiconductor to the metal occurs until the Fermi levels are aligned in equilibrium. To establish this thermodynamic equilibrium the Fermi level (or energy bands) in the semiconductor are lowered by $\phi_m - \phi_s$, and a potential barrier is formed at the surface. This potential difference $q\phi_m - q(\chi+V_n)$ is called the contact potential, where $q(\chi + V_n)$ is the work function of the semiconductor with $q\chi$ as the electron affinity measured from the bottom of the conduction band E_c to the vacuum level, and qV_n is the energy difference between E_c and the Fermi level of the semiconductor (Fig 3.5). As a result of the electron flow from the semiconductor to the metal, a charge is built up on the metal surface. This is balanced by an equal and opposite charge in the semiconductor. Since the donor concentration in the semiconductor is many orders of magnitude less than the concentration of electrons in the metal, the ionized uncompensated donors occupy a depletion layer of thickness W, and the bands in the semiconductors are bent upward.

The barrier height is simply the difference between the metal work function and the electron affinity of the semiconductor.

$$q\phi_{bn} = q(\phi_m - \chi) \tag{3.66}$$

For an ideal contact between a metal and a p-type semiconductor, the barrier height is expressed:

$$q\phi_{bp} = E_g - q(\phi_m - \chi) \tag{3.67}$$

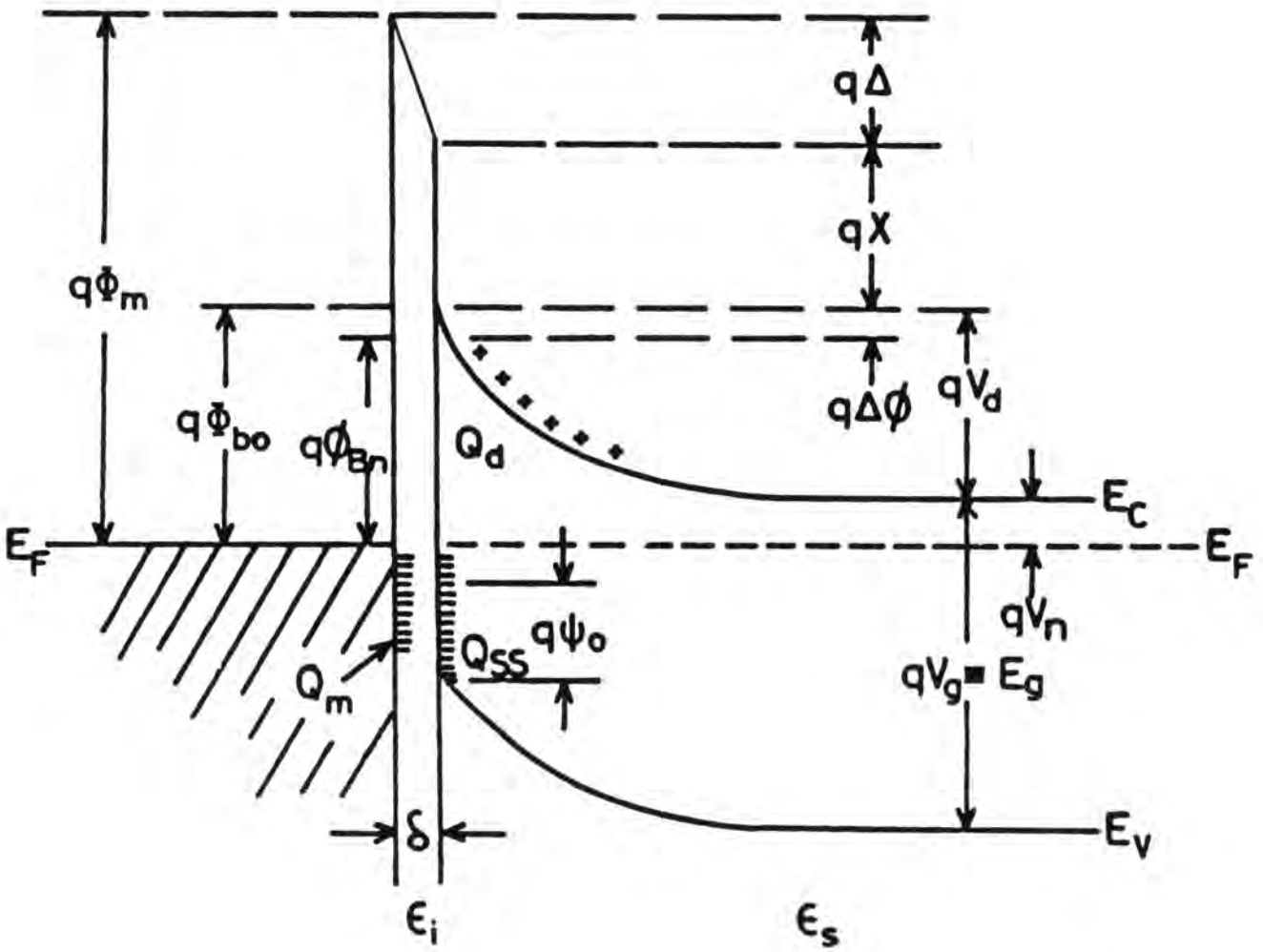

Fig. 3.5 : Detailed energy band diagram of a metal n-type semiconductor contact with a thin interfacial layer (Ref. 36)

Thus for a given semiconductor, the sum of the barrier heights on n and p-type substrates is thus expected to be equal to the bandgap. In practice there will be surface states, and if the density of surface states is sufficiently large, then the resulting surface charge will dominate the junction behaviour. As a result, the barrier height is determined by the semiconductor surface and will be independent of the metal work functions. In practice, the barrier height will also be reduced as a result of the image force, the so called Schottky effect.

When an electron is at a distance x from a metal, a positive charge will be induced on the metal surface. The force of attraction between the electron and induced positive charge, known as the image charge, is given by Coulomb's law

$$F = - q^2/4\pi(2x)^2\varepsilon_o \tag{3.68}$$

The potential energy of an electron at a distance x from the metal surface is:

$$P.E(x) = \int_{\infty}^{x} F.dx = \frac{q^2}{16\pi\ \varepsilon_o x} \tag{3.69}$$

When an electric field E is applied, the total potential energy (in eV) is given by:

$$P.E(x) = \frac{q^2}{16\pi\ \varepsilon_o x} + qEx$$

The Schottky barrier lowering $\Delta\phi_{bn}$ and the location of the lowering x_m are then given by the condition:

$$\frac{d}{dx}\ [P.E(x)] = 0 \tag{3.70}$$

Since $x_m = (q/16\pi\ \varepsilon_o E)^{\frac{1}{2}}$ cm (3.71)

$$\Delta\phi_{bn} = (q/4\pi\ \varepsilon_o)^{\frac{1}{2}} \tag{3.72}$$

The idea of image force lowering of the barrier also applies to metal-semiconductor systems[34]. In this case the field is replaced by the maximum field at the interface and the permittivity ε_o by ε_s. Because of the larger values of ε_s in these sytems, ϕ_{bn} and x_m are smaller than those for corresponding metal-vacuum system (for example, if $\varepsilon_s = 16\ \varepsilon_o$, $\Delta\phi_{bn} = 0.03$ V for $E = 10^5$ V/cm). Although the magnitude of image force lowering is small it can have a significant effect on current transport processes in MS systems.

3.4.2 Depletion Width and Capacitance

The width W of the depletion region is given by Sze[2] as:

$$W = \sqrt{\frac{2\varepsilon s}{qN_D}\ (V_{bi} - V - kT/q)} \tag{3.73}$$

where kT/q arises from the contribution of the majority carrier distribution tail. Thus the depletion width increases with reverse bias and is inversely proportional to N_D, the density of uncompensated donors. The change in W will lead to a corresponding change in capacitance. Neglecting the contribution of free carriers to the electric field, and assuming that the surface density is low, ($< 10^{12}$ cm^{-2} eV^{-1})[35] and that all the donor impurities are ionized, then the capacitance of the barrier is only due to the space charge Q_{sc} (per unit area) and can be written as:

$$Q_{sc} = qN_D W = [(2q\epsilon N_D (V_{bi} - V - kT/q)]^{\frac{1}{2}}\ Col/cm^2 \tag{3.74}$$

and the depletion layer capacitance C per unit area is then:

$$C = |\partial Q_{sc}|/\partial V = [(q\ \varepsilon_s\ N_D)/2(V_{bi}-V-kT/q)]^{\frac{1}{2}} = \varepsilon_s/W \text{ F cm}^{-2} \qquad (3.75)$$

The depletion layer capacitance is inversely proportional to the depletion width W which in turn depends on the applied bias. The equation (3.75) is often written as:

$$1/C^2 = 2(V_{bi}-V-kT/q)(q\ \varepsilon_s\ N_D)^{-1} \qquad (3.76)$$

providing that N_D remains constant throughout the depletion region. A plot of C^{-2} vs V is a straight line, the slope of which is

$$d(C^{-2})/dV = -(2/q\ \varepsilon_s N_D) \qquad (3.77)$$

and gives N_D,

$$N_D = \frac{2}{q\ \varepsilon_s \frac{dC^{-2}}{dV}} \qquad (3.78)$$

The intercept on the voltage axis gives the contact potential.

3.4.3 Current Transport Mechanisms in Schottky Barriers

The current transport in metal-semiconductor barriers is mainly due to majority carriers in contrast to p-n junctions, where minority carriers are responsible. In Schottky barrier diodes the current transport under forward bias is due to the following mechanisms[2]:

(a) transport of majority carriers across the potential barrier,

(b) quantum mechanical tunneling through the barrier;

(c) recombination in space charge region;

(d) minority carrier injection from the metal to the semiconductor.

These processes are illustrated in Fig 3.6 for a metal n-type semiconductor diode in the forward bias mode. The major contribution to the current transport is provided by the first mechanism, and other current paths usually arise from the non-ideal nature of real diodes.

For the emission of electrons over the barrier, the electrons must first be transported through the depletion region of the semiconductor. The conduction in this region takes place by the normal diffusion and drift mechanisms[36]. That is why the first theory of conduction in Schottky diodes was the so called diffusion theory proposed by Wagner[37], and Schottky and Mott[36]. However in 1942, Bethe[38] proposed that thermionic emission over the barrier was the limiting mechanism. Both these ideas were later combined in a joint thermionic emission-diffusion theory by Crowell and Sze[39]. If the space charge region width is less than the diffusion length of electrons, the thermionic emission limited forward current density is expressed by:[36]

$$J_F = J_s \left[\exp(qV/kT)-1\right] \tag{3.79}$$

where the reverse saturation current is given by:

$$J_s = R^* T^2 \exp(-\phi_{bn}/kT) \tag{3.80}$$

Here R^* is the modified Richardson constant (corresponding to effective mass m^*) and is given by

$$R^* = 4\pi q\, m^* \frac{k^2}{h^3} = 120 \frac{m^*}{m} \text{ amp cm}^{-2} \text{ K}^{-2} \tag{3.81}$$

When the space charge region is greater than the diffusion length, then diffusion theory applies and the forward current-voltage relation becomes[36]:

$$J_F = q\, N_c \mu_e E_{max} \exp\left(\frac{-q\phi_{bn}}{kT}\right)\left[\exp\frac{qV}{kT} - 1\right] \tag{3.82}$$

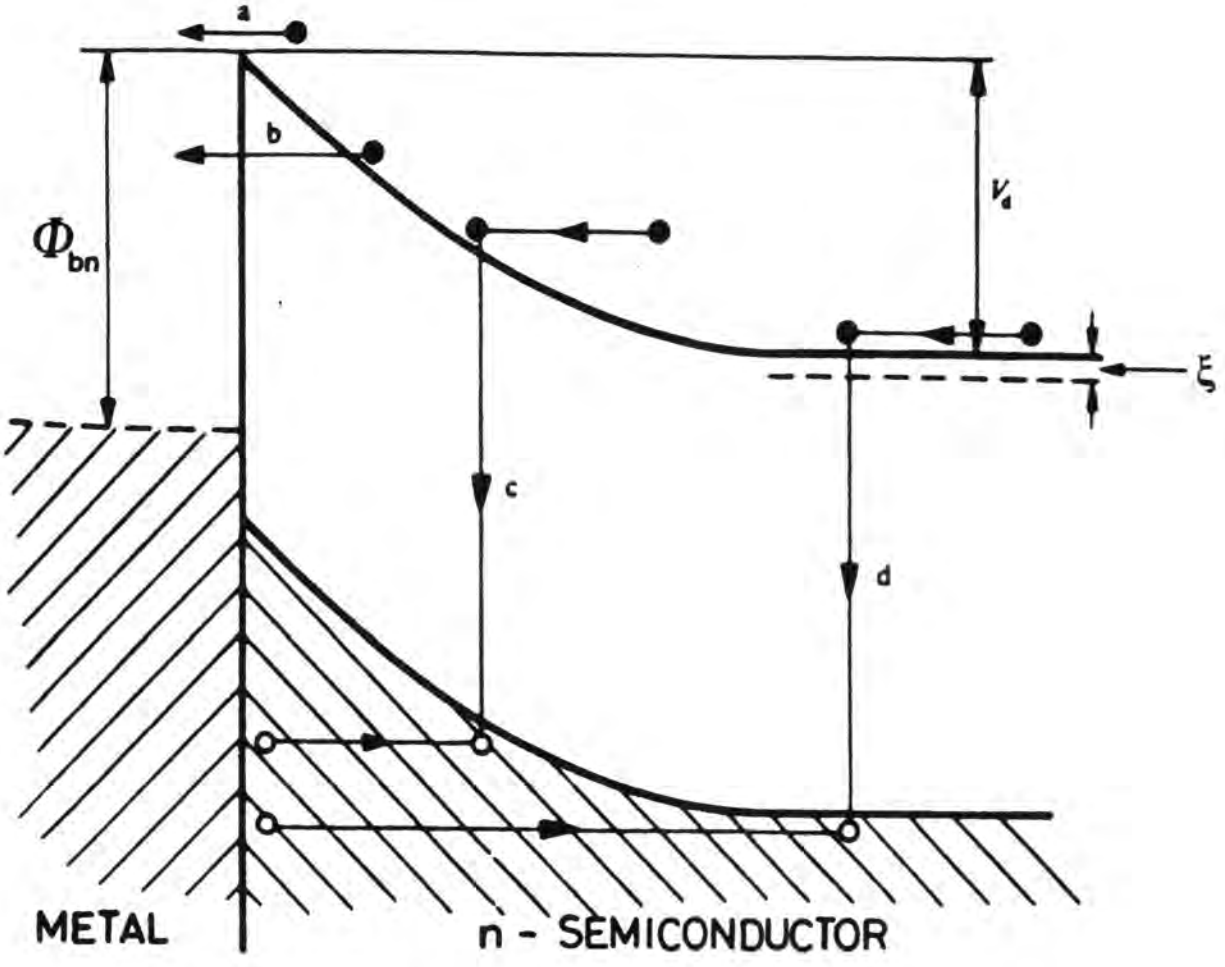

Fig. 3.6 : Current transport mechanisms in a forward-biased Schottky barrier (Ref. 36)

where E_{max} is their maximum electric field at the junction and N_c the effective density of states in the conduction band is:

$$N_c = 2\ (2\ m^*\pi kT/h^2)^{3/2} \tag{3.83}$$

For the general case in which the space charge region is comparable in thickness to the diffusion length, both mechanisms apply. Crowell and Sze derived the following expression for the current-voltage relationship:

$$J_F = (qN_cV_r)(1+V_r/V_d)^{-1}\ [\exp(-q_{bn}/kT)]\ [\exp(qV/kT)-1] \tag{3.84}$$

where $V_r = R^*T/qN_c$ is the effective recombination velocity at the potential energy maximum, and V_d is the effective diffusion velocity for the transport of electrons from the edge of the depletion region to the top of the potential energy maximum. If $V_d << V_r$ the pre-exponential term in equation (3.84) reduces to qN_cV_r and the diffusion theory applies. If $V_d >> V_r$ the thermionic emission process is dominant.

However, in practice Schottky barriers deviate from the ideal behaviour, and the experimental forward current-voltage relation is usually expressed as[21]:

$$J_F = J_s \exp\ (qV/AkT) \tag{3.85}$$

for bias voltages $V > 3kT/q$

The parameter A is known as the ideality or quality factor and is generally greater than unity as a result of non-ideal interface conditions. A detailed discussion of non-ideal diode mechanisms such as recombination and tunneling has been given by Rhoderick[35].

3.5 Defect and Impurity Levels

Real semiconductor crystals always have some imperfections associated with impurities or native crystallographic defects. These defects disturb the periodicity of the perfect crystal potential, and

give rise to new states in the locality of the defect, and with energy levels that often lie within the forbidden gap of the semiconductor. They can have a very strong influence on the properties of the material and the various defect or impurity energy levels are often referred to as recombination centres, electron or hole traps, donor or acceptor centres, optical absorption centres etc. depending on their role in the electrical behaviour of the semiconductor. The parameters necessary to describe a particular energy level are the ionization energy, the density, the thermal and optical capture cross-sections for holes and electrons, and the thermal and optical emission rates for electrons and holes[40].

3.5.1 Shallow Levels

The description of a given defect or impurity level by all its parameters is often unnecessary and inconvenient, so a certain degree of classification is employed. It is common to classify the energy levels as either "shallow" or "deep" states according to their ionization energy. The former (i.e. shallow) energy levels which are located near the allowed bands have ionization energies comparable to kT. They can be classified as either donors (positively charged when ionized) or acceptors (negatively) charged when ionized. Since these centres are usually ionized at room temperature, they are widely used in semiconductor device technology for modifying the type and degree of conductivity. Shallow centres are normally substitutional impurities taken from the group of the periodic table neighbouring that of the host material and have energy levels with binding energy of less than 50 meV.

Subject to an appropriate correction for the dielectric constant of the semiconductor, and the effective mass of the charge carriers, shallow levels are well described by a simple hydrogenic model. Their

ionization energy for a donor impurity can therefore, be calculated from the expression[41]:

$$E_i = (m^* q^4)/(2\ h^2 \varepsilon n^2) = 13.6\ (m^*/m\varepsilon n^2)\ eV \qquad (3.86)$$

This was first proposed by Kohn[42] and has been successfully and widely applied to the characterization of shallow levels in semiconductors.

3.5.2 Deep Levels

Energy levels which are positioned further into the forbidden gap are classified deep levels and cannot be described by the simple effective mass theory. Deep centres with binding energies much larger than those of shallow centres are often generated by native defects or by replacement of the host lattice atom by an atom which does not belong to an adjacent group of the periodic table. These levels seem to be present in all known semiconductors and even in small concentrations may have a very important role in controlling the electrical properties of a semiconductor. Their effect on minority carrier lifetime is perhaps the most direct and important.

The usefulness of deep levels clearly depends on the specific device application and the particular semiconductor. For example, large minority carrier lifetimes are desirable in optoelectronic devices, i.e. LEDs photoconductor and solar cells. In the latter case, deep levels will influence current collection (because of reduced minority carrier lifetimes) and consequently result in poor conversion efficiencies; In contrast fast switching Si devices require short but controlled carrier lifetime which is achieved by the incorporation of deep gold levels.

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CHAPTER 4

PREPARATION OF MATERIALS AND DEVICES

4.1 Introduction

The work presented in this thesis relates to the study of both bulk crystal and thin film photovoltaic devices. This chapter is, therefore, devoted to a description of the techniques employed in the fabrication of the various device structures investigated. Most of the starting material used in this work was prepared in house, and hence the first sections of this Chapter deal with synthesis of CdTe, the growth of crystals, thin film deposition and resistivity control. The Chapter continues with a description of the substrate polishing and preparation procedures, and with the formation of ohmic contacts to the devices. The final part of the Chapter is concerned with the details of the fabrication of photovoltaic p-n junctions and Schottky barrier structures.

4.2 Material Preparation

4.2.1 Synthesis of Cadmium Telluride

The CdTe starting material for the growth of bulk crystals and deposition of thin films was synthesized in this laboratory by direct combination of high purity double zone refined cadmium (99.9999%) and tellurium (99.9999%) supplied by M.C.P.Electronic Material Ltd. A charge of about 450 g of cadmium and tellurium in stoichiometric proportions was loaded into a silica tube sealed at one end. The tube was evacuated to a pressure of $\sim 10^{-6}$ torr and left to outgas for 24 hr . The tube was then sealed using an oxy-acetylene gas torch and placed in a furnace. The furnace temperature was increased slowly to 940°C over a period of a few hours and thereafter maintained at that temperature for 3 days. The charge was cooled down slowly over several

hours. This produced a solid lump of CdTe which was then crushed mechanically and used as source material for the preparation of bulk crystals and thin films.

4.2.2 Purification of the CdS Charge Material

Commercially available CdS was known to contain trace amounts of both volatile and non-volatile impurities. These impurities would seriously affect the opto-electronic properties of the CdS and of the devices fabricated from it. It was therefore necessary to purify the source material, before using it to deposit thin films.

The CdS source material which was supplied by G.E.America, was purified by sublimation in an argon flow-run process. A small quantity (~ 100 g) of CdS was placed in a silica boat and loaded at the one end of a silica tube next to two silica liners. This assembly was then placed in a furnace with one end of the tube connected to a controlled supply of pure argon and the other connected to the exhaust. The tube was first flushed with argon for one hour and then heated to 600°C for six hours to drive off the volatile impurities from the charge. The furnace temperature was next raised to 1160°C while maintaining the argon flow.

The charge was then transported from the source boat (where sublimation was occuring) to the liners in the cooler part of the furnace. Needles and platelets of yellow CdS formed on the walls of the first liner, while most of the more volatile impurities and CdS that had failed to condense on the walls of the first liner were collected in the second liner. Non-volatile impurities such as Zn,Fe and Mn, were left in the residue of the charge. The CdS platelets deposited in the first liner were shaken off the silica but the remaining layer attached to the liner was not removed as it may have contained impurities that had diffused out of the silica. The Durham synthesized CdTe used for thin film growth was also purified by this method.

4.2.3 Growth of CdTe Bulk Crystals

There are three general approaches to the growth of CdTe bulk crystals. The most widely used method is to grow the crystal from congruent melts using Bridgman and Vertical Zone Refining techniques. These methods are capable of producing large single crystals[1] at relatively high growth rates. In addition, the crystal grower has greater freedom in controlling the type and conductivity of the crystals. However, because of the high temperatures involved, contamination from the quartz crucible is possible, and thus lower temperature methods of growth from Te-rich solutions have been investigated. Thirdly, the crystals may be grown from the vapour phase at lower temperaures thus avoiding contaminations associated with the high temperature Bridgman growth. Crystals grown from the vapour phase have been shown to be of comparable perfection and purity.

The cadmium telluride crystals used in the present study were grown in our laboratory by a vapour phase technique originally developed by Clark and Woods[2] for CdS and recently adapted for CdTe. A specially designed growth tube fabricated to our specification by Heraeus Ltd. was used to grow the crystals. In essence, this consisted of a silica capsule in which was fitted a conical growth tip, and a small bore tube formed the "tail". The function of the latter was to provide some control of the constituent partial pressures during growth.

A measured quantity of synthesized polycrystalline charge of CdTe (Section 4.2.1) was loaded into the growth capsule and an appropriate amount of one of the elements was placed in the tail. The tube was then evacuated to a pressure of $\sim 10^{-6}$ torr and allowed to outgas for 24 hrs. After this, the tube was sealed under vacuum. The sealed tube was suspended vertically in a double zone furnace as shown in Fig 4.1. Initially the tube was placed in the furnace with the growth tip at the highest temperature, to sublime any CdTe debris away

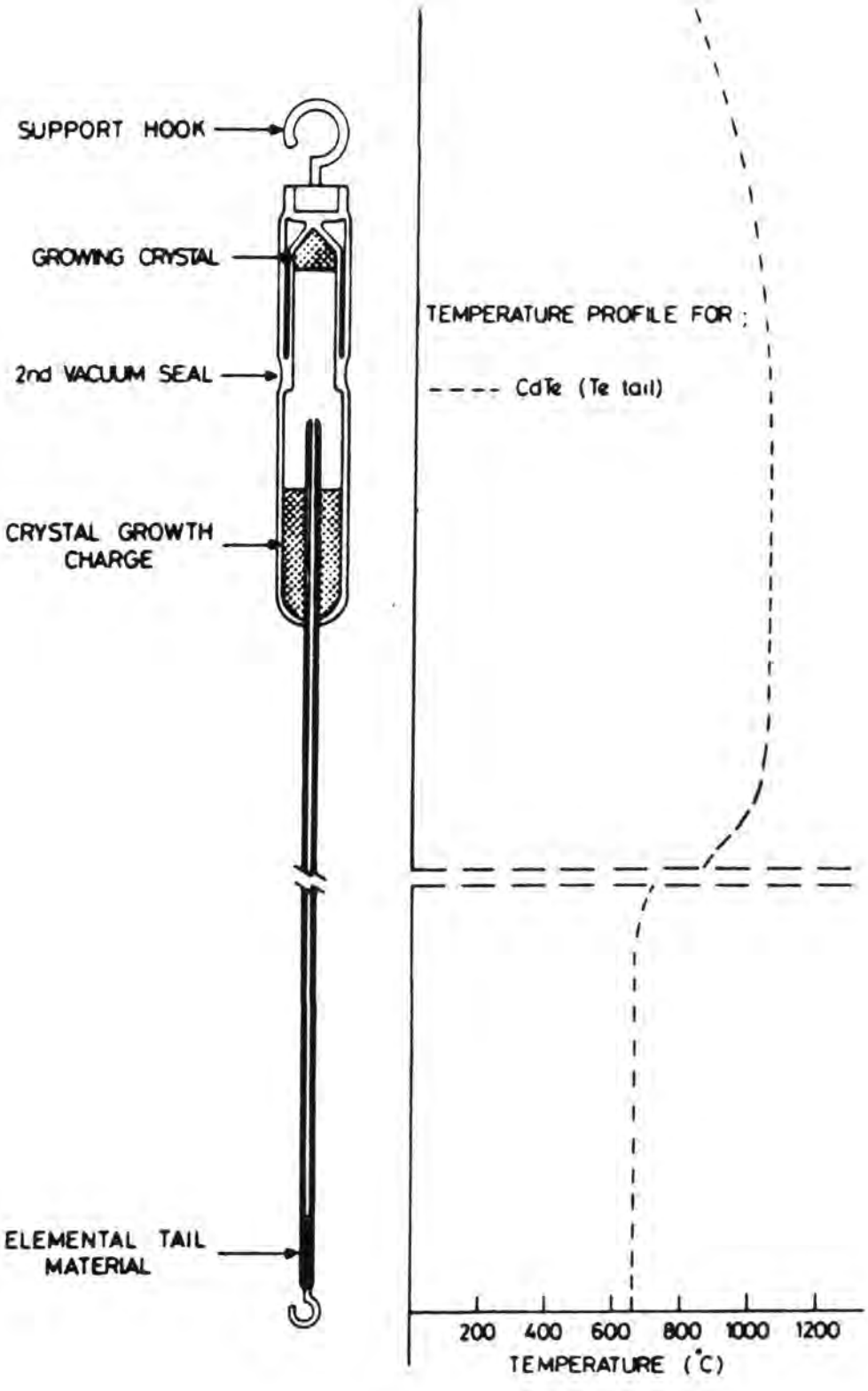

Fig. 4.1 : The sealed growth capsule as it hands in the furnace with the temperature profile on its right

from the growth tip before growth began. The tube was then pulled through the furnace at a rate of 15 mm per day, until a temperature gradient of 50°C was established between the charge and the growth tip. The pulling was then stopped and the tube allowed to remain in this position for seven days. Finally the temperature of the main furnace was gradually reduced to room temperature over ∿ 3 days. The reservoir furnace, which was independently controlled was switched off when the temperature of the main furnace had fallen to that of the reservoir. With this technique, CdTe boules ∿ 29mm in diameter and 5 cm long could be grown from a charge of 150 g .

4.3 Control of Bulk Crystal Resistivity

The as-grown CdTe crystals had a high resistivity (∿ 10^8 Ω cm) and were slightly p-type, consequently they were not suitable for the fabrication of photovoltaic devices without further treatment. As a result, several different techniques were employed to reduce the resistivity of the bulk crystals. To this end methods involving both the introduction of foreign acceptor and donor impurities and the annealing of the crystals in cadmium or tellurium were investigated. The different techniques employed are described below:

4.3.1 Annealing in Tellurium Vapour

Annealing of the samples was carried out in silica tubes divided into two parts by a small constriction in the middle of the tube. Small dice (4 x 4 x $2mm^3$) were loaded in one part of the tube which was then sealed. A small quantity of tellurium was then placed in the second part of the tube. The tube was evacuated to a pressure of ∿ 10^{-6} torr and allowed to outgas for 24 hours before it was back-filled with a small amount of pure argon and finally sealed.

The tube was suspended vertically in a furnace in such a way that the sample was above the Te and maintained at a higher temperature than the tellurium melt. Annealing temperatures in the range 500 to 800°C

were used with correspondingly lower temperatures of 350-450°C for the charge. Annealing times ranged from a few hours to two weeks. Argon gas was introduced to suppress the sublimation of CdTe which would otherwise have set in at ∿ 500°C. When samples were annealed for a long time with no argon filling they were found to have sublimed completely.

4.3.2 Copper Doping

It is generally accepted that p-type conductivity in CdTe may be obtained by doping with elements from groups I and V of the periodic table. Thus copper, which belongs to group I, and acts as an acceptor impurity in CdTe, was used to reduce the resistivity of the as-grown crystals. Two different methods were employed to introduce the copper.

(a) Copper Evaporation:

In this method a calculated quantity of high purity elemental copper was deposited under high vacuum onto a polished surface of the sample, which was then annealed in argon for 20-24 hrs at 500 to 550°C. These samples were then further annealed in Te vapour at 550°C as described in Section 4.3.1.

(b) Immersing in $Cu_2SO_4 5H_2O$ Solution:

In this method samples were polished and cleaned as described in Section 4.4. Polished samples were dipped in a $Cu_2SO_4 5H_2O$ solution of known concentration for 3 to 4 mins. at a temperature of 90 ± 5°C. Simple chemical displacement then produced a layer of Cu_2Te on the sample surface. Such samples were then also annealed in argon for ∿ 20 hours at 550°C to diffuse the copper into the CdTe. The samples were subsequently annealed in tellurium vapour for one to two weeks.

4.3.3 Doping with Phosphorus

In the present study phosphorus doped devices were the most promising. According to the literature phosphorus doping has usually been carried out while growing a crystal from the melt. However, in the

vapour phase method used in Durham, phosphorus was introduced by a post growth technique.

CdTe slices, one centimeter in diameter, were cut from the bulk crystals and pad polished as described in Section 4.4.2. The polished samples were mounted in a silica holder and placed in a reaction tube in a furnace. One end of the tube was connected to a flask containing orthophosphoric acid while the other end was connected through a trap (NaOH Sol.) to the exhaust. The orthophosphoric acid was heated while argon was bubbled through it, and the reaction chamber which was held at 550°C. The experimental arrangement is shown in Fig 4.2. The emerged vapour was condensed in the cold region or dissolved in the NaOH trap. This process was continued for 24 hours, when the heating was switched off and the samples allowed to cool in the argon flow. These samples were then annealed in Te vapour for one week at 550°C. This method produced the lowest resistivity (100-125 Ω cm) p-type CdTe and CdS/CdTe solar cells fabricated on these substrates gave an unoptimised efficiency in excess of 7%.

4.3.4 Production of n-type CdTe

Low resistivity n-type CdTe substrates for fabrication into Cu_2Te/CdTe devices were produced by annealing in Cd or by doping with Cl. The Cl was introduced during growth of the bulk crystals when material with a restivity of ∿ 1-2 Ω cm was obtained. To grow Cl doped crystals the CdTe charge was loaded into the growth tube while some 3 g each of Cd and $CdCl_2$ was placed in the tail. The crystal was then grown as described in Section 4.2.3.

Post-growth annealing in cadmium was done by immersing the sample in the molten metal. Dice were cut from large boules and degreased in 5% Decon-90 solution. A tube similar to that used for the Te vapour annealing (Section 4.3.1) was used for the cadmium anneal. Dice were placed in the lower half of the tube with the cadmium charge in the

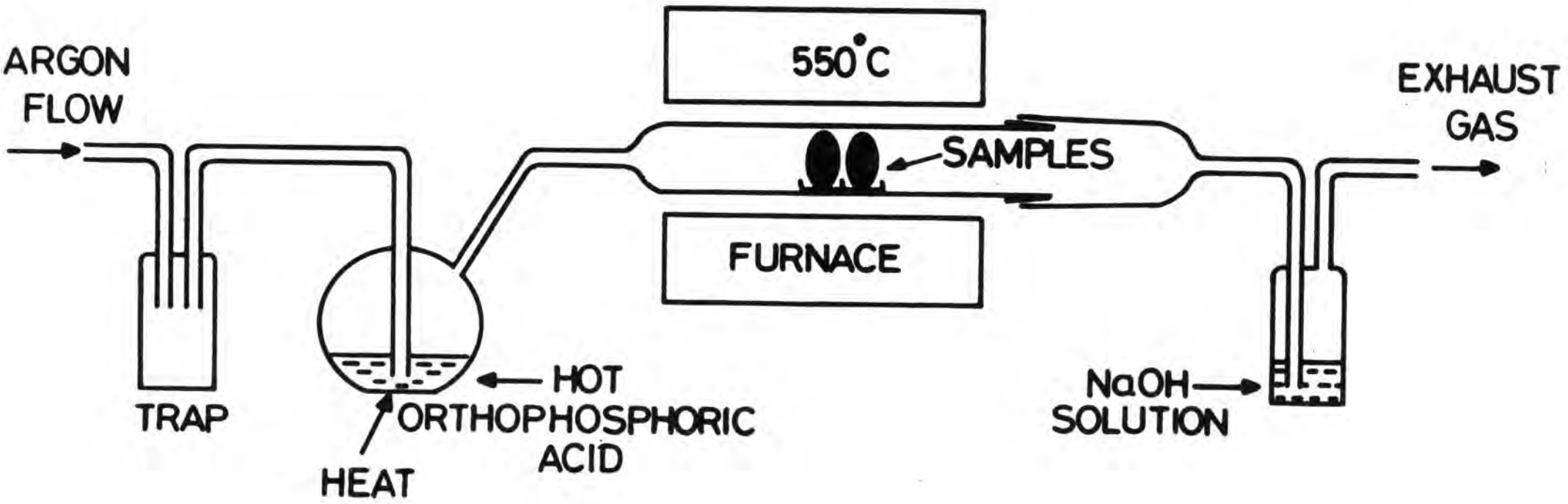

Fig. 4.2 : Experimental arrangement for post-growth phosphorus doping of CdTe

upper half. The tube was then sealed under vacuum and suspended vertically in the furnace with the samples kept at 600°C and cadmium at 400°C. Cadmium melts in the upper part and therefore runs down to the sample section of the tube. The samples were annealed for 36-48 hours. After completion of the anneal, the tube was immediately removed from the furnace and inverted so that the molten cadmium drained off from the dice. The tube was then allowed to cool down to room temperature and samples were taken out. This process produced samples with a varying range of resistivity.

4.4 Polishing the CdTe Substrates

The quality of the substrate surface is an important factor in determining the final device performance. Cutting slices or dice from bulk crystals leaves saw damage on the free surfaces. This damage needs to be removed by polishing a certain amount of the material away. The following polishing techniques were studied for surface preparation.

4.4.1 Mechanical Polish

Here the CdTe substrates were first mechanically polished on 600 grit emery paper and cleaned in deionized water in an ultrasonic bath; then polished with α-alumina (0.3 μm particle size) on a Buehler (T.M.) nylon cloth until the previous polish lines were no longer visible. This was followed by polishing with cotton buds (Q-tips) saturated with α-alumina slurry. The final mechanical polish was done with Q-tips saturated in gamma alumina (0.05 μm particle size) slurry. This process left a specular finish.

The polished samples were washed with deionized water and thoroughly cleaned in an ultrasonic bath, before being subjected to a chemical polish in 2% Br-Methanol solution. These were then rinsed in methanol and blow-dried in nitrogen. Polishing in Br-Methanol removed the work damage produced by the mechanical polish. However, examination of these samples in RHEED revealed that polishing with alumina

invariably left small alumina particles embedded in the surface. Therefore, as an alternative some substrates were mechanically polished using a cerium oxide suspension.

4.4.2 Pad Polish in Br-Methanol Solution

The problems experienced with mechanical polishing led to an investigation of alternative methods, in particular pad polishing in a solution of bromine in methanol. In this the CdTe slice was mounted on the end of a PTFE shaft which in turn was mounted (sliding fit) in a cylindrical housing. A PTFE pad was placed in the bottom of a circular trough containing Br-methanol solution. A sample, mounted on the shaft assembly, could be polished rapidly with no downward pressure directed onto the CdTe substrates, other than from the weight of the PTFE shaft on which it was mounted. The method is close to a contactless polish, since this arrangement traps a very thin layer of Br-methanol solution between the substrate and the pad. With experience the following procedure was developed.

The CdTe substrates were first degreased in 5% Decon-90 solution and washed with deionized water. To remove heavy saw damage the substrates were mechanically polished on 600 grit paper. The substrate was then mounted on the PTFE shaft using an etch resistant lacomit varnish or wax, and then pad polished in a Br-methanol solution. A clean specular surface was obtained after a few minutes. The substrate was removed using acetone and thoroughly washed, first in acetone, then in methanol, and subseqeuntly dried in a stream of nitrogen. RHEED studies of these samples indicated that the surfaces obtained were flat and free from surface damage.

4.4.3 Contactless Polishing

A very attractive method of overcoming the problems of mechanical polishing is to use the technique where the substrate hydroplanes on the polishing fluid[3]. A hydroplane machine using a solution of Br in

methanol was constructed but found to be very wasteful of the polishing fluid. Consequently, a more economical system was developed still using Br-Methanol solution and retaining the non-contact aspects of the hydroplane method, but with less waste.

In this machine the sample is mounted on a PTFE holder which is lowered onto a rotating turntable on which a polishing pad is fixed. Br-Ethaleneglycol-Methanol solution is drip fed onto the pad to keep it wetted and as the substrate is lowered onto the turntable, viscous forces support and rotate the sample ensuring a contactless polish. The detailed procedure is as follows:

The CdTe slices were degreased as described in Section 4.4.2. The slices were then mounted on the PTFE holder with etch resistant wax and lowered onto the turntable and polished using one percent Br solution in (20 + 80%) ethaleneglycol and methanol for 20 min. The samples were demounted from the holder with trichloroethane, thoroughly washed in trichloroethane and IPA, and finally dried in nitrogen. RHEED studies have shown it to be a good technique for producing exceptionally flat surfaces (the diffraction pattern consisted of streaks perpendicular to the shadow edge which is characteristic of highly flat surface) with no detectable evidence of any polishing damage.

4.5 Thin Film Deposition

4.5.1 Thermal Evaporation of CdS

Both thin film and bulk CdTe/CdS devices made use of thin evaporated films of CdS and it is therefore appropriate to describe the deposition of CdS films. Although a large variety of deposition techniques (including thermal evaporation, spray pyrolysis, sputtering, screen printing and electrodeposition) have been exploited to prepare solar cells, it was decided that the cadmium sulphide films should be grown by conventional thermal evaporation. The coating system used was an Edwards Model 19E6/197 employing an oil-diffusion pump and liquid

nitrogen trap. It was capable of achieving pressures of $\sim 10^{-6}$ torr. A schematic diagram of the system is shown in Fig 4.3a, while the bell jar fixtures are shown in Fig 4.3b.

The substrate was heated by radiation from a 1000 W infrared lamp. The substrate temperature was controlled by a Eurotherm controller with a NiCr/NiAl thermocouple which was clamped to the back of the substrate. A second thermocouple was used to monitor the substrate temperature independently and estimate variations in temperature during evaporation. The deposition rate was calculated from the thickness of the films and the time of evaporation. The substrates with their stainless steel mask were fitted into a stainless steel plate in the vacuum system. The substrate to evaporation source distance was approximately 15 cm .

A resistively heated tantalum crucible was used as the evaporation source. The charge temperature was measured using a Pt(13%)Rd/Pt thermocouple sealed in a silica tube with a sharp tip and inserted into the crucible. A stainless steel shutter operating via a rotary seal, positioned immediately below the substrates was used to mask the substrates from the source during outgassing and start-up procedures (i.e. until the evaporation rate had attained the desired steady value).

Typically about 15 g of CdS powder, purified by the argon-flow run method described in Section 4.2.2, was loaded into the crucible for each evaporation. It was covered with a thin layer of quartz wool to prevent spattering of the charge onto the substrate. The full evaporation cycle was as follows:

(1) The cleaned tin oxide coated slides (Section 4.6.2) or the polished p-CdTe substrates (Sections 4.3 and 4.4) were mounted into a stainless steel mask and placed in the vacuum system.

(2) The system was evacuated to a pressure less than 10^{-5} torr, and the substrates were heated to 120-300°C for 30 minutes to provide some preliminary outgassing.

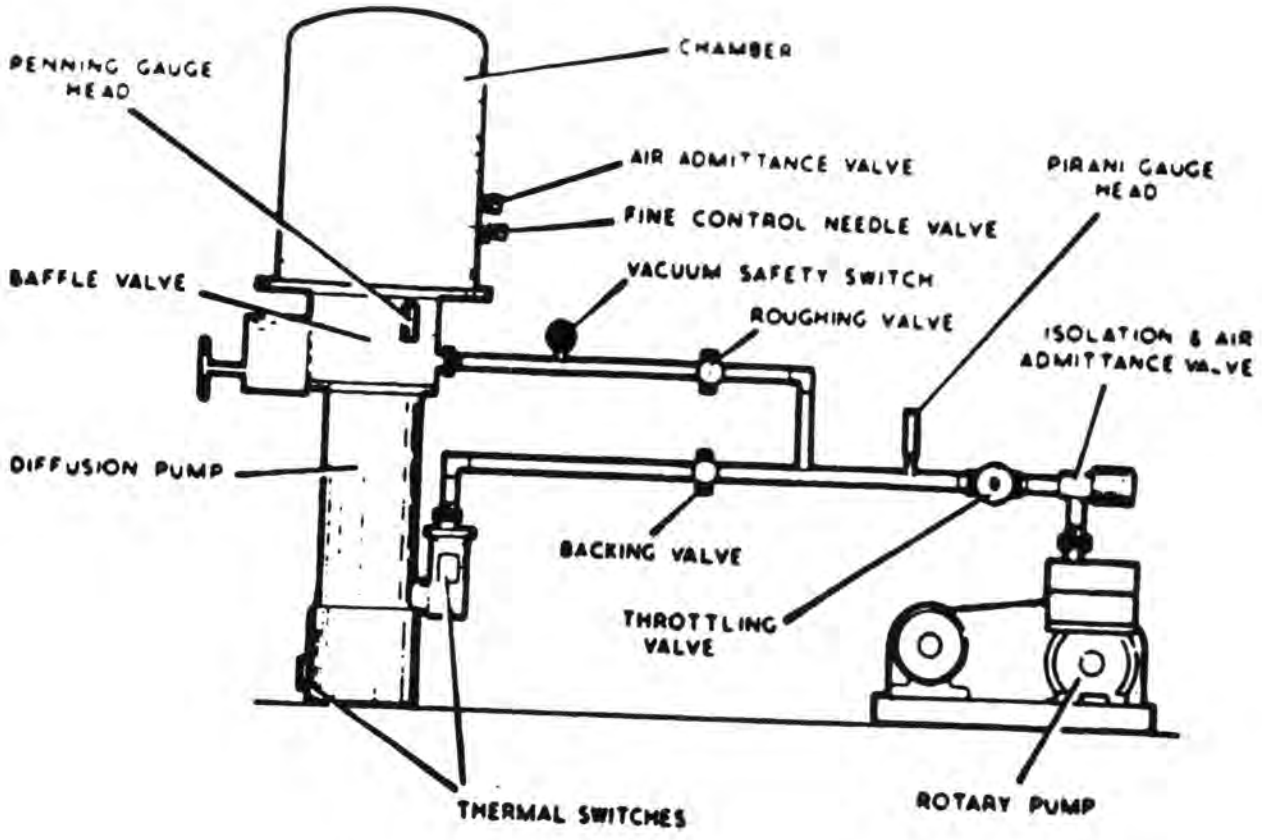

Fig. 4.3 (a) Schematic diagram of an 18" CdS evaporator

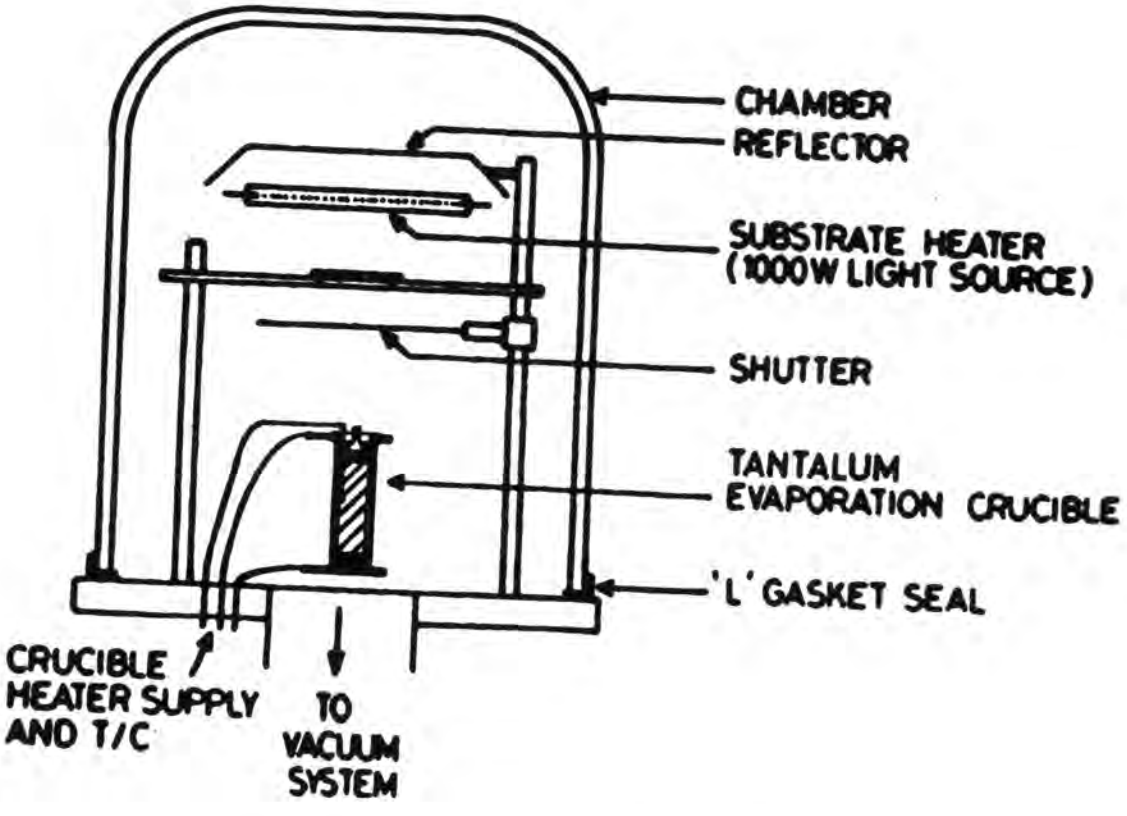

Fig. 4.3 : (b) Bell jar fixtures of the evaporator used in the deposition of CdS

(3) The source temperature was gradually increased to 600°C with the shutter closed. The CdS powder was outgassed at this temperature for about ½ hour and then the source and substrate heater supplies were switched off while the system was left to pump down for another 24 hours.

(4) The substrates were again heated to the desired temperature under high vacuum and the charge temperature was raised to 600°C. After a further ½ hour the charge temperature was increased to between 750-1000°C depending on the choice of evaporation rate. When steady state conditions were attained, the mechanical shutter was opened to expose the substrates to the CdS vapour.

(5) When growth was complete (typically 10-25 mins) the shutter was closed and the source and substrate heating switched off.

(6) The substrates were allowed to cool down to room temperature before being removed from the vacuum system for characterisation and/or further processing.

It was observed that during the CdS evaporation the substrate temperature, as measured by the independent thermocouple, was reduced by 1-2°C at the start of evaporation.

4.5.2 Thermal Evaporation of CdTe

The CdTe films were prepared in an Edwards coating unit. The lowest vacuum that could be obtained in this system, which is illustrated in Fig 4.4, was 5×10^{-6} torr. CdTe films were grown on previously deposited CdS layers, onto commercially available tin oxide coated glass slides, or gold/chromium coated glass slides prepared in this laboratory (Section 4.6.2).

The substrates were mounted in a stainless steel mask and heated radiantly during growth by an infrared lamp (750 W). The temperature of the substrates was monitored by a NiCr/NiAl thermocouple attached at the back of the substrate. A quartz crucible with a spirally wound

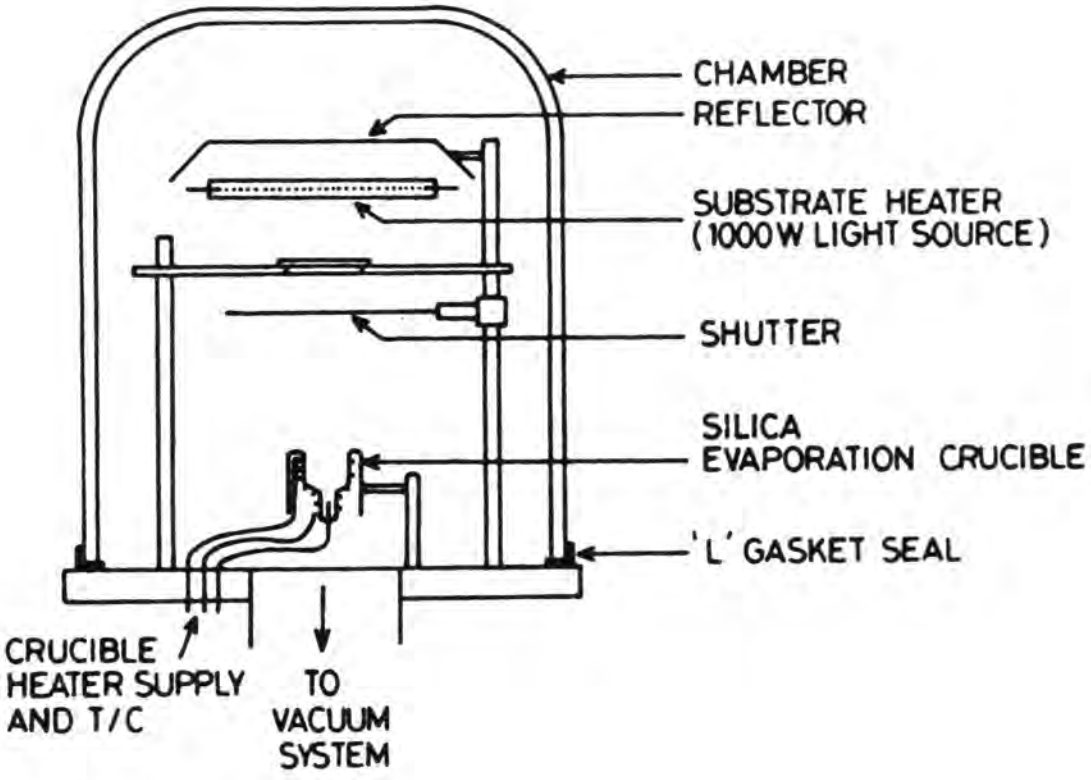

Fig. 4.4 : Bell jar fixtures of the evaporator used in the deposition of CdTe films

molybdenum wire heater was used as the evaporation source. The charge temperature was measured using a Pt(13%)Rd/Pt thermocouple fixed in such a way that its junction touched the bottom of the crucible through a special narrow tube provided for this purpose.

The source material was the high purity synthesized CdTe described in Section 4.2.1. A small quantity (5-10 g) of charge was placed in the crucible for each run. In order to prevent spattering of the charge the mouth of the crucible was baffled with a thin layer of silica wool. Evaporation rates were calculated from the thickness of a film as measured in the SEM, and the deposition time. The evaporation cycle for CdTe film growth was as follows:

(1) After loading the system it was pumped down to a pressure of 5×10^{-6} torr, and the substrates were heated to the selected temperature e.g. 100-400°C.

(2) The evaporation source was then gradually heated to $\sim$ 450°C and the CdTe charge was outgassed for 30 mins.

(3) Depending on the expected deposition rate the source temperature was raised to lie within the range 800 to 1200°C. When steady state conditions were reached, the mechanical shutter was opened to start the deposition.

(4) At the end of the deposition (5-15 mins) the mechanical shutter was closed, and the source and substrate heaters were switched off.

(5) The system was allowed to cool to room temperature, while pumping was continued. The samples were then removed for further processing, etc.

Although unsuccessful, attempts to dope the CdTe films were made using Cu, Sb and Te as additives. For this two evaporation sources were employed, one to deposit CdTe while the other, a molybdenum boat, was used to deposit the required elemental dopant.

4.6 Device Fabrication

4.6.1 Fabrication of CdS/CdTe Solar Cells on Bulk Crystal CdTe

The substrates were cut and polished as described above (Section 4.4) and loaded into the CdS evaporation system. A thin layer ($\sim$ 10 μm) of CdS was then deposited as outlined in Section 4.5.1. The final stage in the fabrication process was to make contacts to the heterojunction. Indium was used to make an ohmic contact to the n-CdS, while gold or carbon were used to make contact to the p-CdTe.

After deposition of the CdS the cell was coated (on the CdS side) with lacomit varnish to protect it from mechanical and chemical damage during subsequent processing. The sample was then immersed in HCl to remove any CdS that may have been deposited on the sides of the substrate. After that the back surface of the CdTe substrate was mechanically polished as described in Section 4.4.1 to remove any CdS deposit and to provide a clean surface. A final static polish in 2% Br in Methanol solution was administered for 3 to 5 minutes.

The gold contacts were produced by evaporation from some 50 mg of high purity gold in a molybdenum boat. The lacomit was then removed from the CdS and a small indium dot (1mm dia.) was deposited to complete the structure. With carbon contacts, after polishing the back surface of the CdTe substrate, the lacomit was first removed and a small quantity of carbon paste was painted onto the CdTe surface and the sample was annealed in nitrogen a ambient at different temperatures (250-350°C) for about 20 to 30 minutes. The samples were allowed to cool to room temperature before an indium dot was evaporated onto the CdS.

4.6.2 Fabrication of Thin Film CdS/CdTe Solar Cells

Two types of thin film structure were used:

(i) a tin oxide coated glass substrate/CdS/CdTe/contact structure;

(ii) a glass substrate/contact/CdTe/CdS/contact. In the first structure, the tin oxide coating on the glass served as an ohmic contact to the n-CdS. Before the deposition of the CdS films the tin oxide coated slides were wiped clean with lens tissue to remove dust. They were then dipped in 5% Decon 90 solution and softly rubbed with lens tissue to degrease the slides before being placed in a silica holder for cleaning in an ultrasonic bath of Decon 90 for ½ hour. After this they were thoroughly washed in deionized water to remove the Decon 90, rinsed in IPA and then loaded into an IPA refluxing system for 24 hrs.

After drying in nitrogen successive layers of CdS and CdTe were deposited as described in Sections 4.5.1 and 4.5.2. Finally, evaporated gold or carbon was used to make contact to the p-CdTe. Gold and carbon contacts were made in the same way as for the bulk CdTe/CdS solar cells (Sect. 4.6.1).

When tin oxide was not used either gold was evaporated onto chromium coated glass slides or carbon paste was screen printed onto uncoated glass. The slides were cleaned as for the tin oxide coated glass. The Au-Cr coated slides were obtained by successive electron beam evaporation in high vacuum of firstly Cr and then Au. The Cr was necessary because Au on its own did not adhere well to the glass. The carbon film was obtained by silk-screen printing an aqueous solution of carbon (Aquadag) directly onto the cleaned glass slides, which were then allowed to dry at room temperature.

The Au-Cr or C coated slides were loaded into the CdTe and CdS evaporators for the deposition of thin films of CdTe and CdS, and finally an indium dot was deposited by vacuum evaporation to make the ohmic contact to the n-CdS.

4.6.3 Fabrication of Copper Telluride/Cadmium Telluride Solar Cells

Cu_2Te/CdTe solar cells were fabricated on bulk crystal CdTe by a chemiplating process. An In/n-CdTe/p.Cu_2Te/Au structure was used for these devices.

(1) The Chemiplating Process:

This method was basically similar to that used for the Cu_2S/CdS heterojunction formations[4-6]. In the first stage of the process, commercially available copper chloride was bleached in a ten percent (10%) solution of HCl in deionized water to remove any traces of $CuCl_2$. About 10 g of the unbleached copper chloride was added to forty ml of dilute HCl. The mixture was thoroughly stirred with a clean silica rod until the greenish colour (indicative of the presence of $CuCl_2$) of the powder had disappeared. The powder was then filtered, rinsed with acetone and finally dried under vacuum. The resultant CuCl, free from $CuCl_2$, was then used for heterojunction formation using the following procedure.

(a) Seventy five ml of deionized water was heated in a covered reaction vessel, whilst oxygen-free nitrogen was continuously bubbled through it to remove any dissolved oxygen.

(b) Simultaneously, twelve ml of concentrated HCl was added to the deionized water.

(c) The pH of the solution was adjusted to a value between 2 and 3 by the addition of about seven ml of hydrazine hydrate.

(d) One g of the bleached CuCl was then added.

(e) The solution was heated to 90 ± 5°C. When all the CuCl powder had dissolved the pH value was checked again and, if necessary, adjusted by the addition of either HCl or hydrazine hydrate to a pH value of ∿ 2.5.

For heterojunction formation CdTe substrates were doped n-type and polished as described in Sections 4.3.4 and 4.4. respectively. The n-type CdTe dice (4 x 4 x 2 mm^3) were completely coated with lacomit

varnish except for a window on the surface to be converted to Cu_2Te. These dice were then dipped in the CuCl solution for different times ranging from 20-120 secs and dried in a stream of nitrogen.

(2) Electrical Contacts:

The best method of making ohmic contacts to n-CdTe was by alloying indium at a temperature of 250-300°C under a non-oxidizing atmosphere [7,8]. It was important to ensure that the temperature did not exceed ∿ 300°C so that the electronic properties of the material were not affected (The properties of In-CdTe alloyed contacts have been investigated by Braithwaite et al[9]). In the present work indium was evaporated under high vacuum to make ohmic contacts to n-CdTe in the same manner as was used to make In-CdS contacts (Section 4.6.1). An evaporated gold grid deposited under high vacuum was used to make an ohmic contact to the p-Cu_2Te.

4.6.4 Preparation of Schottky Barrier Devices

Schottky diodes were used for characterization of the material, and these were fabricated on p-type CdTe. High resistivity CdTe crystals grown in this laboratory (Section 4.2.3) were first cut into 4 x 4 x 2 mm^3 dice using a diamond saw. After ultrasonic cleaning in Decon 90 the dice were polished mechanically and chemically as outlined in Section 4.4. The CdTe was then doped p-type as required using the procedures described in Section 4.3.1, and then repolished mechanically to remove any surface layer of excess tellurium. This was followed by a pad polish in 2% Br-Methanol solution for 3 to 5 minutes.

Both indium and aluminium were used to make rectifying contacts and Au was used to make ohmic contacts to p-type CdTe. Although the resistivity of Au contacts on p-CdTe was high, it did not affect the

results because the substrate resistivity was also comparatively high. After polishing the dice were mounted onto a stainless steel mask with holes of different diameters and loaded into an oil-pumped vacuum system. In or Al was then deposited by evaporation from a molybdenum boat. Au was deposited on the other side of the p-CdTe to make ohmic contacts. In order to avoid scratches and oxidization of the Al layers they were covered with thin layers of silver paste.

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CHAPTER 4

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CHAPTER 5

CHARACTERIZATION OF MATERIALS AND DEVICES

5.1 Introduction

In this Chapter the various experimental techniques used for the structural and electrical assessment of materials and devices are reviewed. These include RHEED, SEM and X-ray diffractometry which are described in Sections 5.2 - 5.4 and which provide information on the structure and morphology of the devices. The experimental procedure for DLTS and conductivity measurements, together with the equipment employed are described in Sections 5.8 and 5.9. Sections 5.5 - 5.7 deal with the techniques for device characterization, i.e. I-V, C-V and spectral response measurements.

5.2 Reflection High Energy Electron Diffraction (RHEED)

Reflection high energy electron diffraction (RHEED) was successfully used to study the crystallinity of the various CdS and CdTe thin polycrystalline and epitaxial films that were grown for this work. RHEED is ideally suited to surface studies and was used to characterize and compare the surfaces of substrates prepared by different polishing techniques. RHEED was also used to confirm that epitaxial deposition of CdS onto CdTe had been achieved, and to identify the orientation of both substrate and epilayer. Finally, it was the only available technique which could be used to investigate and determine the phase of Cu_2Te produced by the dipping process.

RHEED entails the diffraction of mono-energetic electrons with energies in the range 10-100 keV from the atomic planes at the surface of a crystalline specimen. The de Broglie wavelength associated with a

particle of momentum P is given by:

$$\lambda = \frac{h}{P} \qquad (5.1)$$

where h is Planck's constant.

The wavelength of an electron accelerated through a voltage V (in volts) is given by the expression[1]:

$$\lambda = \sqrt{\frac{150}{V(1 + 10^{-6}V)}} \text{ Å} \qquad (5.2)$$

For the accelerating voltages in question the electron wavelengths are of the same order as the interplanar spacings of a crystal and thus the electron beam will experience diffraction in accordance with Bragg's Law:

$$\lambda = 2\, d_{hkl} \sin\theta \qquad (5.3)$$

where λ is the wavelength of electrons, d_{hkl} is the interplanar spacing of the {hkl} planes and θ is the Bragg angle.

The interplanar spacing is of the order of 2 Å for most materials while for the above range of accelerating voltage the wavelength will lie between 0.12-0.04 Å and hence the Bragg angle varies from about 1.5 to 0.5°. In consequence, RHEED is only applicable to those planes that are inclined at less than a few degrees to the surface of the specimen since they are the only planes which can diffract an electron beam at grazing incidence.

The necessary condition for the production of an electron diffraction pattern is illustrated in Fig (5.1). When the incident beam strikes a particular crystal plane (hkl) at the relevant Bragg angle θ, it is diffracted to form a diffraction spot on the fluorescent screen

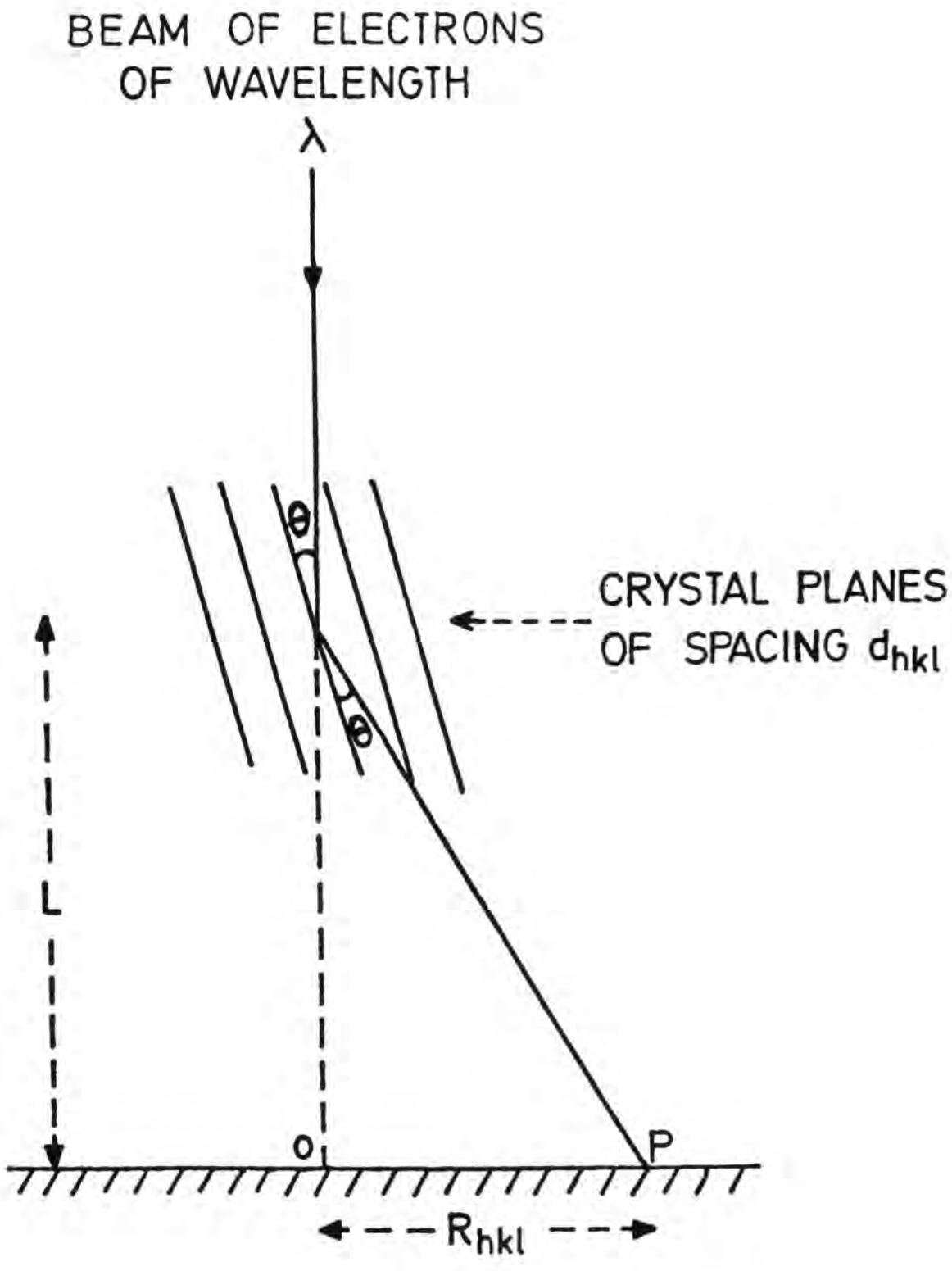

Fig. 5.1 : Schematic diagram illustrating the RHEED technique

(or a photographic film) at a distance L from the sample. Each plane (hkl) in real space produces a spot on the screen and spots corresponding to different planes constitute a pattern which may be interpreted and indexed using the concept of reciprocal lattice, applied originally by Ewald and Von Laue. The reciprocal lattice is one composed of a system of points, each of which represents a reflecting plane in the crystal and has the same indices as the corresponding reflecting plane. The reciprocal lattice is constructed from the real lattice by drawing a line through the origin normal to the corresponding reflecting plane of the crystal of length equal to the reciprocal of the crystal spacing. Thus if d_{hkl} is the distance of the (hkl) plane from origin in real space, the corresponding distance in reciprocal space is $1/d_{hkl}$.

In three dimensions the Bragg reflection condition can be determined using a geometrical construction known as the Ewald sphere (Fig 5.2). In the geometrical representation of Bragg's law, constructive interference takes place only if the reflection sphere intersects points in the reciprocal lattice. The radius of the sphere which is equal to $1/\lambda$ is very large as compared with the reciprocal lattice distances of $1/d_{hkl}$ for the diffraction of a beam of high energy electrons. So at very high energies such as 100 KeV, the reflection sphere can be approximated to a plane section through the reciprocal lattice and the RHEED pattern corresponds to this plane section lying perpendicular to the direction of the incident beam.

With polycrystalline materials the random orientation of individual grains gives rise to a ring pattern, instead of a discrete spot pattern, with each ring corresponding to a particular d_{hkl} spacing. For small values of the Bragg angle the radius of the rings, R_{hkl} is related to d_{hkl} by:

$$\lambda L = R_{hkl}\, d_{hkl} \qquad (5.4)$$

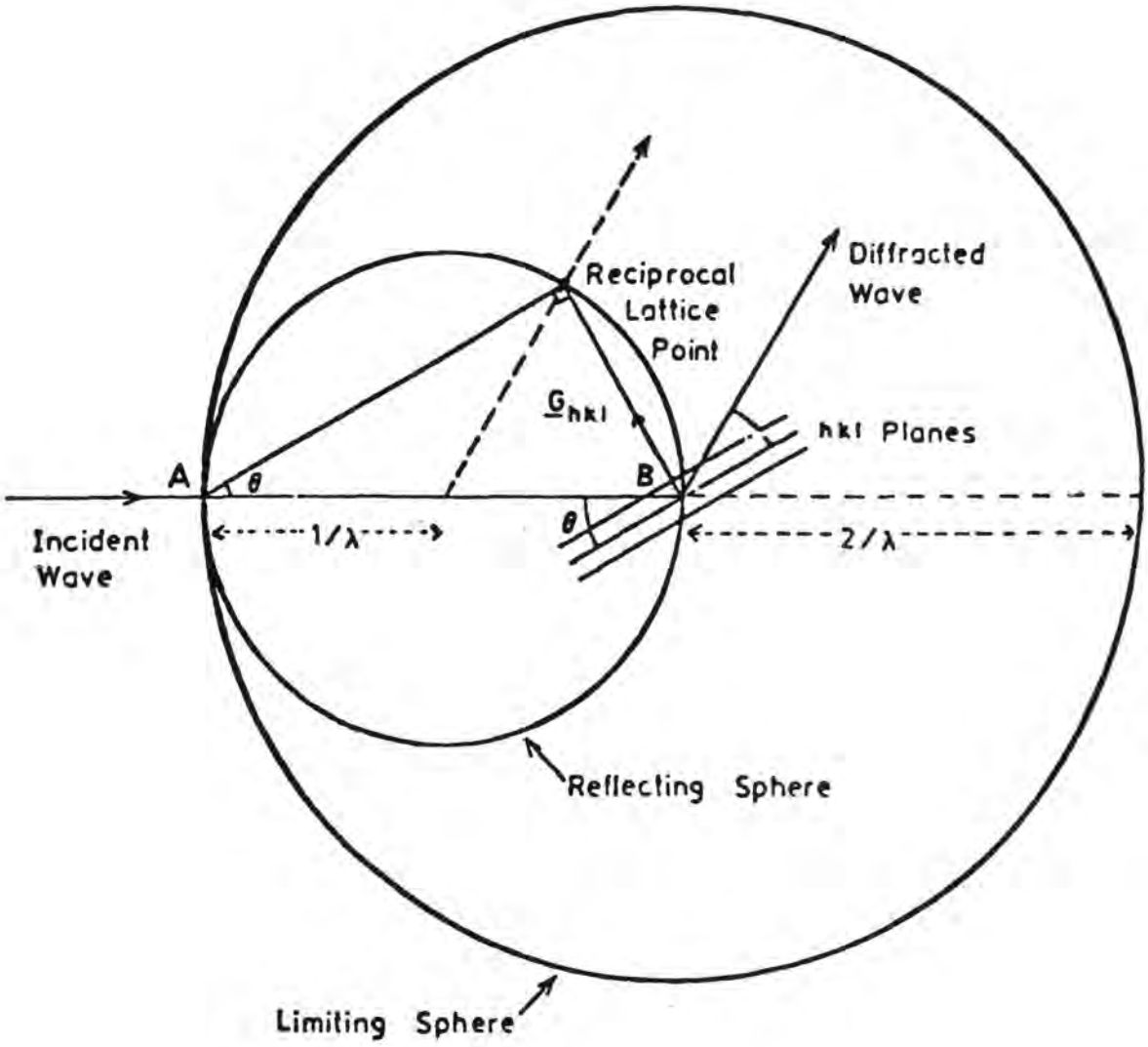

Fig. 5.2 : Ewald's sphere construction

This equation is known as the camera equation and can be derived from the Bragg condition for interference. The term on the left-hand side, λL, is known as camera constant and may be used as a calibration factor to determine interplanar spacings (d_{hkl}) from the recorded diffraction pattern.

RHEED is a very attractive technique for structural assessment of thin films and surfaces for several reasons[1].

(1) This technique is very easy to apply and observations are straightforward to interpret.

(2) It is a non-destructive technique and can easily be employed to obtain diffraction patterns from the surface of samples with dimensions of several millimetres and the thickness of the sample is not a limiting factor.

(3) It is particularly useful in studies of surface layers of thin films of the order of several microns or less where X-rays are uninformative.

(4) Changes in the diffraction pattern with sample rotation and diffraction conditions can readily be observed on a fluorescent screen. No such facility is possible with X-ray diffraction.

(5) For the photographic recording of the diffraction pattern exposure is of the order of seconds for electrons while for X-rays it can be several tens of minutes.

(6) The transformation from real to reciprocal space is easier to visualize than it is with X-ray diffraction because the necessary condition for crystal planes to diffract high energy electrons is that they should be approximately parallel to the incident beam.

(7) Since the Bragg angle for electron diffraction by typical crystal planes is less than 2 degrees, a diffraction pattern extended over a large number of reflections in the reciprocal space can be

recorded on a flat photographic plate, while with X-ray diffraction or LEED a large angular spread of the pattern has to be covered.

In the present study, a JEM 120 transmission electron microscope operating at 100 KeV was used in the RHEED mode.

5.3 Scanning Electron Microscopy

The versatility and rapid turn-round time of the scanning electron microscope (SEM) makes this instrument an extremely powerful tool in the characterization of materials and surfaces. The fundamental idea underlying the operations of a scanning electron microscope is that when an electron beam is scanned across the sample in a raster a number of different interactions occur between the incident electron beam and the specimen as illustrated in Fig.5.3. In particular, the incident electron beam will generate:

(a) secondary electrons which may be collected to form a magnified image of the specimen surface. This is the secondary emission (SE) mode of the SEM.

(b) X-rays from the interaction with surface atoms. These may be collected as well and analysed (energy dispersive anlaysis of X-rays, EDAX) to give information on the elemental species present in the sample.

(c) electron-hole pairs may be produced within the sample. These may be extracted and displayed to give information about electrically active structural features (e.g. grain boundaries) and important electrical (material) parameters such as the minority carrier diffusion length. The different modes of operation in which the SEM was used for the present work were:

5.3.1 Secondary Emission Mode

In the SE mode of operation the secondary electrons emitted from the sample are collected and imaged. The number of electrons emitted is a function primarily of the surface topography and of variation of

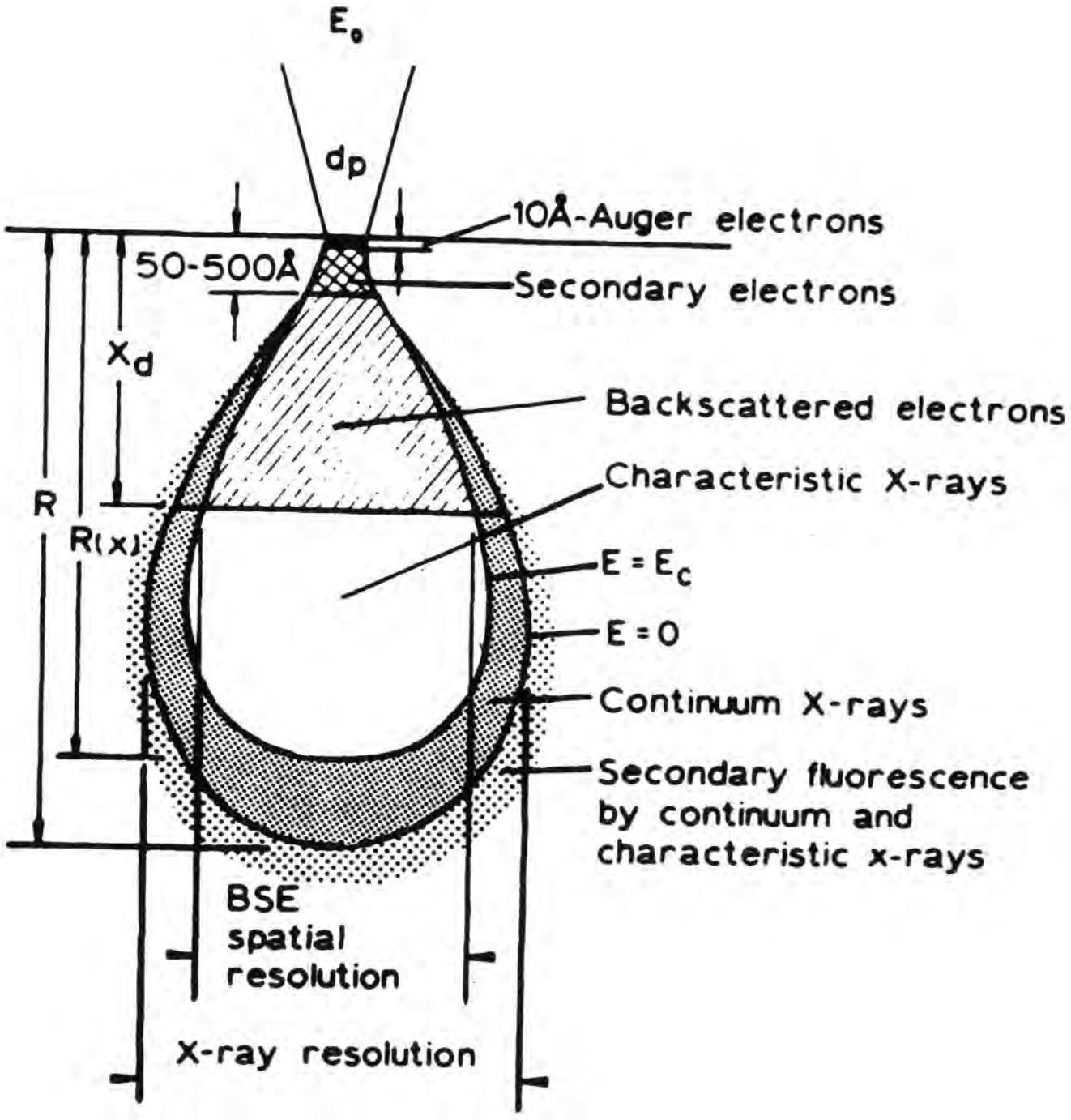

Fig. 5.3 : Summary of range and spatial resolution of various signals from the electron microscope - SEM

secondary emission efficiency across the surface. The secondary electrons are collected by an Everhart-Thornley detector. This is a scintillator and Faraday cage arrangement coupled to a photomultiplier tube. The secondary electrons are generally too low in energy to excite scintillations and so these low energy electrons are accelerated by applying a potential of + 14 kV to the scintillator. To screen the primary electron beam from the influence of the high potential, the scintillator is surrounded by a Faraday cage biased at + 250V to collect the primary back-reflected and secondary electrons. The collected electrons are then accelerated onto the scintillator producing flashes of light (scintillations) which are coupled to the photomultiplier by a light pipe. The photomultiplier signal is applied to the z-modulation of a CRT display which is scanned in synchronism with the primary electron beam to give a video image of the surface. By confining the area of the sample scanned, and using a well-focussed beam it is possible to obtain very high levels of magnification with good depth of field. For a more detailed discussion of image formation etc. the reader is referred to the literature[2,3]. This mode of the SEM was successfully used to study the morphology and cross-section (thickness) of both CdS and CdTe films.

5.3.2 Energy Dispersive Analysis by X-rays

This is an invaluable facility for the identification of the elemental composition within a selected region of the surface on which the stationary electron beam is positioned. In this mode of operation the characteristic X-rays are produced by electron bombardment if the accelerating voltage is greater than the critical potential. Analysis of the X-rays enables the chemical composition of the area under study to be determined[4]. It is thus useful in establishing the position of the interface of a heterojunction to an accuracy of $\sim$ 1 μm.

This technique can be used to detect elements of the periodic table with an atomic number greater than eleven.

5.3.3 Electron Beam Induced Current (EBIC) Mode

The EBIC mode of the SEM is generally used to investigate electrically active areas in a semiconductor. This technique has been widely exploited to measure such transport properties of semiconductors as the minority carrier diffusion length, lifetime and surface recombination velocity[5].

In this imaging mode the incident electron beam generates electron-hole pairs which are collected at electrical barriers in the specimen. In general a potential barrier is deliberately fabricated, (usually in the form of a Schottky or p-n junction diode) in order to separate the electrons and holes generated by the incident electron beam, in an analogous way to the photovoltaic effect. The separated charge carriers are collected, amplified and applied to the z-modulation of the CRT display . Thus, as the electron beam is scanned across the sample, areas where for example preferential recombination is taking place, will show a reduction in the short circuit current which then appears as a change in contrast on the display.

The EBIC mode of the SEM was used in this work to measure the minority carrier diffusion length. The EBIC current was measured as a function of beam distance x,from the junction on both sides. The basic idea behind this technique is presented mathematically as below:

The continuity equation for minority carriers in a p-type semiconductor may be written as[6]:

$$\frac{\partial \Delta n}{\partial t} = G - \frac{\Delta n}{\tau} + \Delta n \mu_n \nabla E + \mu_n E \nabla \Delta n + D_n \nabla^2 \Delta n \qquad (5.6)$$

where

Δn = excess electron population

G = electron-hole generation rate

τ = lifetime

μ_n = electron mobility

E = electric field

D_n = Diffusion constant

Assuming that the electric field E outside the depletion region is zero, the equation reduces in one dimension to:

$$\frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau D_n} = -\frac{G}{D_n} \tag{5.7}$$

This can be solved with the following boundary conditions;

$$\Delta n\ (x = \infty) = 0 \tag{5.8}$$

$$\Delta n\ (x = 0) = \Delta n_o \tag{5.9}$$

to give

$$\Delta n(x) = G\tau + (\Delta n_o - G\tau)\ \exp\left(-\frac{x}{L_n}\right) \tag{5.10}$$

A similar relation can be established for n-type material. Since the current density J is related to Δn by

$$J_n = q\ D_n\ \nabla \Delta n(x)\ \Big|_{x = 0} \tag{5.11}$$

then

$$J_n = J(o)\ \exp\left(-x/L_n\right) \tag{5.12}$$

where

$$J(o) = \frac{eD_n(\Delta n_o - G\tau)}{L_n} \tag{5.13}$$

Equation (5.12) forms the basis of the present measurements. In practice the device was mounted on a copper plate and then cleaved perpendicular to the junction plane. A linescan was carried out across the cleaved surface of the device and from this current measurements were made as a function of distance. A plot of $\ln J(x)/J(o)$ vs x was then constructed in which the gradient gave a measurement of $1/L_n$. A Cambridge stereoscan 600 Scanning electron microscope was used in its different modes of operation to study the texture and thickness of the CdS and CdTe films, measure the diffusion length of minority carriers and composition of the materials. A schematic diagram of this instrument is shown in Fig 5.4.

5.4 X-ray Diffractometry

The crystallinity and the phases of CdS and CdTe films were studied using X-ray diffractometry. The unique feature of the technique is that it samples not only relatively large areas, as does RHEED, but also, unlike RHEED, penetrates throughout the depth of the film. As a result it provides an assessment of crystal structure which is averaged over the entire sample volume. It was found to be particularly useful in comparing the degree of preferred orientation in thin evaporated films grown at different substrate temperatures.

The studies were carried out using a Philips PW1130 diffractometer with cobalt $K\alpha$ radiation of average wavelength 1.7902 Å. It was operated with target voltage and current of 40 KV and 20 mA respectively. The analysis conditions were; divergent slit 1°, receiving slit 0.1°, scatter slit 1°, and a goniometer scan speed of 1° per minute. The instrument was equipped with a sealed proportional detector and a pulse height analyser.

The films were deposited on glass substrates which were then mounted in the sample chamber of the diffractometer. X-ray diffraction scans were recorded from $2\theta = 20°$ to $2\theta = 70°$ and the analysis of the

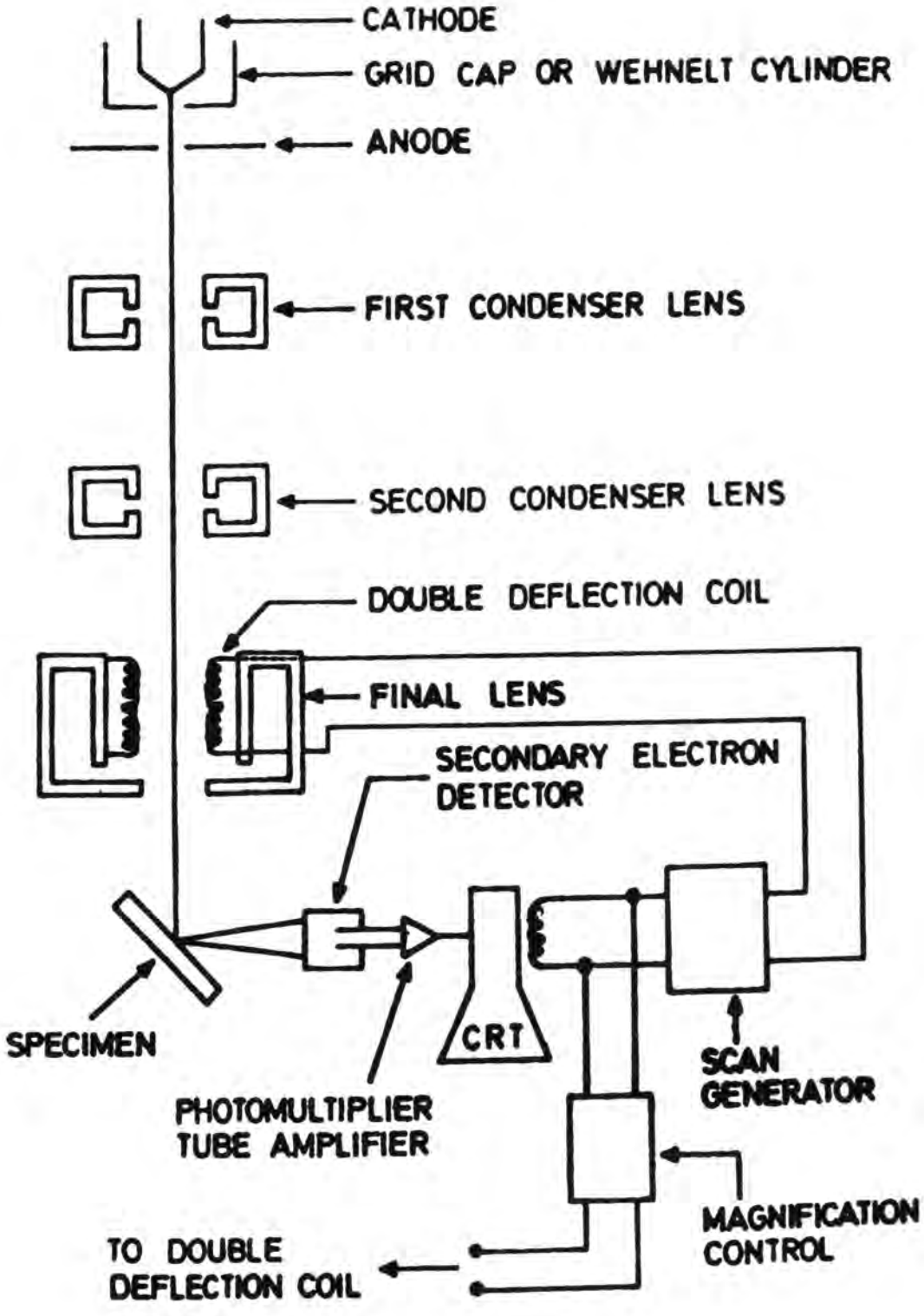

Fig. 5.4 : Schematic diagram of the SEM.

films was carried out using the standard Joint Committee for the Powder Diffraction Standard (J.C.P.D.S) index 1974[7].

5.5 Current-Voltage Characteristics (I-V)

The current-voltage characteristics of the devices were measured using the experimental arrangement shown in Fig 5.5. The characteristics measured in the dark determine what proportion of the electrical energy generated by the device for a given irradiance will be available as useful energy at the output terminals and what fraction will be dissipated as heat. Detailed point-by-point measurements of the I-V characteristics were carried out using a high impedance digital voltmeter and a low impedance Hewlett Packard ammeter (type 3465B) with the device placed in a light tight enclosure. The bias voltage was derived either from a calibrated D.C.Supply (Time Electronics Ltd. type 2003) or from a potential divider arrangement.

The photovoltaic output characteristics were measured under simulated AM1 illumination using the same arrangement. AM1 illumination was provided by a Durham built solar simulator, using a 1.5 kW quartz halogen strip lamp with a parabolic reflector housing. The lamp was mounted in a levelled metal frame fitted with a tray containing 2 cm deep flowing water intended to simulate infrared absorption of the atmosphere. Underneath the tray was placed a table of adjustable height on which the sample was mounted. This assembly is shown in Fig 5.6. The intensity of the illumination at the sample surface was measured using a calibrated silicon PIN diode (type 10 DF, United Detectors Technology) and adjusted to give AM1 illumination by adjusting the height of the table. The PIN diode had a flat spectral response over the spectral range 500-900 nm.

5.6 Capacitance-Voltage and Photocapacitance Measurements

Capacitance-voltage characteristics have been measured for most of the diode structures fabricated during the present work, as a means of

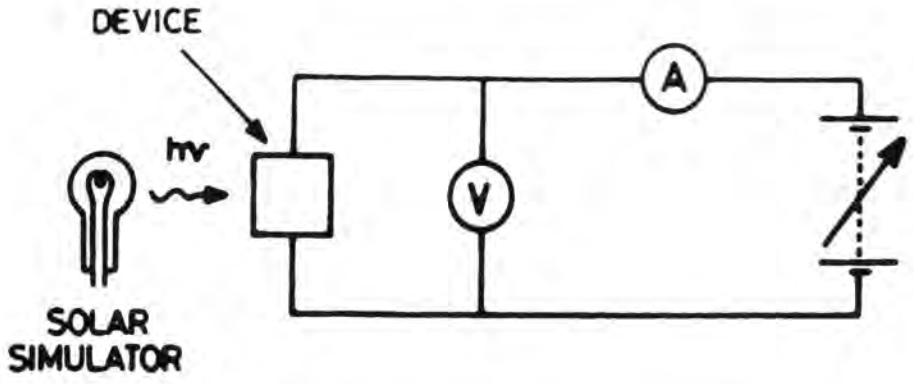

Fig. 5.5 : Experimental arrangement used for measuring current-voltage characteristics

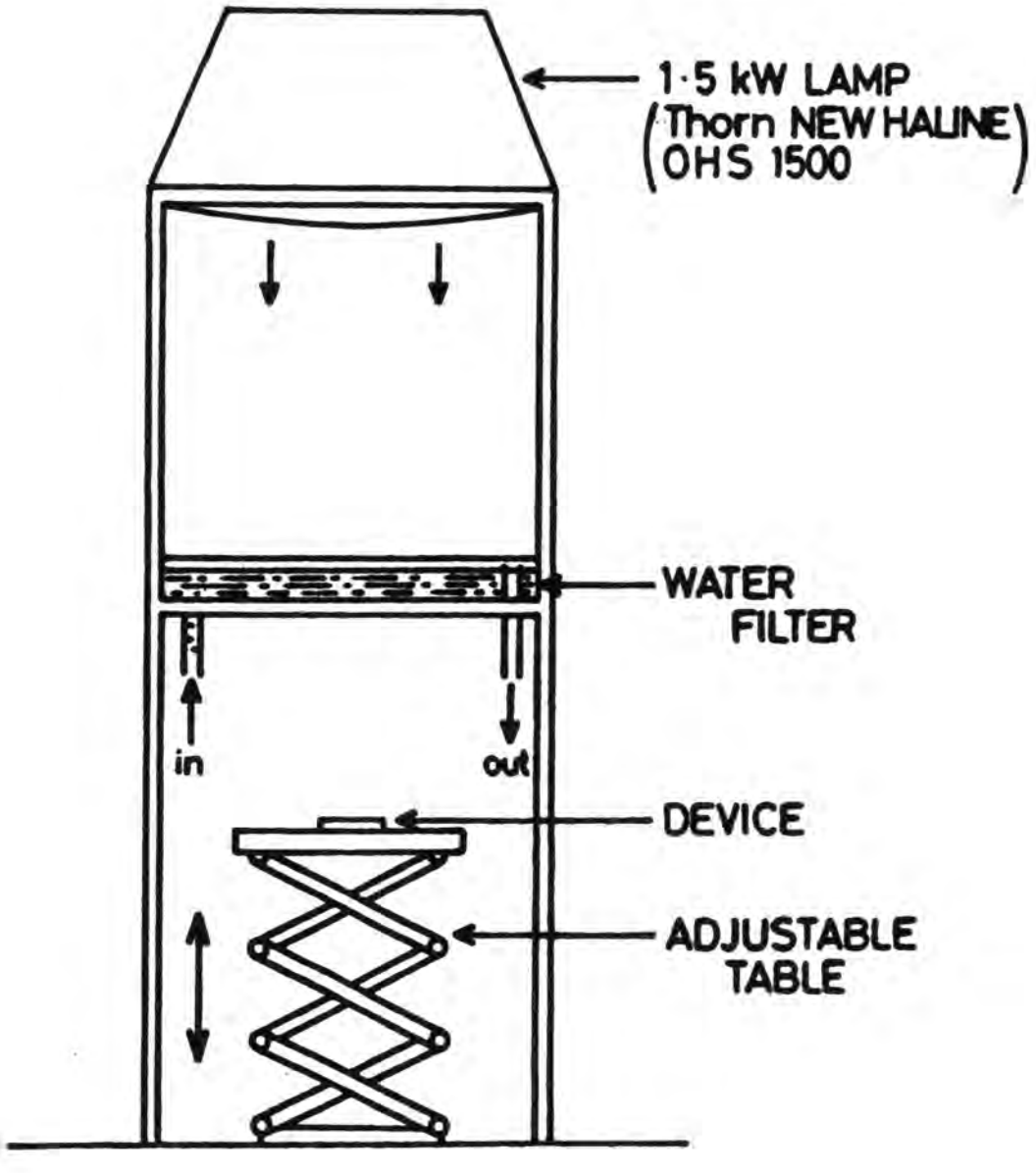

Fig. 5.6 : Solar simulator for AM1 illumination

determining free carrier densities and estimating barrier heights. They also give an indication of interface state activity. In addition, steady-state photocapacitance studies have been carried out to identify the more important deep levels present in the devices.

Capacitance-voltage characteristics were measured manually with a Boonton 72B Capacitance meter, which operates at 1 MHz, together with a D.C. calibrated voltage source (Time Electronics Ltd. Model 2003). The experimental arrangement used to measure steady state photocapacitance is shown in Fig 5.7. Illumination was provided from a tungsten light source with a Barr and Stroud type VL2 prism monochromator. The dark capacitance of the device was first compensated so that small changes induced by the incident monochromatic light could be easily recorded. The steady state photocapacitance measurements were also conducted at liquid nitrogen temperature to minimize thermal effects.

The sample was loaded into the cryostat shown in Fig 5.7 and left in the dark for a sufficient time to achieve steady state. The incident light from the monochromator was scanned from long to short wavelengths.

5.7 Spectral Response Measurements

The spectral response (sometimes known as quantum efficiency or collection efficiency) is one of the most important features of a photovoltaic device and is defined as the ratio of the number of the charge carriers collected by the junction to the number of incident photons at a given wavelength. The spectral sensitivity of the solar cells was measured using a Barr and Stroud double prism monochromator (type VL2) fitted with spectrosil "A" silica prisms. The wavelength range used was 0.4 to 2.0 μm. The light source was a 250 watt, 24 volt quartz halogen lamp driven by 200 V D.C. stabilized power supply.

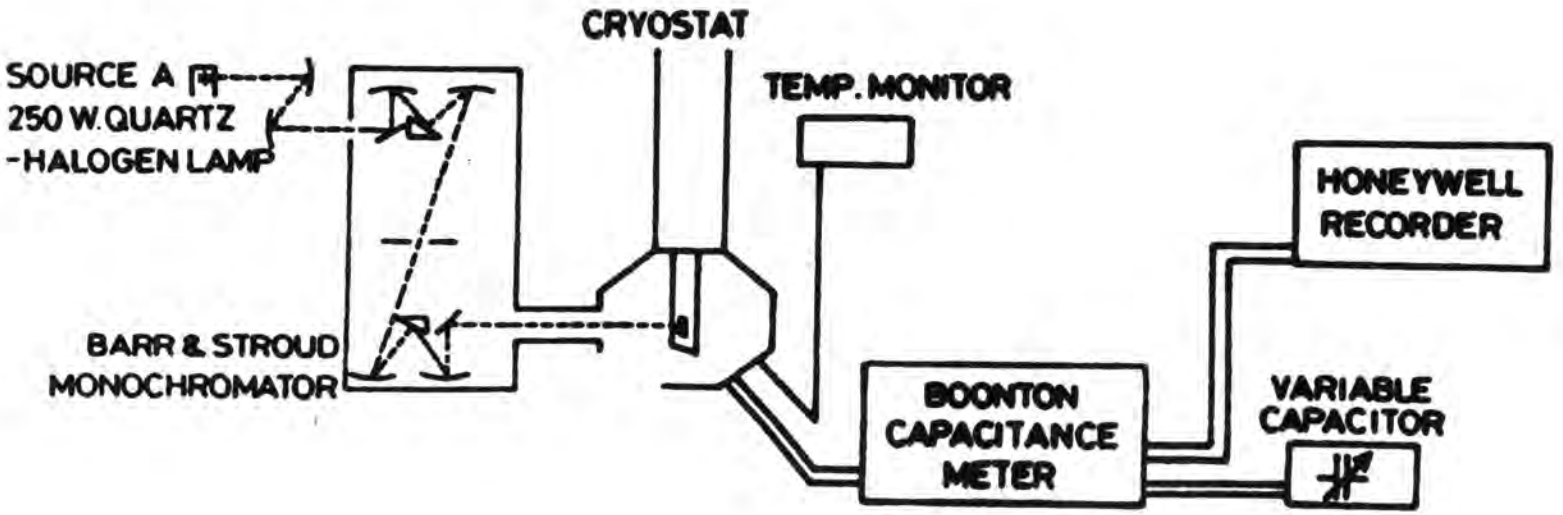

Fig. 5.7 : Experimental arrangement used to measure steady state photocapacitance

The energy distribution of the light source at the exit slit was measured using a Hilger and Watts Schwartz compensated linear vacuum thermopile type FT16. The light was chopped at a frequency of 10 Hz and the thermopile signal was recovered using a Brookdeal 9801 lock-in-amplifier and a Brookdeal type 431 a nanovolt preamplifier. The energy distribution of the light source together with the monochromator is shown in Fig 5.8. In order to avoid the effects of drift in the monochromator the system was calibrated at regular intervals with a sodium lamp and a PIN diode. To ensure a true comparison between different devices the monochromator slits were kept constant at 0.5 mm throughout the measurement.

The experimental arrangement used for photoresponse measurements is shown in Fig 5.9. The device to be characterized was mounted on the specimen block of a cryostat and its temperature was measured by a copper-constantan thermocouple fixed to the block. The devices were illuminated both in the "Front" and "Back" wall modes of operation. The OCV and SCC response of the solar cells at different wavelengths of the incident light were measured with a Keithley 602 electrometer and recorded on an x-t chart recorder.

5.8 Conductivity Measurements

As described in Chapter 4, the as-grown bulk single crystal CdTe was semi-insulating and had first to be doped semiconducting n or p-type before it could be used for device fabrication. However, prior to that, it was important to characterize the electrical behaviour of as-grown material and to identify dominant (electrically) active deep levels. This was done by measuring and analysing the current-voltage characteristics at different temperatures as described in Section 6.2.

The measurements were made using an Oxford Instruments DN1704 variable temperature cryostat. This is a liquid nitrogen reservoir cryostat which uses helium as an exchange gas and is capable of

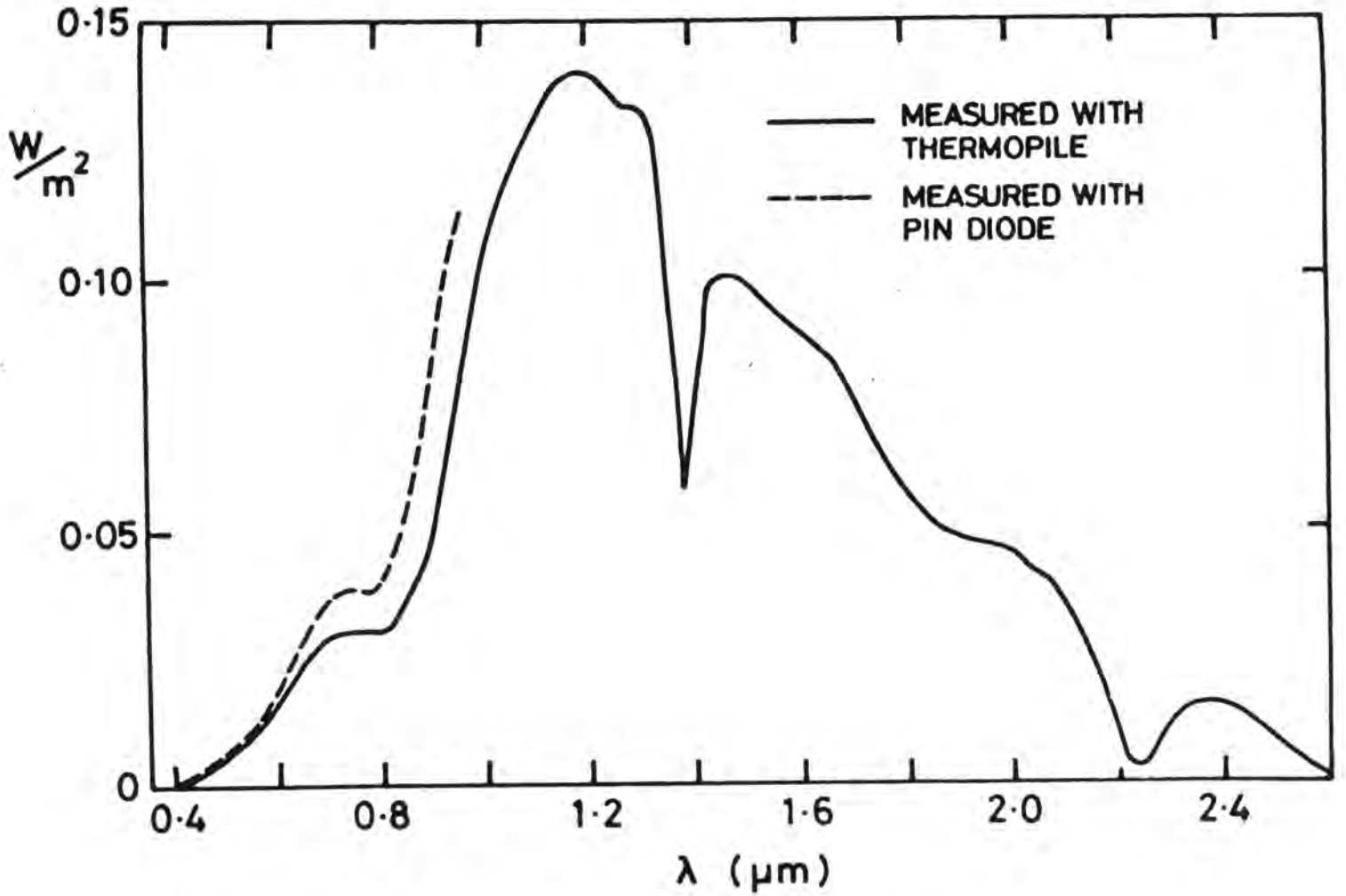

Fig. 5.8 : **Energy distribution of light source and the monochromator**

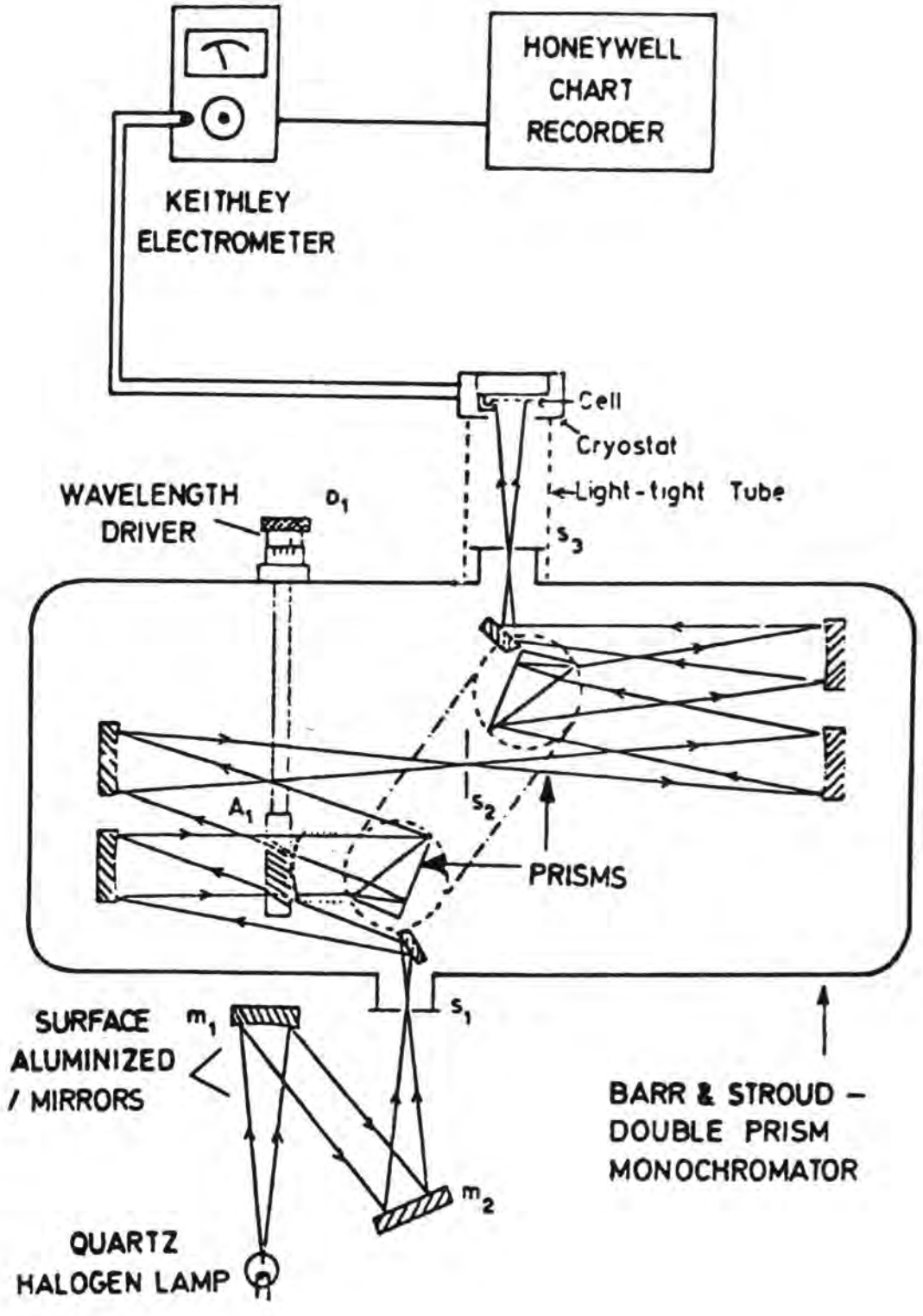

Fig. 5.9 : Experimental arrangement used for spectral response measurements

maintaining any temperature in the range 77K to 500K to an accuracy of ± 1K. Fig 5.10 represents the main parts and dimensions of the cryostat. It operates on the principle of controlled continuous transfer of liquid nitrogen from the reservoir to a heat exchanger which surrounds the sample region. This is a 20mm internal diameter tube passing through the length of the cryostat and which in operation is filled with helium gas.

The sample is loaded from the top and cooled by the static column of the exchange gas that thermally links the sample and the heat exchanger which is positioned at the lower end of the sample tube. The heat exchanger is connected to both the liquid nitrogen reservoir and to an electrical heater, such that the combination of heater current and liquid nitrogen flow from the reservoir, will establish the desired temperature at the copper heat exchanger. Temperature is measured using a platinum resistance thermometer and the cryostat temperature is controlled by an Oxford Instruments DTC2 digital temperature controller to an accuracy of ± 0.1K.

The experimental arrangement is shown in the block diagram, Fig 5.11. A regulated power supply was used to apply the bias potential while the current and voltage were measured using Keithley 602 electrometer and Hewlett ~~and~~ Packard (type 3465B) voltmeter respectively. I-V data was obtained point-by-point at different temperatures and analysed to find the activation energies.

5.9 Deep Level Transient Spectroscopy (DLTS)

The detailed measurement of deep levels in CdTe Schottky and heterojunction devices was carried out using Deep Level Transient Spectroscopy (DLTS) described in Section (6.3). Essentially, DLTS provides quantitative data on the thermal activation energies of deep levels in the bandgap, and in certain cases it may be used to determine capture cross-sections and trap densities.

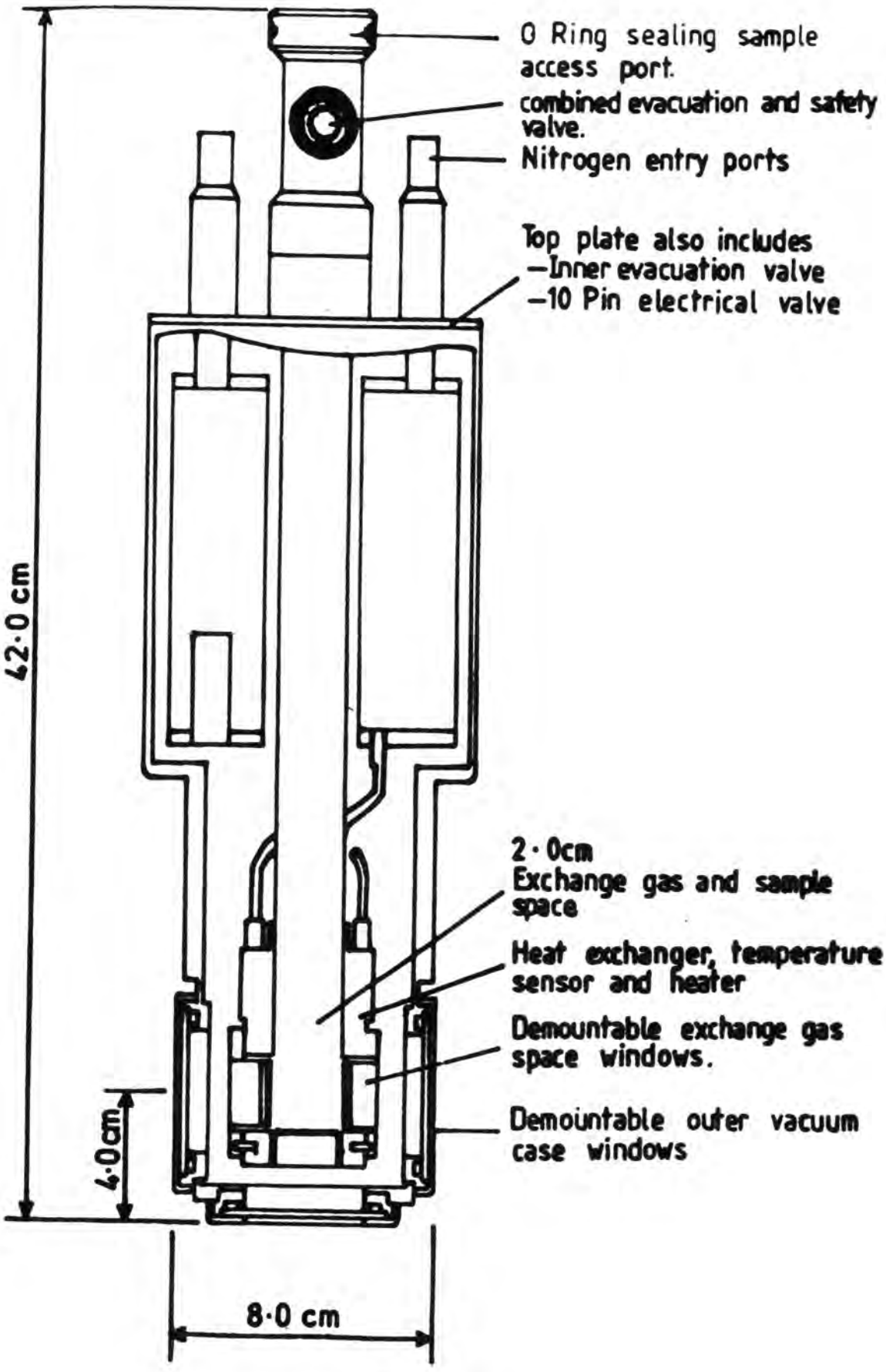

Fig. 5.10 : DN 1704 liquid nitorgen cryostat.

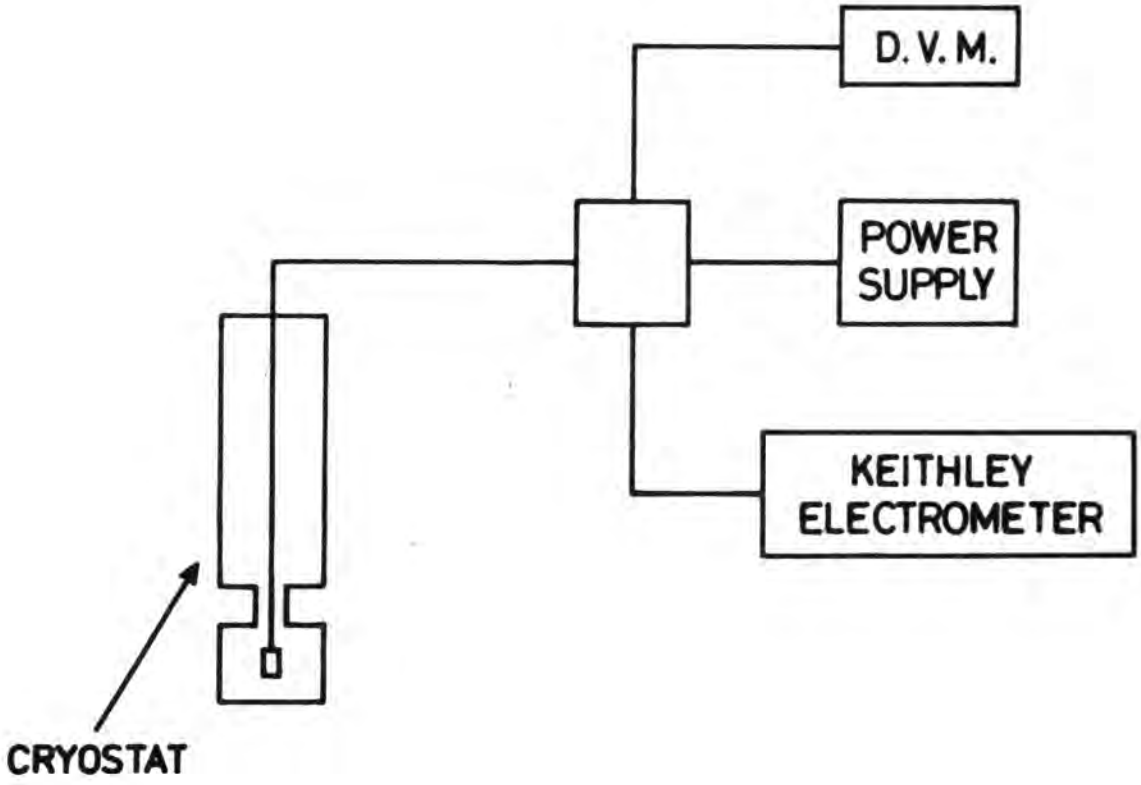

Fig. 5.11 : The block diagram for conductivity measurements

The experimental arrangement used for the DLTS studies was a modified version of the basic dual-gated boxcar method first described by Lang[8]. The system differed from that of Lang in the use of a sampling digital voltmeter to recover the full capacitance transient, and in the use of a computer to control the system and store the data. The DLTS apparatus is illustrated schematically in Fig 5.12.

The sample is mounted in an Oxford Instruments DN704 cryostat and its temperature is controlled by an Oxford Instruments DTC2 digital temperature controller. The capacitance transient was measured using a Boonton 72B differential capacitance meter, and the bias pulses were supplied from a Lyons PG73N pulse generator. The system was controlled by a Commodore PET 4032 microcomputer, equipped with a Commodore 8050 dual disc drive and the DLTS spectra were plotted on a Hewlett Packard 9872C digital plotter.

The sample was first cooled down to liquid nitrogen temperature and allowed to stabilize for about ½ hour. The temperature was then ramped steadily, under computer control, at typically 1 K/min and the capacitance transient was sampled only when the temperature was within ± 0.2K of the desired value. In general an average of four sets of samples was taken and stored on disc, at 1K intervals. The DLTS spectra were then constructed, after the DLTS run was completed, using the normal rate window approach of Lang, and appropriate Arrhenius plots were plotted to determine the activation energies and capture cross-sections (Section 6.3).

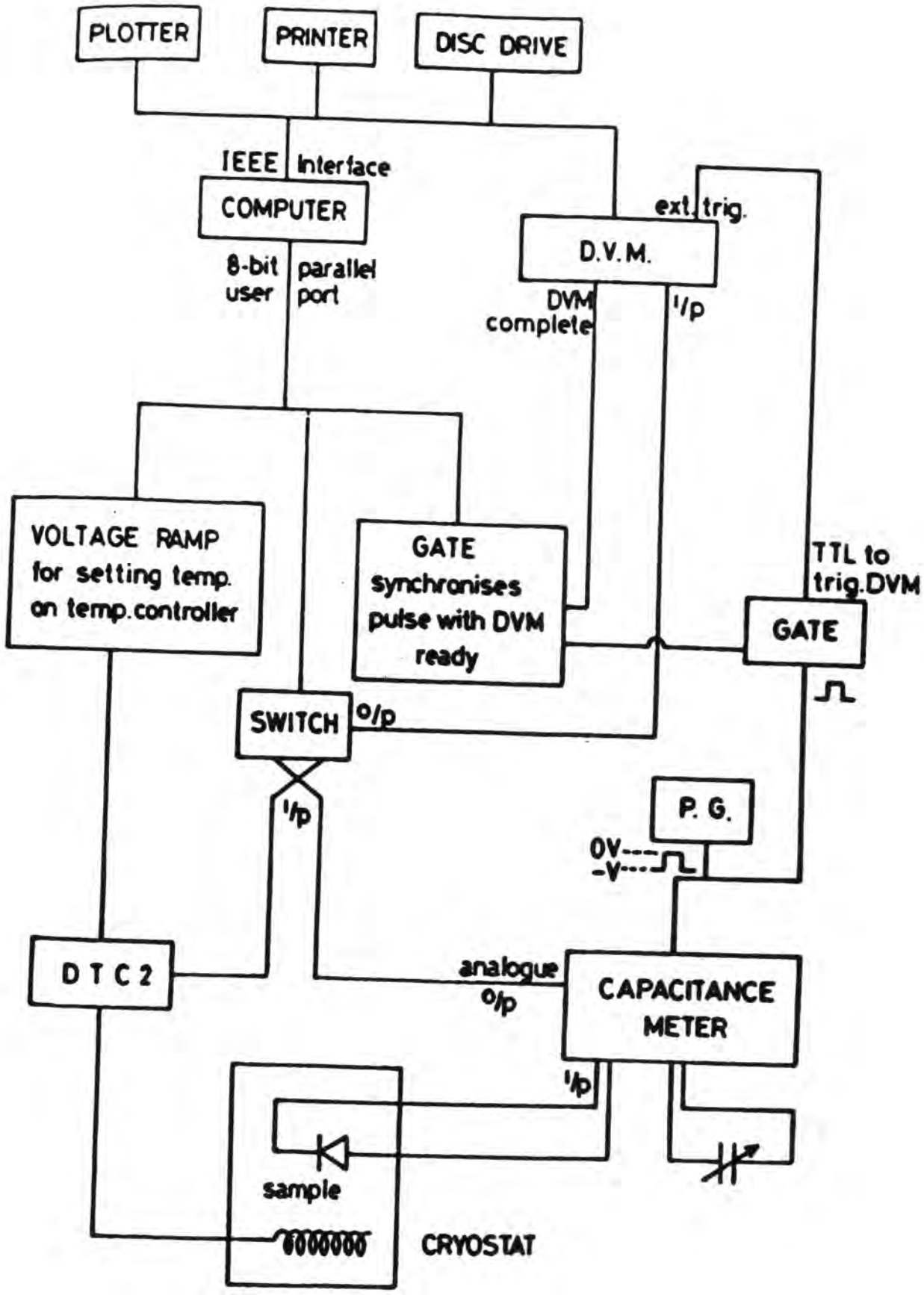

Fig. 5.12 : The block diagram of the DLTS system

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CHAPTER 5

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CHAPTER 6

CHARACTERIZATION OF MATERIALS

6.1 Introduction

The suitability of a semiconductor for device applications depends very much on crystal perfection and the effects of imperfections on the electrical and optical properties[1-3]. In particular, for solar cells the resulting deep levels in the crystal act as trapping or recombination centres and influence the lifetime of minority carriers and hence the device efficiency[4]. It is important therefore to understand the nature and properties of crystal defects in CdTe and to attempt to control them.

Since de Nobels' fundamental and comprehensive study[5] of CdTe, much has been published on the electronic levels introduced during crystal growth, by post-growth heat treatment or by doping with impurities[6] etc. A summary of the energy levels associated with defect centres and tentative identifications of their origins has been reported in reference 4. In the past decade, different techniques such as the thermally stimulated current (TSC)[4,7-10] and time-of-flight[11-13] measurements have been successfully used to characterize defect centres in CdTe. These techniques are only effective with compensated semi-insulating or pure and high resistivity CdTe, suitable for nuclear detectors[4]. Deep levels in low resistivity CdTe essential for solar cells, have not therefore received particular attention. DLTS has been applied very successfully to low resistivity CdTe[3,14-16] but most of this research was confined to n-CdTe and not to the p-type material which is most relevant to solar cells.

The as-grown bulk crystal CdTe used in the present study was semi-insulating, and had first to be doped semiconducting n or p-type before it could be used for cell fabrication. For this purpose CdTe substrates were subjected to various doping procedures as described in section 4.3. Similarly, heat treatments were often employed during contact and device fabrication. Therefore, it was necessary to characterize the CdTe in both as-grown and doped (with Te and Cu) conditions. High resistivity undoped material was characterized using space charge limited current analysis, while doped and more conducting CdTe was analysed by DLTS.

6.2 Activation Energy Analysis

6.2.1 Principles

The study of electrical transport in semiconductors provides information about the basic properties of the material such as type and concentration of free charge carriers contributing to conduction[17]. Measurements of current-voltage characteristics as a function of temperature can be particularly informative. In general, the effect of temperature on the conductivity of the material may often be expressed in terms of an activation energy and analysis of the activation energy in different regions of the current-voltage characteristics will yield information about deep localized energy levels.

Electrical conduction in semiconductors may be classified as intrinsic or extrinsic. Intrinsic conduction is generally only observed at higher temperatures (where the bandgap is a small multiple of kT) in high purity materials and will not be applicable in our case. When the number of charge carriers supplied by the impurities exceeds the carriers contributed by interband transitions the material is said to be extrinsic, and two types of extrinsic region may be distinguished

as: (a) uncompensated; (b) compensated. In the majority of semiconductors both acceptor and donor impurities are present and influence the conductivity. When the densities of the donor and acceptor impurities are equal the material is described as compensated. However, in general a semiconductor is only partially compensated and the free carrier concentration is then given by[17,18]:

$$n = N_c/N_a\ (N_d - N_a)\ \exp\ (E_d - E_a)/kT \qquad (6.1)$$

where N_d and N_a are the densities of donor and acceptor impurities respectively, N_c is the effective density of states in the conduction band and the activation energy for this type of conduction is $(E_d - E_a)$.

In addition to the three cases described above a fourth possibility, that is particularly important in wide gap materials, also exists. It is known as pseudo-intrinsic or non-extrinsic conduction. In narrow bandgap materials transport bands known as dominant levels contribute overwhelmingly to conduction whereas in wide bandgap materials certain discrete localized levels may be dominant. The concentration and position in energy of these dominant levels together with the concentration of carriers supplied by excess uncompensated impurities completely determine the location of the Fermi level[17]. This model is presented in Fig. 6.1, where E_o is the arbitrary reference level and there are localized deep levels E_q (donor) and E_m (acceptor). In order to obtain a constant activation energy (i.e. a straight line segment on a plot of logJ versus 1/T) the two conditions are[17]:

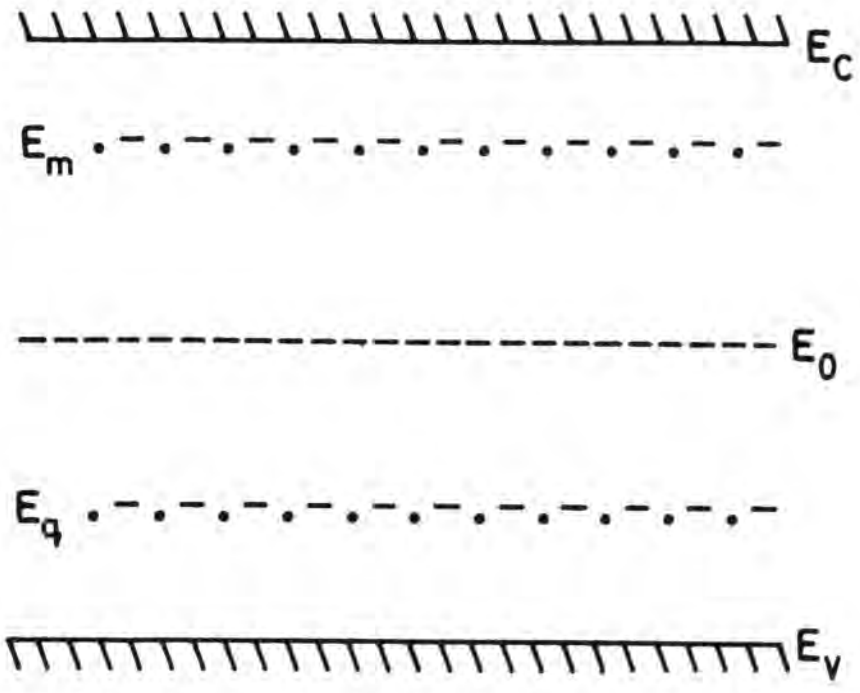

Fig. 6.1 : Schematic energy level diagram for a material showing an arbitrary reference level E_o and localized donor (E_q) and acceptor (E_m) levels.

(1) the number of uncompensated donor impurities is much larger than the square root of the product of the electron-hole densities.

(2) the number of uncompensated donor impurities is much smaller than the product of the electron and hole densities.

In the first case the Fermi level E_f and carrier concentration n are given by[17]:

$$E_f = E_m + kT \ln (N_d - N_a)/N_m \tag{6.2}$$

$$n = N_c/N_m (N_d - N_a) \exp (E_m - E_c)/kT \tag{6.3}$$

where N_m is the concentration of levels E_m. For the second case E_f and n are:

$$E_f = \tfrac{1}{2} (E_m + E_q) + \tfrac{1}{2} kT \ln (N_q/N_m) \tag{6.4}$$

$$n = N_c(N_q/N_m)^{\frac{1}{2}} \exp \left[\{(E_m - E_c) + \tfrac{1}{2} (E_q - E_m)\}/kT \right] \tag{6.5}$$

The activation energy for the second case is[19]:

$$\Delta E = (E_c - E_m) + (E_m - E_q)/2 \tag{6.6}$$

It is evident from equation 6.6 that the activation energy involves a combination of energy $(E_c - E_m)$ required to raise carriers from the dominant level to its transport band, plus the energy $(E_m - E_q)/2$ required to create carriers in the dominant majority carrier level. The two cases known as extrinsic and non-extrinsic can be

differentiated by the Roberts and Schmidlin theorem[17,20] which states that "the existence of different (or identical) activation energies for ohmic and space charge limited conduction is both a necessary and a sufficient condition for ohmic conduction to be non-extrinsic (or extrinsic)".

The electrical conductivity of a semiconductor depends on the density of free carriers, distribution of their thermal velocities, and variation from an equilibrium distribution caused by an external electric field. When the drift velocities (due to an applied field) are small compared to the mean thermal velocity, the following relation holds.

$$V_d = \mu E \tag{6.7}$$

where V_d is the drift velocity, μ the mobility of free electrons and E is the applied field. The current density J is expressed as[17]:

$$J = \sigma E \tag{6.8}$$

where the conductivity σ is[17]:

$$\sigma = ne\mu$$

$$= (N_c e \mu)e^{-\Delta E/kT} \tag{6.9}$$

where e is the electronic charge, k is the Boltzmann constant, T is the absolute temperature and ΔE is the activation energy. A plot of logσ

vs reciprocal temperature will result in a straight line from the slope of which an activation energy can be calculated. However, for materials where the mobility is controlled by impurity scattering ($\mu \propto T^{3/2}$) the plot of the logrithm of J/T^3 vs reciprocal temperature might be expected to yield a straight line[17] (in the latter case the $T^{3/2}$ dependence of μ does not cancel the temperature dependence of N_c).

When the electric field applied to a solid with ohmic contacts is sufficiently high, the injection of charge carriers into the solid is observed[17,21]. For a trap-free material, when the injection of carriers takes place a cloud of space charge carriers will form in the vicinity of the contact, with a mutual repulsive force between the carriers which limits the total injection of charge into the body of the crystal. This current is known as space charge limited (SCL) current and has a close analogy with SCL conduction in vacuum diodes. The difference, of course, arises from the interaction of space charge with the lattice and is due to trapping centres. The relation between the current, voltage and thickness of the sample is given by[19]:

$$J = 9(\theta_n \varepsilon \mu_o)V^2/8L^3 \qquad (6.10)$$

where μ_o is the microscopic mobility and θ_n is the fraction of injected carriers which are free. A similar equation is valid for holes. The general form of this expression for bulk space charge currents in a homogeneous medium is:

$$J \propto L\,(V/L^2)^n \qquad (6.11)$$

where n is a constant, for a trap-free region n=2, while for double injection n=3, and for recombinative space charge injection n=½. The ohmic and space charge limited regions are shown in Fig. 6.2. The lowest region of the curve (at low voltage), where the excess injection of free carriers is negligible and conduction is mainly due to thermally generated carriers, is known as the ohmic region. The first threshold V_x where the ohmic current crosses over to SCL current is expressed by the relation:

$$V_x = 8(enL^2)/9\varepsilon\theta_n \qquad (6.12)$$

The second threshold of interest is that which corresponds to the Fermi level approaching the trap level (when all the space charge enters the transport band thus causing a steep rise in the current-voltage characteristics) is known as traps filled limit voltage and given by[19]:

$$V_{TFL} = N_m e L^2/\varepsilon \qquad (6.13)$$

6.2.2 Results

The d.c. conductivity measurements presented in this section were carried out in an Oxford Instruments DN1704 variable temperature cryostat described in section 5.8. The dark steady state current-voltage characteristics were measured for the as-grown p-CdTe (boule BA10) samples using sandwich type structures. These were in the form of small dice (4x4x2 mm^3) cut from the single crystal CdTe boules. The dice were then mechano-chemically polished as outlined in section 4.4.1. Gold evaporated under high vacuum (10^{-6} torr) was used to make ohmic contacts.

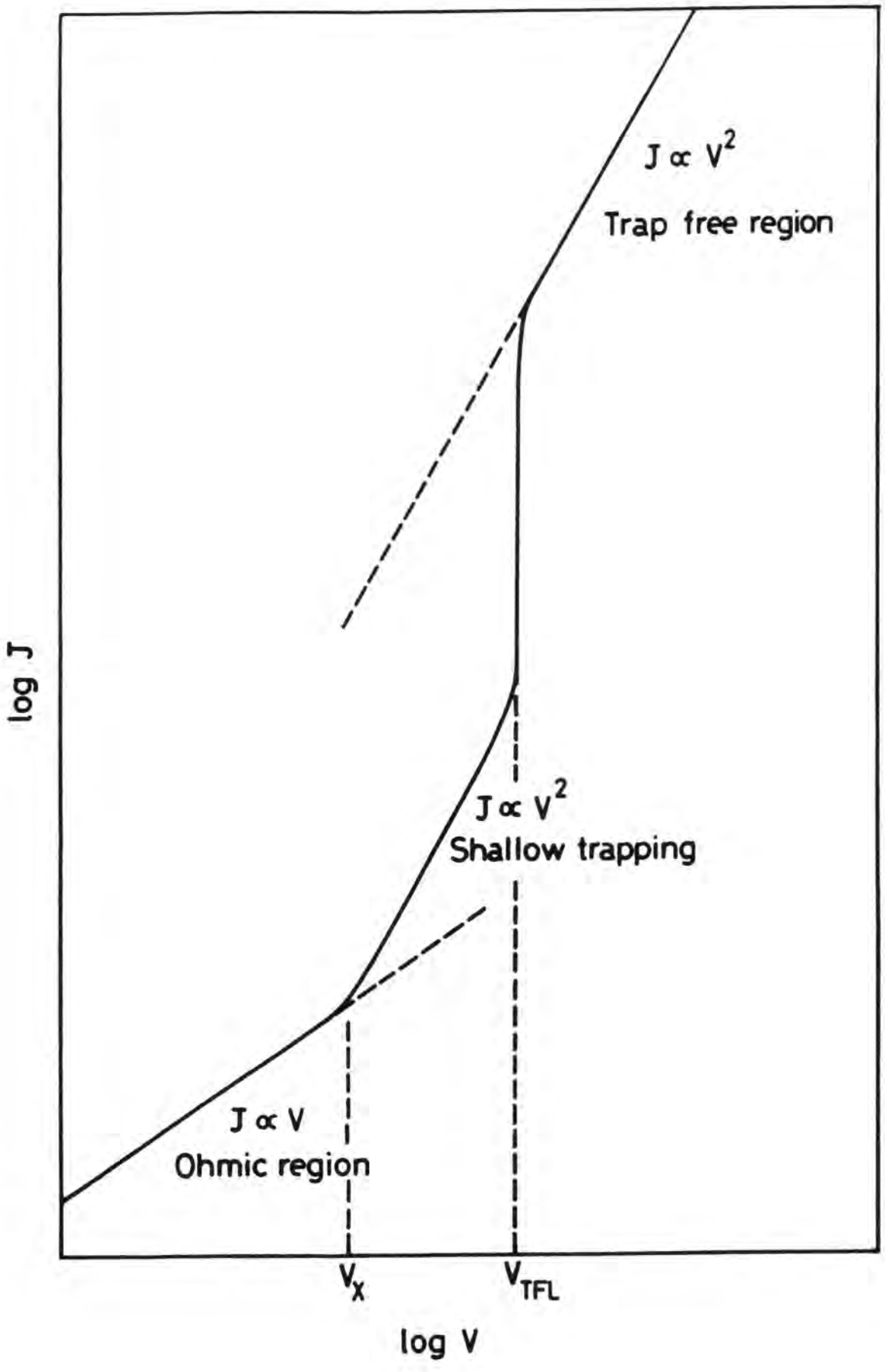

Fig. 6.2 : Typical current-voltage characteristics for a one carrier SCLC controlled by a single set of trapping centres

The current-voltage characteristics were measured at different temperatures in the range 200-360K. The data was obtained point-by-point and at each applied bias time was allowed for the current to achieve a steady state condition. A selection of typical current-voltage curves for one of the samples at several temperatures is shown in Fig. 6.3. The curves exhibit a low field ohmic region (1-15 V) followed by a square law (space charge) region. However, the trap filled limit voltage[19] was not clearly defined since the forward bias applied did not reach that limit.

In order to calculate the activation energy, plots of logJ versus reciprocal temperature for both ohmic and space charge regions were constructed and used to determine the activation energies. Typical plots of logJ vs reciprocal temperature for the ohmic and space charge limited currents are presented in Fig. 6.4. In this temperature range (200-360K) of measurements the activation energy for ohmic and SCL currents was found to be 0.5 eV. Since the activation energy for both the currents was identical then according to the Roberts and Schmidlin Theorem[20] the material was extrinsic. Activation energies of 0.5 eV have been reported in the literature[22-24] and are generally attributed to cadmium vacancies.

6.3 DLTS Studies of Single Crystal CdTe

6.3.1 Principles

DLTS measures a high frequency capacitance transient, utilising a thermal scanning technique, to study a wide variety of defects (traps) in a semiconductor. It was introduced by Lang[25], and because of its immunity to noise and surface channel leakage current has the ability to distinguish between majority and minority carrier traps[26], thus making it more versatile than admittance spectroscopy which is limited

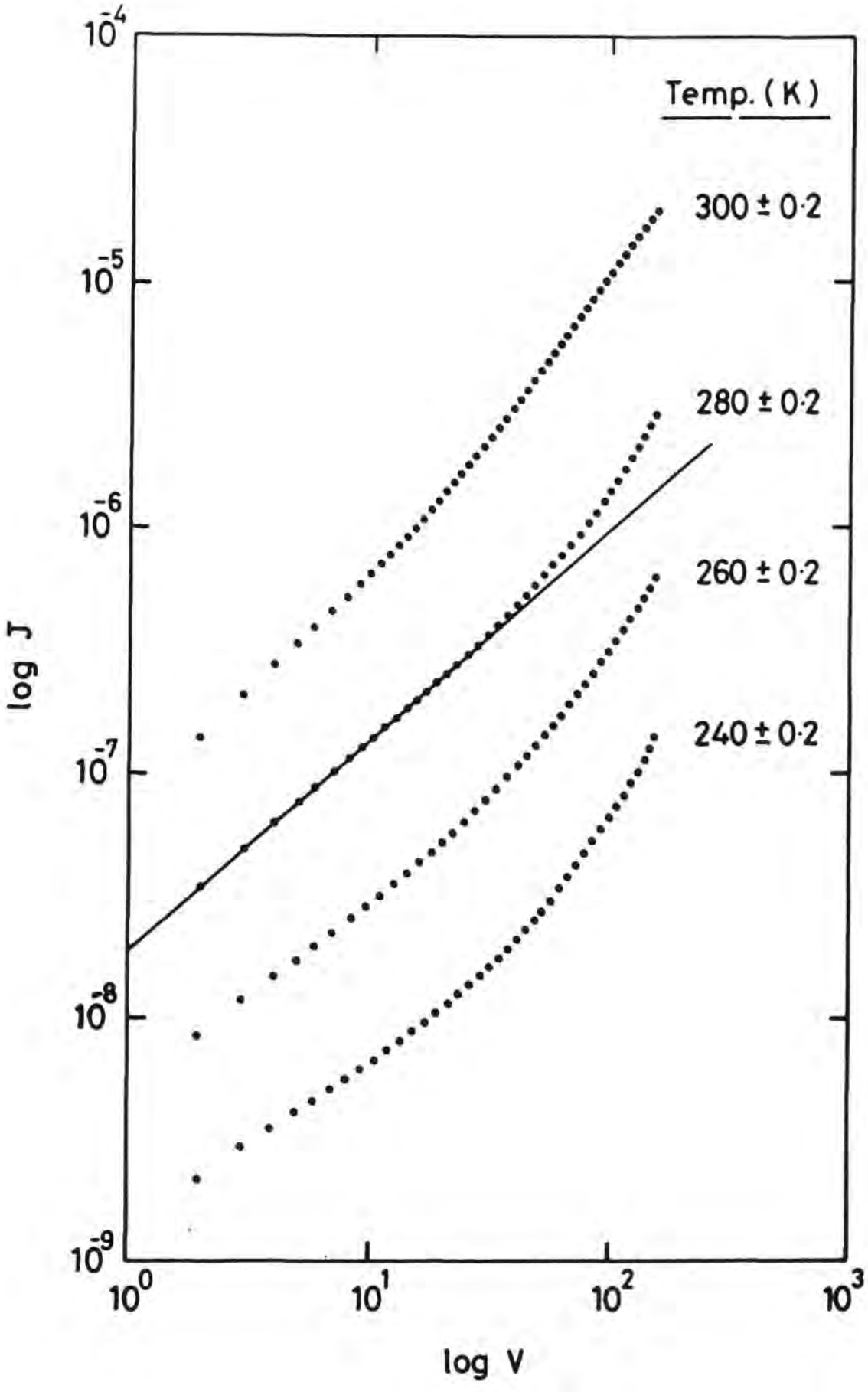

Fig. 6.3 : Current-voltage characteristics at several different temperatures for a typical sample of CdTe

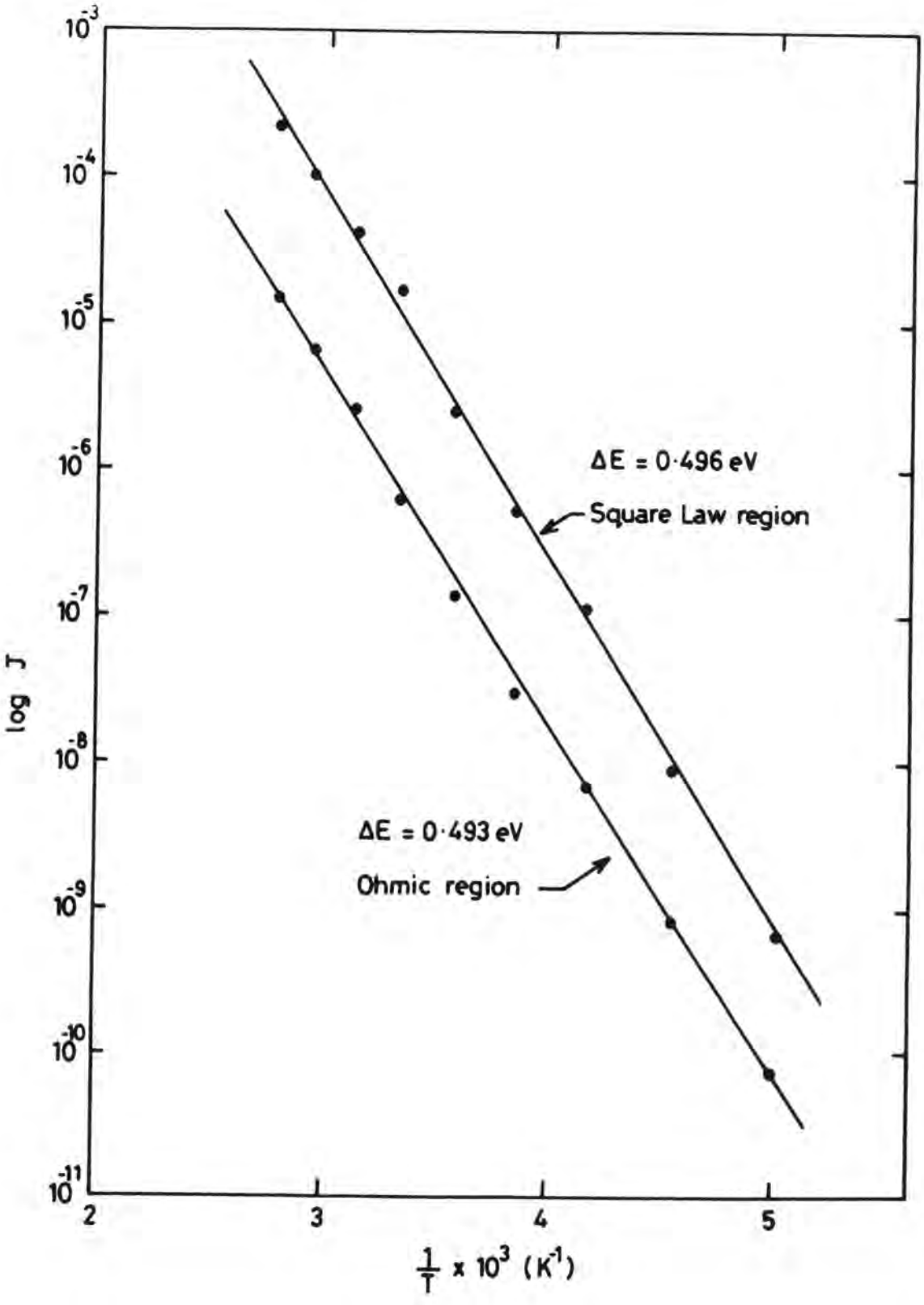

Fig. 6.4 : Typical plots of logJ vs reciprocal temperature for the ohmic and square law regions of the I-V curves in fig. 6.3.

to majority carrier traps[27]. It is also a much more sensitive technique than thermally stimulated capacitance[26,28] (TSCAP). DLTS is based on the observation of the capacitance transient associated with the relaxation of the trapped carrier population to thermal equilibrium following some perturbation of the steady state trap occupancy. The time constant of the transient can be measured as a function of temperature to obtain the activation energy of the level.

The central idea of the DLTS technique is to set an emission rate window such that the response is a maximum when the transient matches the rate set by the window. At the particular temperature, where the trap emission rate is the same as the window, a peak with a magnitude proportional to the trap density is observed in the DLTS spectrum. Therefore, replotting the spectrum for a number of different rate windows enables the dependence of emission rate on temperature to be determined.

The emission rates are thermally activated and are given, according to the principle of detailed balance as[25]:

$$e_1 = (\sigma_1 < v_1 > N_{D1}/g) \exp(-\Delta E/kT) \qquad (6.14)$$

where σ_1 is minority carrier capture cross-section, $< v_1 >$ is the mean thermal velocity of the minority carriers, N_{D1} is the effective density of states in the minority carrier band, g is the degeneracy of the trap level and ΔE is the energy separation between the trap level and the minority carrier band. A similar equation holds for majority carriers with all subscripts changed from 1 to 2. The pre-exponential term in equation 6.14 has a T^2 dependence on temperature, if σ is independent of temperature and thus a plot of $\log(T^{-2}e_1)$ vs 1000/T will yield the

activation energy for the trap from the slope of the resulting straight line.

The DLTS technique makes use of a dual-gated signal averaging (double boxcar) which samples the capacitance transient at two times t_1 and t_2, to determine the difference ΔC in capacitance at these times. The boxcar method also provides signal averaging capability to enhance the signal to noise ratio for detection of low concentrations of traps. The rate window is selected by the choice of the times t_1 and t_2 as:

$$e = \left(\ln(t_2/t_1)\right)^{-1} \times (t_2 - t_1) \qquad (6.15)$$

The process is illustrated in Fig. 6.5 where the left hand side of the figure represents the capacitance transients at various temperatures, and the right hand side shows the corresponding DLTS signal $C(t_1) - C(t_2)$ from the double boxcar. It is evident from the figure that $C(t_1) - C(t_2)$, goes through a maximum when the transient rate constant matches the selected rate window. The experimental arrangement used has been described in section 5.9.

6.3.2 Sample Preparation

DLTS studies were undertaken on Schottky barrier devices fabricated on single crystal substrates. The substrates were selected from two different boules (BA36, BA25) and subjected to different treatments before they were used for device fabrication and characterisation. BA36 had an unusually low as-grown resistivity of $\sim$300 Ω - cm. The boule was oriented and dice (4x4x2 mm^3) were cut parallel to the (100) planes. These were degreased and polished as described in section 4.4.1. The samples were then annealed in Te vapour for one week at 550°C (section 4.3.1) after which they were

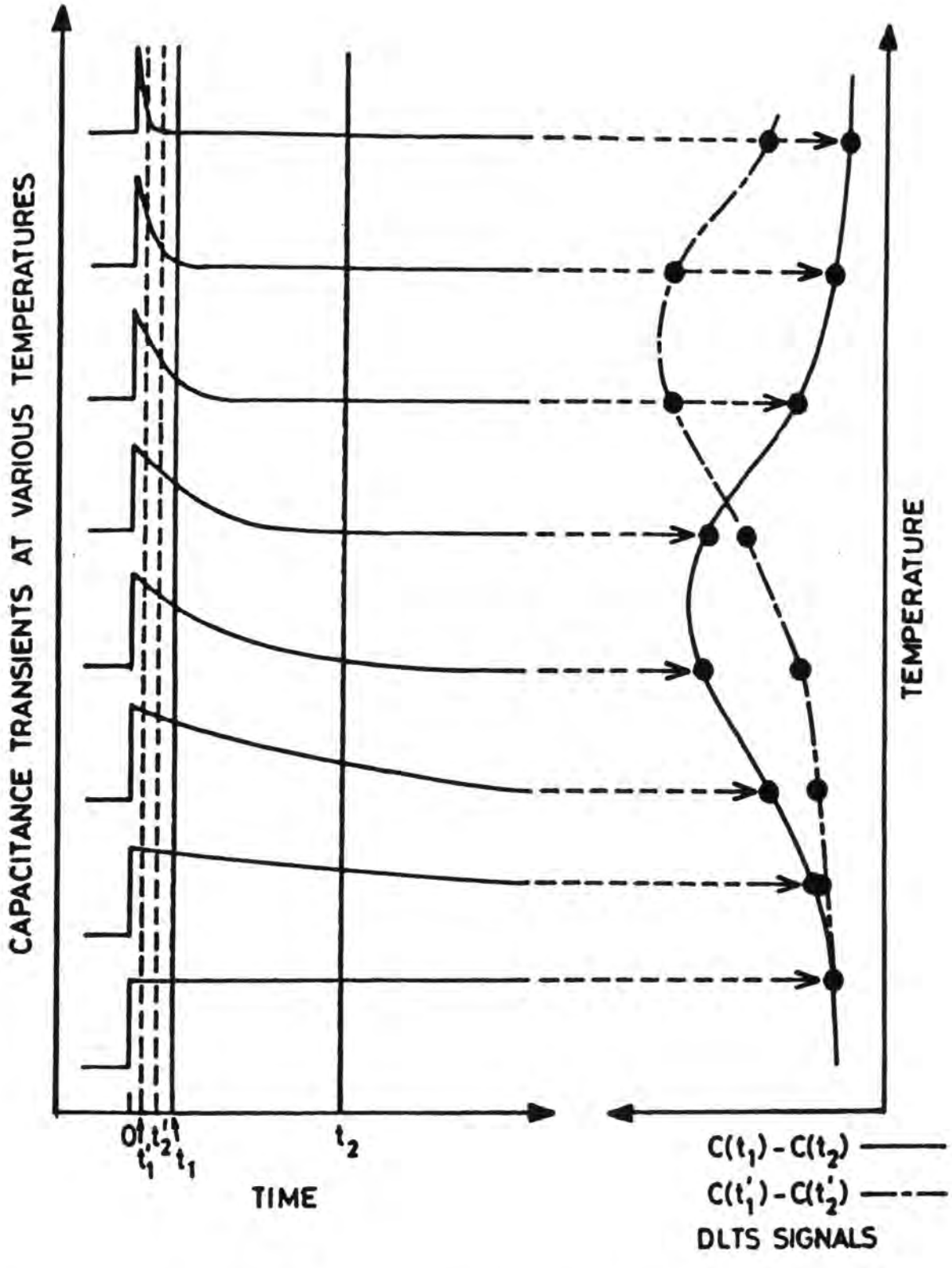

Fig. 6.5 : Implementation of a rate window by means of a double-boxcar integrator[25]

repolished to rid the surface of any Te deposit. Evaporated In/Al and gold were used to make the Schottky barrier and ohmic contacts respectively.

In contrast, boule BA25 was much more typical with an as-grown resistivity of the range of M Ω - cm. Unoriented dice (4x4x2 mm^3) were cut from it and after polishing, were annealed for different periods (1 and 4 hours) at 800°C. Gold and Al/In were again used to make ohmic and Schottky contacts.

6.3.3 Device characteristics

The Schottky devices used for DLTS study were first characterized by measuring the current-voltage and C-V characteristics. The diode and photovoltaic output characteristics of a typical Schottky diode fabricated on a p-CdTe (BA36) substrate after annealing in Te vapour for one week at 550°C are shown in Fig. 6.6. Since devices were not intended to be investigated as solar cells, attempts were not made to measure and optimize their efficiency. It is however, evident from Fig. 6.6 that the junction was fairly rectifying, with negligible reverse bias leakage (rectification ratio of $\sim$ 200 at 0.5 V).

The C-V measurements were made at room temperature at a frequency of 1MHz. A typical C^{-2} vs V plot for the device described above is shown in Fig. 6.7. The plot is a straight line for a reverse bias range up to 3 V but beyond this the capacitance decreases more slowly with increasing reverse bias. The voltage intercept on the V axis is 1.5 V which is relatively high. The net ionized acceptor density obtained from the slope of C^{-2} vs V plot is 2×10^{14} cm^{-3}.

Large values of the intercept on the voltage axis have been reported by several workers[29,30] and have been recognized as the result of an interfacial layer between the metal and the semiconductor.

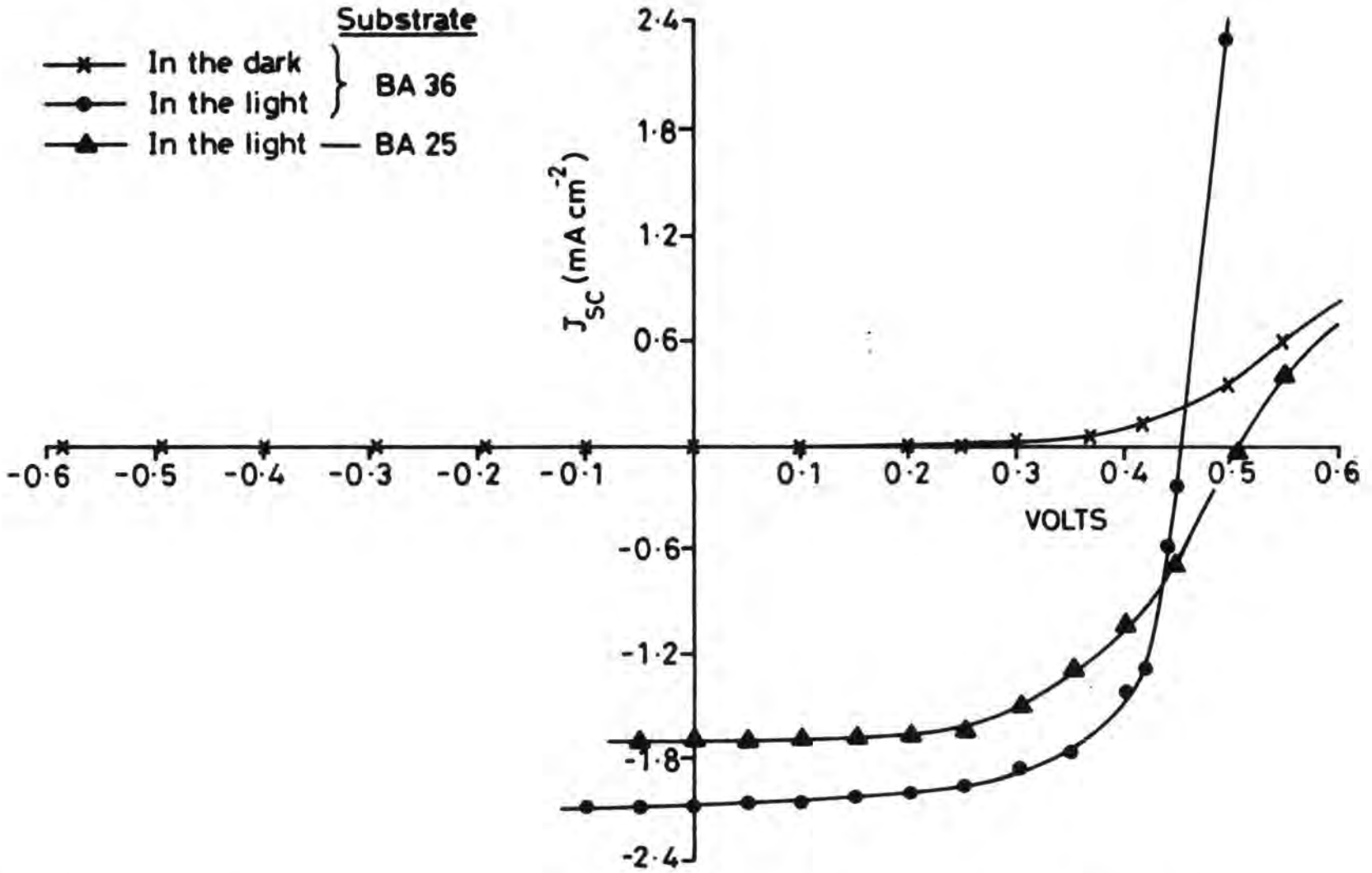

Fig. 6.6 : Current-voltage characteristics of the Schottky diodes fabricated on p-CdTe substrates.

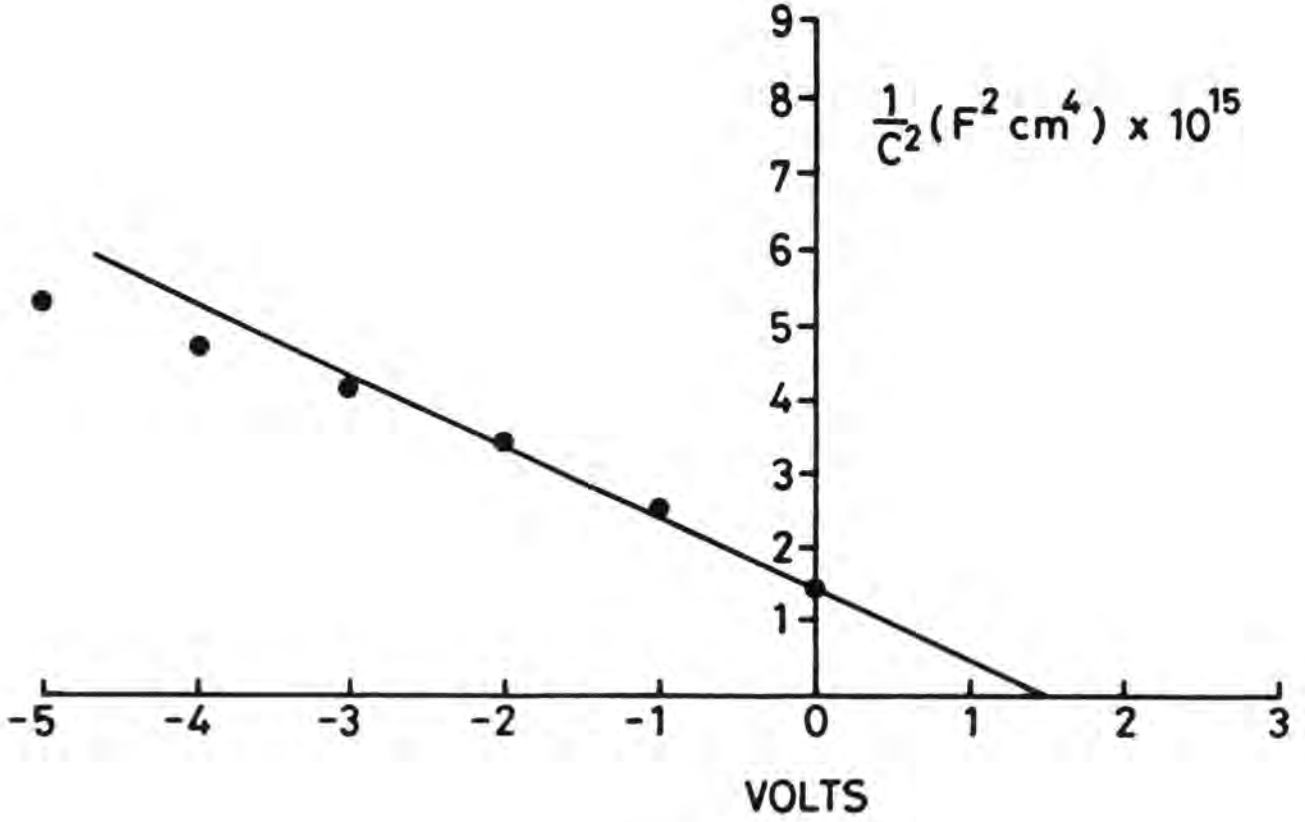

Fig. 6.7 : C^{-2} vs V plot for an In-CdTe Schottky device fabricated on a p-CdTe substrate (BA36)

A model which includes the interfacial layer (assuming that the charge in surface states is independent of applied bias) has been analysed by Goodman[31] who derived an expression for the voltage intercept (V_o) which is always larger than the built-in potential (V_b) when an interfacial layer is present. Cowley[32] developed Goodman's assumption and also predicted higher values of V_o. Crowell et al[33] showed that an effective interfacial layer of non-zero thickness must exist between the metal and semiconductor even when both are in intimate atomic contact. This interfacial layer may be produced during processing and can arise due to chemical reactions, oxide layers etc.

The Schottky devices fabricated on substrates (BA25) annealed in Te vapour at 800°C (for one and four hours) were relatively resistive and the diode characteristics were less rectifying with rectification ratios of ∿50 at 0.5 V. The output characteristic measured for a typical Schottky made on a substrate annealed in Te vapour at 800°C for 4 hours is included in Fig. 6.6. The C-V characteristics showed the same general behaviour as diodes fabricated from BA36; the most notable feature being the large intercept on the voltage axis.

6.3.4 DLTS measurements

DLTS measurements were carried out in the temperature range 200-400K. The resultant spectrum for a typical Schottky device fabricated on a p-CdTe substrate annealed in Te vapour for four hours at 800°C is shown in Fig. 6.8. It clearly displays three distinct peaks at about 289, 347 and 377K, corresponding to hole traps designated as H_1, H_2 and H_3 respectively. DLTS spectra for the Schottky barrier sample (with substrate annealed at 550°C for one week) were identical to that in Fig. 6.8. However, for the device made on a

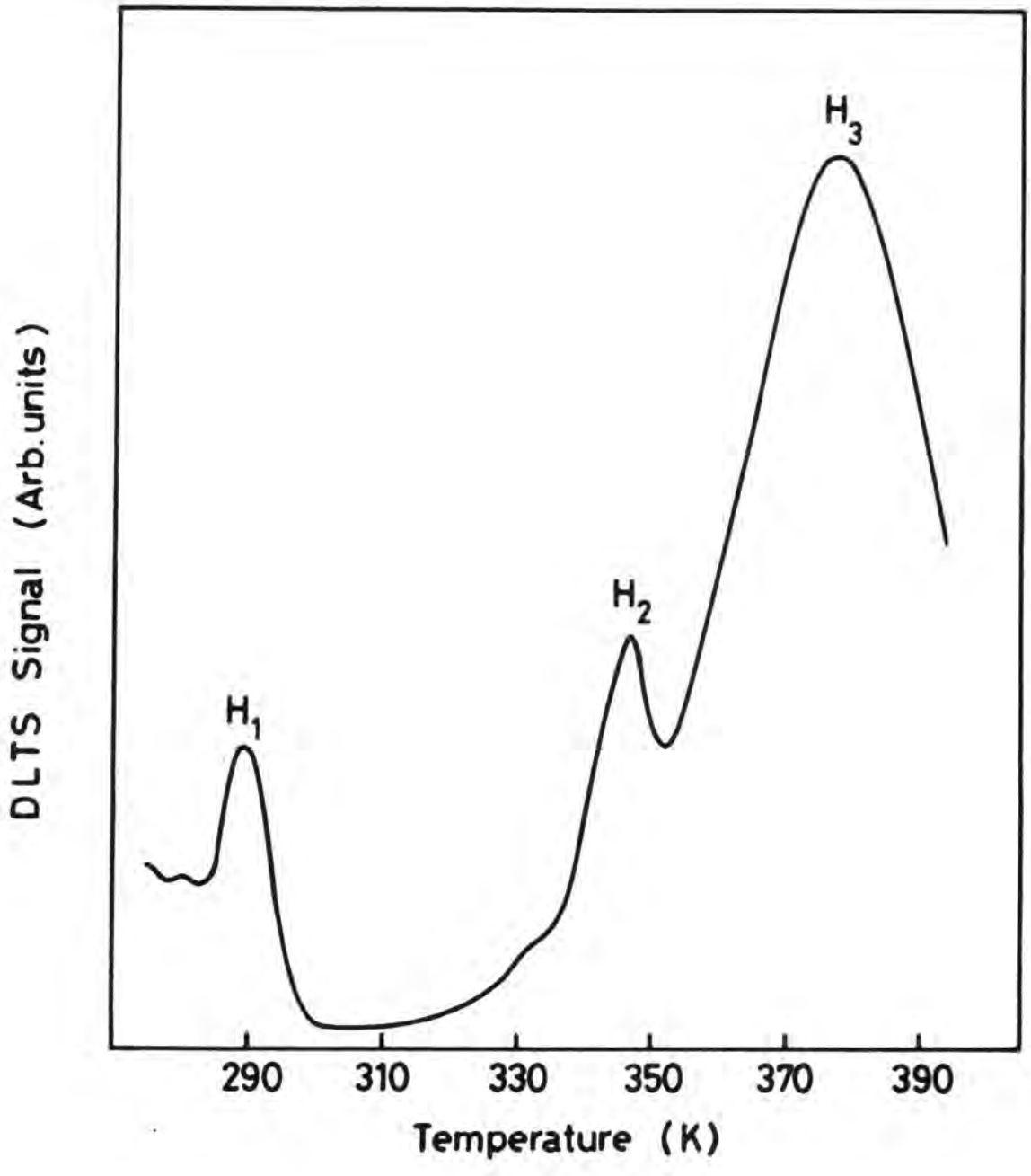

Fig. 6.8 : DLTS spectrum for a Al-CdTe Schottky device (Te-annealed for 4 hours at 800°C).

substrate annealed for one hour at 800°C the peak corresponding to hole trap H_3 was not observed.

Arrhenius plots of $\ln(T^2\tau)$ versus 1000/T for the three peaks in Fig. 6.8 are shown in Fig. 6.9. The calculated activation energies are 0.53 (H_1), 0.71 (H_2) and 0.84 eV (H_3) with capture cross-sections of $(2.3\pm1.6)\ 10^{-15}$, $(6.5\pm1.7)\ 10^{-12}$ and $(2.6\pm0.5)\ 10^{-14}$ cm^2.

6.3.5 Discussion

In principle, it would be very useful to compare the present results with published data but unfortunately there have been few DLTS studies of p-type CdTe[16,34,35]. Data obtained from differently grown materials and studied using different techniques are available however. Ou et al[35] have reported a trap at $\sim$ 0.54 eV above the valence band in electrodeposited p-CdTe thin films using DLTS technique. The existence of this level in electrodeposited CdTe (p-type) films was also confirmed by SCLC analysis[36]. Collins and McGill[16] have also observed a majority carrier level at 0.5 eV in nominally undoped p-CdTe using DLTS. It is also important to note that a hole trap at 0.48 eV (which is close to 0.53 eV) above the valence band has been found in n-CdTe studied by DLTS method[37]. In addition several other researchers have reported hole traps in the range 0.5 - 0.57 eV and this level is thought to be due to Cd vacancies[38,39]. These results together with the observation that a level at 0.5 eV was found in the as-grown material strongly suggest that the hole trap H_1 (0.53 eV) found in the present study is identical with the trap level reported by Ou et al and others and is probably a native defect level such as a Cd vacancy.

The hole trap H_2 (0.71 eV) seems identical with an energy level at 0.72 eV also observed by Ou et al[36] using SCLC. Hole traps at 0.65 -

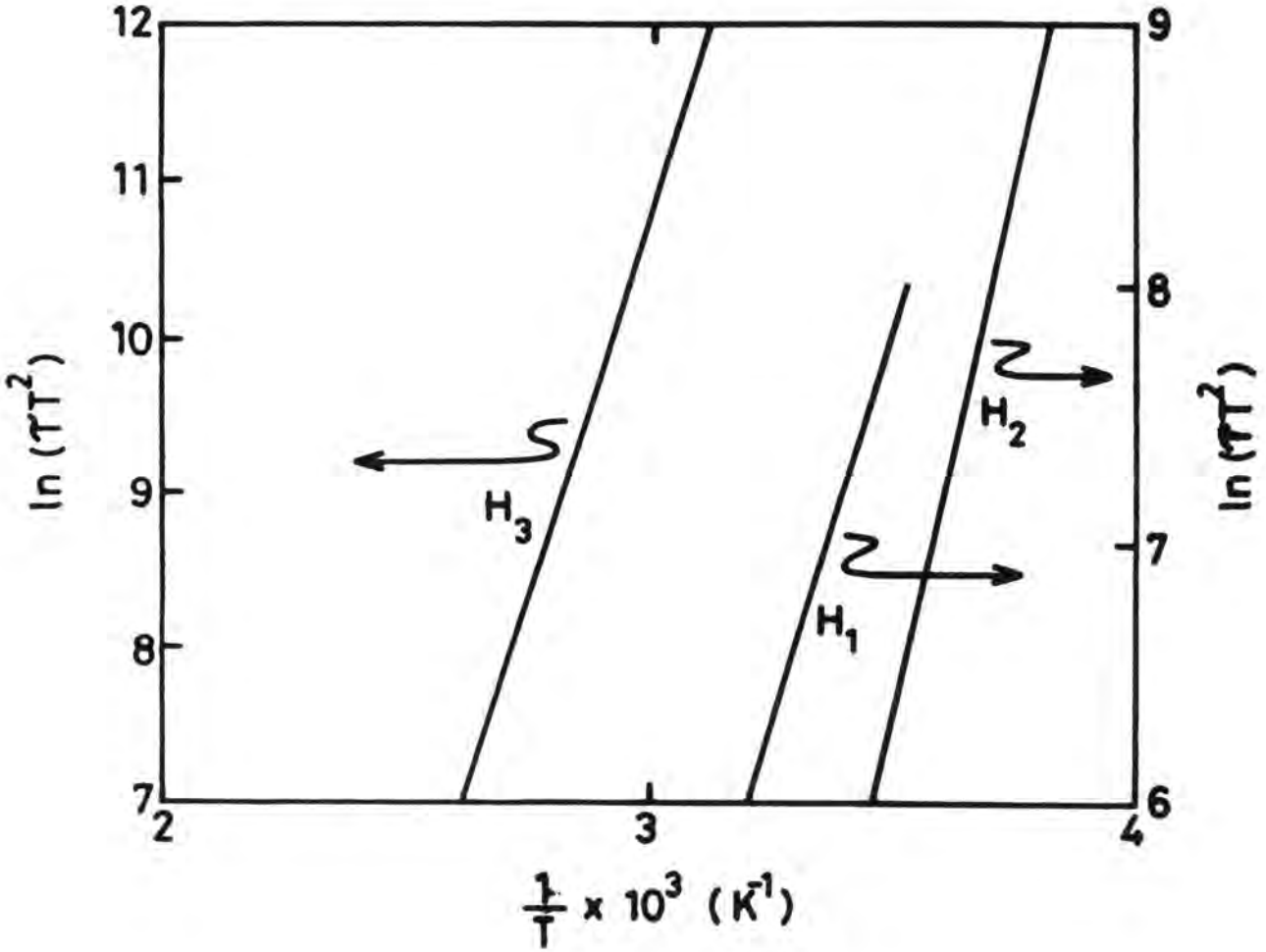

Fig. 6.9 : Arrhenius plots for traps H_1, H_2 and H_3 (Fig. 6.8)

0.75 eV above the valence band have often been reported in the literature[40-42] and are attributed to either doubly ionized Cd vacancies or native defect-impurity complexes. These results imply that the hole trap H_2, although not observed in the as-grown high resistivity material, may be associated with impurities or native defects which are either commonly found in CdTe, or easily introduced during the vapour anneal performed on the samples.

The energy level H_3(0.84 eV) which was not observed in the samples annealed at 800°C for one hour compares well with published results. Energy levels at 0.6-0.9 eV have been reported by Zanio[6]. Although little or no evidence is available as to their origin, they have been previously assigned to V_{Cd}^{-} and V_{Cd}^{2-}. The latter is however, preferred because the singly ionized Cd vacancies can more conveniently explain the levels close to the valence band[6]. The level (0.84 eV) observed during the present work is the result of annealing the samples in Te vapour for longer times. It is reported that annealing CdTe at elevated temperatures under fixed partial pressure of its constituent elements, Cd and Te can modify the material defect structure[5,43]. Thus, it is possible that this trap might well be associated with interstitial Te or V_{Cd}^{2-}.

6.4 DLTS Studies of Thin Film CdTe/CdS Heterojunctions

In an attempt to characterise CdTe thin films, p-CdTe/n-CdS heterojunctions were also investigated by DLTS. In these devices the CdS and CdTe layers were sequentially deposited onto a tin oxide coated glass slide (section 4.5). A calculated amount of Cu (300 ppm) was evaporated onto the CdTe layer and then covered with a thin layer of carbon paste. This was followed by a 30 minute anneal at 330°C in a nitrogen ambient. Thin copper wires were attached to tin oxide and

carbon paste using silverdag to serve as electrodes to the device. The devices were first characterized using current-voltage, spectral response and photocapacitance measurments (Chapter 8).

These measurements were made using a more recently developed DLTS system than that used for earlier studies on single crystal CdTe (section 6.3). The DLTS system used here was based on a Gould model 1425 digital storage oscilloscope (DSO) under the control of a BBC microcomputer. The DSO was used to capture the full capacitance transients at 1024 points. At each temperature several transients were captured and averaged by the DSO before transmitting the averaged data to the BBC computer for storage to disc. The computer was then used to simulate a double boxcar, constructing several DLTS spectra for a wide range of rate windows.

DLTS measurements were made over the temperature range 100-350K (section 5.9). Typical DLTS spectra obtained are presented in Fig. 6.10. There is a large peak (labelled E_A in Fig. 6.10) in the temperature range 320-350K. This peak did not exhibit the behaviour associated with a deep level, since a large change in the rate window did not produce a singificant change in the peak position, suggesting that it was related to a shallow level. However, the position of the peak (320-350K) implied that the level was very deep. These two contradictory observations could not be explained and the nature of this level is still unknown.

In addition, several other peaks in the temperature range 100-250K were present (Fig. 6.10). These peaks are very close and it is difficult to resolve the individual peaks accurately. A careful

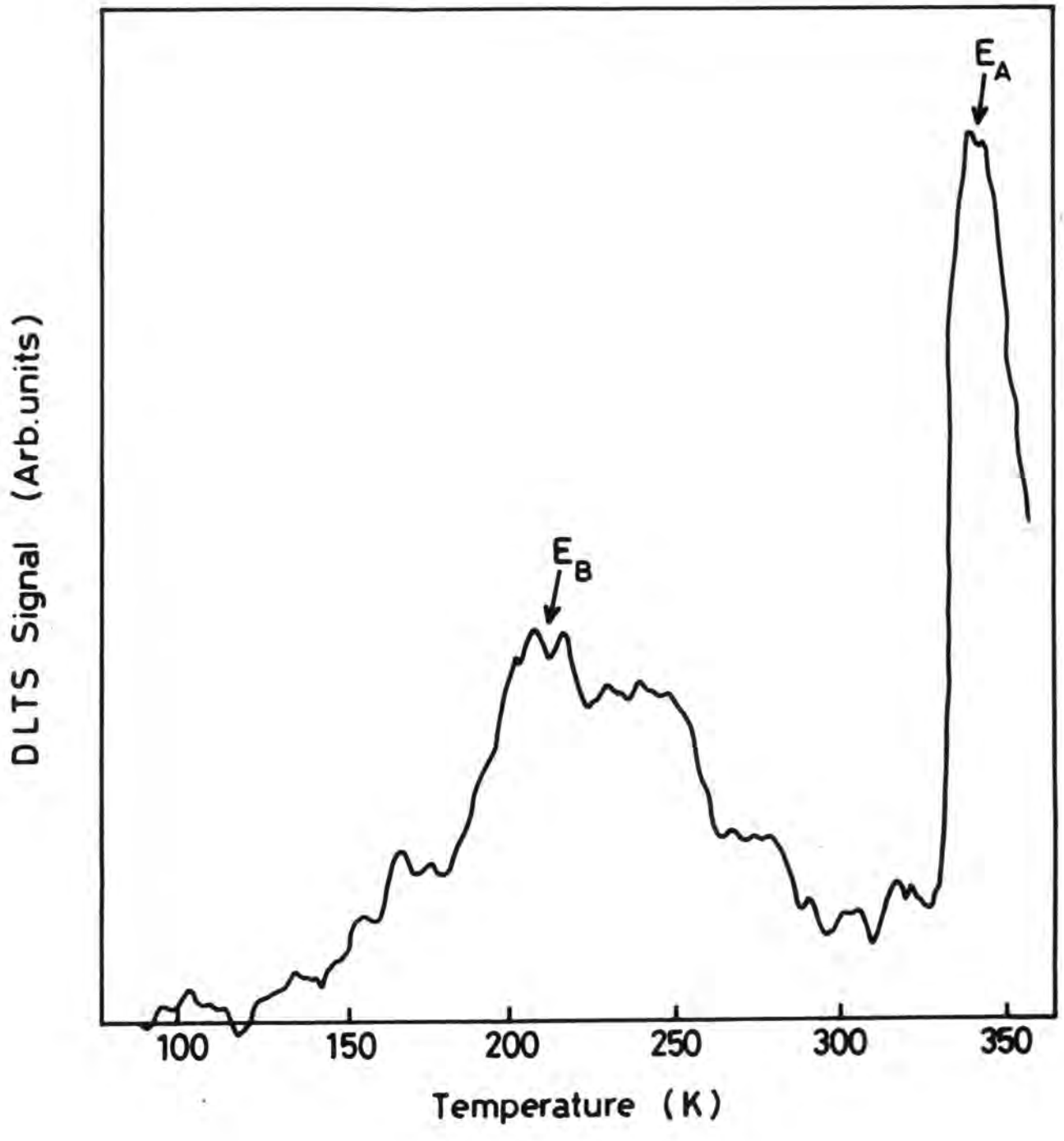

Fig. 6.10 : Typical DLTS spectrum for a thin film CdTe:Cu/CdS heterojunction

analysis of one peak (labelled E_B in Fig. 6.10), following its movement with changes in the rate window enabled an Arrhenius plot to be constructed which is shown in Fig. 6.11. The activation energy was found to be 0.35 eV with a capture cross-section of 10^{-22} cm^2.

As described in section 8.5.1, Au, Ag and Cu primarily substitute for Cd in CdTe, and act as acceptors and secondarily fill interstitial positions where they act as donors[6]. de Nobel found an acceptor level at 0.33 eV for Au, Ag and Cu using Hall measurements[5], but Lorenz and Segal using the same technique have shown that Cu gives rise to an acceptor level 0.35 eV above the valence band[44]. Although the levels associated with these metals (Au, Cu and Ag) are very close to each other, the fact that our CdTe layers were deliberately doped with 300 ppm of Cu makes it almost certain that this level was associated with copper. This level was also observed in the photocapacitance studies made on these heterojunctions.

6.5 Conclusions

The main results presented in this chapter are summarized in table 6.1. As-grown bulk crystal CdTe was characterized by a careful analysis of the current-voltage characteristics which displayed the usual ohmic and space charge limited current forms. The activation energy analyses of the linear and square law regions gave the same activation energy of 0.5 eV. This indicates that the conduction was extrinsic.

DLTS was used to characterize p-CdTe in both bulk crystal and thin film forms. Deep levels with energies 0.53, 0.71 and 0.84 eV above the valence band and corresponding capture cross-sections of $(2.3\pm1.6)10^{-15}$, $(6.5\pm1.7)10^{-12}$ and $(2.6\pm0.5)10^{-14}$ were found in the bulk CdTe samples annealed in Te-vapour. The level at 0.53 eV above the valence band

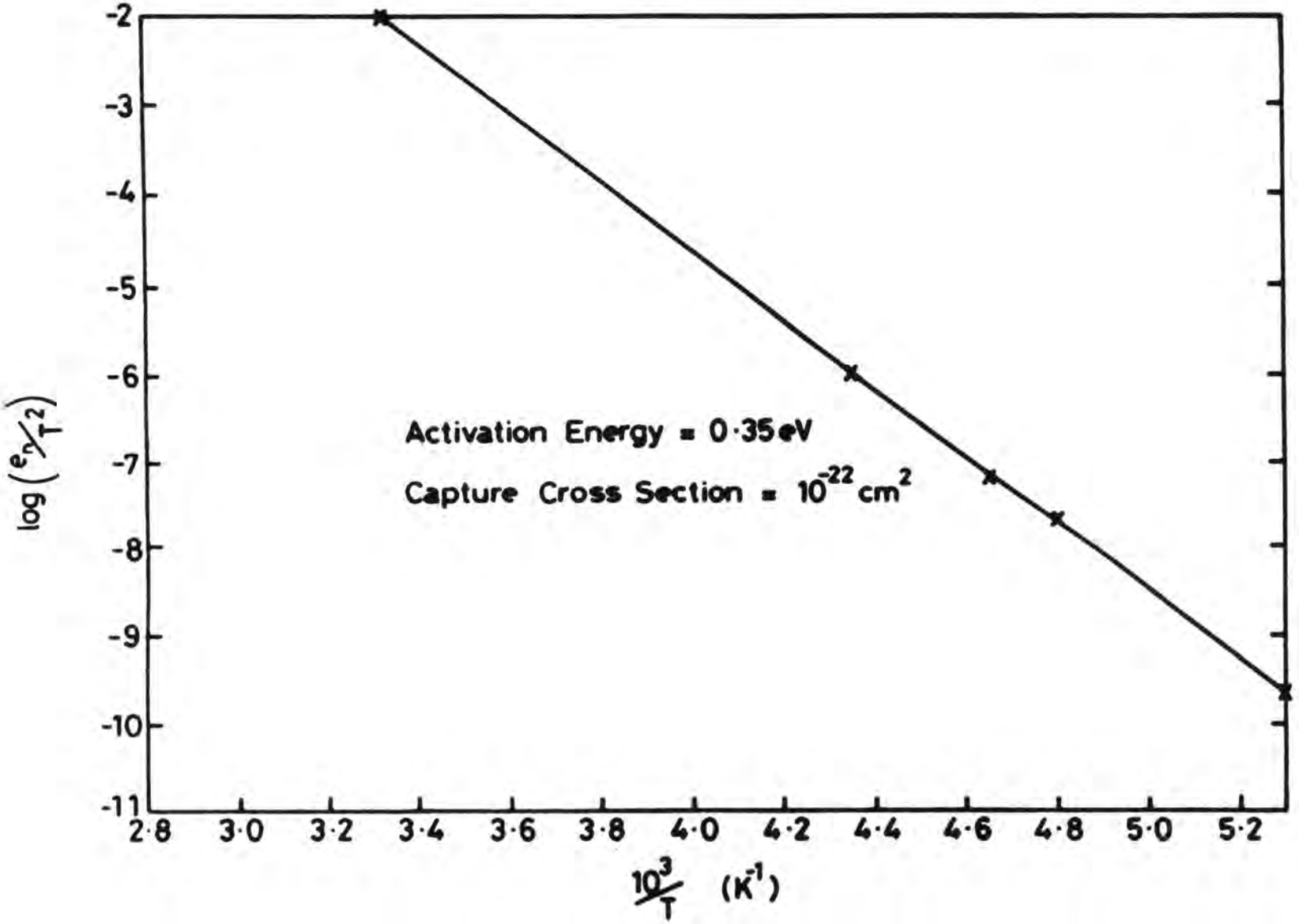

Fig. 6.11 : Arrhenius plot for the trap E_B (Fig. 6.10)

TABLE 6.1 Summary of the energy levels observed in CdTe

Material	Post-growth Treatment	Energy Levels (eV)	Technique Employed
Single Crystal (BA10)	As-grown	0.50	SCLC
Single Crystal (BA36)	Te-Vapour anneal at 550°C for one week	0.53 0.71 0.84	DLTS
Single Crystal (BA25)	Annealed in Te-vapour at 800°C for four hours	0.53 0.71 0.84	DLTS
Single Crystal (BA25)	Annealed in Te-vapour for one hour at 800°C	0.53 0.71	DLTS
Thin film CdTe	Cu-doped	0.35	DLTS

seems to have an intrinsic character, and was probably a native defect such as a cadmium vacancy. The other levels (0.71 and 0.84 eV) appeared to have been introduced due to annealing in Te-vapour. Thin film CdS/CdTe heterojunctions with a copper doped CdTe layer displayed a level at 0.35 eV above the valence band which was probably related to the copper impurity.

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CHAPTER 7

BULK SINGLE CRYSTAL CdTe/CdS SOLAR CELLS

7.1 Introduction

The CdS/CdTe heterojunction only holds promise as a low cost terrestrial solar cell in thin film form. Nevertheless, studies on bulk crystal cells are useful in obtaining a basic understanding of the junction properties, and of the effects of various material parameters, without the added complications of grain boundaries, etc. Thus, while not commercially viable devices, bulk crystal structures do serve as a guide to future thin film work.

Single crystal CdTe grown in our laboratory was generally highly resistive ($\rho \sim 10^8$ Ω-cm). Since the desirable value of bulk resistivity for solar cell fabrication is between 1-10-Ω-cm a number of techniques (Section 4.3) were employed to reduce the resistivity. A variety of dopants such as phosphorus, copper and tellurium were employed and will be discussed in Sections 7.2 and 7.3.

Low resistance ohmic contacts are essential for efficient solar cells. The choice of the contacting metal to make an ohmic contact to a semiconductor depends on its conductivity type and the work function. Ohmic contacts to n-CdS are relatively simple to make using In or Al. The problem is much more difficult with p-CdTe. High resistance contacts constitute one of the main losses in solar cells and thus the need to find a reliable, low resistance contact to the p-CdTe is of particular importance. Previously, other workers have used both Au and carbon as contacts and the relative merits of each have been investigated here and are discussed in Section 7.2.

The effects of heat treatment and substrate preparation on device performance have also been investigated and are described in Sections 7.4 and 7.5. Finally, minority carrier diffusion lengths were also measured in both Au and carbon-contact devices using the EBIC technique (Sect. 5.3.3.) and the results are related to device characteristics.

7.2 Comparison of Gold and Carbon Contacts

7.2.1 Introduction

In the past efforts to obtain low resistance contacts to p-type CdTe have been directed towards special etching treatments of the surface, the nature of the contacting metal and its mode of deposition[1]. As for the contact metals, the work functions of Cu, Au, Ag, Zn, In and Pb on p-CdTe have been determined and Au has been found to be the most favourable[2]. Since the pioneer work of de Nobel[3], gold has mainly been used to make ohmic contacts to p-CdTe, although platinum has a higher work function and low resistance ohmic contacts to P-doped low resistivity p-type CdTe have been obtained with platinum[4]. Ni has also been used successfuly[5], but unfortunately the resistance of contacts made with Ni, Au or Pt increase with time[6].

The use of carbon contacts in p-CdTe/n-CdS solar cells was first reported by Nakayama et al[7] in 1980. Using a screen printing technique they found that carbon contacts led to an efficient device with improved stability. Since then there have been many reports of carbon contacts in both thin film[8-13] and bulk crystal devices[14].

In this study both gold and carbon were used to make ohmic contacts to p-CdTe. In this Section a comparison of the performance of these contacts is made using P-doped substrates which gave most efficient devices.

7.2.2. Experimental Details

In an attempt to investigate the effects of Au and C contacts, p-CdTe/n-CdS heterojunctions were first fabricated on P-doped CdTe substrates. CdTe slices 2mm in thickness were cut from bulk single crystal boules and pad polished as described in Section 4.4.2. The polished samples were doped with phosphorus by heating them at $\sim$ 550°C in a stream of argon containing orthophosphoric acid vapour (Section 4.3.3.), and then annealing in Te vapour (Section 4.3.1). After that the phosphorus doped substrates were polished, and a CdS layer about 10 μm thick was vacuum deposited to fabricate a p-CdTe/n-CdS heterojunction.

Indium was deposited by vacuum evaporation to make contacts to the n-CdS. Contacts to the p-CdTe were obtained by vacuum evaporation of gold (typically 3mm dia.) or by painting a small quantity of C paste (Aquadag) as described in Section 4.6.1. The C contacts were annealed in a N_2 ambient for $\sim$ 30 mins at $\sim$ 300°C.

7.2.3 Device Characterization

The diode characteristics of the solar cells fabricated on P-doped substrates with both Au and C contacts are shown in Figs 7.1a and 7.1b. The diode characteristics were fairly rectifying for both types of device, although with Au there was a higher series resistance. Also, the ideality factor A was greater than two, resulting from the polycrystalline nature of the CdS layer. The value of the reverse saturation current J_o for the Au and C-contact devices was $\sim 3 \times 10^{-7}$ and 10^{-7} A/cm^2 respectively. A rectification ratio of 3.6×10^3 at 0.8V was measured for the C-contact cells in comparison with $\sim 5 \times 10^2$ for the Au-contact cells at the same bias voltage.

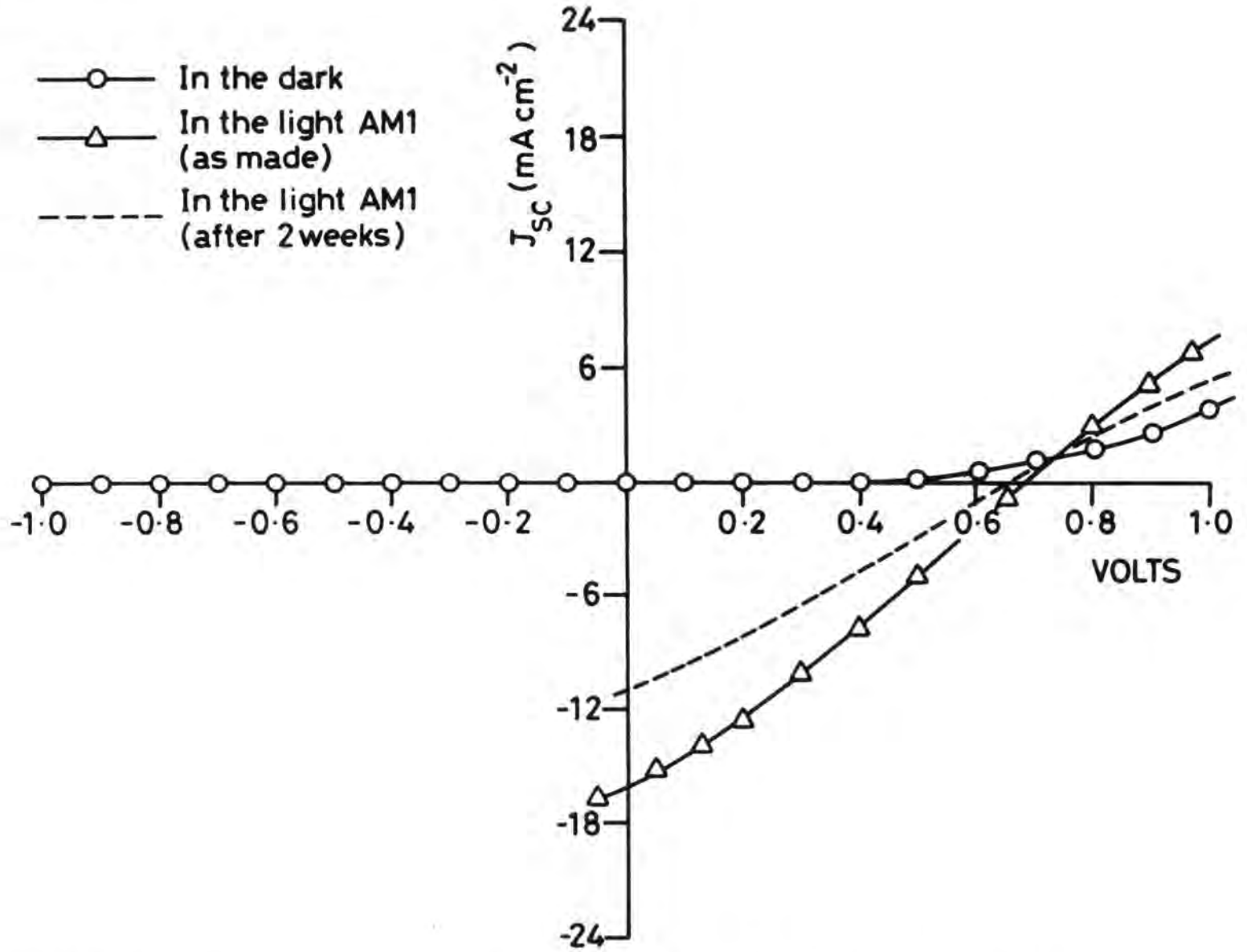

Fig. 7.1 (a) Current-voltage characteristics for a device with an Au contact to p-CdTe

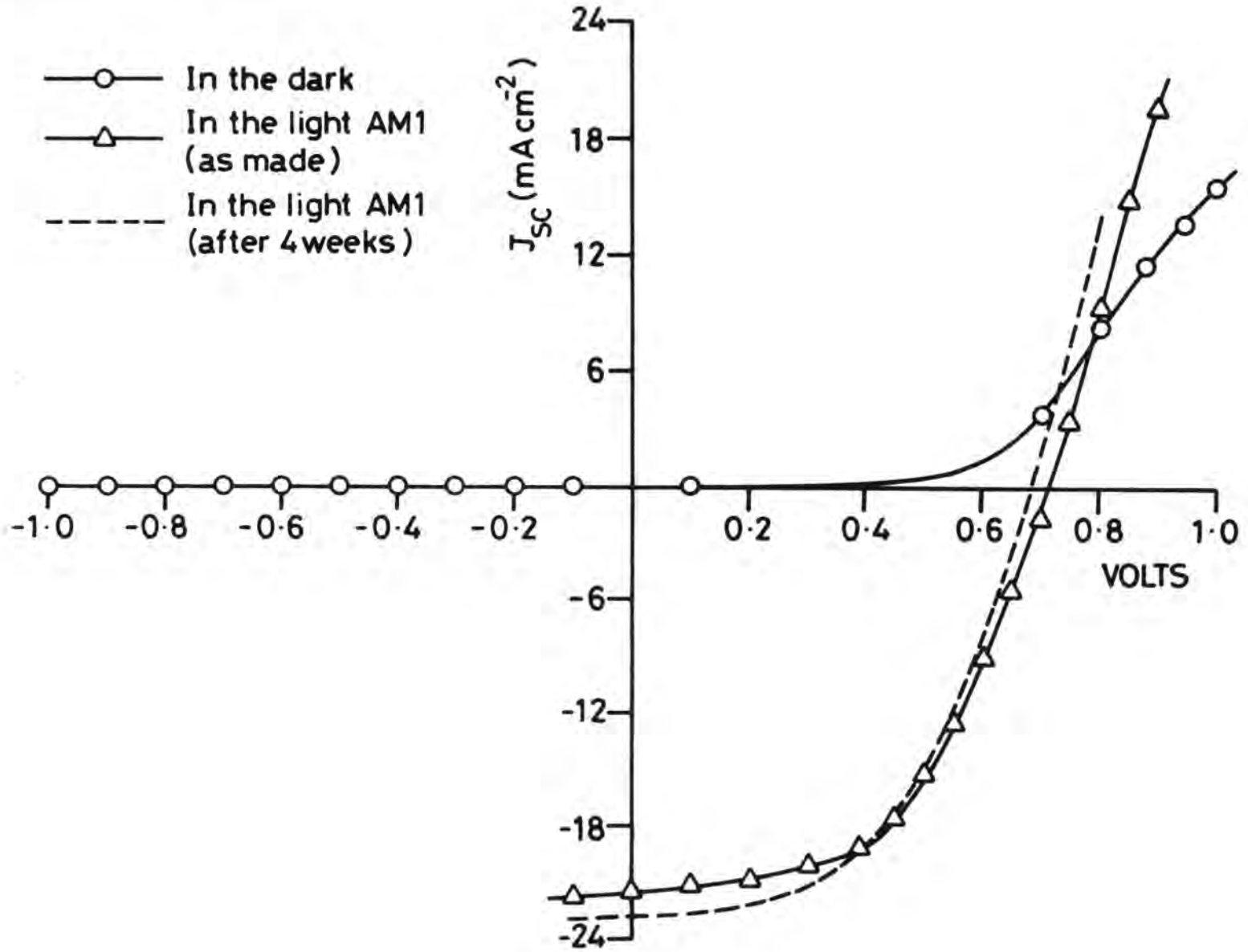

Fig. 7.1 (b) Current-voltage characteristics for a C-contact device

The photovoltaic output characteristics, for the cells were measured under AM1 illumination and are shown in Figs 7.1a and 7.1b. The values of SCC, OCV, FF and efficiency η are listed in Table 7.1.

TABLE 7.1: Cell parameters with Au and C contacts.

Device	OCV	FF	SCC	η
	volts	(%)	mA/cm^2	%
C-contact	0.72	47	21.00	7.20
Au-Contact	0.69	29	15.85	3.10

The carbon contact device exhibits a relatively low series resistance, giving a better fill factor, and hence a higher efficiency (7.2%). The higher series resistance of the Au-contact devices could have arisen both from the substrate and/or the contact resistivity, but since the substrates for both types of device were nominally identical, it would seem reasonable to believe that the higher series resistance resulted from the contact, and is responsible for the poor efficiency in these cells. A slight bending of the photovoltaic characteristic of the Au device towards the voltage axis in the first quadrant (Fig 7.1a) is indicative of the non-ohmic behaviour of the contacts and supports the above mentioned idea. Significantly, there is no such bending of the characteristic for the C-contact devices. However, the fill factor (47%) in the carbon contact devices is still low in an absolute sense. This is probably the result of the relatively high substrate resistivity ($\rho \sim 125$ Ω-cm).

Both types of device also displayed a cross-over effect between the dark and illuminated current-voltage characteristics. A similar effect has been observed in $Cu_2Te/CdTe$[15] and Cu_2S/CdS[16-18] cells. This is generally attributed to photoconductive behaviour as described in Chapter 9, and is often associated with the presence of sensitizing impurities[14].

In order to investigate the effect of contacts on the spectral sensitivity of the devices the spectral responses of their OCVs and SCCs were measured at room temperature, see Figs 7.2a and 7.2b respectively. In both cells, the threshold for OCV starts at a photon energy of ∿ 1.2 eV and peaks at about 1.5 eV. The OCV response for the C-contact cells was larger and broader than that for the Au cells. The increased response of the C-contact cells is more pronounced for the SCC (Fig.7.2b).

The characteristics of devices that had been stored in the laboratory for up to four weeks were also measured, and are also included in Figs 7.1a and 7.1b. Devices with C-contacts proved to be more stable than their counterparts with Au-contacts, showing essentially no degradation after storage for four weeks. In fact the SCC improved slightly. In contrast the performance of the cells with Au-contacts was found to have severely degraded after only two weeks.

Importantly, very similar values of V_{oc} were measured for both types of device and did not show any pronounced change with time even in Au devices. The V_{oc} is mainly affected by the junction between the CdS and the CdTe rather than by contact effects[14]. Thus the fact that the V_{oc} did not change with the contacts suggests that the actual heterojunctions were similar, and implies that the degradation effects observed in the Au cells were related to the contact degradation. Moreover, the decrease in the fill factor with ageing in these cells also implies an increase in the contact resistivity with time.

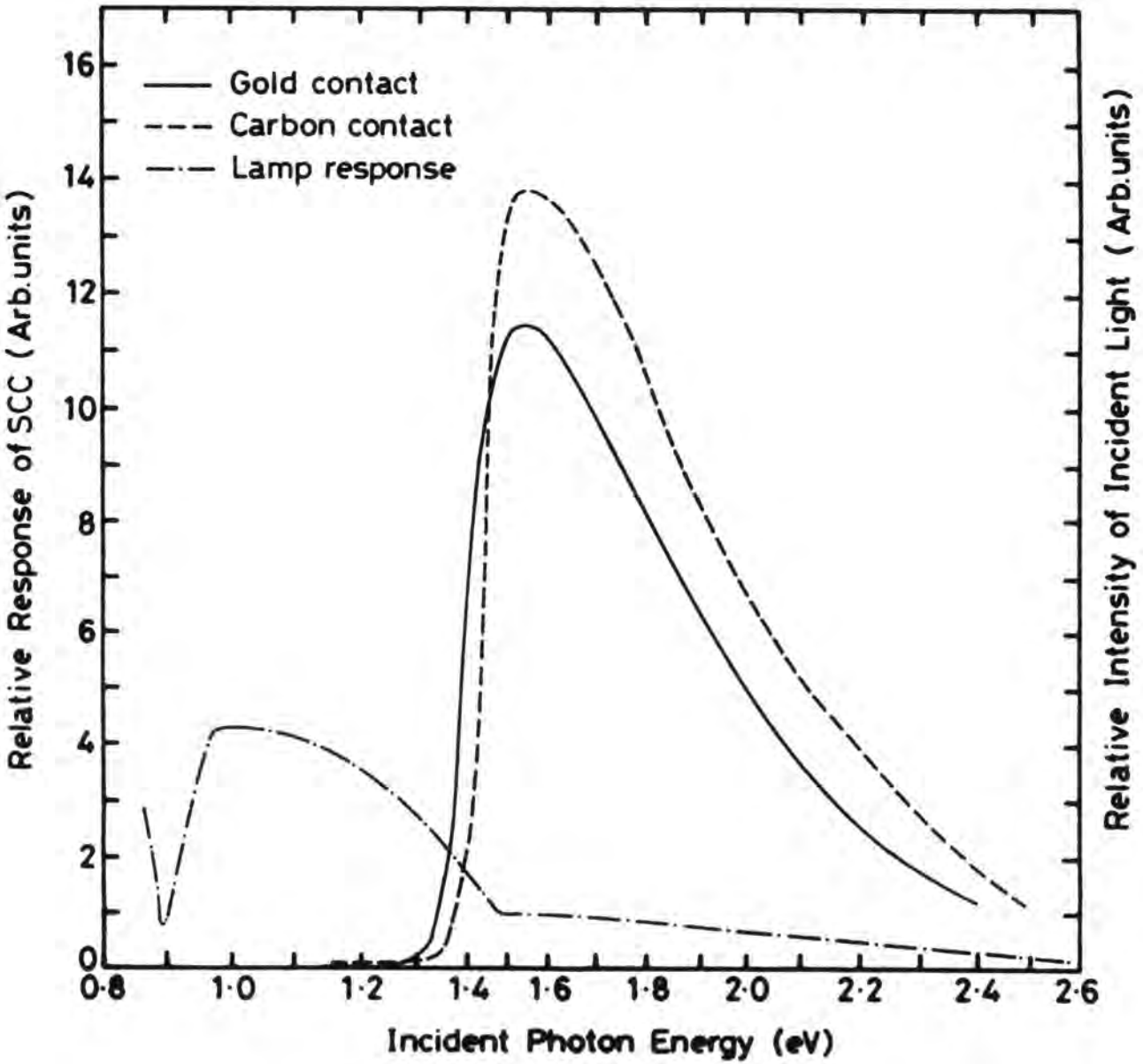

Fig. 7.2 (a) :The effect of Au and C contacts on the SCC spectral response of bulks CdTe/Cds cells.

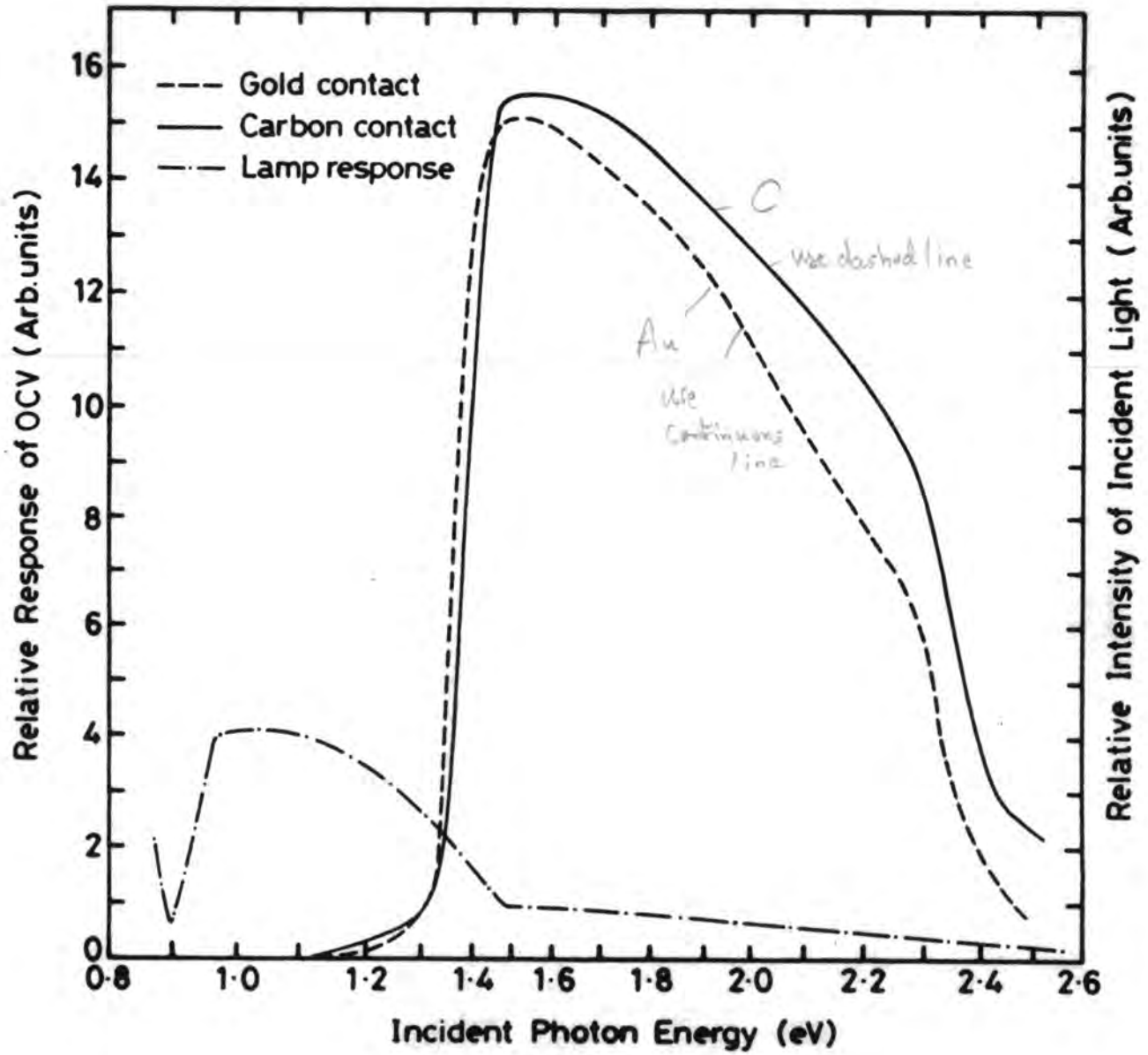

Fig. 7.2(b) : Open circuit voltage spectral responses of solar cells with Au and C contacts

7.2.4 Discussion

Gold contacts were found to be inferior to the carbon contacts. Solar cells with Au contacts had poor performance parameters as is evident from Table 7.1, particularly the low fill factor because of the high contact resistivity, and correspondingly a low efficiency. Moreover, these cells were unstable as compared to C-contact cells and this behaviour also resulted from the degradation of Au contacts.

According to the theory of ohmic contacts, a barrier free contact to a p-type semiconductor is obtained when the work function ϕ_m of the metal is greater than that of the semiconductor (i.e. $\phi_m > \phi_s$). An alternative possibility is to produce a tunneling contact through a Schottky barrier, and this in turn requires the ability to dope the surface of the semiconductor heavily under the contact[19]. The work function of gold is $\phi_{Au} \sim 5.1$ eV[20] and of p-type CdTe is ~ 5.9 eV[1]. Consequently, an accepted minimum value of ϕ_m should be about 5.9 eV to make an ohmic contact to p-CdTe. Thus the rectifying behaviour and high resistivity of Au contacts can be explained in terms of the mismatch between the work functions of the p-CdTe and Au.

Carbon contact devices were however, much more efficient and stable. Table 7.1 clearly shows the superior performance of these cells. Particularly noteworthy are the high (compared to Au devices)FF, and overall efficiency of 7.2% in contrast to 3.1% for the Au-contact cells.

It is possible that the heat treatment administered during carbon contact fabrication may have reduced the resistivity of the CdS layer, leading to an improvement in fill factor and hence efficiency, through a reduction in series resistance. However, this alone cannot explain the increase in the SCC and moreover, similar heat treatments of Au-contact devices did not improve performance to the same extent.

The work function of carbon is $\sim$ 5.05 eV[20] which is very close to that of Au. There is therefore no possibility that carbon will make a direct ohmic contact to p-CdTe and some other mechanism must be invoked to explain the ohmic nature of these contacts. The carbon paste (Aquadag) used to make the contacts contains many acceptor-like impurities including copper and lithium[11,21,22]. These may well diffuse into the p-CdTe surface during annealing. The CdTe surface could thus become comparatively heavily doped, reducing the width of the carbon-CdTe barrier with a corresponding reduction in contact resistance.

In addition, the annealing stage in contact formation could result in a pronounced acceptor impurity concentration gradient, leading in turn to a Back Surface Field (BSF) effect[23]. Hovel[23] has shown that the BSF effect may enhance both SCC and OCV since such cells have a very small recombination velocity at the back contact[24]. Silicon cells with improved parameters as a result of the introduction of BSF have been reported in the literature[24-26]. Further, the current collection efficiency of the cell may also be significantly improved, if the carrier diffusion is aided by the built-in electric field resulting from dopant concentration gradients[27]. A number of authors have considered this case theoretically[28-31] and silicon solar cells containing built-in fields have shown the expected increase in efficiency[23].

The fill factor in the C-CdTe cells was still low by normal standards. This was probably due to relatively high substrate resistivity. Paradoxically this would tend to increase the depletion region at the junction and hence the collection width, but would result in a lower value of OCV($\sim$ 0.7 V) than expected and a reduced fill factor as observed.

The charge carriers which establish a photovoltage across the p-n junction are generated mainly by absorption in the CdTe, and the direct transitions in CdTe are expected to dominate the spectrum. The bandgap of CdTe is $\sim$ 1.5 eV[7] at room temperature and thus the peak at about 1.5 eV for both the OCV and the SCC corresponds to the energy gap of CdTe. However, the response at photon-energies less than the energy gap can be explained in terms of impurities or defect states close to the valence band[27] and the effect of the junction field[32]. The improved spectral response in the C-contact devices may also result from the BSF effect and the built-in electric fields due to dopant concentration gradients.

The Au-contact devices degraded very quickly with time and this was related to the Au contact degradation. In the literature, it is reported that the resistance of Au contacts increases with time, and is possibly due to oxygen diffusion towards the interface[6]. Tyan et al[33] and Fahrenbruch et al[5] have also reported the instability of Au contacts on p-CdTe. In comparison, C-contact devices were more stable (with small increase in SCC which may have resulted from the indiffusion of acceptor impurities at room temperature).

7.3 Substrate Doping

7.3.1 Introduction

As already pointed out in Section 7.1, the as-grown CdTe crystals had a high resistivity and were slightly p-type, and hence were not suitable for the fabrication of solar devices without a further reduction in resistivity. Although the phosphorus doped substrates (Sect. 4.3.3.) were found to give the best results as shown in Section 7.2, other alternatives were also investigated in an attempt to find the best possible dopant to obtain optimum efficiency.

The different alternatives examined for the reduction of CdTe resistivity included copper and tellurium doping. On one occasion an as-grown crystal of CdTe was found to have a low p-type resistivity, for unknown reasons (possibly accidental contamination). This was also investigated as a substrate material and the results are given in Section 7.3.2. The details of the tellurium and copper doping procedures are outlined in Sections 4.3.1 and 4.3.2. The photovoltaic devices fabricated on copper and tellurium doped substrates are described in Sections 7.3.3 and 7.3.4, and discussed together with the p-doped and nominally undoped CdTe devices in Section 7.3.5.

7.3.2 Nominally Undoped Substrates

Generally the as-grown CdTe was highly resistive but unusually one boule (BA36) had a low as-grown resistivity ($\sim$ 250-350 Ω-cm). This boule like others was not intentionally doped. It was used to fabricate n-CdS/p-CdTe heterojunctions without further doping. The CdTe substrates were cut and polished (Section 4.4); and a CdS layer was deposited. Both Au and C were used to make ohmic contacts to the p-CdTe.

The diode characteristics of two typical solar cells, one with Au contact (device A) and the other with carbon contact (device B) are shown in Figure 7.3. The diode characteristic of a third device(C) is also included. This cell differed from device A in that the CdTe surface was slightly doped with copper before the Au was evaporated. As with their P-doped counterparts the Au-contact cells had higher series resistances than C-contact devices. The value of the ideality factor A in these devices was measured to be $\sim$2. As with the C-contact cells described in Section 7.2, the rectification ratio at 0.8V for

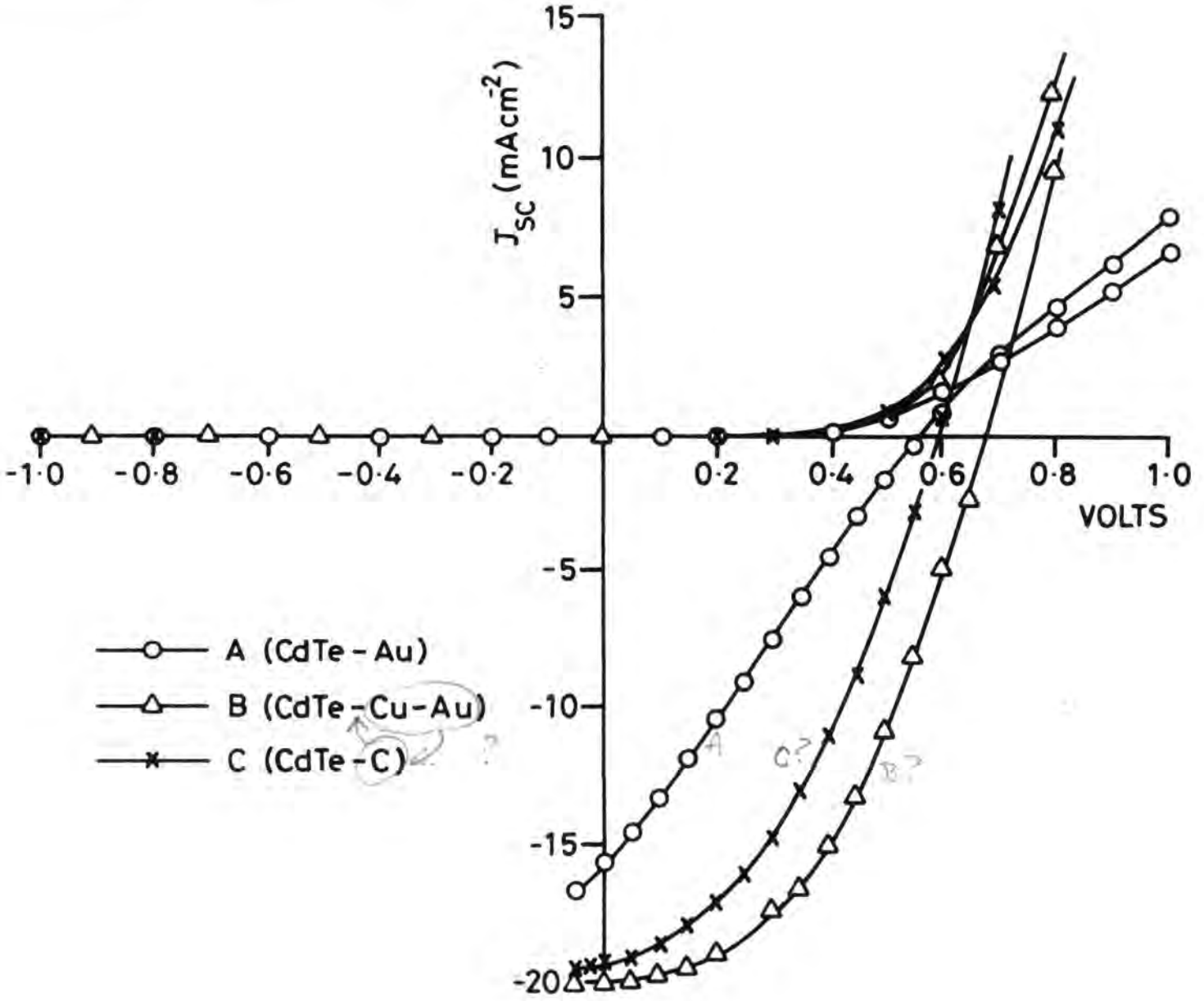

Fig. 7.3 : I-V characteristics for solar cells fabricated on nominally undoped CdTe substrates

device B was $\sim 2.3 \times 10^{3}$ whereas for the other devices (A and C) it was a few hundred. The reverse saturation currents for devices A, B and C were $\sim 3 \times 10^{-7}$, 6×10^{-8} and 2×10^{-7} mA cm^{-2} respectively.

The photovoltaic output characteristics for these devices are also shown in Fig.7.3. The values of the SCC, OCV, FF and η are given in Table 7.2. The output characteristic for device A bends towards the voltage axis in the first quadrant, indicating a rectifying (non-ohmic) action at the Au-CdTe contact as discussed in Section 7.2.3. Such behaviour was not observed in devices B and C. The Au-contact device (A) also showed a higher series resistance.

TABLE 7.2: Parameters of devices formed on different substrates using Au and C contacts.

Device	OCV volts	FF (%)	SCC mA cm^{-2}	η %
P-doped-C	0.72	47	21.00	7.20
P-doped-Au	0.69	29	15.85	3.10
Undoped-C	0.69	42	19.85	5.98
Undoped-Cu-Au	0.6	38	18.49	4.15
Undoped-Au	0.57	25	15.60	2.25
Cu-doped-C	0.56	31	7.12	1.24
Cu-doped-Au	0.49	25	4.46	0.54
Te-doped-Au	0.53	23	3.90	0.36

The improvement in device B again appears to result from the use of carbon contacts as discussed in Section 7.2.4. With the device C, the improved contact behaviour, and consequently higher efficiency (than device A) was probably because of the surface doping with Cu that provided a p^+ region under the Au contact. Although the improved contacts in these devices (B & C) led to higher values of their parameters, they still have low fill factors resulting from high series resistance. This is the result of the substrate resistivity.

7.3.3 Copper Doped Substrates

The CdTe dice were doped with different concentrations (100, 500, 1000, 1500, 2000 ppm) of copper as described in Section 4.3.2. The optimum value of copper concentration was found to be 1000 ppm to give a resistivity of $\sim$ 300-450 Ω-cm. The CdS/CdTe cells were then fabricated on substrates doped with 1000 ppm concentration of copper. Evaporated Au and carbon paste were used as contacts to the p-CdTe substrates as previously.

The diode characteristics were however, poor with poor rectification ratios at 0.5 V of 6 and 16 and high reverse saturation currents $\sim 10^{-5}$ and 10^{-6} mA cm^{-2} respectively for Au and C-contact devices. The photovoltaic output characteristics of typical devices are shown in Fig. 7.4. The performance parameters are also given in Table 7.2. The cell parameter for the C-contact device although better than the Au-CdTe devices, were much lower than for the nominally undoped and P-doped devices with either C or Au contacts. The better performance of C-contact devices is again presumably due to the lower resistivie contact. However, with these cells the dominant effects seem to have arisen from the Cu-doping.

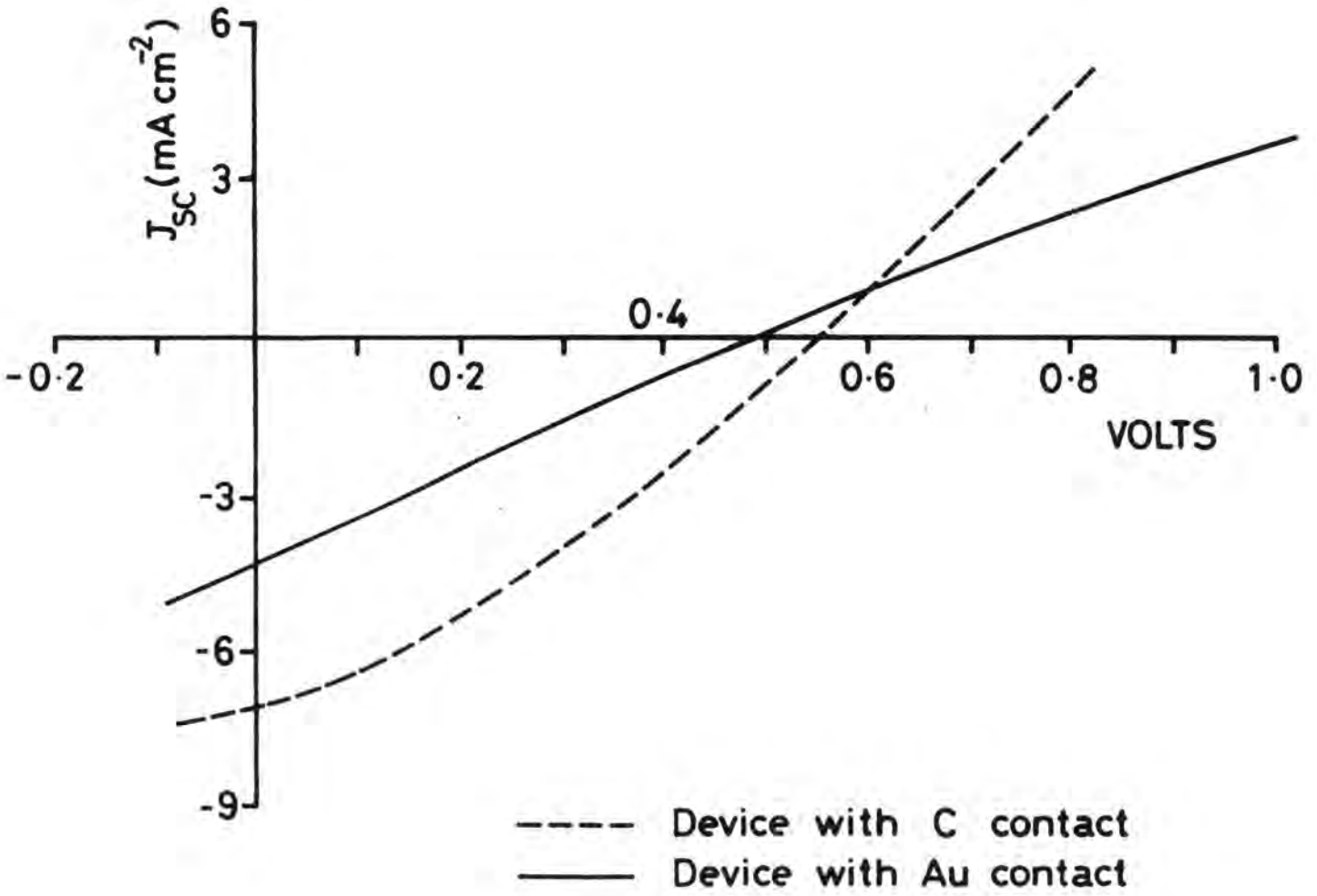

Fig. 7.4 : Photovoltaic output characteristics of devices with Cu-doped CdTe substrate (with different contacts)

7.3.4 Tellurium Doped Substrates

The properties of Te-doped CdTe substrates were investigated in CdS/CdTe heterojunctions with Au contacts only, but the results are sufficient to show the behaviour of these substrates. The as-grown CdTe dice were annealed in Te vapour at $\sim$ 550°C for one week, to reduce their resistivity to $\sim$ 700-800 Ω-cm. The dice were processed to produce n-CdS/p-CdTe solar cells with evaporated indium and gold contacts.

As with the Cu doped heterojunctions, the diode characteristics were very poor with a rectification ratio at 0.5V of $\sim$ 4 and reverse saturation current of $\sim 3 \times 10^{-5}$ mA cm^{-2}. The photovoltaic output characteristic for a typical device is shown in Fig.7.5. The values of SCC, OCV, FF and η presented in Table 7.2 are, except for the OCV, the lowest of all devices with Au contacts. The gold contact appears to be non-ohmic as indicated from the output curve. The series resistance of the device was also high as evidenced by the low FF of 23%. Attempts to improve ρ with Te annealing were not successful. It was concluded that this was not a good procedure for controlling substrate resistivity.

7.3.5 Discussion

The device parameters for the different types of bulk crystal substrate cells are summarized in Table 7.2 for ease of comparison. The P-doped substrates gave the most efficient device while Cu-doping and Te-annealing were unable to produce low resistivity CdTe. Devices fabricated on the nominally undoped substrates were reasonably efficient, particularly with C-contacts but the reasons for such behaviour of these undoped substrates are not known.

In spite of the high level of Cu doping, the resistivity of the CdTe was still rather high and would have contributed towards series

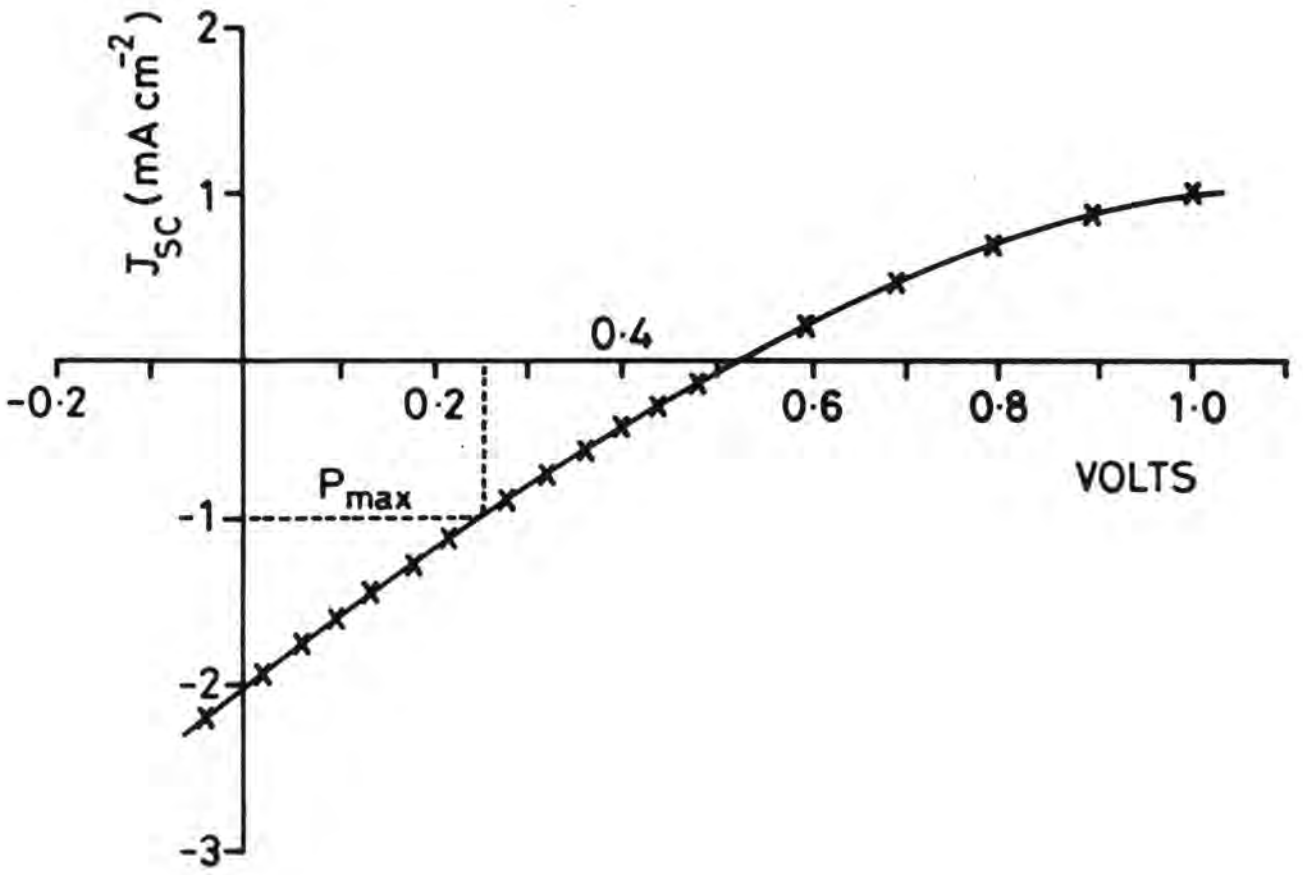

Fig. 7.5 : Typical photovoltaic characteristic of a device fabricated on a Te-annealed substrate (Au Contact)

resistance as well. This could have resulted from the amphoteric character of Cu in CdTe[6]. Normally, like Au, copper acts as an acceptor impurity in CdTe but in high concentrations it also forms interstitial donors and so acts as compensating centre[34].

Annealing CdTe at elevated temperatures under fixed partial pressures of its elements (Cd or Te) can modify the defect structure of the material[3,35]. As discussed in Chapter 6, energy levels found at the middle of the bandgap of CdTe may be due either to impurities or they can arise directly from the annealing processes. Similar annealing procedures have been found to produce sub-grain boundaries in CdS, which have subsequently been associated with deep levels[36,37]. It has also been shown in CdTe that dislocation polygonization produces sub-grain boundaries[38] and it is possible that Te annealing process could, in analogy with CdS, produce additional deep levels. These localized levels can act as recombination centres and strongly reduce carrier lifetimes and consequently affect device performance.

To conclude the P-doping was the most efficient procedure to produce low resistivity CdTe substrates for fabrication of efficient solar cells, whereas Cu and Te doping were unsatisfactory for reducing the CdTe resistivity.

7.4 Effect of Heat Treatment on Contacts

7.4.1 Heat Treatment of Carbon Contacts

The carbon contacts were made by applying carbon paste onto the CdTe substrates and then heating them in a nitrogen ambient. Initially, this heat treatment was found to produce variable results and it was therefore necessary to optimize the annealing conditions. A set of cells were fabricated with carbon paste contacts using nominally undoped CdTe substrates and then annealing at temperatures of $\sim$ 250, 300 and 350°C for about 30 mins in a nitrogen ambient.

The photovoltaic characteristics of the devices were measured under AM1 illumination and the output characteristics of three typical devices heat treated at 250, 300 and 350°C are recorded in Fig.7.6. Values of SCC, OCV, FF and η are listed in Table 7.3.

TABLE 7.3: Parameters of devices heated at different temperatures

Annealing Temp. (°C)	OCV (volts)	SCC mA cm^{-2}	FF (%)	η (%)
250	0.58	18.75	28	3.00
300	0.57	19.39	33	3.61
350	0.59	16.10	24	2.32

Although the OCV was almost unaffected by the heat treatment, FF, SCC and η were, with the highest values being obtained for devices heated at 300°C. Devices annealed at 350°C had contacts that displayed non-ohmic behaviour as indicated by the shape of the characteristic in the first quadrant. For devices heated at 250°C the contact remained ohmic but was more resistive than for cells treated at 300°C.

The carbon paste used for the fabrication of a contact, acts not only as a positive electrode for the solar cell but also as a source of acceptor impurities for CdTe. The paste is thought to contain traces of group I and V elements[11,21,22] such as Cu and P. Heat treatment at 250°C was probably insufficient to cause the impurities to diffuse into CdTe. This resulted in a relatively high series resistance and consequently low fill factor. At the higher annealing temperature of 300°C the impurities diffuse more readily into the CdTe producing the

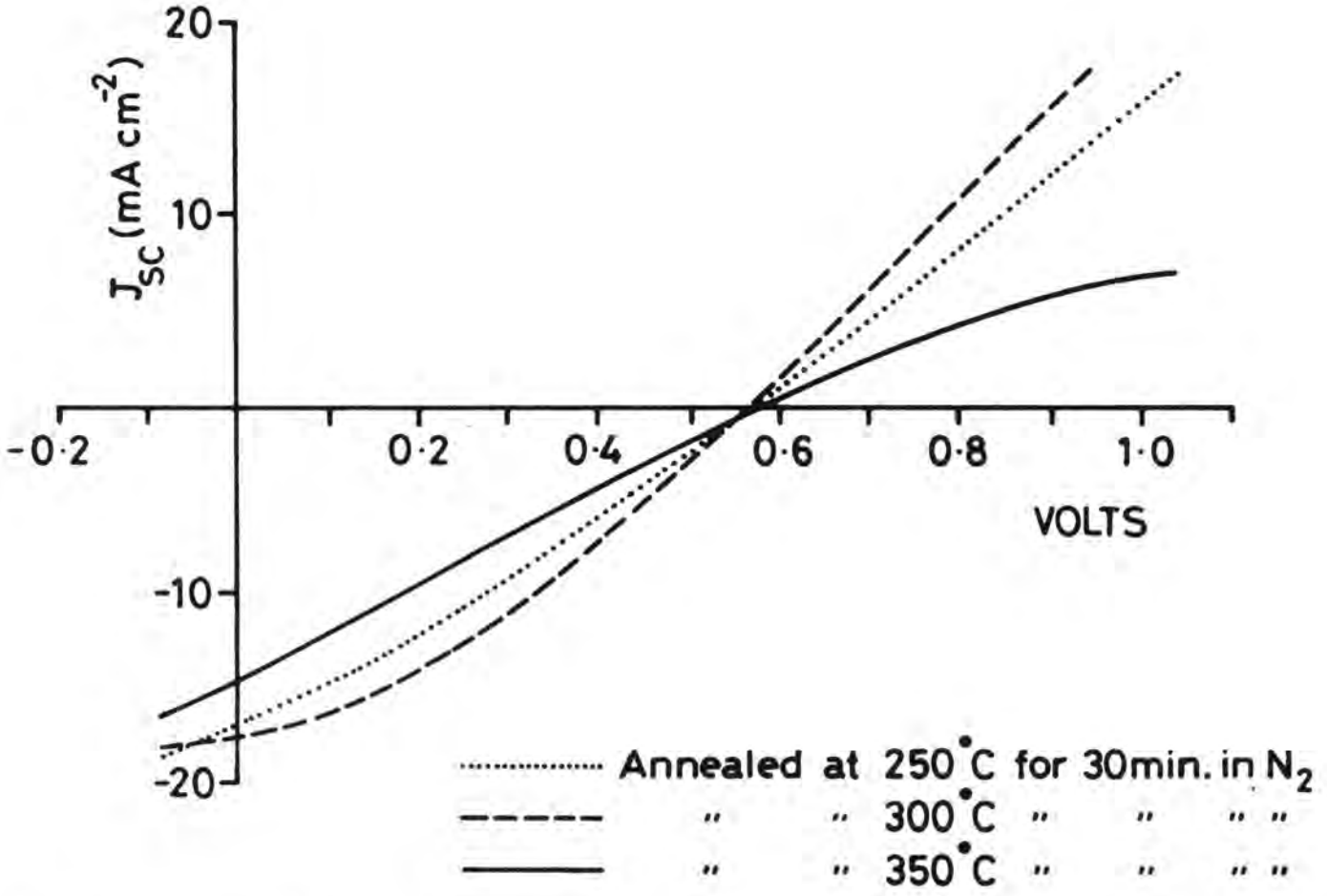

Fig. 7.6 : Photovoltaic characteristics of devices with C contacts and annealed at different temperatures

desired highly doped region below the contact. The rectifying behaviour of contacts heated at 350°C may have resulted from a net reduction of the acceptor doping in the CdTe surface as the impurities diffused more deeply into the substrate. Alternately, it may be the result of compensation effects in the CdTe.

7.4.2 Effect of Heat Treatment on Au Contacts

Although Au has been widely used as a contact it was found (Section 7.2) that an evaporated layer of gold did not produce a low resistance ohmic contact to p-CdTe. It was also observed that an annealing process was essential in obtaining ohmic contacts between carbon and CdTe. Moreover, it has also been reported that low resistance Au contacts to CdTe substrates can be produced after firing at 200°C in a hydrogen ambient[39]. It was therefore, necessary to investigate the effects of annealing on Au contacts. Devices were fabricated as usual, and evaporated gold contacts were applied to the p-CdTe. The device was characterized and then heat treated in an Ar ambient for 7-15 mins at 180°C.

Figure 7.7 shows the photovoltaic characteristics of the device after heating for periods of 7, 10 and 15 mins together with the characteristic of the as-made device. It is evident that the SCC and fill factor improved after heating from 7 to 10 minutes but thereafter began to degrade. The shape of the graph in the first quadrant also shows the effect of heating on the nature of the contacts. After 10 mins heat treatment the contact was ohmic if still resistive, and there was a significant improvement in the SCC. However, after 15 mins the

characteristic indicates non-ohmic behaviour and the SCC was reduced nearly to its original value. The values of the SCC, OCV, FF and η are shown in Table 7.4.

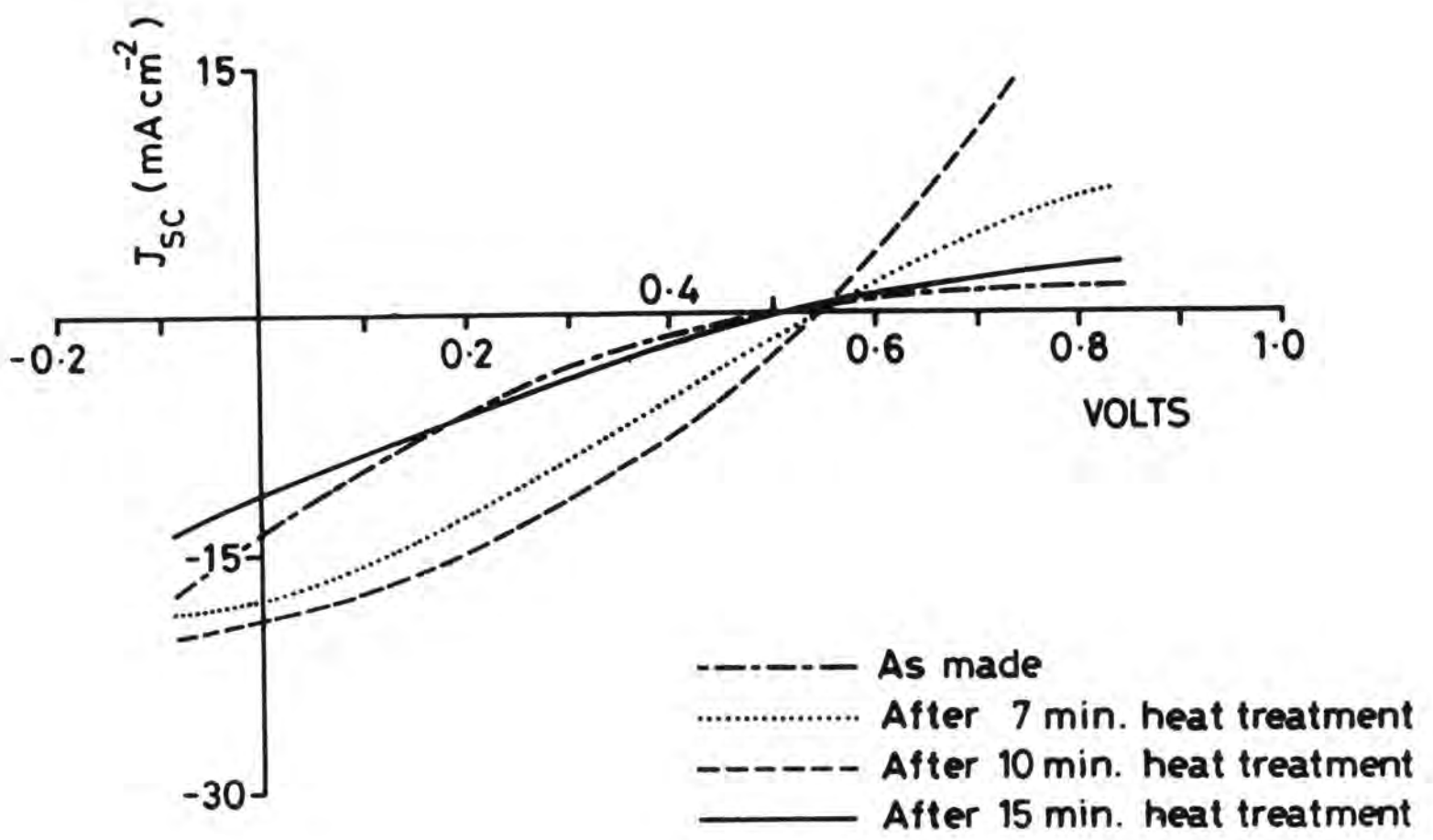

Fig. 7.7 : Effect of annealing time on PV characteristics of a device with Au contacts

TABLE 7.4: Parameters of a device heat treated for different time periods

Heat Treatment	OCV volts	SCC mA cm^{-2}	FF (%)	η (%)
As-made	0.54	12.87	18	1.23
7 mins	0.55	16.78	28	2.64
10 mins	0.55	18.10	34	3.30
15 mins	0.53	10.61	22	1.25

In his early work, de Nobel[3], used $AuCl_3$ to make ohmic contacts to p-CdTe. Cd^{++} ions were believed to trasnfer to the $AuCl_3$ solution leaving behind a tellurium layer on the CdTe surface, and in order to maintain the neutrality of the material Au atoms precipitate onto this layer forming a Te-CdTe Schottky barrier[6]. This model is supported by RBS measurements[40] and by atomic absorption analysis of the gold chloride solution after reaction with CdTe[41].

Structural studies of these contcts on p-CdTe revealed[41] that, in addition to the model proposed by de Nobel, gold diffused into the semiconductor and introduced dopant sites which were responsible for the increase in current through a tunneling mechanism when compared to a simple Au or Te surface barrier. Arienzo[42] has also shown that the resistivity of the as-made $AuCl_3$ contacts was very high but heat treatment in $Ar-H_2$(85 + 15)percent mixture for 15 mins at 425°C produced lower resistance contacts. The effect of the heat treatment in our devices can be explained in terms of the observations made on $AuCl_3$ contacts.

The work function of gold ϕ_{Au} = 5.1 eV[20] is not well matched to that of p-CdTe for the direct formation of ohmic contacts. The Au-CdTe contact therefore appears to function through a Schottky barrier tunneling process and the barrier height may be reduced by producing a heavily doped layer under the metal contact. This has been produced in the form of an excess tellurium layer by etching in bichromate solution[5] and by implantation of As^+ ions onto the CdTe surface[43]. The contact between a stoichiometric CdTe surface and Au will have a high barrier height. Moreover, gold has a low doping efficiency as an acceptor in CdTe[44] and therefore does not give a large tunneling effect.

In the present study when the samples were annealed for 7-10 mins at 180°C, gold diffused into the CdTe to produce a more highly doped surface under the metal contact and consequently improved the tunneling effect in a manner similar to the C contacts. It is also possible that Cd^{++} ions left the CdTe surface during heating, leaving behind excess tellurium as with the electroless gold contact with a consequent reduction of the barrier height. A second possibility is that a thin layer of Te may be left on the CdTe surface after the Br-Methanol polish (Sect.4.4) and this could well diffuse during heating to give a better contact.

It would seem that the optimum heat treatment results in the diffusion of Au and/or Te into the CdTe creating a p^+ layer between the Au and the CdTe. The conduction would therefore be through a narrow Schottky barrier. However, heat treatment for longer times would be expected to cause the Te/Au to diffuse more deeply, effectively reducing the concentration under the contact and so leading to a reduction in the

tunneling. The results suggest that extending the heat treatment to 15 mins is sufficient to prevent any significant tunneling effect and the contact returns to its initial non-ohmic state.

It is also possible that with excessive heating a solid-solid reaction between Au and CdTe takes place to form gold telluride. This could not be expected to form an ohmic contact.

These studies suggest that annealing of Au-p-CdTe contacts at 180°C in an Ar ambient for 7-10 mins gives improved contacts but the carbon contacts are much better than Au contacts.

7.5 Substrate Preparation

7.5.1 Introduction

Surface preparation strongly influences the properties of layers used to form heterojunctions and often governs the interface properties of a metal/semiconductor junction[45]. When substrates are cut from bulk crystals the surfaces of the substrates suffer severe saw damage. This has to be removed in some way, often entailing mechanical lapping followed by chemical etching. However, the amount of material removed during the chemical polish stages should be minimized in order to maintain uniformity since preferential etching along particular directions will lead to an uneven surface in a prolonged process[46].

The choice of an effective method should provide a means for the supply of fresh etching solution to the surface, remove the residue effectively and prevent the formation of any unwanted surface layer. CdS/CdTe heterojunctions often suffer from reduced open circuit voltage as a result, it is thought, of recombination at interfacial defects[47]. So, a primary aim of any polishing technique for CdTe substrate preparation must be the preservation of the crystalline properties of the bulk material without the introduction of any additional defects as

a consequence of the preparational procedures. Different polishing techniques were studied during the course of the present work and their influence on surface structure and device performance was investigated.

7.5.2 Structural Studies

Following orientation by the Laue X-ray back reflection technique, bulk crystals were cut into wafers using a diamond saw. They were then polished in one of the following ways (Section 4.4.).

(1) Alumina polish: Substrates were mechanically lapped using a paste of alumina powder (particle size 1-0.05 μm) in water on Buehler (TM) nylon polishing cloth to remove saw damage. The samples were washed in deionized water and then immersed in 2% Br-Methanol solution for various periods of time before a final rinsing in methanol.

This process gave a shiny and highly reflective surface, but RHEED studies revealed the presence of some deposit on the surface. A RHEED diffraction pattern taken from a CdTe substrate polished in 2% Br in methanol solution for two minutes is shown in Fig 7.8a. This contains a set of continuous and "spotty" rings which are indicative of a polycrystalline surface layer on the single crystal substrate. An analysis of the rings is presented in Table 7.5 and they were found to be related to both alumina and CdTe. It seemed therefore that alumina particles became embedded in the surface during the lapping process and were not removed during a 2 minute chemical etch. Increasing the etch time reduced the intensity of the rings in the diffraction pattern but did not eliminate them. Fig 7.8b shows a diffraction pattern taken from a sample etched for 10 minutes following polishing with alumina. A quantitative analysis of the pattern is given in Table 7.6. It is obvious (Fig 7.8b) that even after etching for 10 minutes

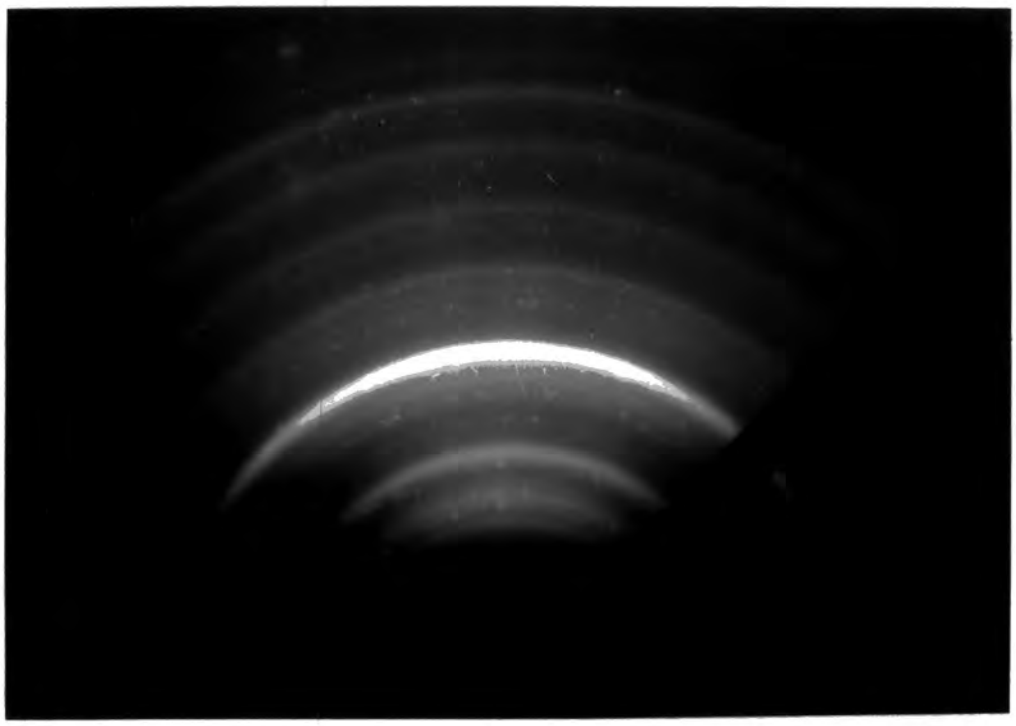

Fig. 7.8(a) : RHEED pattern from an alumina-polished CdTe surface after 2 mins. Br/methanol polish.

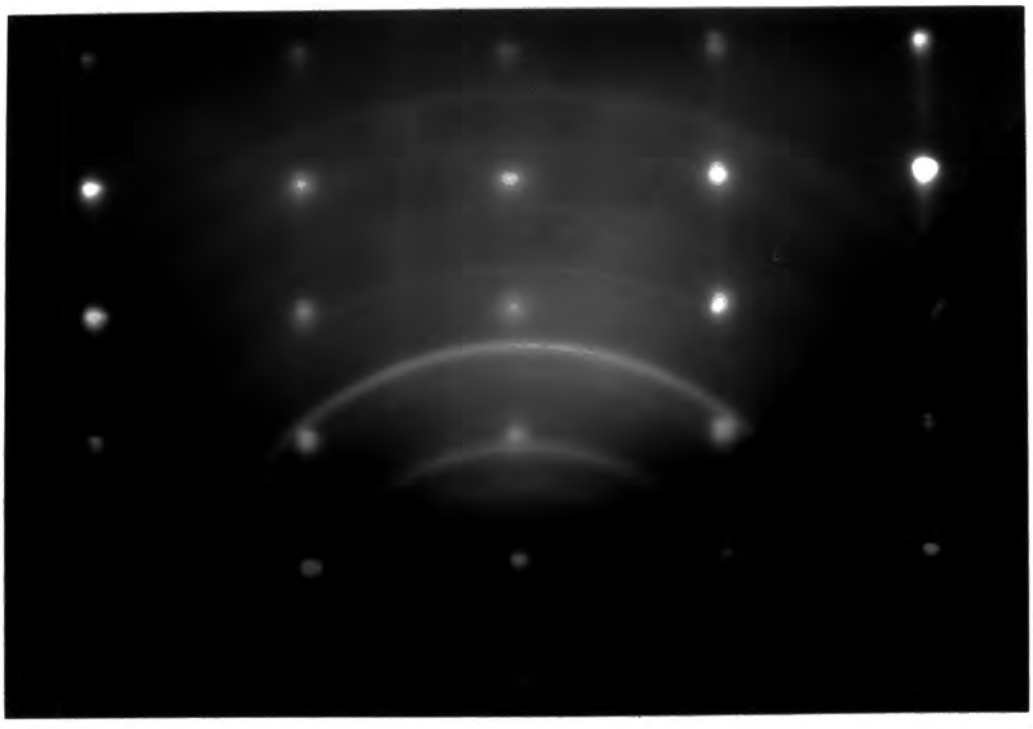

Fig. 7.8(b) : RHEED pattern from an alumina-polished CdTe surface after polishing in Br/methanol solution for 10 minutes.

TABLE 7.5: Indexing of a RHEED pattern from a single crystal CdTe substrate polished for two minutes

EXPERIMENTAL DATA			ASTM DATA			
			α -Alumina		CdTe	
Radius of Diff.rings (cm)	Estimated relative intensity	Measured interplanar spacing Å	Interplanar spacing Å	Relative Intensity %	Interplanar spacing Å	Relative Intensity %
3.1	spotty	2.50	2.55	90		
3.8	"	2.04	2.08	100		
4.0	very strong	1.94			1.954	30
4.55	spotty	1.70	1.74	45		
4.95	"	1.57	1.60	80	1.619	6
5.20	weak	1.49			1.488	10
5.70	very strong	1.36	1.37	50		
6.40	spotty	1.21	1.23	22		
6.70	medium	1.16				
7.70	spotty	1.01				

* Note that only the more intense lines from the ASTM data of both materials are included.

TABLE 7.6: Indexing of a RHEED pattern from a CdTe substrate polished for ten minutes

EXPERIMENTAL DATA			ASTM DATA			
			α -Alumina		CdTe	
Radius of Diff.ring (cm)	Estimated relative intensity	Interplanar spacing Å	Interplanar spacing Å	Relative Intensity %	Interplanar spacing Å	Relative Intensity %
2.50	medium	2.38	2.379	40		
2.60	weak	2.28			2.29	60
2.95	very strong	2.01	2.085	100		
3.75	weak	1.58	1.601	80		
4.20	very strong	1.41	1.404	30		

* Note that only the more intense lines from the ASTM data of both materials are included.

polycrystalline rings were still present, though weaker, indicating that reduced polishing damage still remained. Careful examination and analysis (Table 7.6) also showed that the "spotty" rings were also still present, showing that the alumina particles had not been removed.

When these samples were further etched in HNO_3 a thick grey deposit appeared on the surface. This was not analysed but was believed to be some compound of alumina with nitric acid. It thus became apparent that a procedure entailing the use of alumina powder was not capable of producing satisfactory surfaces.

(2) Cerium oxide pad polish: The alumina paste was replaced by a cerium oxide slurry and samples were then lapped, and chemically polished in 2% Br in methanol solution as before. RHEED analysis revealed a different ring pattern from that with alumina polished samples. Fig 7.9a shows such a diffraction pattern from a sample chemically etched for 4 minutes. It is probable that the rings resulted from a combination of reduced surface damage and possibly, the presence of a cerium oxide layer on the surface. As with alumina, it was observed that increasing the chemical polishing time reduced the intensity of the rings but they were not totally removed in about 15 min polishing.

(3) Pad polish: With this method samples were first briefly lapped on 600 grade SiC paper to remove the worst of the saw damage. The samples were then washed in deionized water and polished by the Pad Polish technique as described in Section 4.4.2, using a 2% solution of Br in methanol. The samples were then studied by RHEED in the usual way.

The diffraction pattern of a pad polished sample in Fig 7.9b shows an ordered spot pattern typical of sphalerite CdTe. Kikuchi lines were

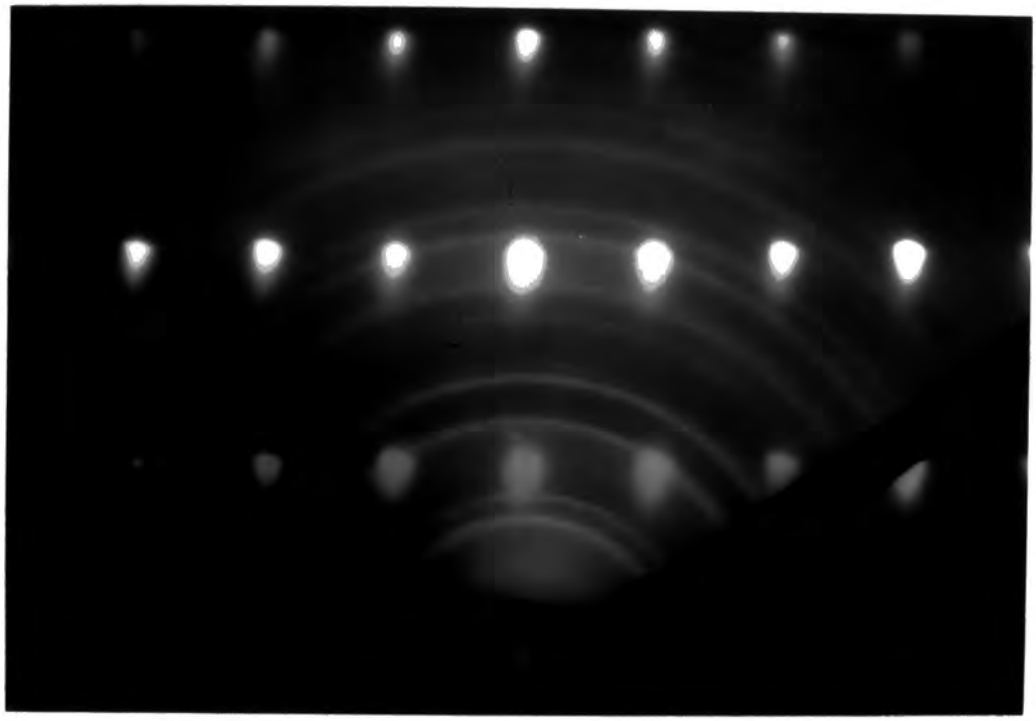

Fig. 7.9(a) : RHEED pattern from a cerium oxide polished CdTe surface after 4 mins Br/methanol polish.

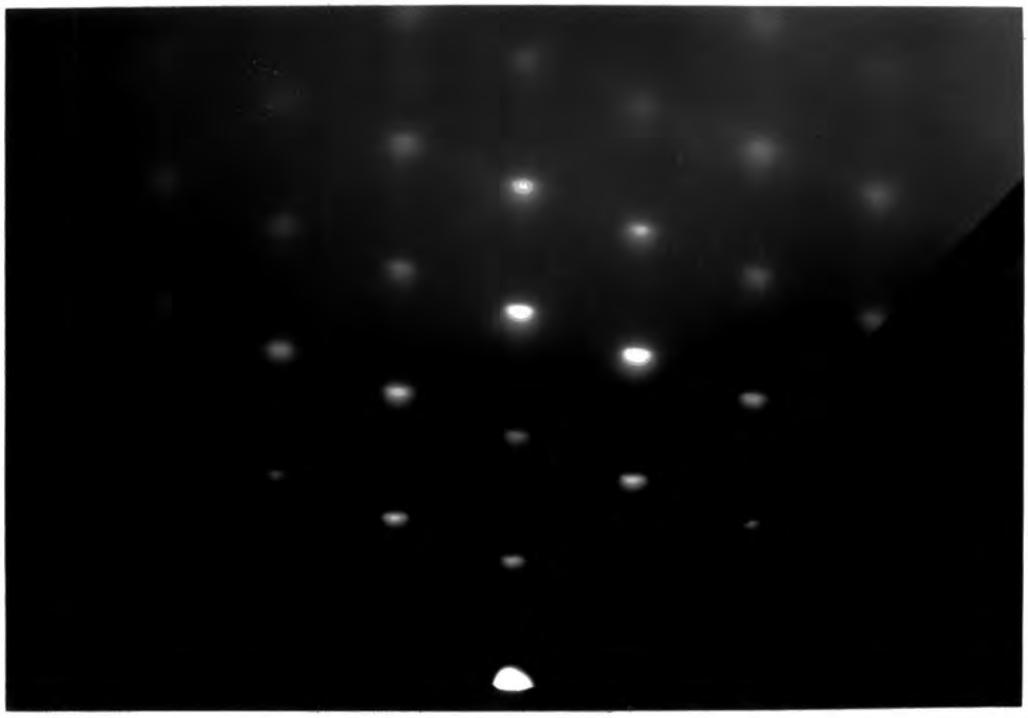

Fig. 7.9(b) : Typical spot pattern from a pad polished CdTe substrate.

also seen in these samples as further evidence of the high quality of the surface. The polishing time with this technique was found to depend on the initial surface conditions. If the samples were first mechanically polished on SiC paper, then a polishing time of 3-5 mins was required to obtain a good surface. However, with as-sawn samples a polishing time of 5 to 7 mins was necessary.

7.5.3 Electrical Characteristics of Devices

Layers of CdS, $\sim$ 10 μm thick, were deposited under nominally identical conditions (source and substrate temperatures of $\sim$ 900°C and 180°C, growth rate of 0.69 μm/min) on to alumina polished and pad polished CdTe substrates. The alumina polished substrates had been etched for 3 minutes in 2% Br-methanol solution.

The diode and photovoltaic characteristics of both types of device were measured in the dark and under AM1 illumination. Fig 7.10 shows the diode and photovoltaic output characteristics of two typical devices, one alumina polished, the other pad polished. The latter device had a higher OCV although the SCC and FF were almost similar for the two devices. Consequently, a higher efficiency of 3.1% was found for the pad polished cell as compared with 2.4% for the alumina/Br-Methanol polished device. The diode characteristics revealed less reverse bias leakage for pad polished samples.

These results are very much as one might expect. The RHEED study clearly demonstrated the superior quality of pad polished CdTe surfaces. Heterojunctions formed on these surfaces should therefore have a reduced density of interface states, compared to those formed on alumina polished substrates. Interfacial recombination would be less, resulting in a lower level of reverse saturation current, as observed in the diode characteristics. This, in turn, could give increased OCV, as was

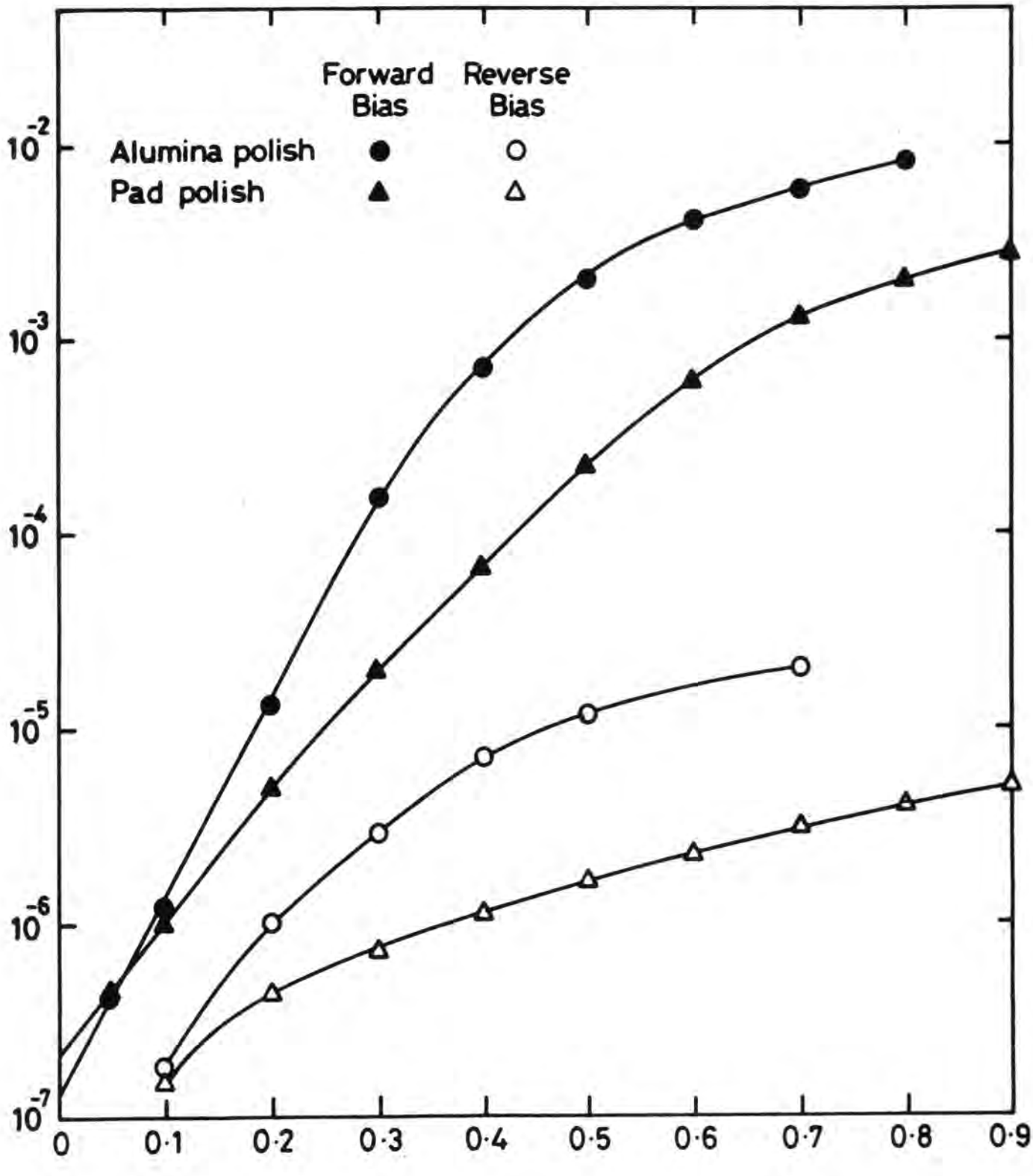

Fig. 7.10 (a) : Diode characteristics of devices fabricated on pad polished and alumina polished substrates

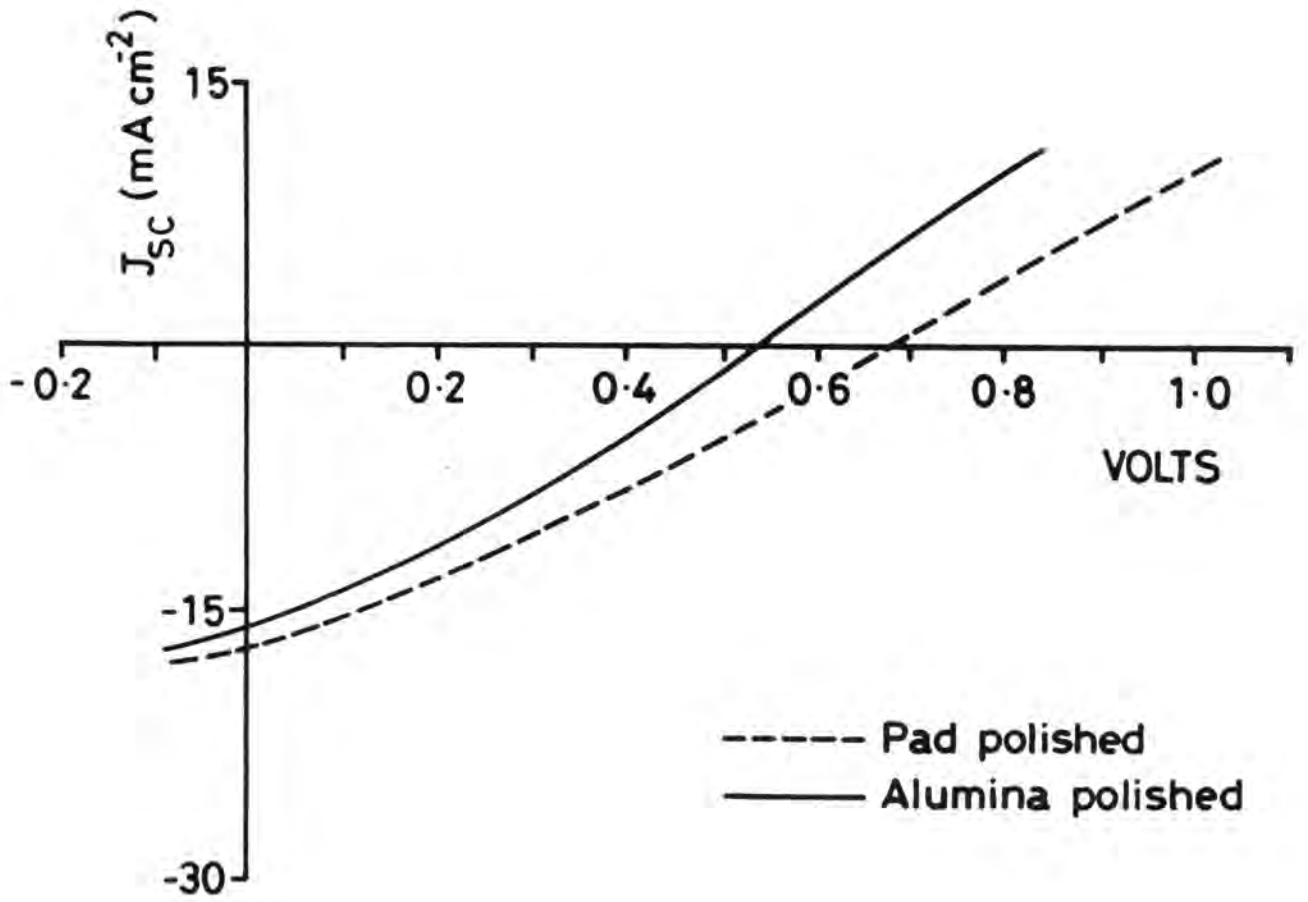

Fig. 7.10(b) : Photovoltaic characteristics of the same devices (Fig. 7.10(a))

observed experimentally. The low FF and SCC measured in both types of device was due primarily to the resistivity of the CdTe. As this was the dominant influence in all the devices studied, any secondary effects due to the polishing on SCC and FF (through improved carrier collection, etc) were not distinguishable. However, it would seem reasonable to suppose that there might be some difference on polishing.

7.6 EBIC Studies

Measurement of the minority carrier diffusion length is important in determining the volume of the semiconductor near the junction from which light generated carriers are collected. Diffusion length is readily measured using the EBIC technique in the SEM[16,48,49] as described in Section 5.3.3. EBIC may also be used to image potential barriers, and comparison with the corresponding secondary electron (SE) image can often help in identifying electrically active features.

The diffusion length measurements were made using a single linescan across the cleaved section through the junction and analysed in accordance with equation 5.12 (Section 5.3.3). All the measurements were made with a beam energy of 25 KeV, to ensure that surface recombination effects could be neglected. However, the generation volume will be correspondingly larger, resulting in a loss of spatial resolution.

A typical EBIC linescan of a device fabricated on nominally undoped CdTe and employing a carbon contact is shown in Fig 7.11a. A plot for $\log \frac{I(x)}{I(o)}$ vs x for the linescan is shown in Fig 7.12. The values of diffusion length L_n (in CdTe) and L_p (in CdS) obtained were 2.35 μm and 0.74 μm respectively. A similar device with a gold contact gave a value of L_n that was almost half the value for the C-contact device as shown

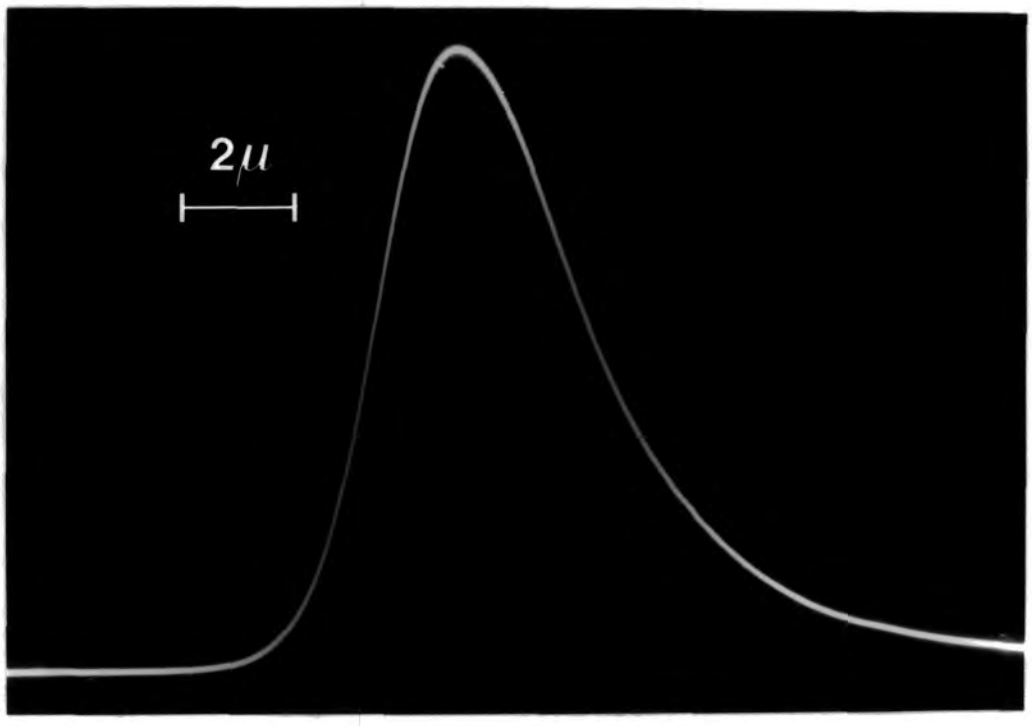

Fig. 7.11(a) : A typical EBIC linescan taken across a CdS/CdTe cleaved junction fabricated on a nominally undoped CdTe with carbon contacts.

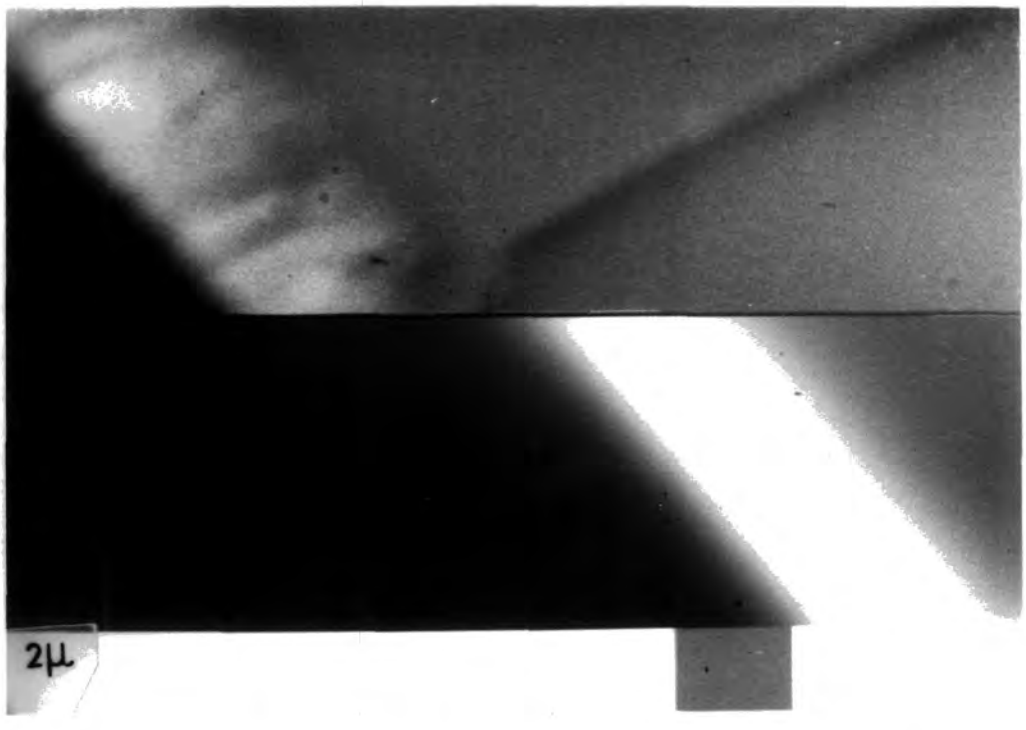

Fig. 7.11(b) : Split screen SE/EBIC image taken across the junction of the same device (Fig. 7.11(a)).

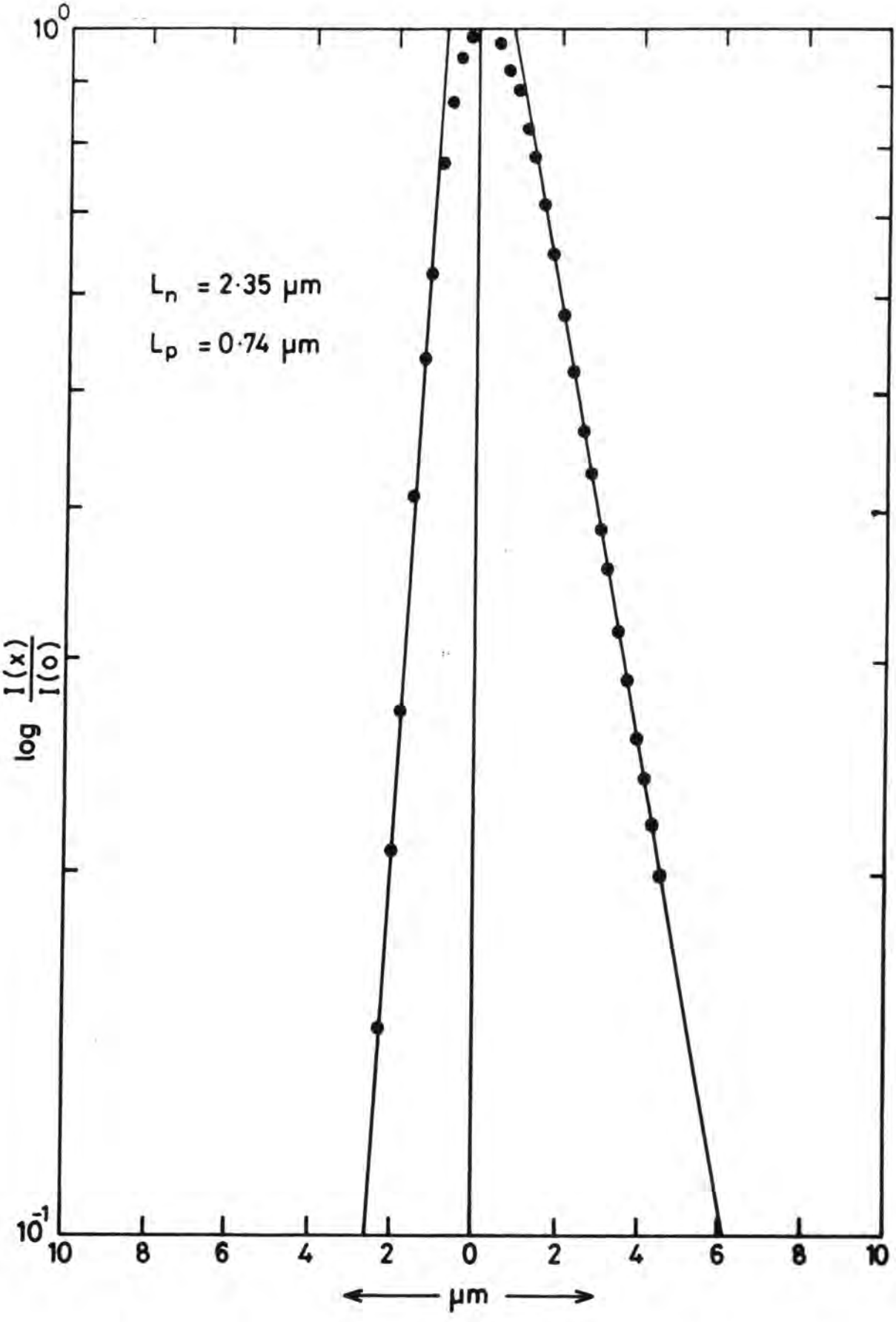

Fig. 7.12 : A typical plot of logI(x)/I(o) vs distance from the junction for the EBIC linescan of fig. 7.11(a).

in Table 7.7. The results show that the diffusion length of minority carriers was larger in undoped CdTe than in the p-doped material.

TABLE 7.7: Minority carrier diffusion length in different CdTe substrates with Au and C contacts

Substrate	Contact used	L_n (μm)	L_p (μm)
Undoped	C	2.35	0.74
"	Au	1.20	0.66
P-doped	C	1.12	0.80

A split-screen SE-EBIC image of a section across the junction of a cell fabricated on P-CdTe, and with a C-contact is shown in Fig 7.11b. This demonstrates that the p-n junction was located at metallurgical interface and the cell was therefore a true heterojunction rather than a buried homojunction. In addition, the majority of the EBIC bright contrast was on the CdTe side of the junction indicating that most of the depletion region is in the CdTe.

The values of L_n and L_p measured for these devices are higher than the values reported in the literature. Mitchell[50] has measured L_n = 0.4 μm and L_p = 0.43 μm using a beam energy of 21 KeV for a cell fabricated on a P-doped CdTe (10^{19} cm^{-3} concentration) with vacuum evaporated CdS. Yamaguchi et al[51] found the diffusion length of electrons in P-CdTe to be 0.7 μm.

As discussed in Chapter 2 the diffusion length of the minority carriers depends among other things on impurity concentration, crystallinity and stoichiometry. The single crystals, used in the present work were grown from the vapour phase. The generally higher

values of L_n measured in Durham grown material would suggest that it is of better crystallinity and stoichiometry than the P-doped single crystals used by Mitchell and Yamaguchi et al which were grown by the Bridgman technique. However, the fact that the diffusion length in nominally undoped CdTe was higher than that for the phosphorus doped substrates suggests that the lower values of L_n observed in Bridgman grown CdTe were due more to the p-dopant than to crystalline defects.

The increase observed in the diffusion length of minority electrons in devices with carbon contacts can be explained in terms of the BSF and the built-in field established in the contact region due to the doping concentration gradient. This assists the minority carriers to diffuse towards the junction. The increase in diffusion length in the C-contact devices can explain in part the higher values of SCC and efficiency observed in these devices. The EBIC and SE micrograph shown in Fig 7.11b indicated that the junction was a true heterojunction and this agrees with previous studies[45]. This is important, because the short anneal given to the carbon contacts might have been expected to produce a buried homojunction in the CdTe due to donor impurity diffusion but it is shown clearly that this did not occur.

7.7 Conclusion

The work described in this chapter was concerned with CdS/CdTe heterojunctions formed on bulk single crystal CdTe. Contacts, dopants and substrate preparation techniques were all investigated to determine their effects on the device characteristics. Minority carrier diffusion lengths and effects of ageing were also investigated.

The performances of evaporated Au and C paste contacts to p-CdTe were compared in detail. Generally, C contacts gave an improvement in

FF and η of about two times compared with identical devices with Au contacts. The results suggest that C contacts had a significantly lower resistance, with correspondingly larger values of FF and SCC. The reason for this is thought to be due to the diffusion of acceptor impurities from the C paste into the surface of the CdTe, creating a highly doped region under the contact which led to a tunneling contact. Minority carrier diffusion lengths were also found to be larger in the C-contact devices, probably as a result of the BSF effect associated with the impurity concentration profile under the contact.

The annealing temperatures required for the contacts were investigated, and the optimum value for C contacts was found to be $\sim$ 300°C. Carbon contacts were also found to be stable with time. In contrast, the heat treatment of Au contacts made relatively little difference to performance, although a 10 min anneal at 180°C in Ar was found to be optimum. Au contacts were not stable with time.

The effects on resistivity of doping the CdTe substrates were also investigated. Devices formed on CdTe doped with Cu, P or Te and on undoped material, were compared. P doping was found to be the best, yielding a higher FF than the other dopants. However, the minority carrier diffusion length was larger in the undoped material.

Substrate polishing procedures were also investigated in terms of surface structure and morphology as well as in device performance. A procedure involving pad polishing in a 2% Br-methanol solution was found to give the best results. Polishing with alumina or cerium oxide paste gave poor results and left residues on the surface.

In summary the best single crystal CdS/CdTe devices were fabricated on P-doped CdTe using carbon contacts. These gave a SCC, FF, OCV and η of 21 mA cm^{-2}, 47%, 0.72 V and 7.2% respectively.

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CHAPTER 7

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CHAPTER 8

THIN FILM CdS/CdTe SOLAR CELLS

8.1 Introduction

The primary aim of current research into terrestrial solar cells is to reduce the manufacturing cost while maintaining respectable conversion efficiencies and device lifetimes. In this connection thin film structures have been prominent because of their smaller material utilization and low cost depositional procedures. Of the various material systems that have been investigated[1], amorphous silicon, copper indium diselenide and cadmium telluride have emerged as leading contenders[2-6]. All these are amenable to thin film processing of one form or another and the latter two have particularly suitable band gap energies.

In parallel, therefore, with the bulk crystal cell studies described in the previous chapter, an investigation into all-thin film CdS/CdTe structures was carried out where both the CdS and CdTe were deposited by vacuum evaporation. Acceptor impurities such as copper, antimony and elemental tellurium were studied as possible dopants to produce p-type CdTe of suitable resistivity. The electrical and structural properties of the films (CdS & CdTe) were investigated and correlated with the performance of CdS/CdTe heterojunctions produced. Thin film devices with efficiencies in excess of 3% were achieved.

8.2 Properties of Cadmium Sulphide Films

8.2.1 Introduction

The optical and electrical properties of the CdS film strongly influences the overall efficiency of the CdS/CdTe solar cell. The properties of these films in turn depend on the substrate temperature.

Therefore, the structural and electrical properties of the thermally evaporated CdS films were investigated as a function of the preparational conditions.

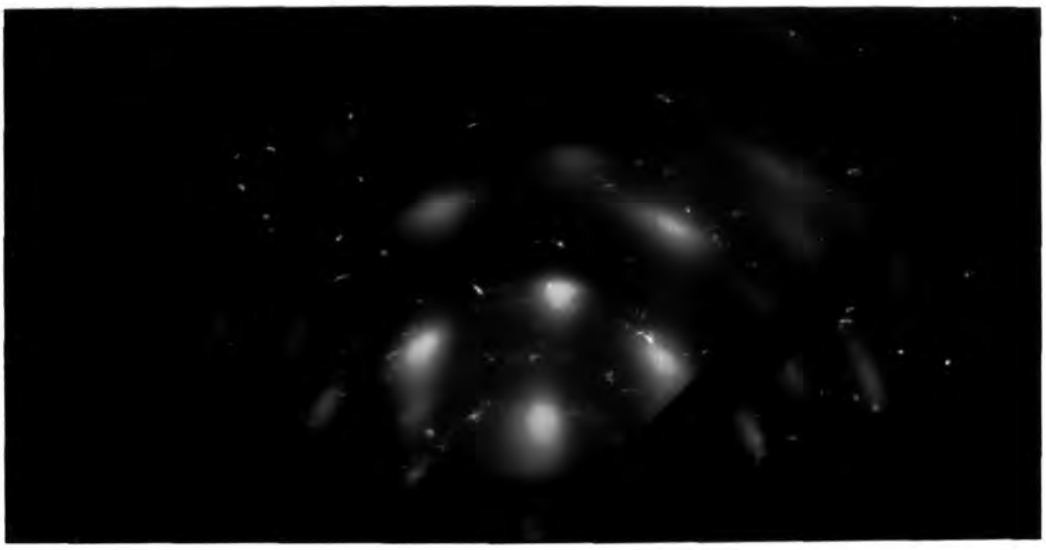
The CdS films were deposited on tin oxide coated glass substrates (from Pilkington plc) by thermal evaporation (Sect.4.5.1). Substrate temperatures ranged from 120 to 300°C and the source temperature was held at between 800 and 1100°C.

For the structural investigations, RHEED studies were made of the films grown at different substrate temperatures. The texture of the films was investigated using the SE mode of the SEM. X-ray diffraction studies were also made with a diffractometer using CoKα radiation (Sect.5.4). The resistivity of the films was also measured.

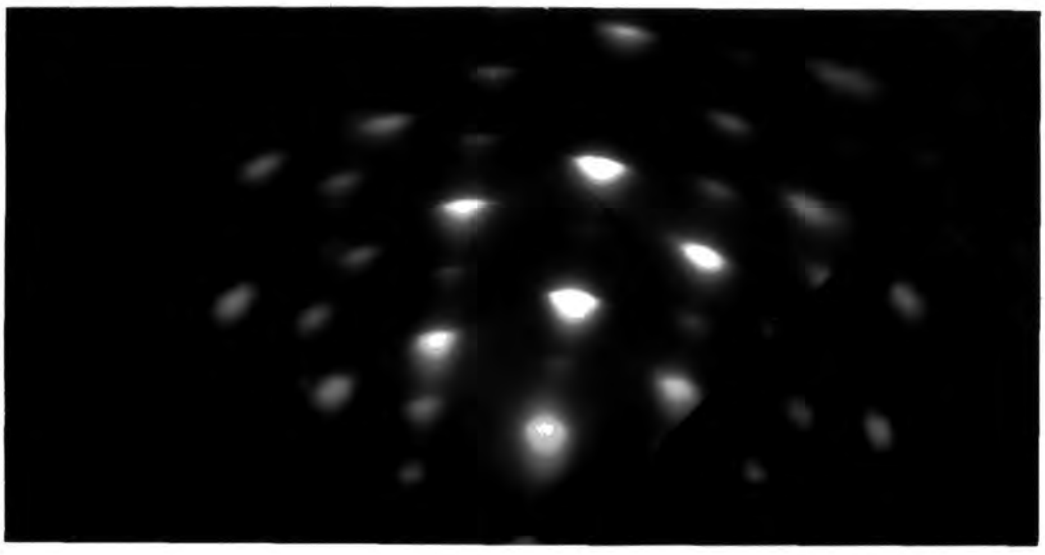
8.2.2 Structural Studies

The RHEED diffraction patterns of CdS films grown at 120, 180 and 300°C substrate temperatures are shown in Fig 8.1. It is evident that the length of the arcs is a minimum when the substrate temperature is ∿180°C, whereas they are wider at lower and higher temperatures. As the extent of the arcs in RHEED indicates the degree of ordering, these observations suggest that the optimum crystallinity was obtained at 180°C.

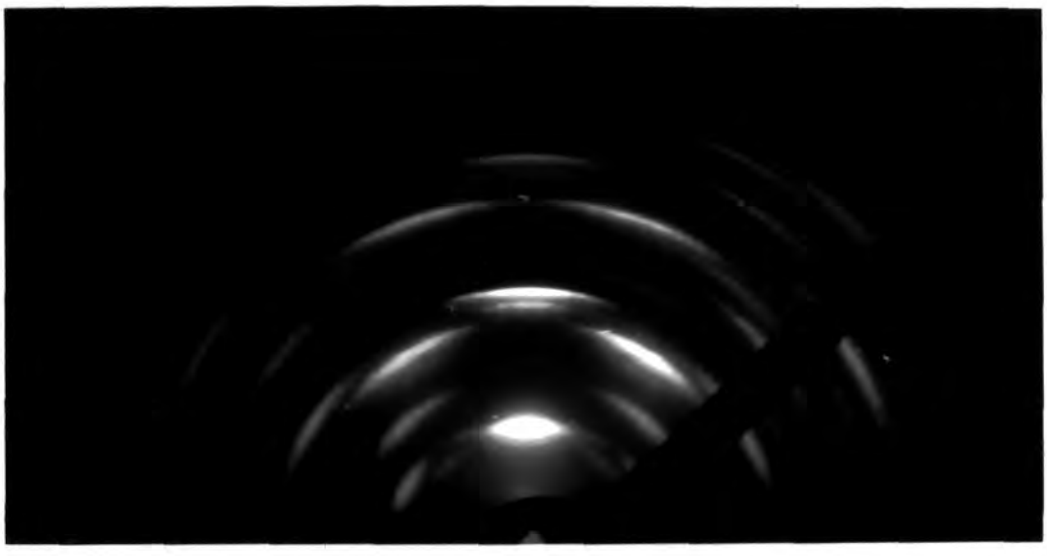
X-ray diffraction studies were made in order to determine the structure and identify the phases present in the films. Fig 8.2 shows the X-ray diffraction spectra of a typical film grown at 180°C. There is a sharp peak at an angle 2θ equal to 30.9° which corresponds to a diffraction from (0002) planes of the hexagonal phase. The intensity of the diffraction at an angle of 30.9° decreased when the substrate temperature exceeded 200°C and additional peaks appeared at 2θ equal to 28.9 and 32.8 degree which correspond to diffraction from $(10\bar{1}1)$ and $(10\bar{1}0)$ planes of the hexagonal phase.



120°C



180°C



300°C

Fig. 8.1 : RHEED patterns of CdS films grown at substrate temperatures of : (a) 120°C; (b) 180°C; and (c) 300°C.

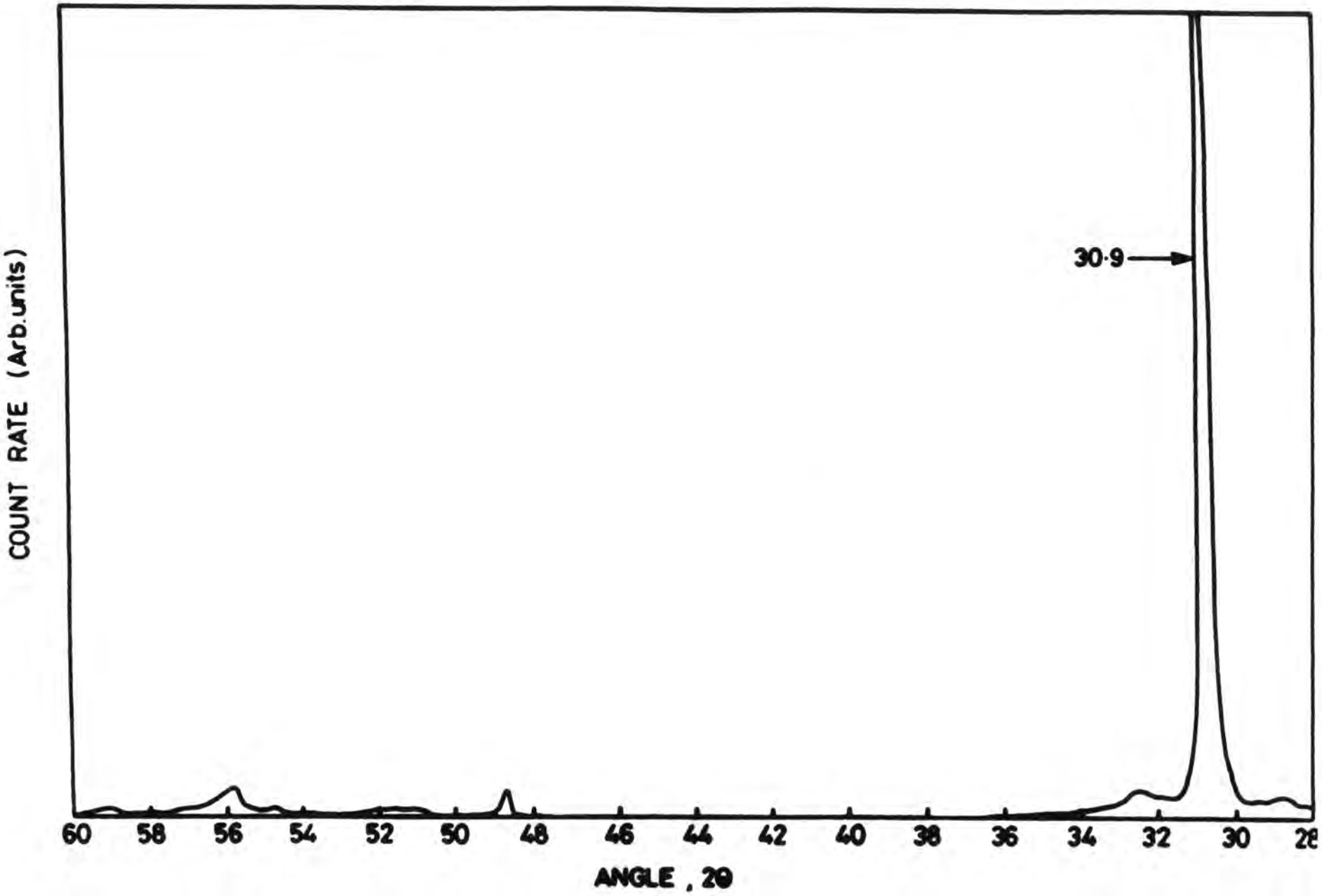


Fig. 8.2 : X-ray diffraction spectrum of a typical CdS film grown at 180°C

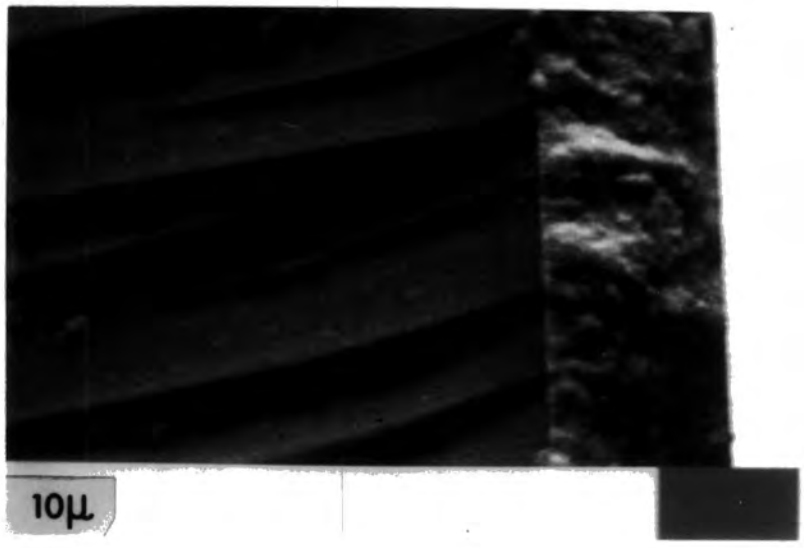
The morphology of the films was also studied in the scanning electron microscope. Fig 8.3 represents the SE micrographs of three films grown at different temperatures. It is clear that the film grown at 180°C had the best columnar growth with the c-axis perpendicular to the substrate. At other substrate temperatures columnar growth was less evident and there was a greater proportion of randomly oriented material.

8.2.3 Film Resistivity

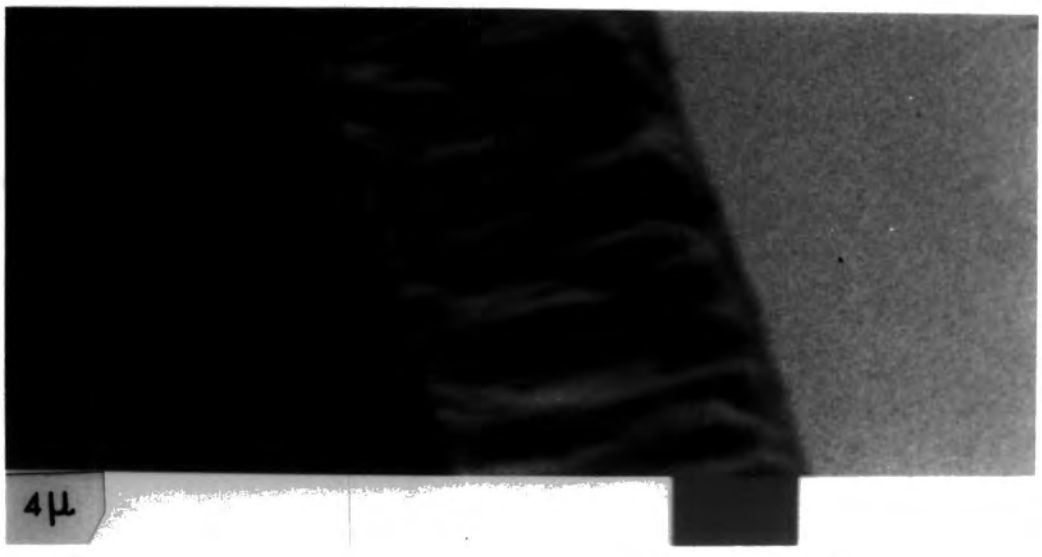
The electrical properties of the films were not studied extensively except to measure the resistivity. Three different source temperatures (800, 900, 1000°C) were selected to give different evaporation rates of 0.54, 0.69 and 1.08 μm per minute. Electrical measurements revealed that the film resistivity increased with increasing substrate temperature whereas there was a gradual decrease in resistivity at higher rates of evaporation. The growth rate of films deposited at temperatures above 200°C was slower than at lower temperatures. Table 8.1 shows the relation between the resistivity and deposition conditions of the films.

TABLE 8.1: Effect of substrate and source temperature on the resistivity of CdS films

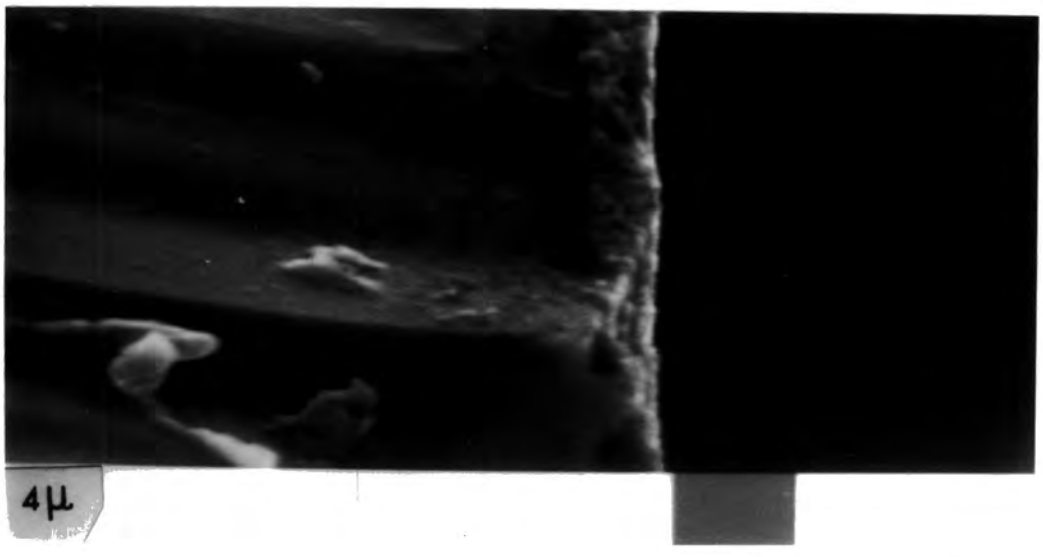
Effect of Substrate Temperature			Effect of Evaporation Rate		
Substrate Temp.(°C)	Thickness μm	Resistivity Ω-cm	Charge Temp (°C)	Evaporation Rate μm	Resistivity Ω-cm
120	15	34	800	0.54	670
160	15	50			
180	11	230	900	0.69	215
200	6	540			
240	4	878	1000	1.1	65
300	3	1050			



(a) 120°C



(b) 180°C



(c) 300°C

Fig. 8.3 : SE micrographs of the fractured edges of CdS films deposited at : 120°C; (b) 180°C; and (c) 300°C.

8.2.4 Discussion

There has been a substantial volume of research into the preparation of thermally evaporated CdS films[7-13], which has been reviewed by Stanley and by Hill[14,15]. The effects that different depositional conditions have on the structural and electrical properties of films 1-25 μm thick range has also been extensively studied in this laboratory[16,17].

The films examined during the present work were 1-20 μm thick. The substrate temperature appeared to be the main parameter controlling the crystallinity, the optimum temperature was 180°C. The electrical properties were also governed by the substrate temperature and to a lesser extent by the evaporation rate.

During thermal evaporation the CdS is believed to dissociate according to the following reaction[17-21].

$$CdS = Cd(g) + \tfrac{1}{2} S_2(g) \qquad (8.1)$$

It has also been suggested that the stable configuration of sulphur in the vapour at lower and higher temperatures is S_8 and S_2 respectively[22,23]. At lower temperatures when the cadmium and sulphur recombination rates on the substrate are different from the impingement rate of the species, the unreacted S_8 molecules re-evaporate and hence films rich in cadmium are obtained. When the substrate temperature is increased the stoichiometry of the film improves, possibly due to the fact that the reassociation rate becomes more equal to the impingement rate. At substrate temperatures above 200°C, re-evaporation takes place

resulting in thinner layers. The decrease in the textured growth of the film at temperatures above 200°C may be related to the increase in the adsorbed sulphur[17]. This would also explain the increased resistivity of layers deposited at higher substrate temperatures[17]. The inverse relationship between film resistivity and evaporation rate is possibly related to excess Cd. It is thought that higher impingement rates lead to Cd rich layers[16].

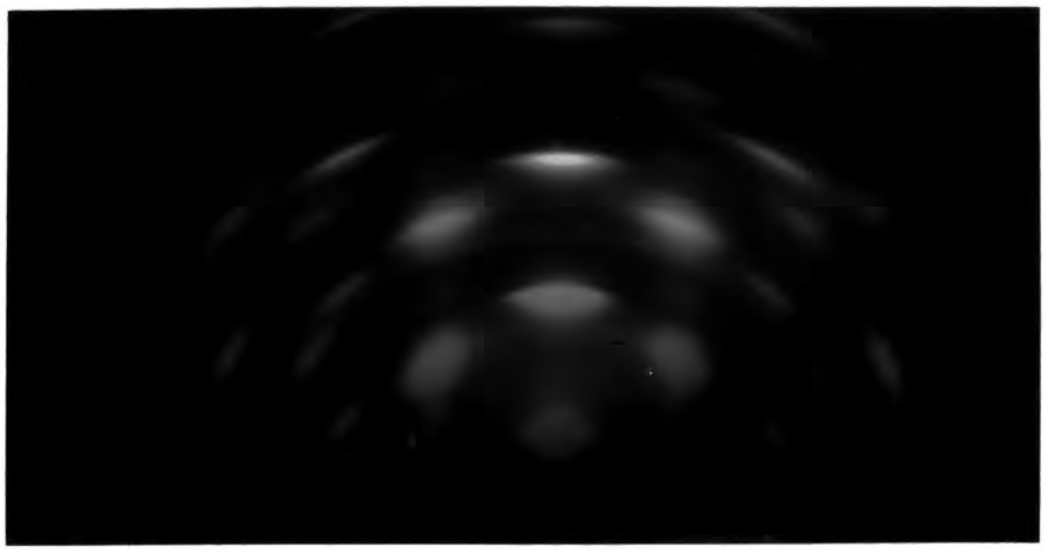
8.3 Properties of Cadmium Telluride Films

8.3.1 Structural Properties

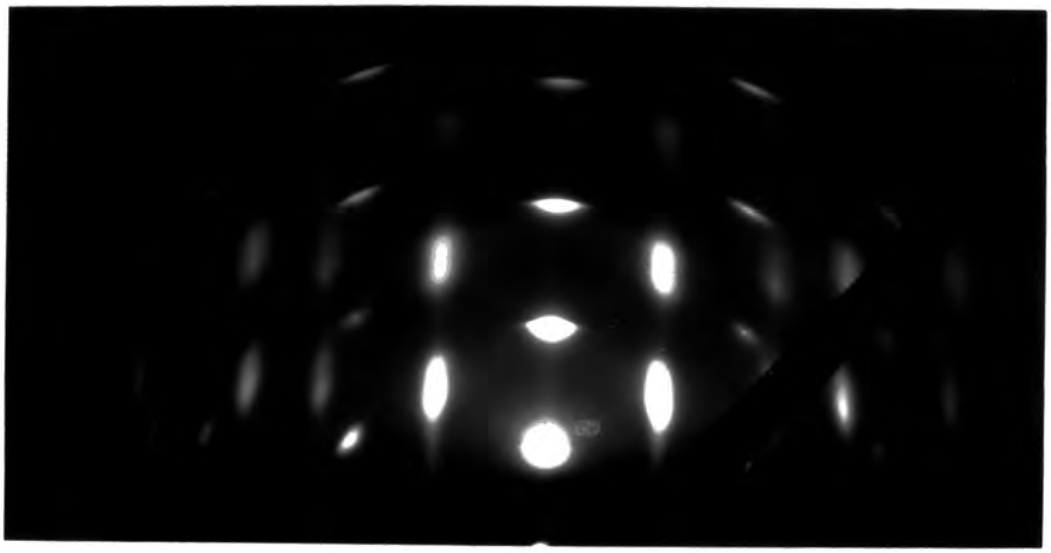
All the films were prepared in a conventional vacuum evaporation system as described in Section 4.5.2. CdTe synthesized in Durham, was used as starting material and was evaporated from a quartz crucible at temperatures between 800-1200°C. The substrate temperature was varied from 18 to 400°C. Evaporation rates ranged between 1.5-2.5 μm/min. The films had a smooth shiny surface when deposited at lower temperatures but with temperatures above 250°C were grey in colour. Film adhesion on gold coated glass slides was reasonably good.

Fig.8.4 shows the RHEED diffraction pattern of films grown at 150,200 and 300°C. As with the CdS films the arc length decreased with increasing substrate temperature T_s, becoming a minimum at ∿ 200°C. The length of the arcs stayed approximately constant up to T_s at ∿ 250°C when they began to increase in width. It follows that the films grown at substrate temperatures in the range 200-250°C had the better crystallinity.

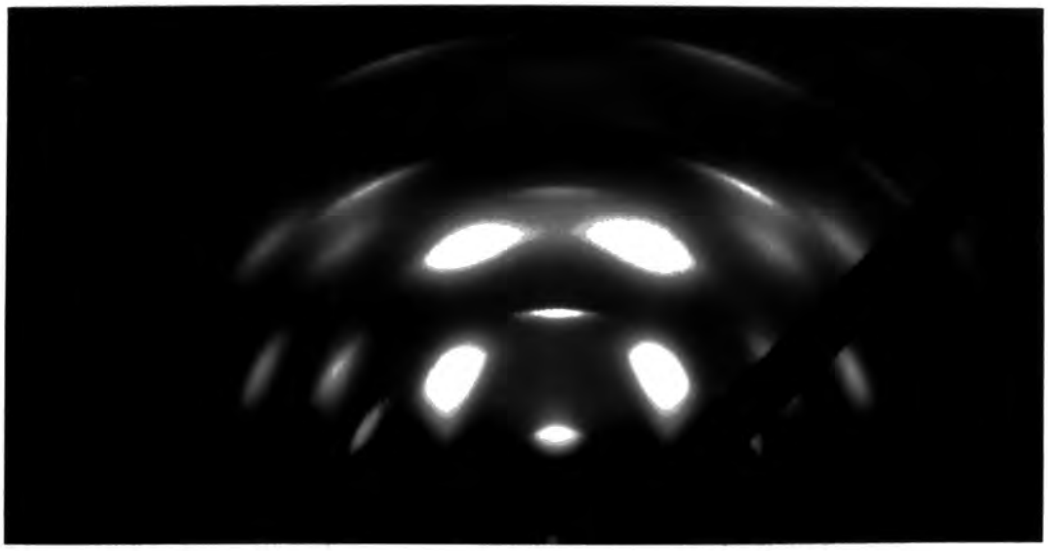
X-ray diffraction studies were also carried out on films grown simultaneously on plane glass slides (i.e. without the Au coating) at temperature of 100, 150, 200, 250 and 300°C. The diffraction spectra for a typical film grown at 200°C is shown in Fig 8.5. There were three principal peaks at 2θ equal to 27.6, 45.9 and 54.5° which corresponded



(a) 150°C



(b) 200°C



(c) 300°C

Fig. 8.4 : RHEED patterns of CdTe films deposited at substrate temperatures of : (a) 150°C; (b) 200°C and (c) 300°C.

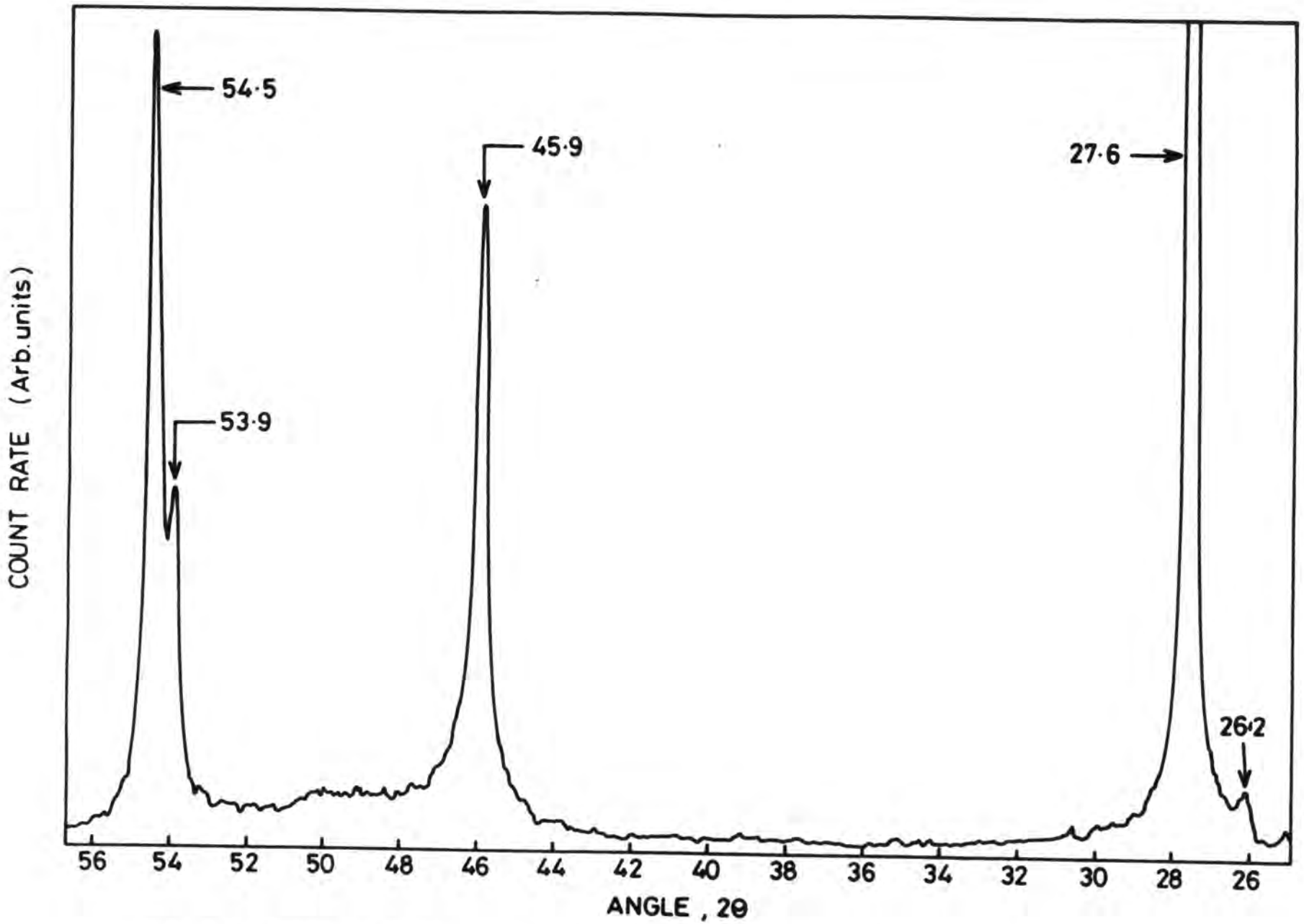


Fig. 8.5 : X-ray diffraction spectrum of a typical CdTe film grown at 200^{o}C

to diffractions from the (111), (220) and (311) planes of cubic CdTe. The intensity of the (111) diffraction line increased with increasing substrate temperature up to 250°C, providing confirmation for the RHEED results. Annealing a film (grown at 150°C) at 325°C for 25 mins in nitrogen led to an increase in the intensities of peaks corresponding to the (111), (220) and (311) diffractions. This was probably due to an increase in preferential growth. A small peak at about 26.2°(see Fig 8.5) was observed at temperatures below 300°C but could not be fully resolved. It could be due to excess tellurium[24]. Table 8.2 summarizes the X-ray diffraction results.

TABLE 8.2: X-ray diffraction data of CdTe films

Deposition Temperature (°C)	Relative Intensities (111)	(220)	(311)
standard*	100	60	30
100	100	0.5	0.1
150	100	43	11
200	100	72	50
250	100	-	-
300	100	26	48

* Relative intensities for randomly oriented CdTe powder, from ASTM X-ray powder data file Card No.15-770 (CuKα radiation).

The morphology of the films was examined by scanning electron microscopy. Fig 8.6 shows the micrograph of a cross-section through a film deposited at 200°C. The film displayed good columnar growth which was found to improve with increasing substrate temperature up to 250°C. As with CdS, CdTe films deposited at T_s>250°C were thinner than those grown with the same evaporation rates but at lower substrate temperatures.

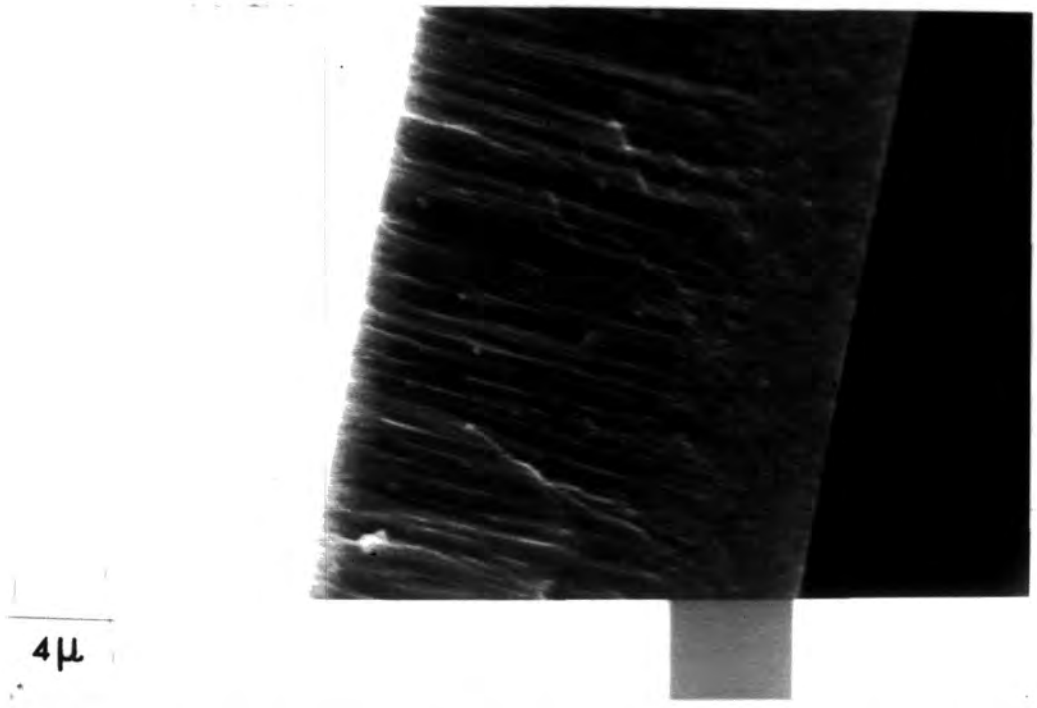


Fig. 8.6 : SE micrograph of a cross-section through a CdTe film deposited at 200°C.

8.3.2 Resistivity

The resistivity of the CdTe films did not show a pronounced dependence on substrate temperature. All the films grown had resistivities of the order of 10^6 Ω-cm. As a result, Hall measurements could not be made. Attempts to make the films more p-type conducting by doping them during growth with Cu, Sb and elemental Te were unsuccessful. However, post-growth doping with copper did reduce the resistivity as discussed in Section 8.5. Post-deposition heating in oxygen has been reported to have a dramatic effect on the performance of CdS/CdTe solar cells prepared by close space vapour transport[25,26]. This possibility was investigated by growing the CdTe films in an oxygen ambient and by providing a post growth heat treatment in oxygen at ∿ 400°C for 30 mins. This reduced the resistivity by a factor of three only.

8.3.3. Discussion

Thin films of cadmium telluride prepared by conventional vacuum evaporation have been investigated in the past[27-34]. Their resistivities were very high (10^7 Ω-cm at room temperature) despite the addition of dopants into the charge. Menezes, however, produced low resistivity (10-100 Ω-cm) p-type CdTe films utilizing a hot wall flash evaporation (HWFE) technique[35], although electron microprobe analysis revealed the presence of 25-50% of free tellurium. Myers et al[36] used a molecular beam deposition technique to produce good CdTe layers, but this is very expensive and cannot be employed for low cost cells.

The resistivities of the films deposited during the present work were similar to those discussed by other workers[27-34]. The high resistivity is believed to be due to native defects[37]. Glang et al[34] have attributed the high resistivity to very low effective carrier mobilities, or low carrier concentrations, or both. The low

effective mobilities may be caused by electrical barriers at the grain boundaries similar to those postulated by Goldstein and Pensak[29] and Hutsin[33] to explain the large photovoltages observed in CdTe films prepared under an oblique angle of deposition. de Nobel[38] has also measured large potential drops across grain boundaries in CdTe crystals.

The low density of charge carriers may be due to the fact that at the deposition temperatures used, CdTe does not have the ability to dissolve an appreciable excess of its constituents. Although the accommodation coefficients of Cd atoms and Te_2 molecules differ substantially (to allow the condensation of unreacted tellurium up to 150°C), a significant deviation from stoichiometry in the compound is not produced. This conclusion is supported by the data published by de Nobel[38] who determined the excess of Cd or Te dissolved in CdTe crystals using Hall measurements. He was able to show that the solubilities of both the constituents decreased toward lower temperatures. Assuming that the trend of decreasing solubilities extends to temperatures below those investigated (i.e. room temperature to 400°C) the deviation from stoichiometry in CdTe films condensed at these lower temperatures must be small leading to low carrier concentrations.

When films are intentionally doped with impurities such as Cu, Sb and Te, a reduction in resistivity is not necessarily to be expected. Kroeger et al[39] have shown that in contrast to Si and Ge, the incorporation of impurities into semiconducting compounds may occur by different mechanisms. The ambient conditions during preparation are important in determining whether the introduction of an impurity will contribute charge carriers or not. In CdTe, indium has been found to be an effective donor only if the crystals are annealed in Cd vapour to establish a metal excess. Similarly, crystals doped with Cu or Au show

p-type conductivity only if treated in excess tellurium. If CdTe films deposited at temperatures below 300°C do not show significant deviation from stoichiometry, then neither acceptor nor donor impurities would be expected to be electrically active, on the basis of Kroeger et al[39] and de Nobel's work.

CdTe sublimes into its constituents according to the reaction[34,38,40]

$$CdTe(s) = Cd(g) + \tfrac{1}{2} Te_2(g) \qquad (8.2)$$

and the cadmium and tellurium condense on the substrate. The free tellurium expected in films (X-ray spectra peak at 26.2°) deposited at lower temperatures (< 250°C) may be explained in terms of different sticking coefficients of Cd and Te at the various substrate temperatures, i.e. Te would appear to have a much larger sticking coefficient at 150°C than Cd. Similarly thinner films were obtained at higher substrate temperatures (> 250°C) as a result of the re-evaporation of the films when the sticking coefficients become too small. Glang et al[34] found the same effect. Interestingly, this behaviour was not reflected in the resistivity of the films. The fact that post-growth annealing in oxygen did not produce films with low resistivity as reported by MaCandless et al[25] may be due to the rather low annealing temperature employed here.

8.4 Contact Studies

8.4.1 Introduction

The question of contacts to bulk CdS and CdTe was discussed in some detail in Section 7.2. The problems of making reliable, ohmic and low resistance contacts to p-CdTe were emphasised. The best contacts were made with C paste. Similar results were found with the thin film devices, so that the discussion will be limited to a brief presentation of the findings.

The heterojunctions were formed by the successive evaporation of CdS and CdTe onto tin oxide coated glass slides, to form SnO_x-CdS-CdTe-(Au or C) structures. Occasionally, evaporated indium was used instead of SnO_x as the contact to n-CdS.

8.4.2 Devices with Au Contacts

Fig.8.7 shows the diode characteristic of a typical device using evaporated Au and SnO_x as the contacts to the CdTe and CdS respectively. This characteristic shows the device to have a rectification factor of 380 at 0.6 V. The corresponding photovoltaic output characteristics are shown in Fig.8.8 for both front and back-wall illuminations (i.e. light incident through the CdTe and through the CdS respectively). The values of SCC, OCV, FF and efficiency are listed in Table 8.3.

TABLE 8.3: Device parameters with different contacts in different operation modes

Contact	Mode of Operation	OCV volts	FF %	SCC mA cm^{-2}	η %
C	Back-wall	0.36	33	0.460	5.6×10^{-2}
Au	Front-wall	0.34	27	0.065	5.9×10^{-3}
"	Back-wall	0.39	32	0.320	4.02×10^{-2}
$AuCl_3$ solution	Back-wall	0.38	34	0.490	6.5×10^{-2}

Although the device parameters are very low because of the high series resistance of the CdTe (as discussed in Section 8.3) they were higher in the back-wall mode than in the front-wall mode. This is entirely expected since in the front-wall mode, most of the electron-hole generation will occur close to the CdTe surface, and will be lost to surface and bulk recombination before diffusion to the junction can

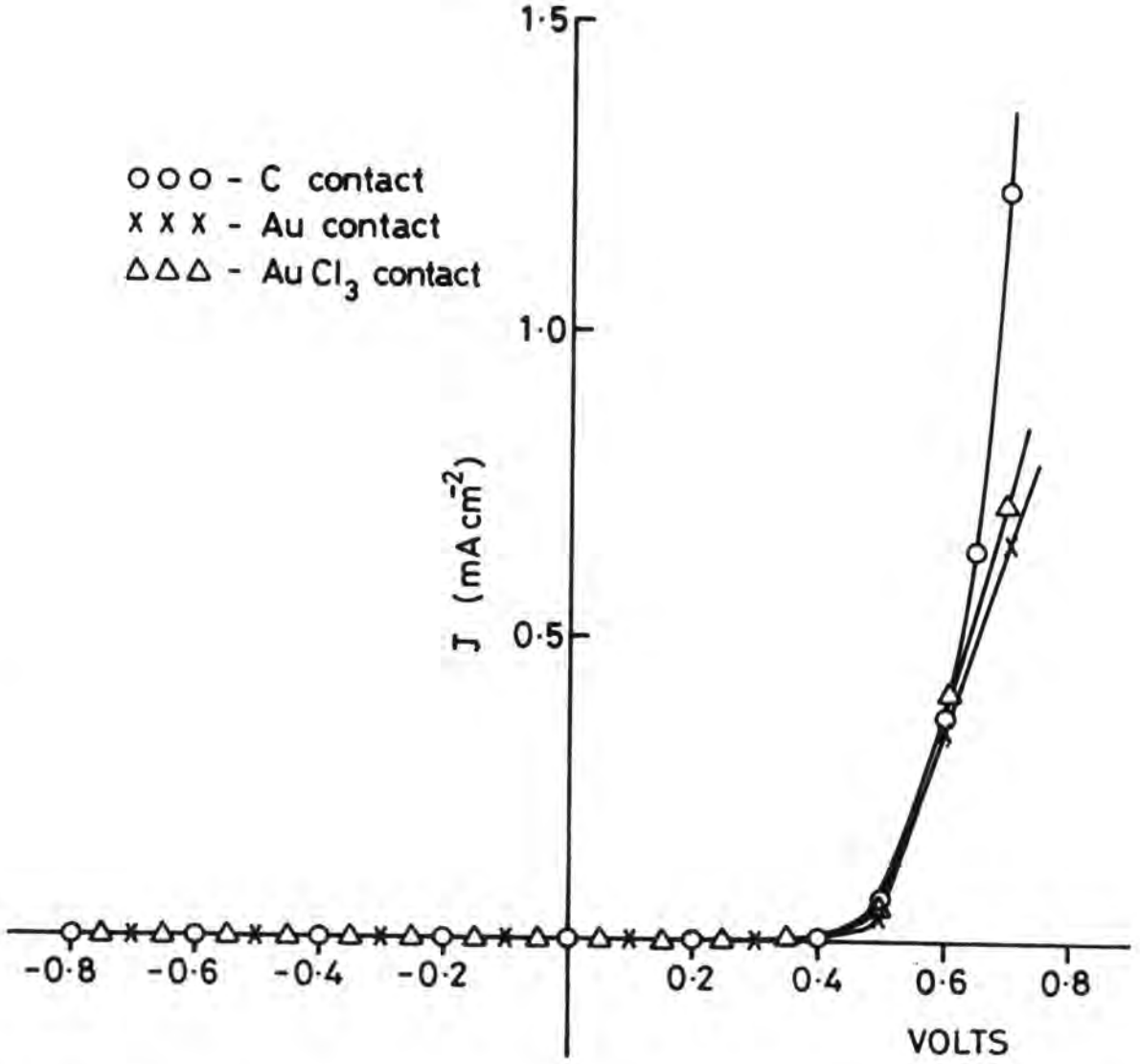


Fig. 8.7 : Diode characteristics of different devices with Au, $AuCl_3$ and C contacts p-CdTe

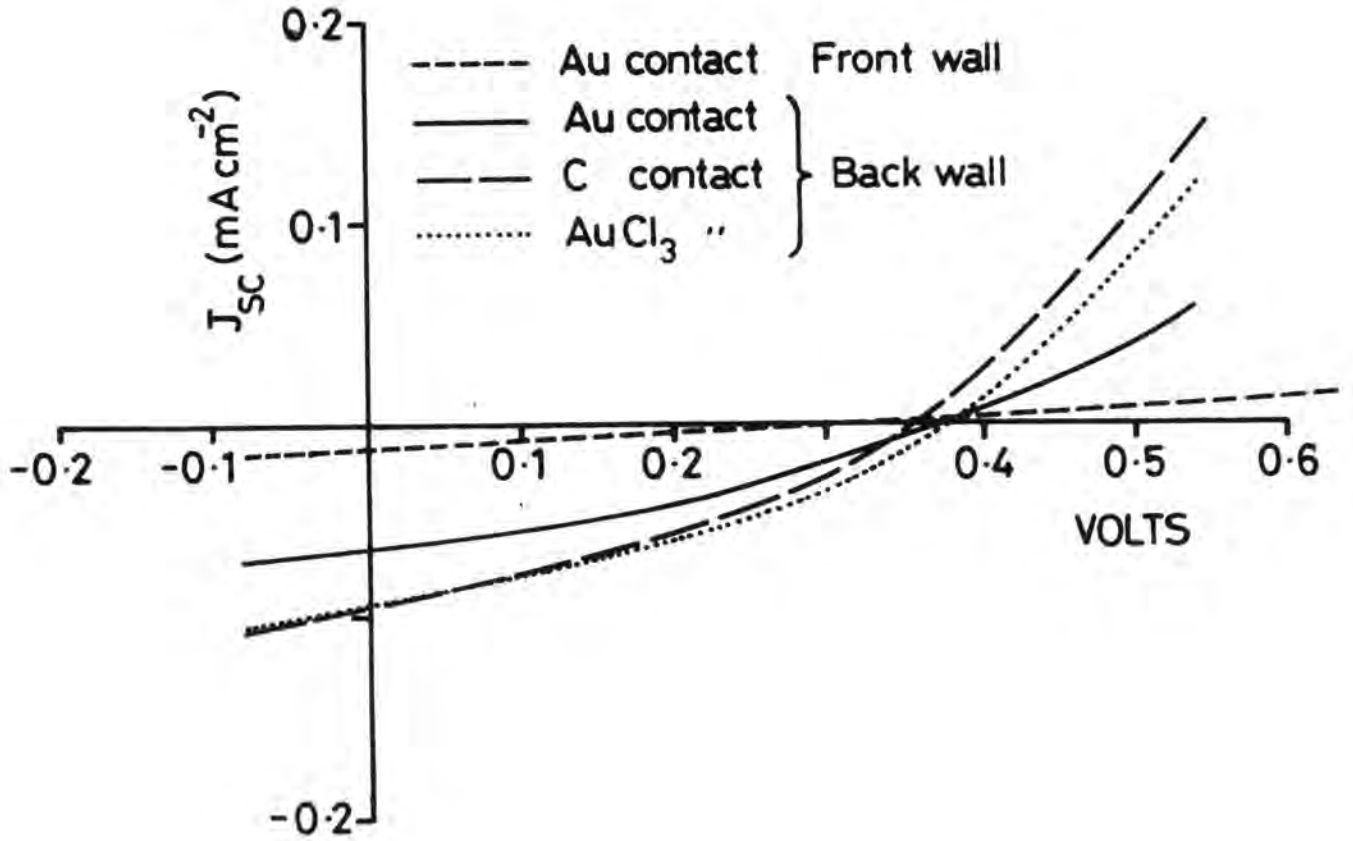


Fig. 8.8 : Photovoltaic characteristics for devices with Au, $AuCl_3$ and C contacts

occur. In the back-wall mode, absorption takes place close to the CdTe/CdS interface, where carrier collection is most efficient.

Some devices were made using an aqueous solution of $AuCl_3$ to form the gold contact to p-CdTe. These had a better response as shown in Fig 8.8 and Table 8.3 for back-wall illumination. The overall performance however, is still dominated by the CdTe resistivity.

The spectral response was investigated by measuring the SCC and OCV as a function of the wavelength of incident monochromatic radiation. The spectral responses of an evaporated Au-contact device in both the front and back-wall modes of operation are shown in Fig 8.9. The response in the back-wall mode is higher than that in the front-wall mode as expected. The SCC response in the front-wall mode is very narrow. In both modes the long wavelength threshold corresponds to the CdTe band gap and indicates that absorption occurs in the CdTe. On the short wavelength side, the response of front-wall devices falls off rapidly due to surface recombination effects. However, in the back-wall mode, the response is more nearly that expected of the window effect.

8.4.3 Devices with Carbon Contacts

Carbon contacts to p-CdTe films were made by applying a small quantity of carbon paste to the p-CdTe films and annealing in nitrogen at temperatures between 330 and 340°C for about thirty minutes. The heterojunctions were otherwise no different from those with Au contacts. Since the carbon layer was thick and absorbed the incident light, these devices were studied in the back-wall mode.

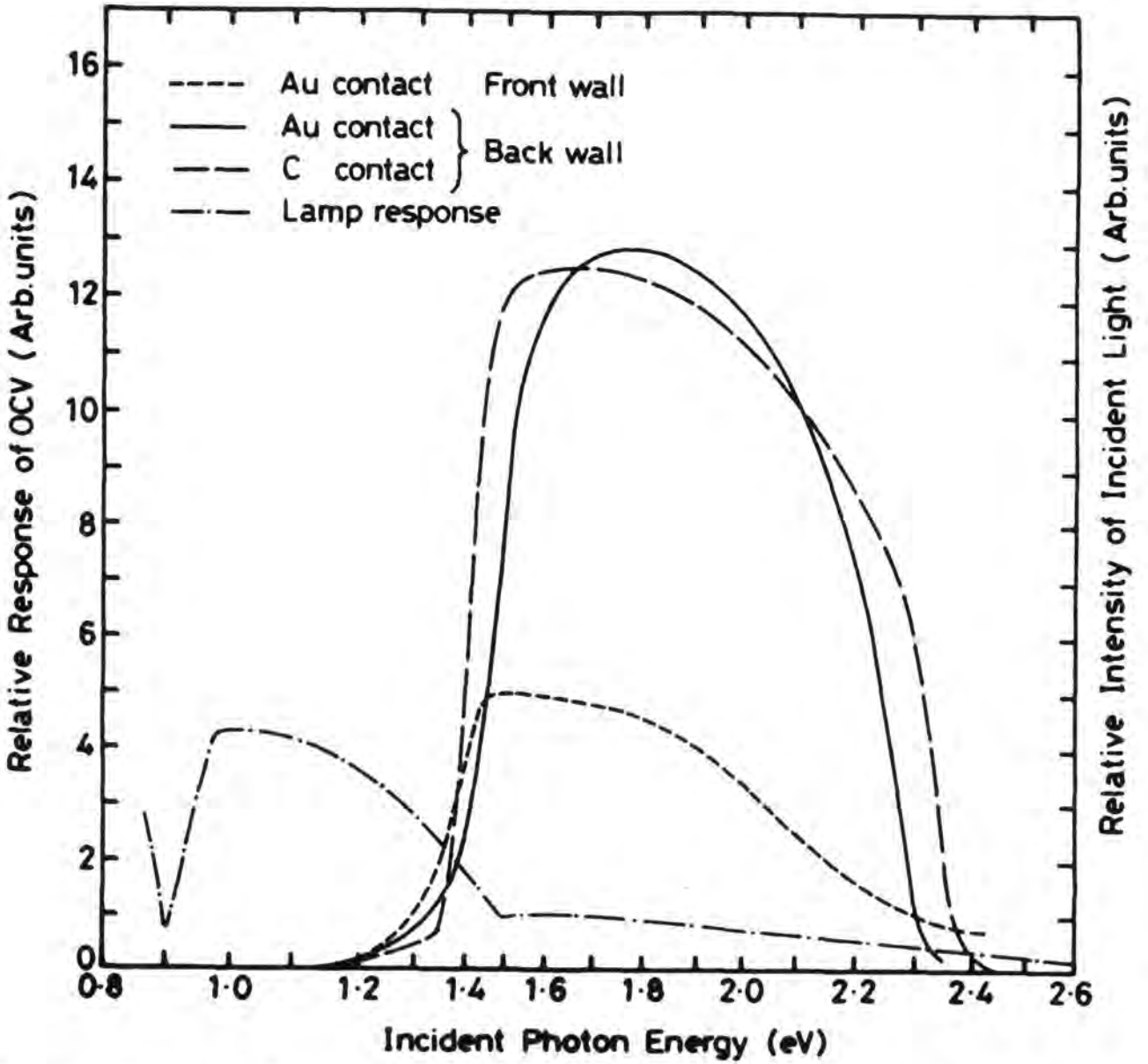


Fig. 8.9 (a) : Open circuit voltage spectral responses of devices with different contacts (Au and C)

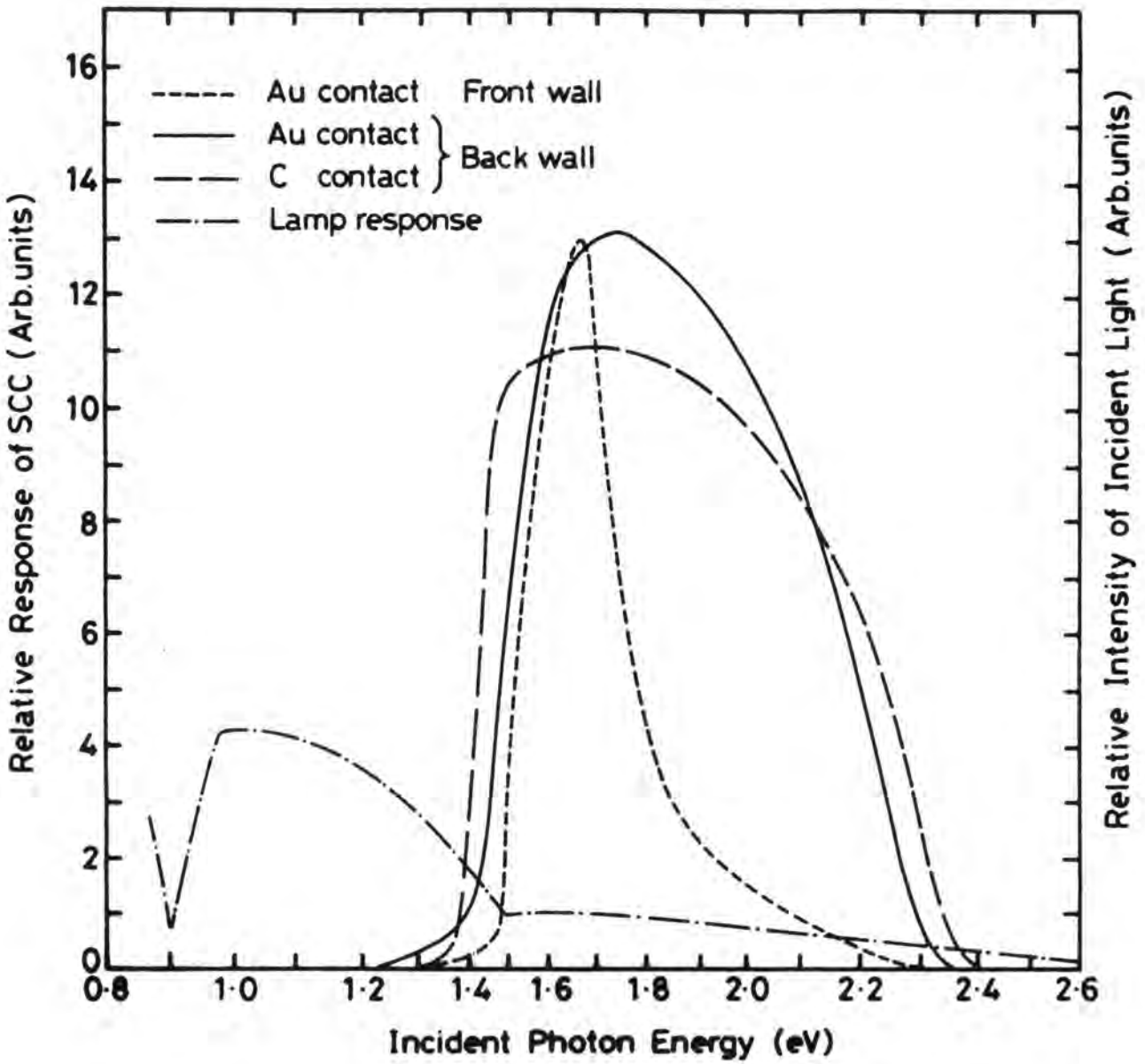


Fig. 8.9 (b) : SCC spectral responses of devices with different contacts (Au and C)

The diode and photovoltaic characteristics of a typical device are included in Figs 8.7 and 8.8 respectively. As with bulk crystal devices the diode characteristics with carbon contacts were much more rectifying than those with gold contacts. The rectification factor at 0.7 V, of 2×10^3 was more than 6 times higher than that of the Au-contact devices. The values of SCC, OCV and FF (Table 8.3) were correspondingly larger, particularly compared with the devices with evaporated Au contacts. Nevertheless, the photovoltaic output characteristic shows that these devices still had a high series resistance (mainly due to the CdTe) and thus a very low conversion efficiency. The spectral response of SCC and OCV for devices with C contacts did not differ markedly from those with Au contacts, except for magnitude (Fig 8.9).

As with the bulk single crystals, carbon contacts were superior to Au, although the performance of the thin film devices was limited by the high CdTe resistivity, rather than by the contact.

8.5 Optimization of Devices

8.5.1 Copper Doping of CdTe Layers

The as-grown CdTe layers had high resistivities leading to the high series resistance of the devices. Attempts to dope the CdTe films p-type with acceptor impurities during growth proved unsuccessful. However, a substantial reduction in resistivity was achieved using a post-deposition Cu doping procedure. This entailed the evaporation of a calculated quantity of copper onto the CdTe/CdS/SnO_x devices. Carbon paste for the contacts was then applied to the copper layer and the whole assembly was heated in nitrogen at 330-340°C for 30 minutes.

The improvement in the diode characteristics of devices treated in this way is evident from Fig 8.10 which compares the I-V characteristics of undoped devices with those doped with (nominal) concentrations of

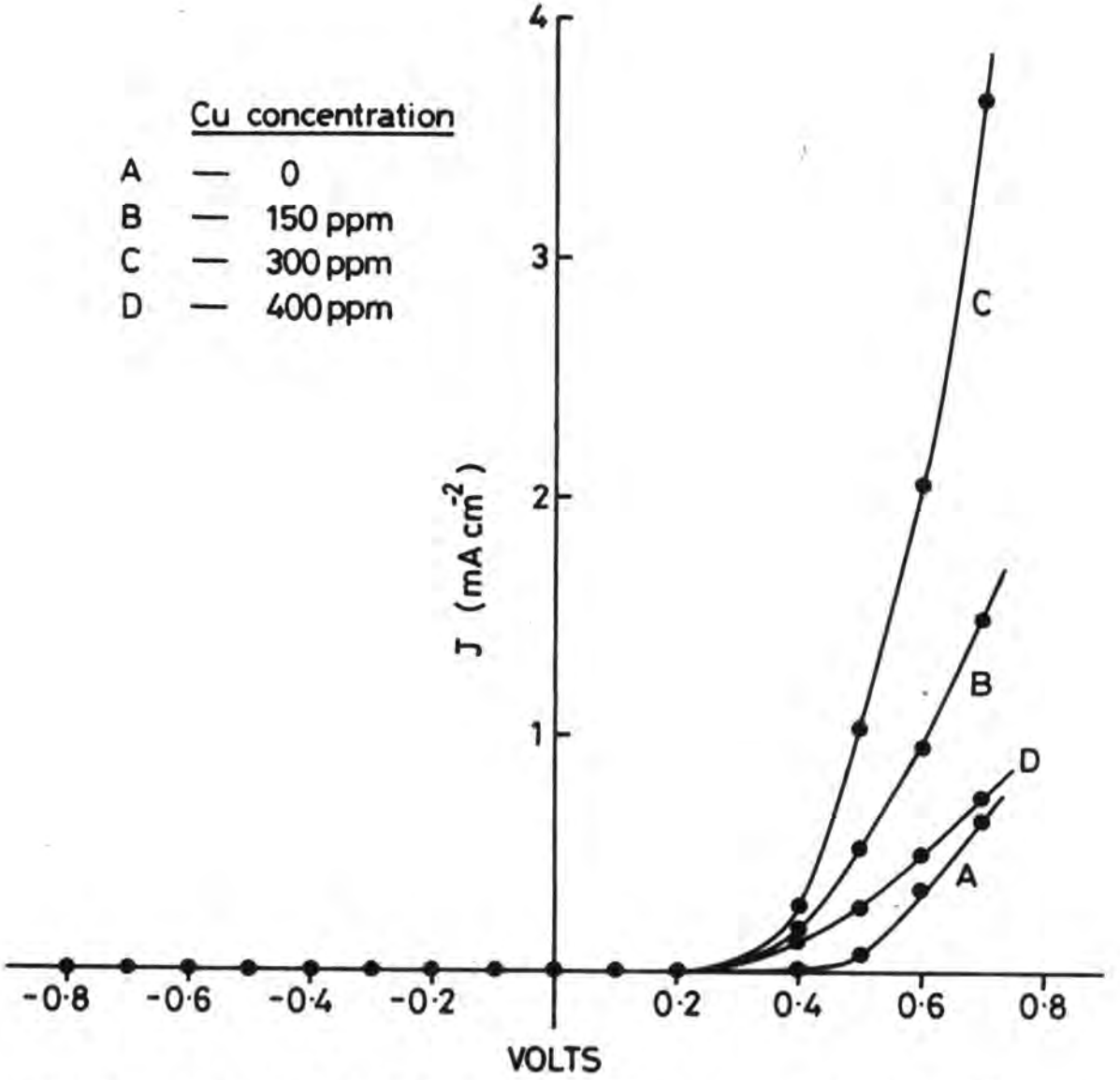


Fig. 8.10 : Diode characteristics of devices with different concentratins of Cu.

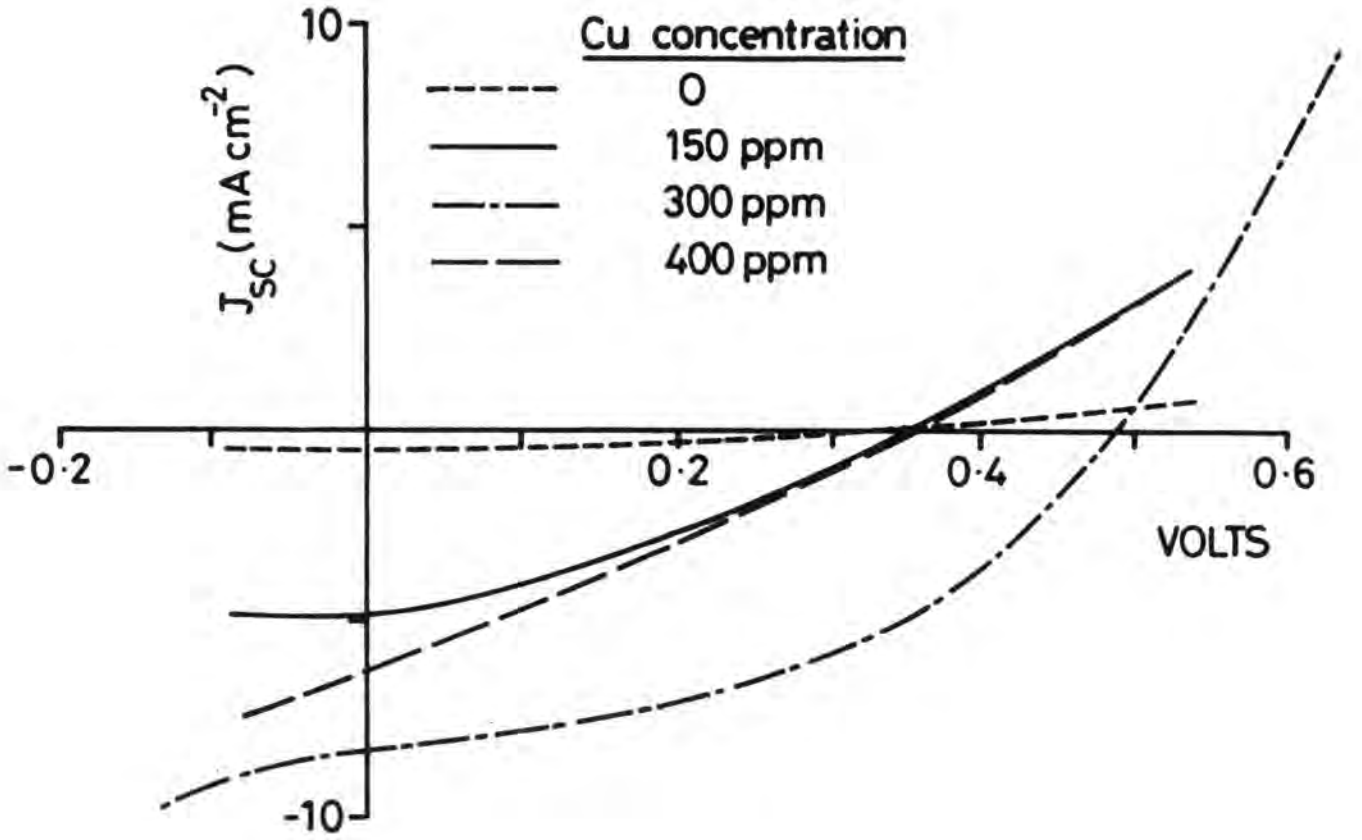


Fig. 8.11 : Photovoltaic characteristics of devices with different concentrations of Cu.

In general the noble metals Au, Cu and Ag substitute for the cadmium in CdTe where they act as acceptors. However, they may also occupy interstitial positions where they behave as donors (Section 7.3.5). With copper doping it is usually found that the free hole concentration is much less than the actual quantity of copper incorporated[37], suggesting that copper is being accommodated at both types of site, with a correspondingly high level of compensation. The degradation in performance at higher concentrations of Cu may indicate that an increased proportion of Cu ions were being located at interstitial sites, with a resulting increase in compensation. In addition it is possible that copper was precipitated at grain boundaries[41].

A similar effect has been reported by Akutagawa et al[42] and de Nobel who found that for large doping concentrations of Au, the resistivity of CdTe increased.

8.5.2 Effect of CdTe Thickness

If the absorber generator layer is thicker than required for complete absorption of the incident sunlight then the efficiency is reduced, since the resistance of the device will be larger than necessary. This is particularly important for devices using evaporated CdTe, where the resistivity is very high and a modest increase in the film thickness can add significantly to the series resistance. Consequently, a range of devices with different CdTe layer thickness was studied in order to determine the optimum thickness. Devices with different CdTe thicknesses of 10, 6 and 4 μm, but which were otherwise nominally identical and which had been doped with Cu as described in Section 8.5.1, were fabricated for this study.

The photovoltaic characteristics are given in Fig 8.12 ; performance parameters are given in Table 8.5.

TABLE 8.5: Solar cell parameters with different CdTe layer thickness.

CdTe Thickness μm	OCV volts	SCC $mA\ cm^{-2}$	FF %	η %
10	0.49	8.4	43	1.8
6	0.50	17.7	32	2.9
4	0.41	11.3	30	1.4

These results show that reducing the CdTe thickness from 10 to 6 μm increased the SCC by a factor of ∿ 2. However, this trend was not maintained and instead both the SCC and the OCV began to decrease when the thickness was reduced to 4 μm. These results indicated that a thickness of ∿ 6 μm was the optimum. However, the photovoltaic characteristics also showed that the best FF was obtained with a 10 μm thick layer. This result was unexpected, since one would suppose that the FF would be reduced with thicker layers due to increased series resistance. The reason for this is not clear, but may indicate that the Cu doping procedure was not fully optimized for the thinner layers. It may have been that copper had diffused into the CdS and consequently increased its resistivity.

The increase in the SCC with reducing thickness from 10 to 6 μm can be attributed to the reduction in the series resistance of the devices. It has been estimated[43] that a minimum thickness of 5 μm for the CdTe layer is necessary to ensure complete absorption of the light, so that the decrease in SCC and OCV with decreasing thickness from 6 to 4 μm may be partially due to incomplete absorption of light.

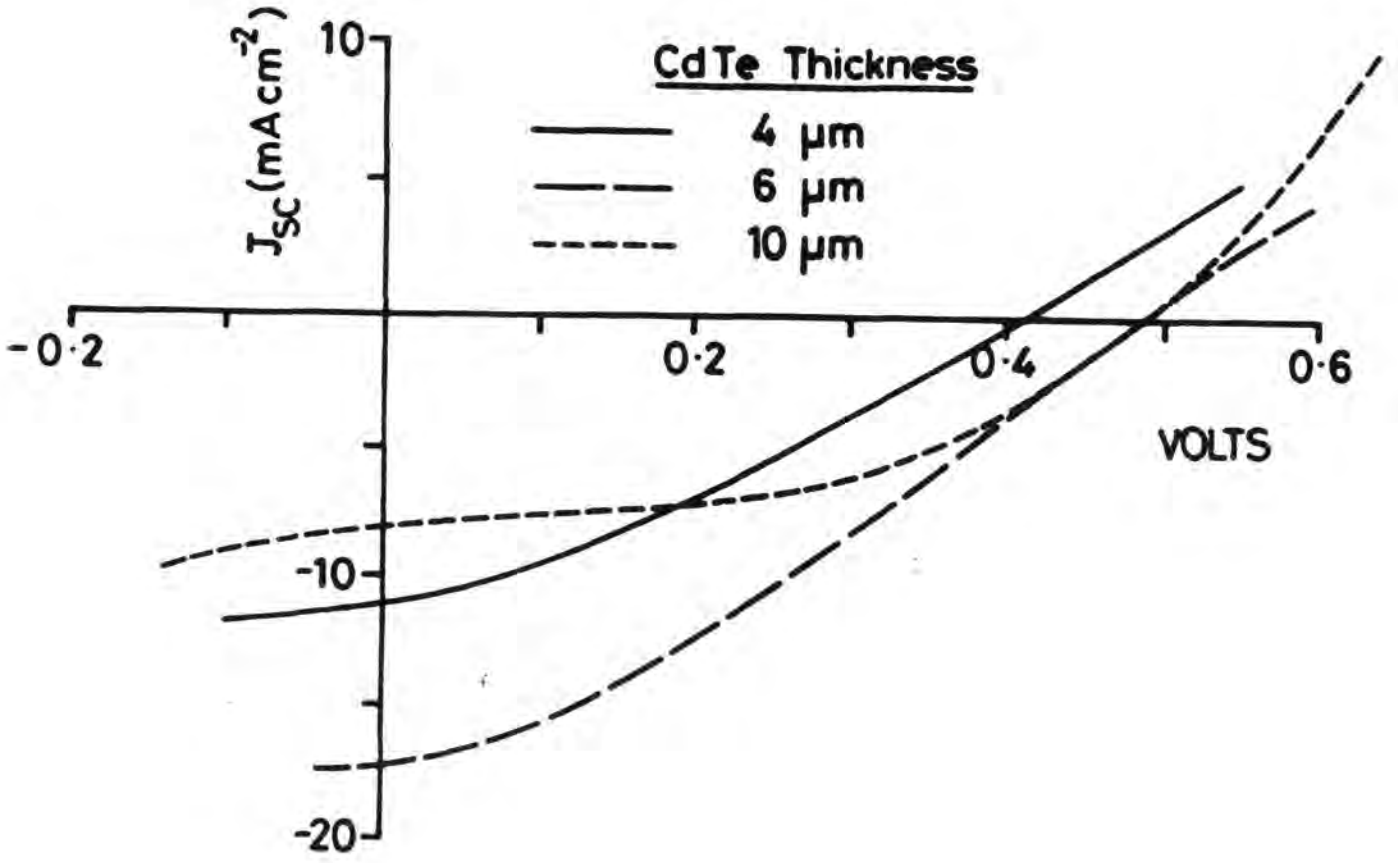


Fig. 8.12 : Effect of CdTe layer thickness on the photovoltaic characteristics

8.5.3 Effect of CdTe Layer Structure

It is important for efficient operation of most thin film solar cells that the crystallographic axis be correctly aligned with respect to the substrate[15]. Many thin films have a preferred axis along which the crystallites grow, and if deposition does not take place at normal incidence, then this preferred axis will not necessarily be perpendicular to the substrate. Instead it will lie at an angle between the substrate normal and the angle of incidence and will be dependent on film thickness[44].

It was found that films grown at T_s = 200°C had the best crystallinity. Therefore, all the CdTe thin films for CdS/CdTe devices were prepared at a substrate temperature of 200°C. In oder to determine whether an inclination of the substrate to the vapour beam during deposition of CdTe would affect performance, devices were fabricated with the CdS substrate located either directly above the CdTe crucible or to one side of it.

The photovoltaic characteristics of two devices - one with CdTe vapour beam normal to the substrate and the other at an inclination of 40-50° are given in Fig 8.13. It is clear that the parameters of the device with vapour beam normal to the substrate are superior to that grown off the normal incidence.

This can be explained in terms of the orientation of the crystallites with respect to the substrate normal. When the substrate was exactly over the charge crucible the orientation of the crystallites was normal to the substrate (RHEED and SEM micrograph in Figures 8.4 and 8.6). In this case the charge carriers can flow down the columnar crystallites without crossing grain boundaries. With crystallites inclined to the substrate normal, as shown by the RHEED diffraction

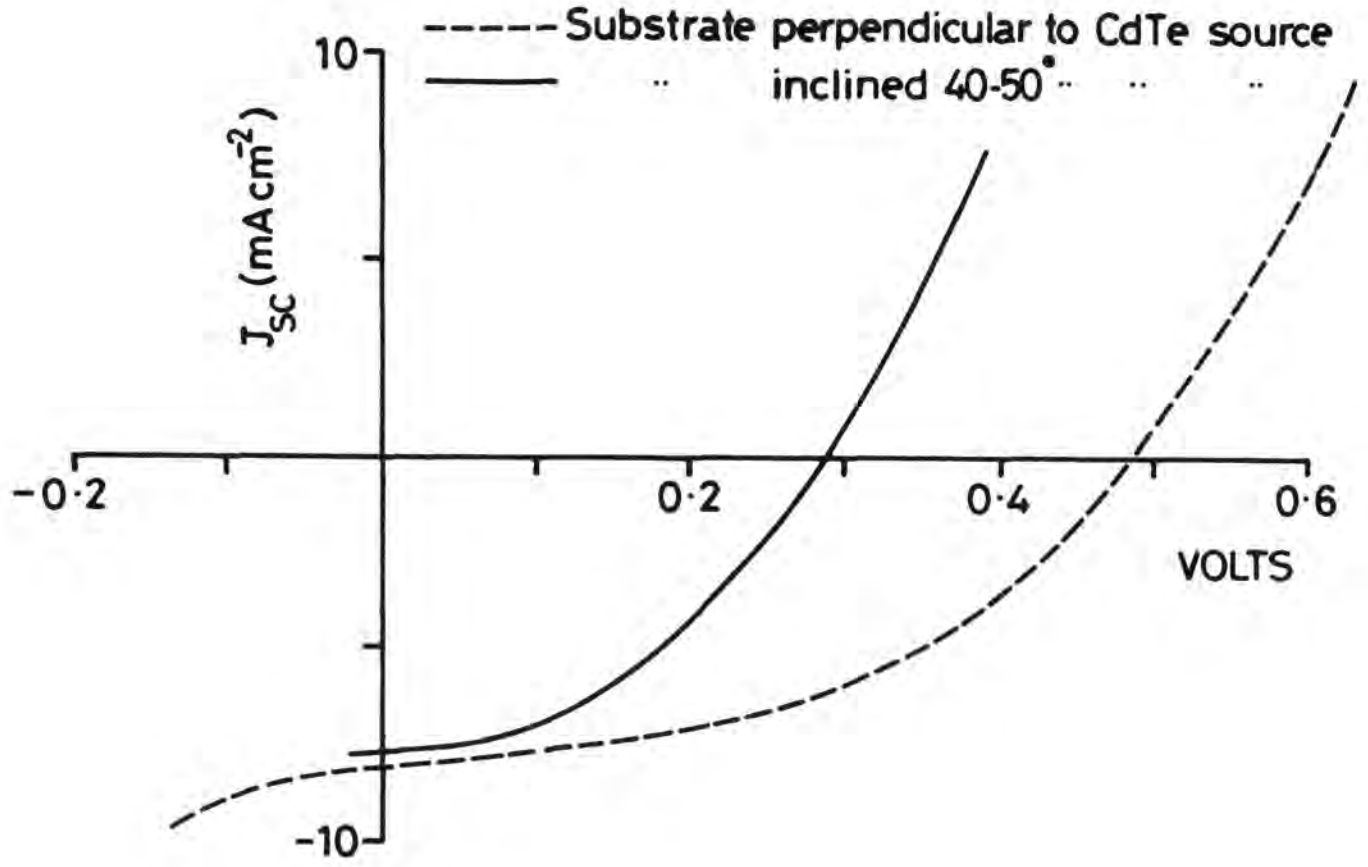


Fig. 8.13 : Photovoltaic characteristics of two devices employing layers deposited: (a) with the vapour beam normal to the substrates; and (b) at an inclination of $\sim 45^{o}$.

pattern in Fig 8.14, the charge carriers would have to cross different crystallites during transport, which would lead to increased recombination losses and a higher series resistance. Performance would necessarily be poorer. Moreover, the devices formed on films in which grains were not perpendicular to the substrates had a higher reverse saturation current. This would explain the small value of OCV (0.28 V) obtained with these devices.

8.5.4 Effect of Annealing Temperature

In order to optimize the annealing temperature, devices were fabricated under the same conditions but annealed at different temperatures for 30 minutes in nitrogen. Temperatures of 250, 330 and 450°C were used.

The photovoltaic characteristics of the devices measured under AM1 illumination are shown in Fig 8.15 and the performance parameters are listed in Table 5.6.

TABLE 8.6: Effect of annealing temperature on fevice parameters

Annealing Temp. °C	OCV volts	SCC $mA\ cm^{-2}$	FF %	η %
250	0.40	1.8	27	0.1
330	0.49	8.4	45	1.9
450	0.32	1.1	35	0.2

It is clear that devices annealed at 250 and 450°C had small values of SCC and OCV, and their characteristics indicated that they suffered from a high series resistance. The best performance was obtained when the devices were annealed at $\sim$ 330°C. This improved performance was also evident from the diode characteristics. The rectification ratio was greater than 10^3.

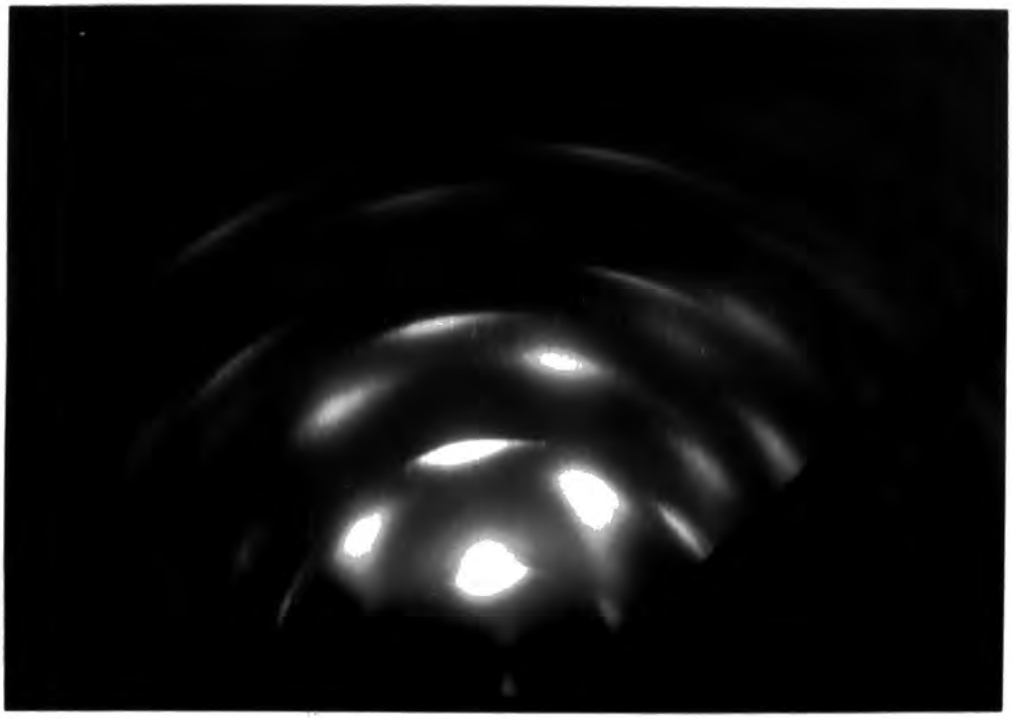


Fig. 8.14 : RHEED pattern from a CdTe film (grown at 200°C) with the vapour beam inclined at an angle of $\sim$ 45° to the substrate normal.

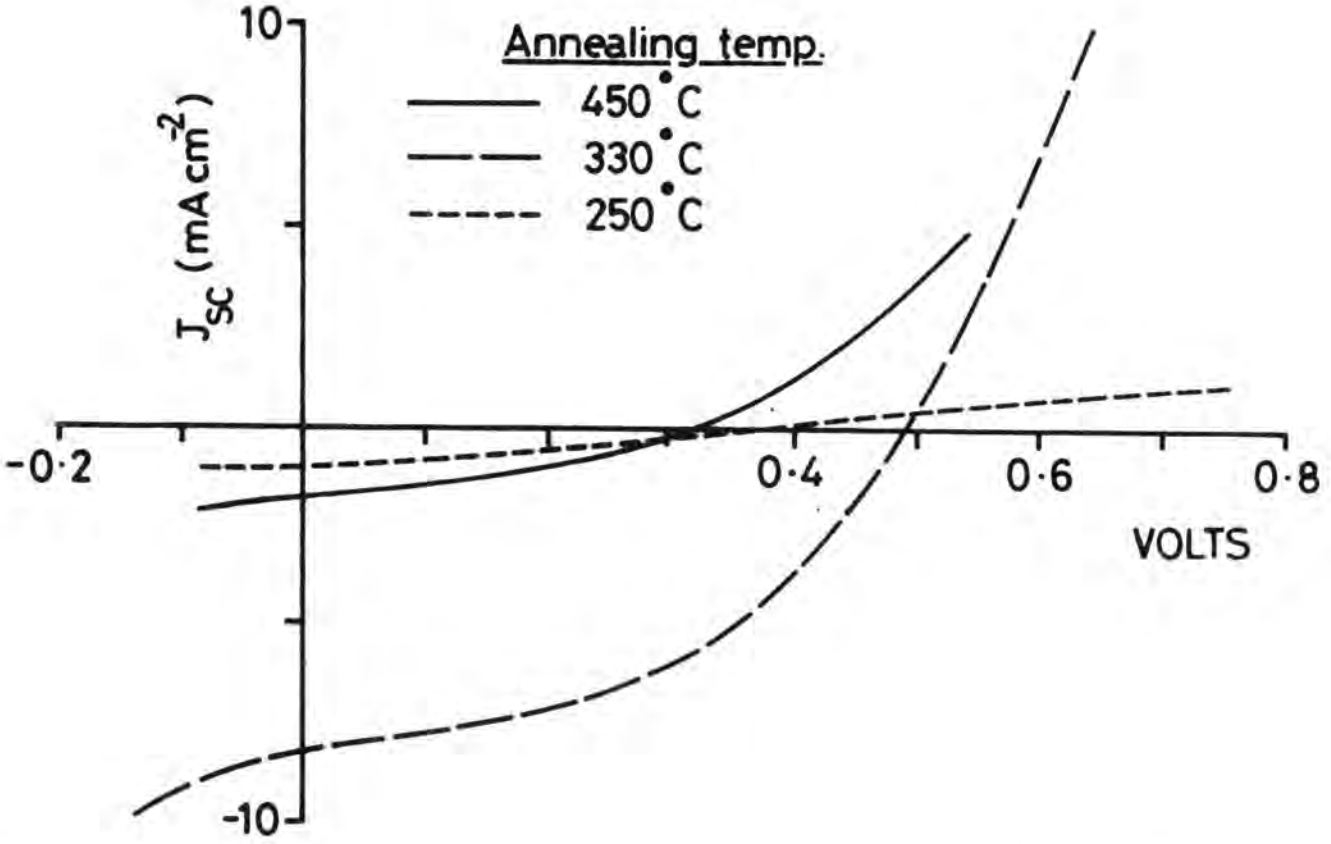


Fig. 8.15 : Photovoltaic characteristics of devices annealed at 250, 330 and 450°C in a nitrogen ambient.

The spectral response of the SCC and OCV is shown in Figs 8.16 and 8.17 where the greatest response is obviously for the devices annealed at 330°C. The device annealed at 450°C exhibited a sharp dip in the SCC and OCV characteristics at a photon energy of ∿ 1.52 eV.

As is evident from Fig 8.15 the series resistance of the devices annealed at 250 and 450°C was very high. The high series resistance for the devices annealed at 250°C could indicate that 250°C was too low for adequate diffusion of the copper into the CdTe layer. Conversely, a temperature of 450°C was too high, resulting possibly in the fast diffusion of Cu into the CdS layer. This idea is supported by the dip in the SCC and OCV spectral response of these devices which may indicate the presence of some impurity trapping levels in the CdS. Kuribayashi et al[45] have reported an otpimum annealing temperature of 400°C for the screen printed CdS/CdTe cells.

8.5.5 Effect of CdS Deposition Conditions

As already discussed in Section 8.2 the structural and electrical properties of the CdS films are strongly influenced by the substrate temperature T_s. The effect of these properties on thin films device performance was therefore investigated and is reported in this section. Heterojunctions were fabricated with CdS films deposited at substrate temperatures of 120,160, 180 and 300°C. All other conditions such as CdTe deposition, copper concentration, annealing temperature etc. were kept nominally the same (i.e. at optimum values).

The diode characteristics of the devices fabricated on CdS layers grown at different temperatures are shown in Fig 8.18, and the log J vs voltage plot of a device fabricated with a layer at 180°C is shown in Fig 8.19. It is evident that the diode characteristic was very rectifying for the device on the CdS layer deposited at 180°C (Fig 8.18)

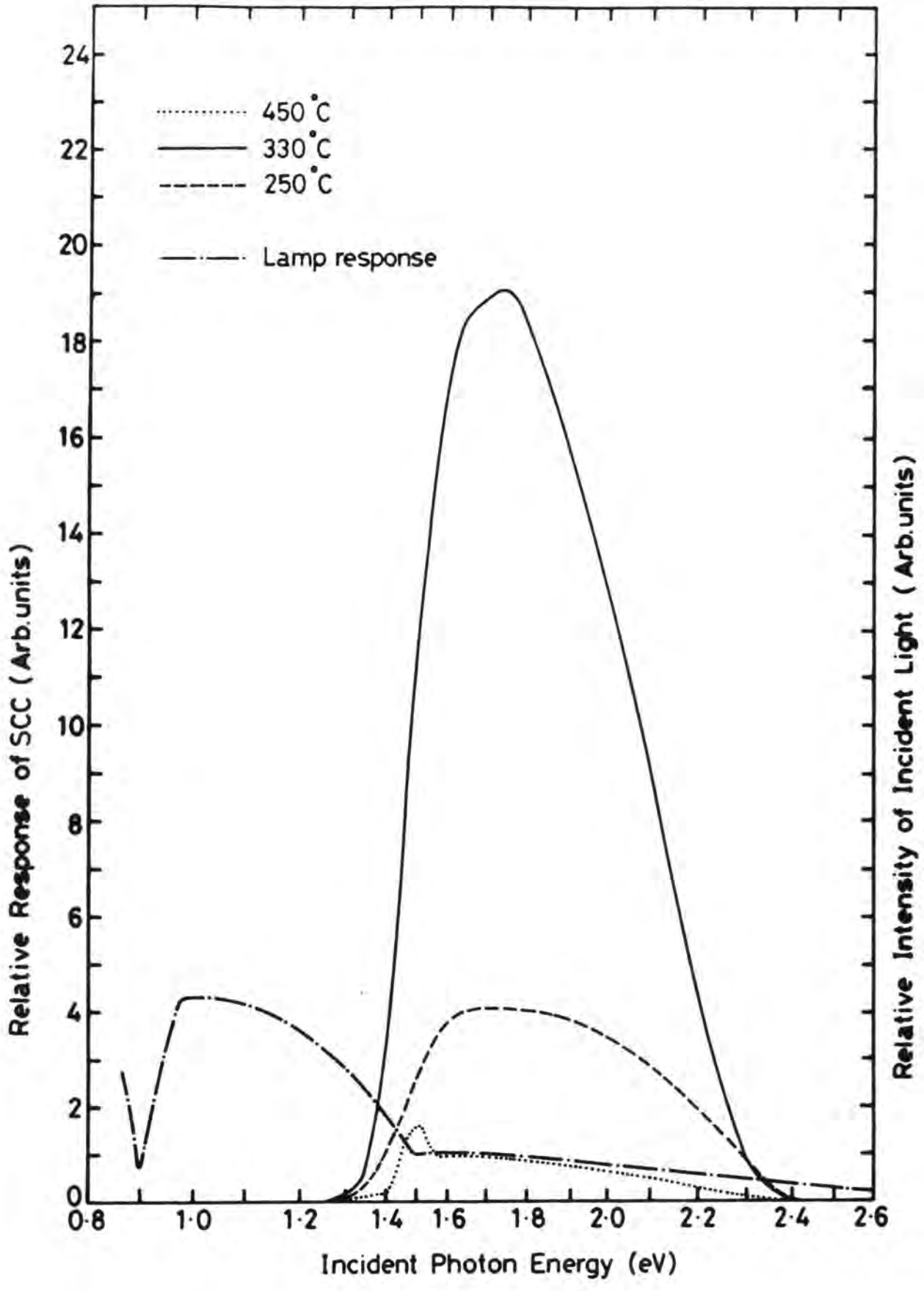


Fig. 8.16 : SCC spectral responses of devices annealed at different temperatures

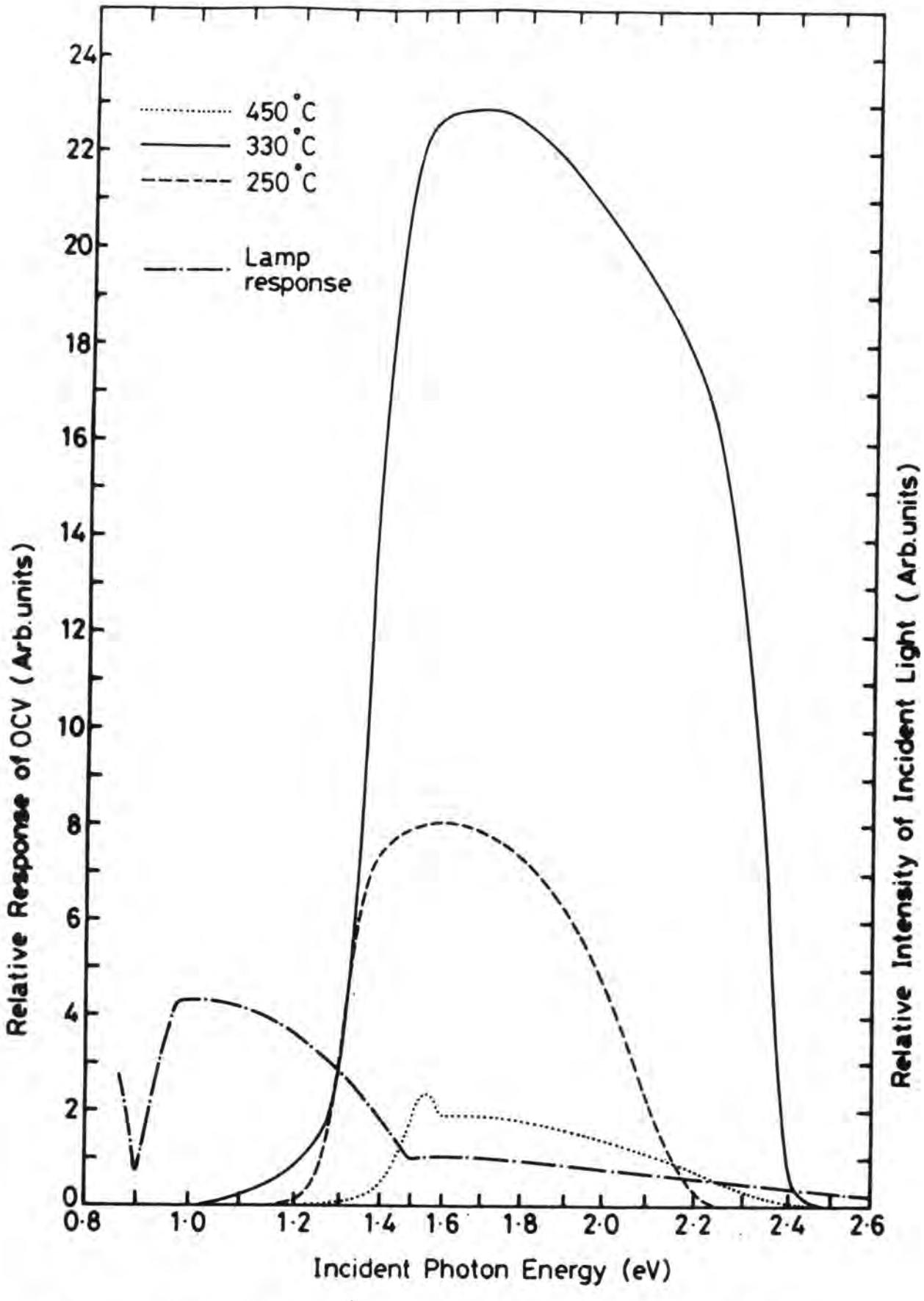


Fig. 8.17 : OCV spectral responses of devices annealed at different temperatures

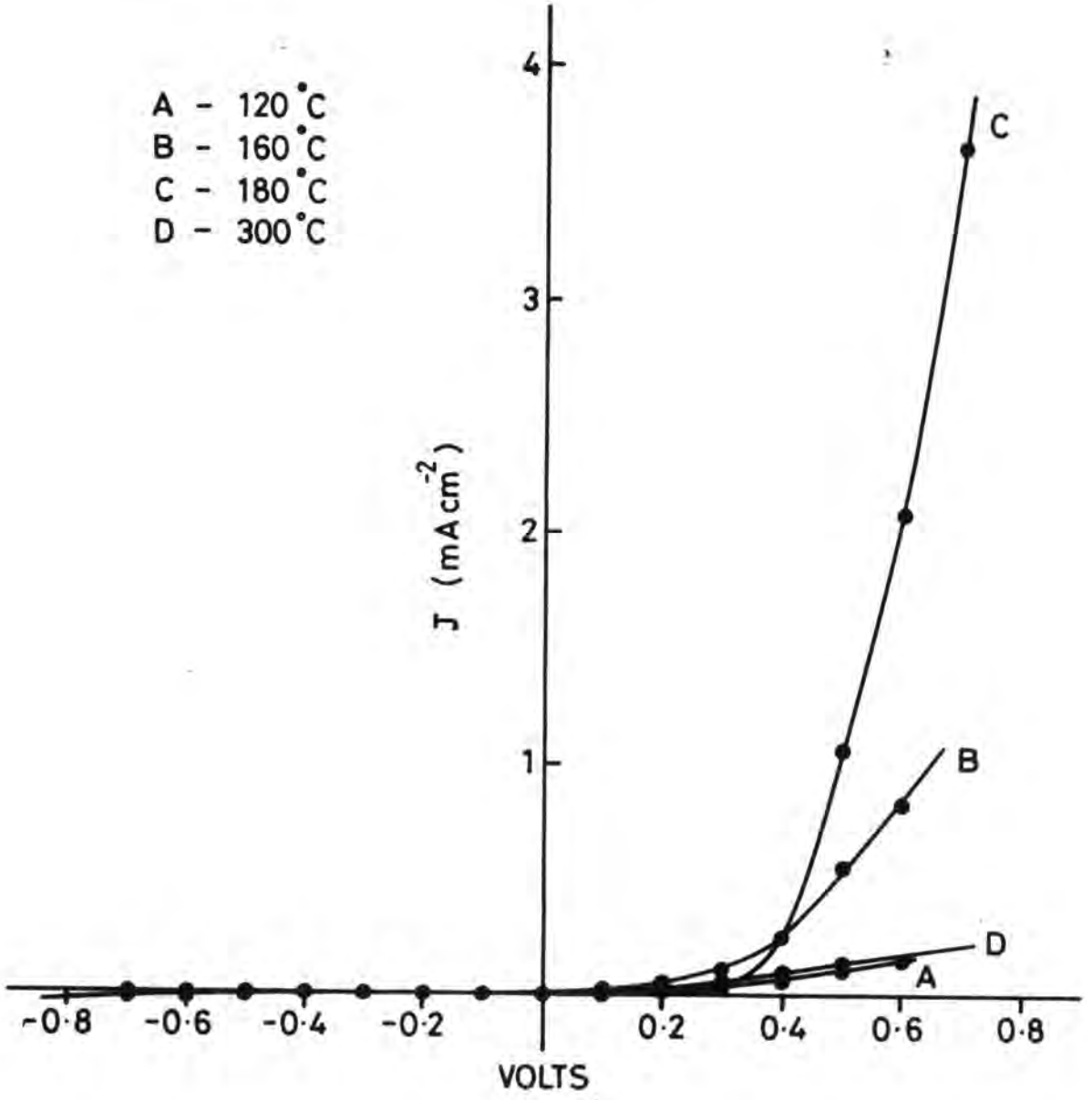


Fig. 8.18 : Diode characteristics of devices fabricated on CdS layers grown at different substrate temperatures

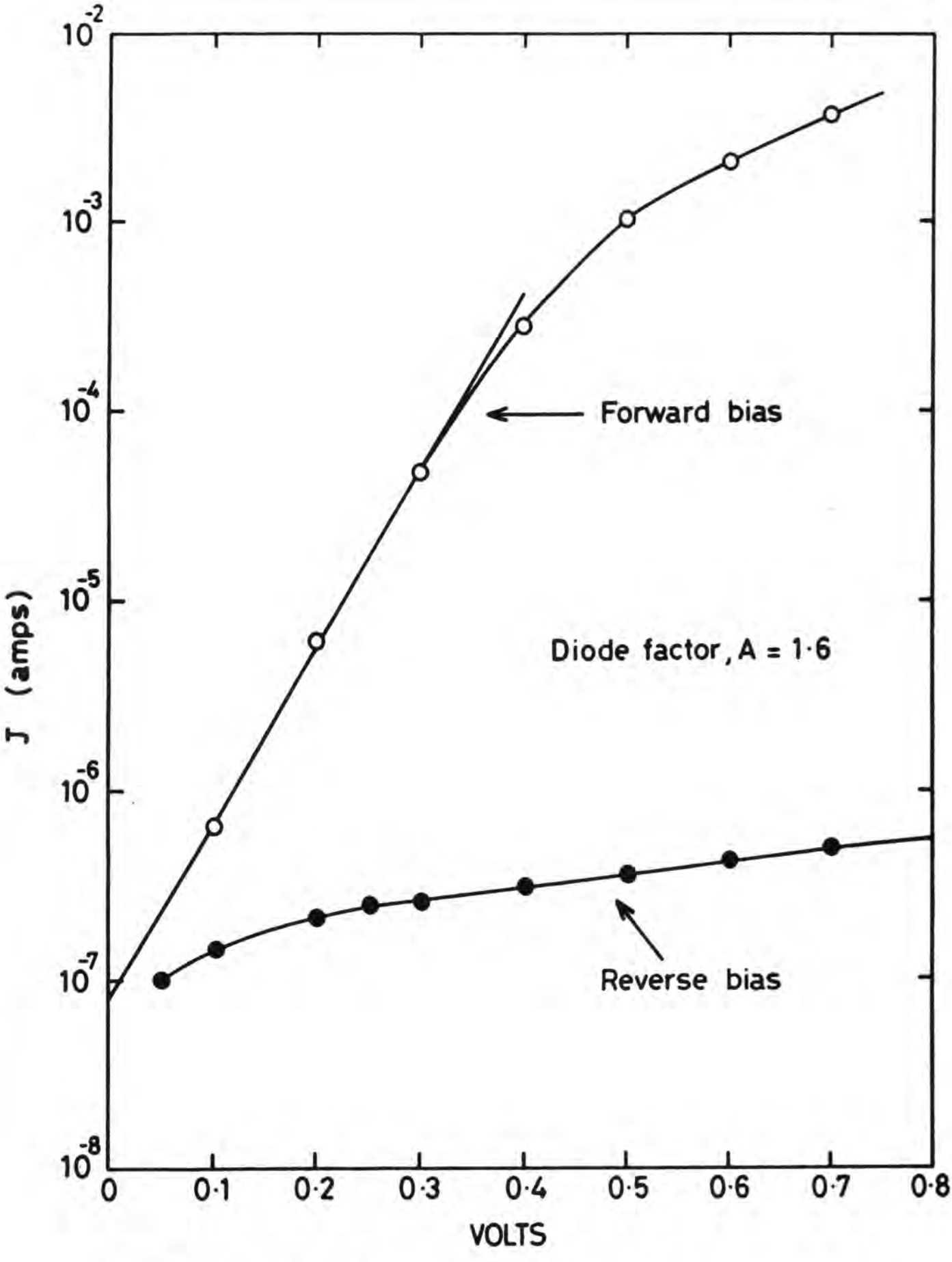


Fig. 8.19 : LogJ vs V plot of a typical device fabricated with a CdS layer grown at 180°C.

and was quite good for devices made using a temperature of 160°C. The ideality factor was 1.6 for the 180°C CdS device, whereas it lay between two and three for other devices. The value of the reverse saturation current for devices in which the CdS was grown at 120, 160 and 300°C was high.

The photovoltaic characteristics of the devices under AM1 illumination are shown in Fig 8.20. The performance parameters are listed in Table 8.7. The SCC, OCV, FF and efficiency η were highest for the 180°C device. These parameters improved with increasing substrate temperature (during CdS deposition) from 120-180°C and degraded when the temperature was increased beyond 180°C.

TABLE 8.7: Effect of CdS deposition temperature on device parameters

CdS Substrate Temp.	OCV volts	SCC $mA\ cm^{-2}$	FF %	η %
120	0.25	1.00	29	0.1
160	0.43	6.16	30	0.2
180	0.49	8.40	45	1.9
300	0.24	1.10	27	0.1

The OCV spectral responses are shown in Fig 8.21. The threshold occurs at ∿ 1.0 eV, well below the energy of the CdTe bandgap. Moreover, the peak response (∿ 1.5 eV) for devices fabricated on CdS deposited at 160 and 180°C was very much higher than in the other devices. The SCC response was similar except that the threshold occurred at ∿ 1.37 eV.

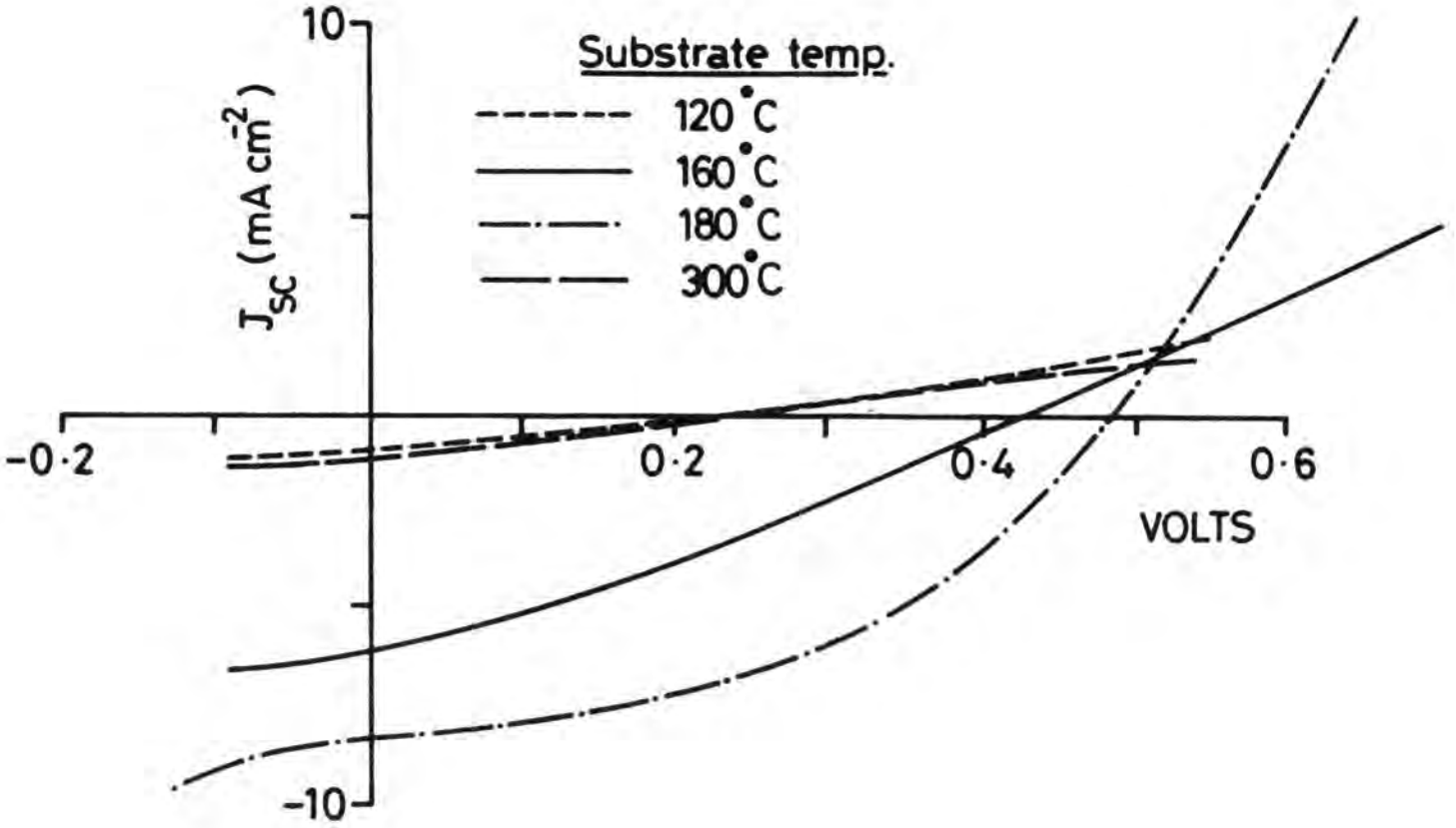


Fig. 8.20 : Photovoltaic characteristics of the same solar cells (Fig. 8.18).

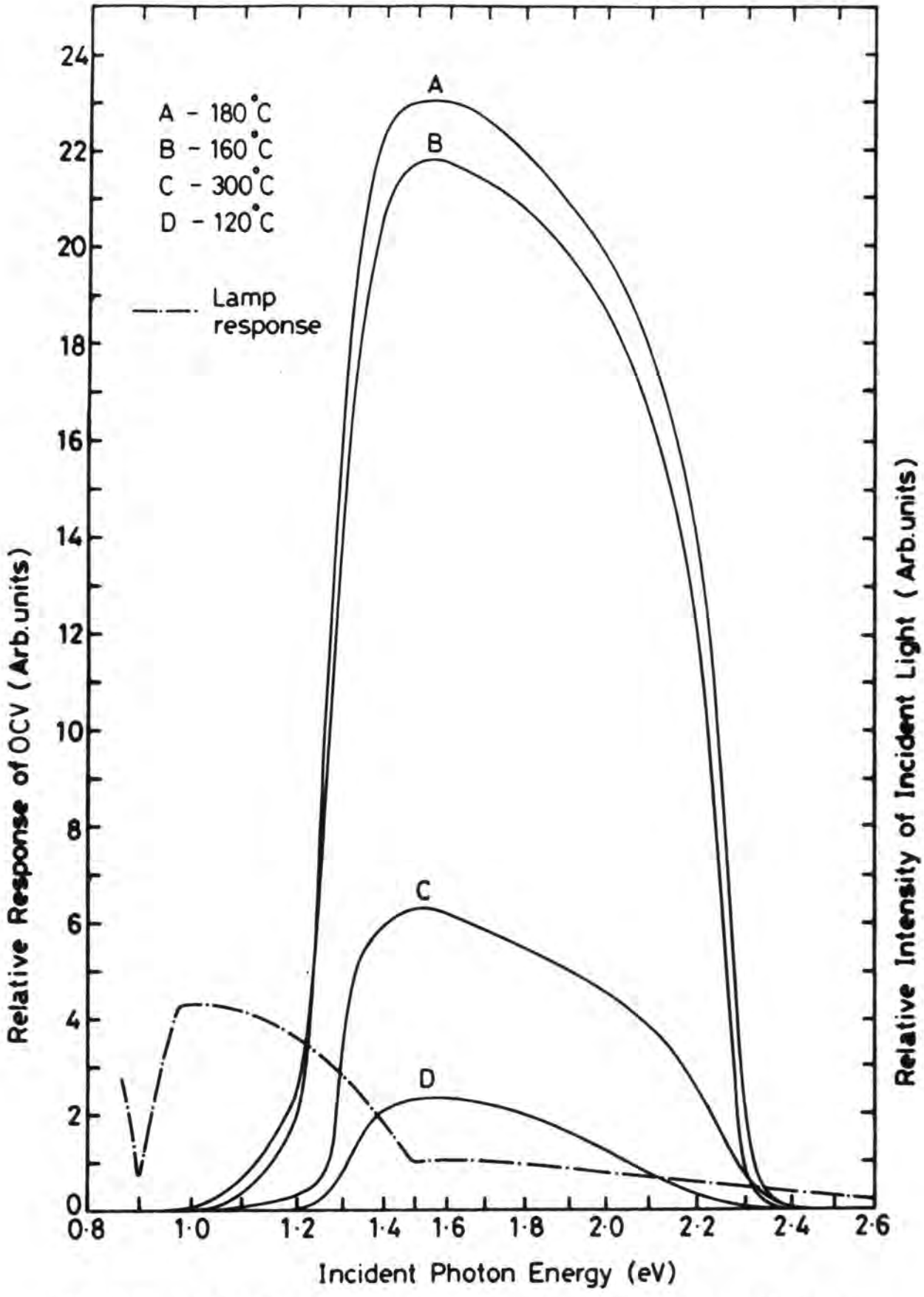


Fig. 8.21 : OCV spectral responses of devices fabricated on different CdS films

The effect of substrate temperature on the properties of CdS films (Sect. 8.2) was fully reflected in the device performance. The crystallinity of the film improved with increasing substrate temperature T_s from 120 to 180°C and it deteriorated thereafter. The resistivity of the films was also found to behave similarly. At the optimum substrate temperature of 180°C, the layer displayed a good columnar structure (Fig 8.3), with a reasonable grain size. This correlates well with the better photovoltaic properties of the devices with a CdS substrate temperature of 180°C.

The variation in OCV with the CdS substrate temperature has been observed by Anthony et al[46]. This dependence may be attributed to; (a) a change in the CdS carrier density with substrate temperature[47] and the consequent changes in junction profile (Rothwarf[48] has described a similar mechanism for $CuInSe_2$ solar cells) or (b) chemical changes at the CdS/CdTe interface, such as the formation of a CdS_xTe_{1-x} interlayer as described by Uda et al[5]. Since the substrate temperatures involved are not very high, the probability of chemical changes at the interface are remote. The low values of OCV observed at other CdS deposition temperatures are more probably the result of higher reverse saturation currents. These in turn may be associated with the poor crystallinity and reduced shunt resistance. The low fill factors of devices fabricated with 120, 160 and 300°C CdS substrate temperature are indicative of a higher series resistance. For CdS layers deposited at 300°C, this was probably the result of excess sulphur[17] as discussed in Section 8.2.1. However, at the lower temperatures, the high series resistance was more possibly the result of reduced crystal order.

The OCV threshold at photon energies well below the bandgap edge of CdTe may be due to defect or impurity states and possibly to the

Franz-Keldysh effect[44]. Here the field in the junction can enable the generation of electron-hole pairs at photon energies below the bandgap, by a tunneling assisted transition.

8.5.6 Effect of Cell Dimensions

The fabrication of large area solar cells for terrestrial applications is one of the ultimate aims of solar cell research. In this work small scale devices with different dimensions were studied, in an attempt to understand the effect of the size of the active area of the cells. Generally the devices were fabricated in circular shape (5 mm dia) but for optimization of the cell area, devices with rectangular geometries were used. In these structures a uniform layer of CdS was deposited on a tin oxide coated glass slide and then CdTe was evaporated through a steel mask with rectangular slits of fixed length (12 mm) and variable width (3,4,5 and 6 mm). Other fabrication conditions were kept nominally identical.

The diode characteristics of four typical devices with widths of 3,4,5 and 6 mm are shown in Fig 8.22a and the photovoltaic output characteristics are given in Fig 8.22b. The device parameters are summarized in Table 8.8.

TABLE 8.8: Effect of cell dimensions on performance parameters

CdS Dimension (Width in mm)	OCV volts	SCC $mA\ cm^{-2}$	FF %	η %
3	0.48	13.75	39	2.6
4	0.51	14.80	41	3.1
5	0.29	9.34	41	1.1
6	0.17	2.35	40	0.2

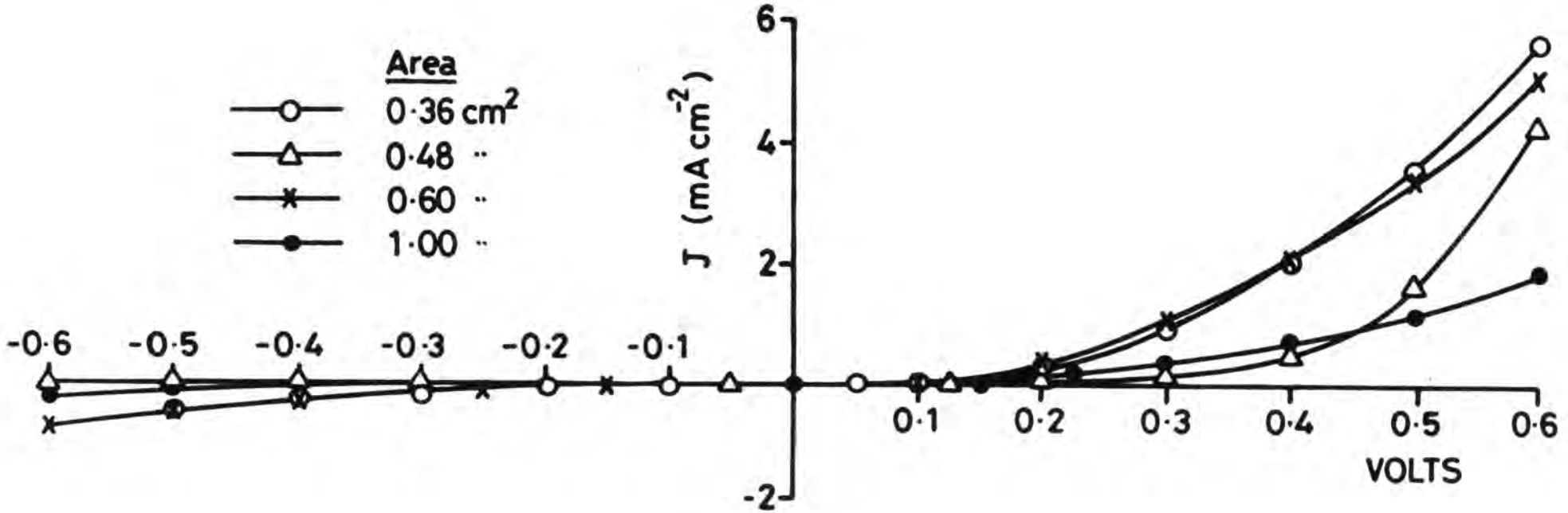


Fig. 8.22 (a) : Effect of cell area on the diode characteristics.

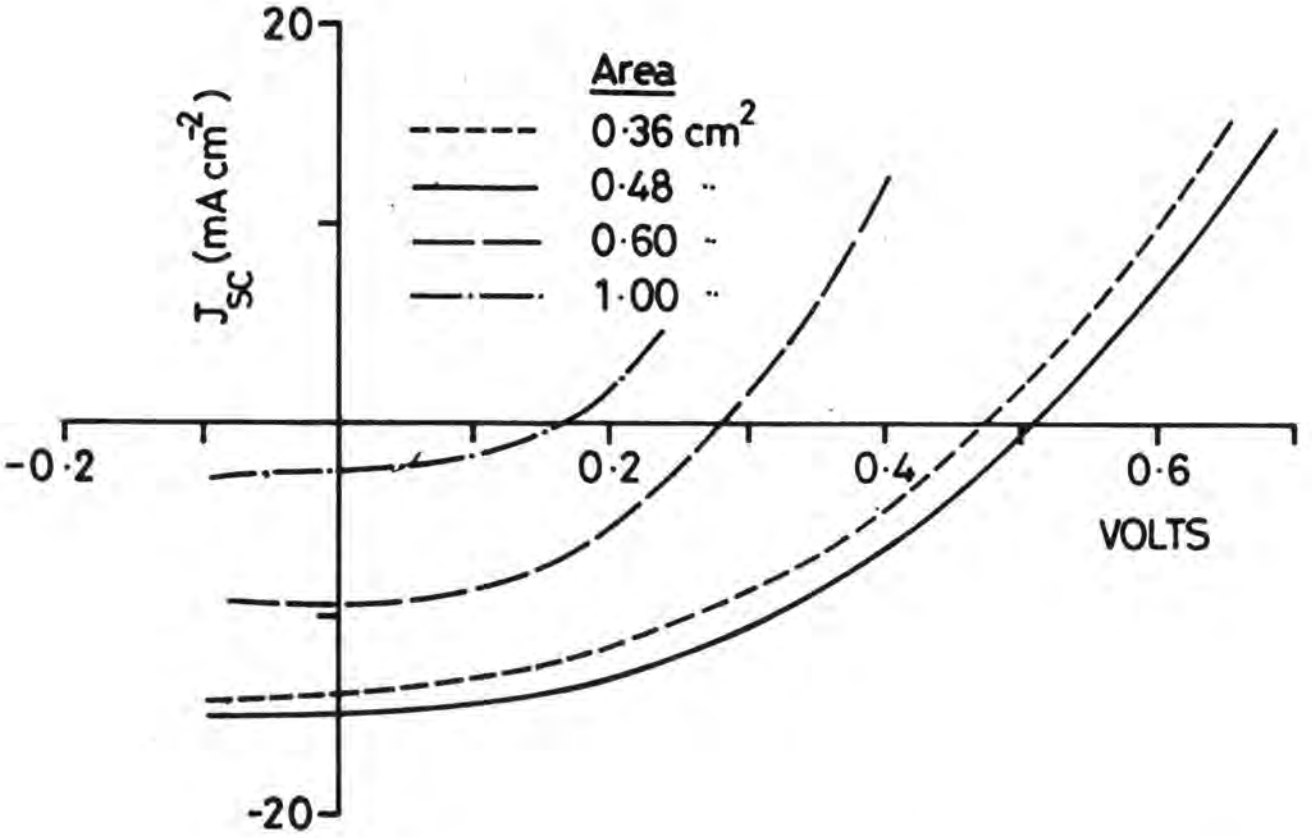


Fig. 8.22(b) : Effect of cell area on the photovoltaic characteristics

It is clear from Fig 8.22a, that the 4 mm wide devices had the best diode characteristics. As the width was increased beyond this the devices became progressively less rectifying. A similar situation was obtained for the photovoltaic characteristics. Again, the best performance occurred for the 4 mm width devices, although 3 mm devices were only marginally less good. When the cell width was increased beyond 4 mm the OCV and SCC fell sharply. The reduction in OCV was in line with the increase in reverse saturation current observed in the diode characteristics. These results approximately confirm the findings of Matsumoto et al[50] in screen printed cells that the optimum width of CdTe was around 5 mm. In the present case the most efficient device had an area of 0.48 cm^2 when an efficiency of 3.1% was achieved. The reason why large area devices had poor characteristics is not entirely clear, but may be related to decreased shunt resistance and the greater chance of junction defects being present.

8.5.7 Degradation Studies

The effects of ageing on device performance were also studied. SnO_x/CdS/CdTe/C devices were fabricated in the usual way with 300 ppm Cu, and then given a 30 min anneal in nitrogen. The photovoltaic output characteristics were recorded and subsequently remeasured after several months storage in the laboratory. Surprisingly, it was found that the overall efficiency of the devices improved with time. The output characteristic of a typical device (180°C CdS) measured immediately after fabrication and 10 months later are shown in Fig 8.23. The SCC had slightly degraded over this period but at the same time the value of the OCV and the fill factor had improved so that the overall efficiency of the device had increased from 2.2 to 2.4%. The characteristics show that the series resistance of the device decreased during this period.

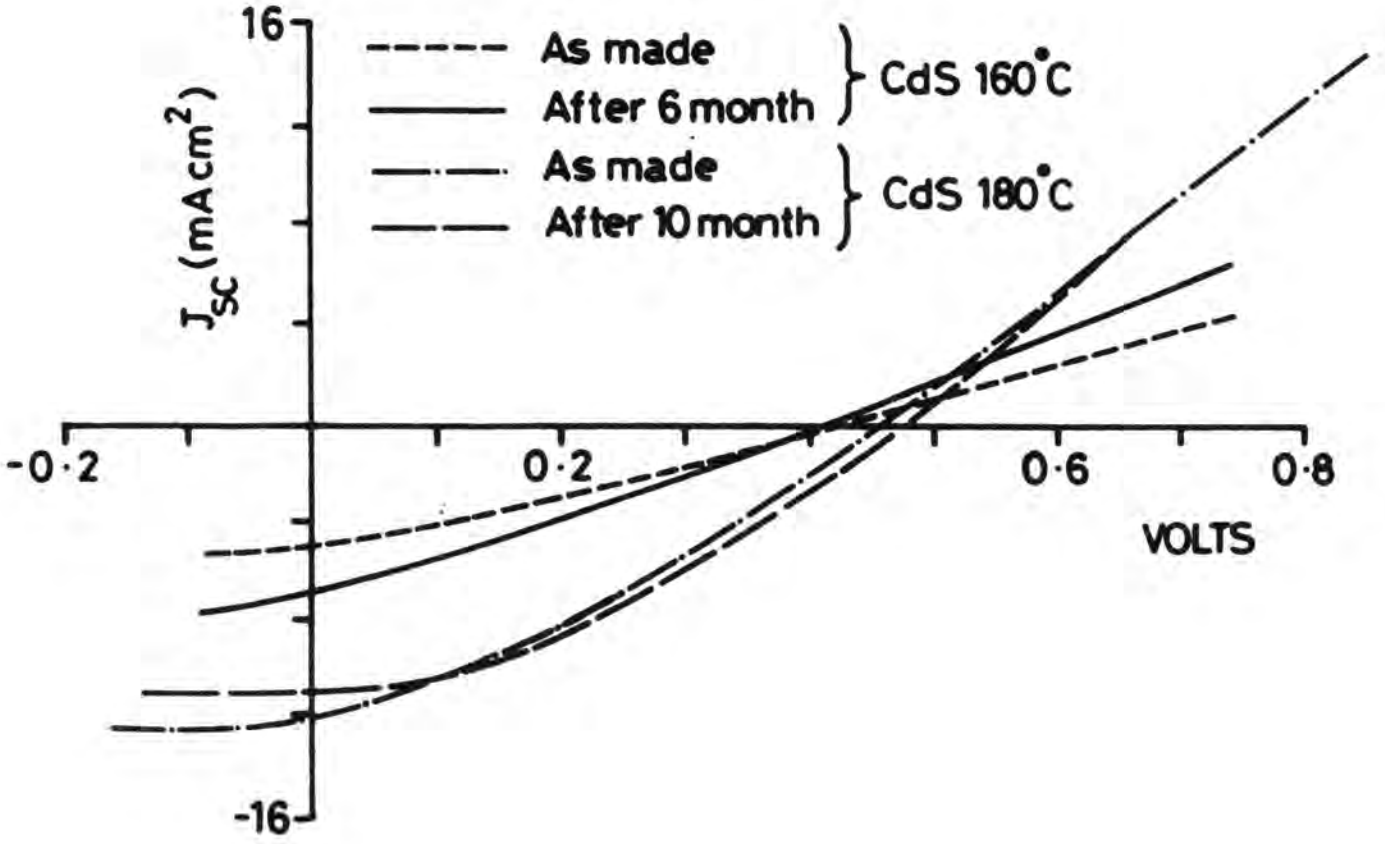


Fig. 8.23 : Photovoltaic characteristics of as-made and aged devices

In another device (CdS deposited at 160°C) there was a significant improvement in the SCC and the overall efficiency improved from 0.2% to 1.0% over a period of 6 months. The PV characteristics of this device are shown in Fig 8.23. The spectral response of the SCC and OCV of the as-made and aged devices were also measured. The spectral response of the devices had again improved with ageing.

The improvement was due to a decrease in the series resistance of the devices with time. The reason for this is not known, but may be related to additional in-diffusion of acceptor impurities into the CdTe from the carbon paste used to form the ohmic contacts. It was also found that with the device made on CdS layer deposited at 160°C there was an improvement in SCC and overall efficiency but a slight reduction in the OCV and fill factor. As observed during the structural studies the films grown at 160°C had poor crystallinity and a smaller grain size than the films grown at 180°C. This could lead to an increase in number of the shunting paths and the in-diffusion of impurities may have resulted in the reduction of shunt resistance and hence a slight decrease in the OCV and FF.

8.5.8 Devices with CdS on CdTe

(a) Carbon contacts: Most of the devices fabricated during this work had the tin oxide glass/CdS/CdTe/contact structure, but some devices, in which the CdS and CdTe layers (and their respective contacts) were inter-changed, were also investigated. In this structure a thin layer of carbon paste was screen printed onto an ordinary glass slide. Copper was then evaporated onto the carbon layer. Next, CdTe and CdS were deposited sequentially (Sect. 4.5) and finally indium was evaporated to provide the ohmic contact to the n-CdS.

The I-V characteristics of these devices were measured in the dark and under illumination as usual. A typical set of characteristics is shown in Fig 8.24. The reverse saturation current was much higher than for corresponding devices with the mirror structure. The device parameters were also low. Heat treatment $\sim$ 330°C for 30 minutes in nitrogen produced a slight improvement with the SCC increasing from 3.4 to 4 mA cm^{-2}, but the overall performance was still poor. The spectral response of the SCC and OCV of the as-made and heat treated devices did not differ greatly from those of the mirror devices, except in magnitude.

The photovoltaic characteristics show that the series resistance was higher than that in the more usual structure. This indicates that the copper did not diffuse fully into the CdTe at the substrate temperatures ($\sim$ 200°C) employed for the CdTe and CdS evaporation. Nevertheless, the value of SCC which was achieved was still greater than that for undoped devices, indicating that some diffusion of copper had occurred. The high value of reverse saturation current and lower copper concentration at the CdTe/CdS heterojunction interface would give rise to a small barrier height at the junction and consequently a low OCV. The high value of reverse saturation current may have been due to the fact that the surface of the screen printed carbon was not smooth enough to ensure that short circuiting through a few micron thick CdTe did not occur. These shunting paths would lead to an increase in reverse saturation current.

(b) Cr/Au contact: A few devices were fabricated where the cadmium telluride layer was deposited onto a glass slide coated with successive layers of chromium and gold. A CdS layer was then evaporated onto the CdTe in the usual way. The gold layer was intended to make an ohmic

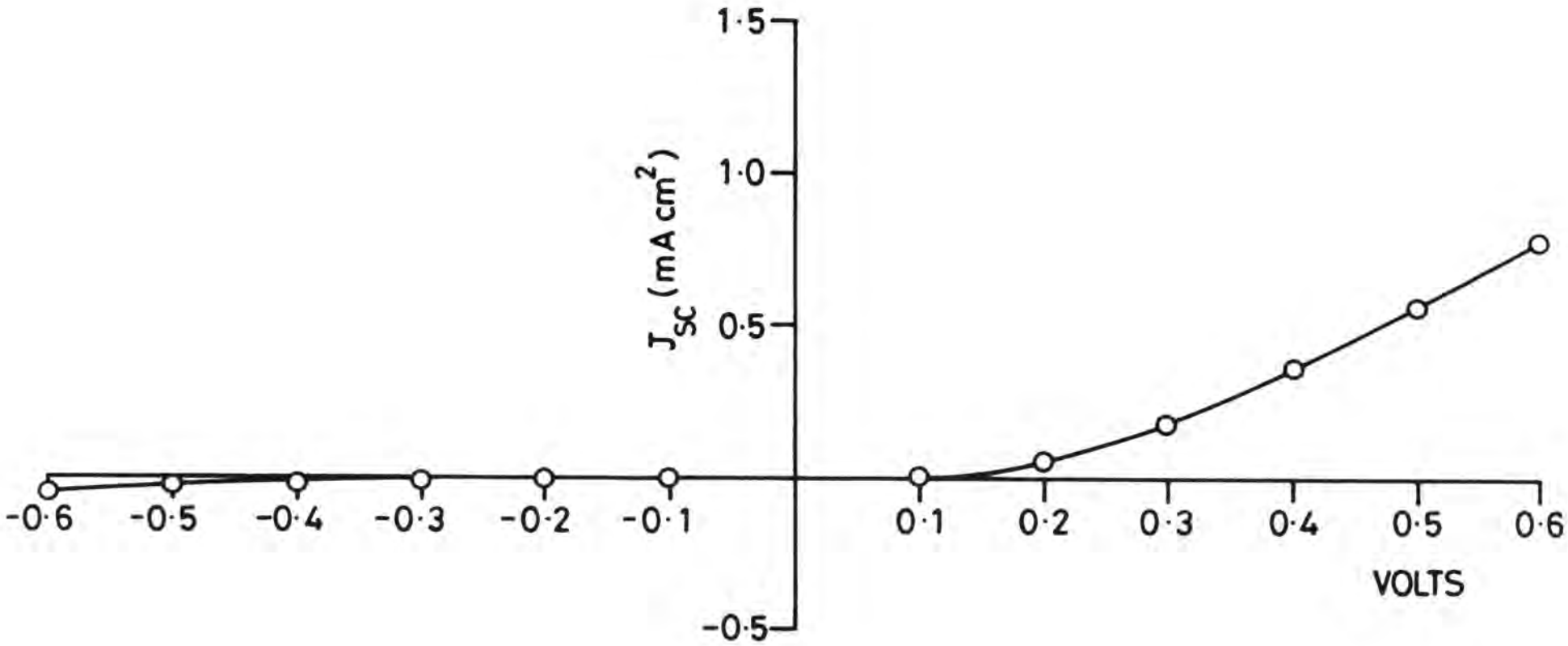


Fig. 8.24 (a) Diode characteristic of a device with screen printed C contact to CdTe

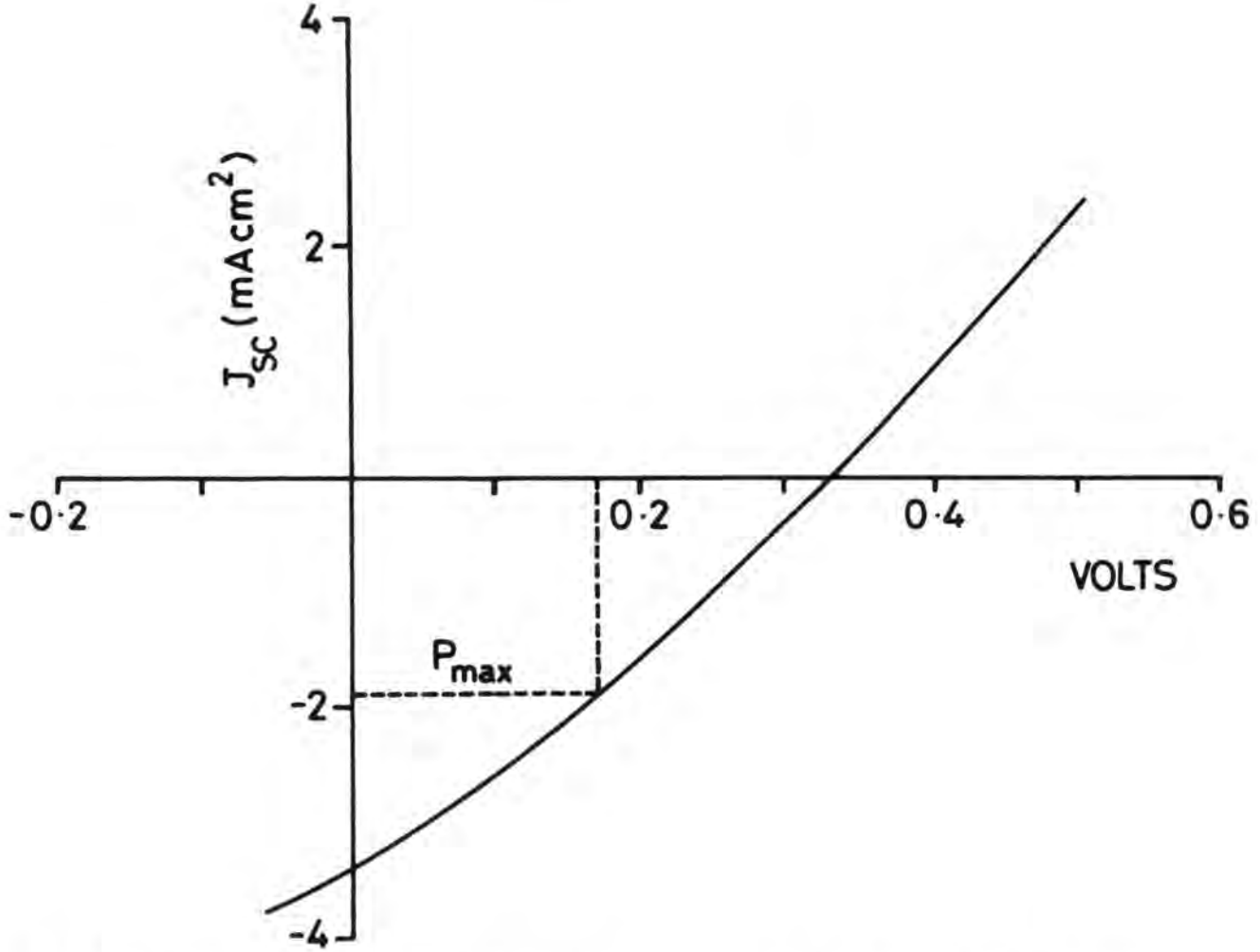


Fig. 8.24(b) : Photovoltaic characteristic of the same device (Fig. 8.24(a))

contact to the CdTe while an evaporated indium dot (∿ 1mm diameter) was used to make contact to the n-CdS. The CdTe layers were undoped. When these devices were characterised, it was found that their photovoltaic performance was very poor with a very small short circuit current and a low OCV of ∿ 0.35 V. This behaviour resembled that of devices with a tin oxide/CdS/CdTe/Au structure (Sect.8.4.2). After heat treatment in vacuum at ∿ 375°C for 20 minutes the device performance was found to degrade.

Since the SCC was very low the photovoltaic output characteristics were not measured in detail. However, the spectral responses of the SCC and OCV were measured both before and after heat treatment. Fig 8.25 shows the OCV and SCC spectral response of an as-made and a heat treated device. The threshold for the SCC and OCV responses occurred at 1.2 eV and ∿ 1.0 eV respectively. A sharp dip at photon energies of ∿ 1.5 eV appeared in the SCC response of the as-made device. In the heat treated devices the spectral response of the OCV and SCC can be seen to reverse direction over the wavelength range 1.3 to 0.85 μm (Fig.8.25a)i.e. when the photon energy was less than the band gap of CdTe, the device showed a negative response.

The poor performance of these devices can be attributed firstly to the high resistivity of the CdTe layer and secondly to the high contact resistivity between CdTe and gold. The sharp dip at 1.5 eV in the SCC response may be related to impurity (accidental) levels in the CdS, while the low energy thresholds (at photon energies below the band gap of CdTe) probably indicated the presence of defect states near the valence band of CdTe[15]. The most interesting effect of the chromium-gold contact appeared when the devices were heat treated. The change in polarity of the response probably implies the presence of two

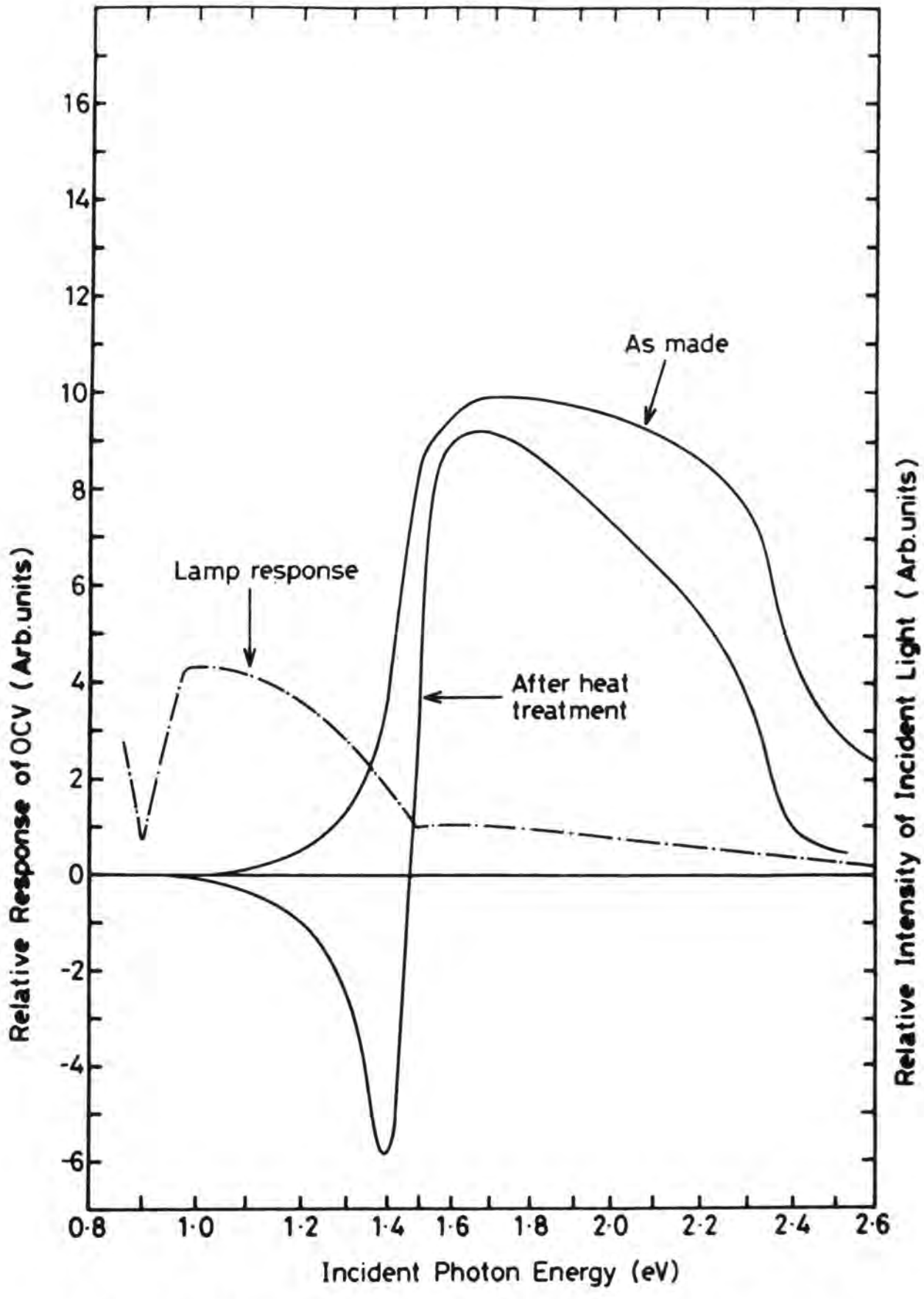


Fig. 8.25(a) : OCV spectral responses of an as-made and heat treated (375^{o}C) device with Cr/Au contact to p-CdTe.

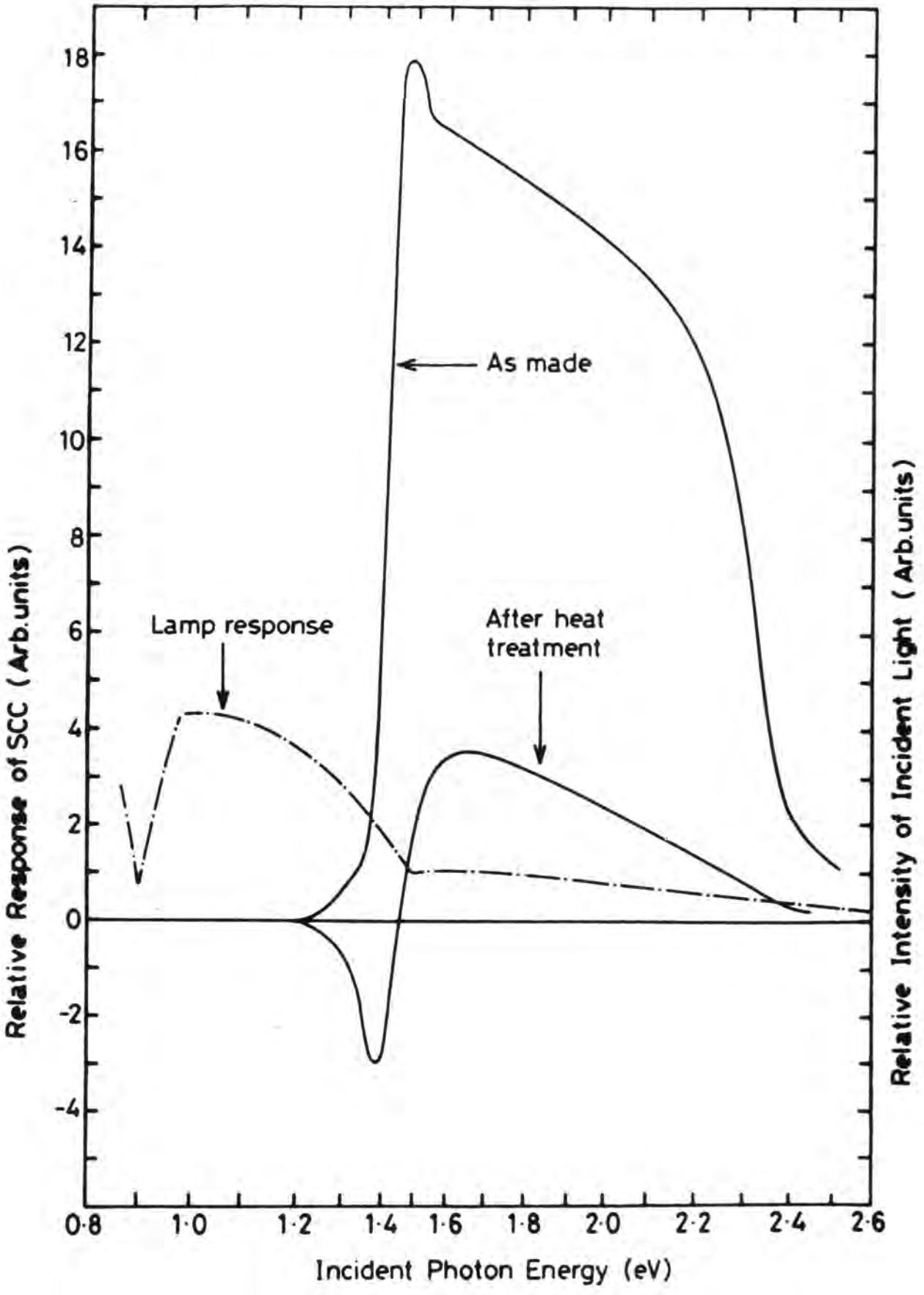


Fig. 8.25(b) : SCC spectral responses of an as-made and a heat treated (375°C) device with Cr/Au contact to p-CdTe

junctions with opposite senses (this indicates that the annealing temperature was too high). This argument is supported by the fact that excessive heat treatment of Au or Ni contacts on p-CdTe causes a solid-solid reaction and the formation of Ni/Au telluride[51] which forms a heterojunction with the underlying CdTe. This would appear to have happened here. The corresponding junction would give a photovoltaic effect in the reverse direction to the CdS/CdTe heterojunction as is indicated by the spectral response.

8.6 Photocapacitance Measurements

In order to gain a full understanding of the devices, the spectral dependence of steady state photocapacitance (PHCAP) was measured. For this, SnO_x/CdS/CdTe/C structures were fabricated in the usual way but with 300 and 400 ppm (nominal) concentrations of Cu.

Fig 8.26 shows the PHCAP spectra of a device with 300 ppm of Cu, measured at 300 and 85K. It is evident from the room temperature spectrum that the main positive going threshold occurred at $\sim$ 1.14 eV. This would correspond to the transition of electrons to the conduction band from a level $\sim$ 0.36 eV above the valence band of CdTe. Independent confirmation of this was provided by DLTS (Sect.6.4) which indicated the presence of a majority carrier (hole) trap 0.35 eV above the valence band. The steady decreasing trend in the photocapacitance at energies below 1.14 eV, probably arises from the filling of this level with valence electrons. Had the instrumentation been capable of resolving lower energies (lower energy limit was $\sim$ 0.6 eV) then one would have expected to observe a negative going threshold at $\sim$ 0.35 eV. This level is probably due to the copper dopant, which would be expected to give rise to an acceptor level at this energy[37,38]. The 1.14 eV threshold would move to higher energies at lower temperatures in proportion to the

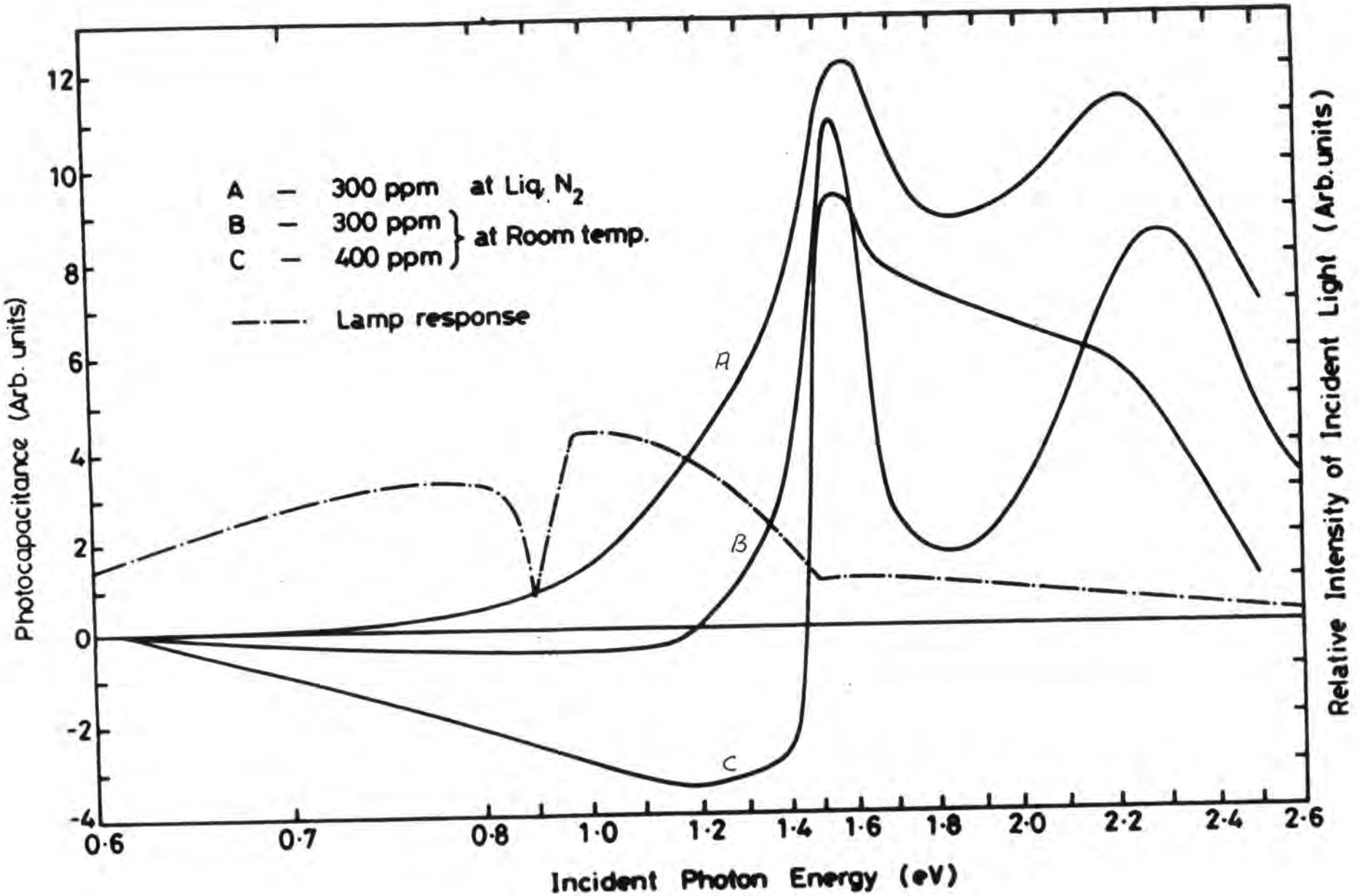


Fig. 8.26 : Steady state PHCAP spectra of devices doped with 300 and 400 ppm of Cu

increase in the width of the CdTe bandgap. However, this threshold is not well resolved due to the presence of another threshold of an unknown origin at ∿ 0.73 eV (Zanio[37] has reported levels at the middle of CdTe band gap).

There was an additional positive threshold at ∿ 1.86 eV at 85 K which, since this energy is greater than the CdTe bandgap, must have corresponded to an energy level at about 0.64 eV above the valence band in the CdS. There is a pronounced threshold at 2.22 eV (85 K) which indicates the presence of a level ∿ 0.28 eV below the conduction band of CdS. A similar level has been reported by Pande[17] who suggested that it might be associated with substitutional chlorine[52] (Cl was not intentionally used in the present devices). The negative going threshold at ∿ 1.55 eV (85 K) may be related to either bandgap absorption or a level in the CdS. There is also some evidence for a negative going threshold in the room temperature photocapacitance around 2.2 eV but it is not well resolved.

The PHCAP of the device with 400 ppm of Cu was measured at room temperature only and is included in Fig 8.26. This spectrum is very similar to that for the device with 300 ppm Cu (at L.N.) except that the thresholds are more pronounced, presumably as a result of higher copper concentration. The positive thresholds at 1.18 and 1.80 eV (as discussed earlier) correspond to energy levels of ∿ 0.35 and 0.64 eV above the valance band of CdTe and CdS respectively. The sharp negative going threshold at about 1.5 eV may, as before, be attributed either to some level in the CdS or to bandgap absorption in CdTe. The second negative going threshold at 2.28 eV indicates the presence of a donor level like state 0.12 eV below the conduction band of CdS. Such a level has been observed by Pande[17] and Balabanov[53] and is believed to be a surface state trap formed during the cooling.

An important point to be noted is that the negative trend in PHCAP at low energies is missing in the spectrum at liquid nitrogen. The absence of this threshold was unexpected because normally such details should be enhanced at lower temperatures due to the reduction in thermal quenching. Photocapacitance is thermally quenched when the thermal capture and emission rates exceed the optical rates, so that optical excitation cannot sufficiently alter the steady state trap occupancy to produce any measurable change in capacitance. It is probable that at room temperature this level lay above the Fermi level and thus in equilibrium would be at least partially empty. However, on colling to 85 K it is possible that the Fermi level may have risen above this level thus increasing its equilibrium occupancy. In such a situation, there would be no reduction in PHCAP at $\sim 1.15 < h\nu < 0.35$ eV due to filling of this level.

8.7 Conclusions

The work reported in this chapter was related to an investigation of the electrical and structural properties of thermally evaporated CdS and CdTe films as a function of deposition conditions, particularly the substrate temperature, and the optimization of the thin film CdS/CdTe heterojunction fabrication process. The effects of ageing on device performance and spectral dependence of photocapacitance were also investigated.

As expected, deposition conditions were found to affect the structural and electrical properties of both CdS and CdTe films, with corresponding effects on the final device performance. The optimum substrate temperature for the deposition of CdS and CdTe was found to be 180 and 200°C respectively, which produced layers with good crystalline order and excellent columnar growth. Devices fabricated with such films

gave the most efficient performance. As-grown undoped CdTe films had very high resistivity (10^6 Ω-cm) and attempts to dope the films during growth were unsuccessful. Post-deposition doping with copper, however, gave more encouraging results. The resistivity of the CdS films, although comparatively low, was found to increase with increasing substrate temperature from 120 - 300°C. Increasing the evaporation rate had the reverse effect.

Optimization studies indicated that many factors such as CdTe layer thickness, concentration of Cu dopant, sintering temperature during contact fabrication and dimension of the cell played an important role in producing efficient devices. The most efficient devices were obtained with a CdTe layer thickness of 6 μm, copper concentration of 300 ppm, using carbon contacts which were annealed at ∿ 330°C in a nitrogen ambient. The optimum cell dimensions were found to be 12 x 4 mm^2 (0.48 cm^2). The heterojunctions had respectable values of SCC but suffered from comparatively low OCV and poor fill factor. Efficiencies in excess of 3% were recorded. A crucial feature of these devices was that none of them degraded over a period of a few months; indeed their efficiency improved slightly with time.

Photocapacitance studies suggested that the copper level in CdTe lies ∿ 0.35 eV above the valence band. Other levels were observed at 0.64 eV above the valence band in CdS, 0.26 and 0.12 eV below the conduction band in CdS.

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CHAPTER 9

COPPER TELLURIDE-CADMIUM TELLURIDE SOLAR CELLS

9.1 Introduction

One of the more potentially interesting photovoltaic structures based on CdTe is the p-Cu_2Te/n-CdTe heterojunction[1,2]. This is analogous to the Cu_2S/CdS cell and should offer a number of advantages over the more widely studied CdS/CdTe cell. In the latter the CdTe provides the p-type side of the junction, and this has led to some problems, as it is difficult to make p-CdTe sufficiently conducting. As a result CdS/CdTe cells often display relatively high values of series resistance with correspondingly low values of fill factor[3,4]. However, in the Cu_2Te/CdTe device, the CdTe is n-type and can be made highly conducting. Series resistance is therefore lower in these devices and fill factors as high as 60-70% may be obtained without problems[1,2]. A second potential advantage is that the cell fabrication is similar to the Cu_2S/CdS process[5,6] and is therefore, straightforward and inexpensive. Thirdly, since the diffusion rate of Cu is lower in CdTe[7] than in CdS, and the phase diagram for Cu_2Te is less complex than that of Cu_2S[8], Cu_2Te/CdTe devices should be much more stable than their Cu_2S/CdS counterparts.

The work reported in this chapter includes a description of the fabrication of Cu_2Te/CdTe devices by the chemiplating of n-CdTe substrates in an aqueous solution of cuprous chloride. The structural and electrical properties of the cells are also described. The effects of chemiplating time, annealing and ageing, have been systematically investigated to determine the optimum preparative conditions. Most of

the devices used were prepared on oriented single crystal CdTe substrates so that the crystal structure could be more readily studied by RHEED and scanning electron microscopy. In particular, minority carrier diffusion lengths were measured by EBIC in as-made and heat treated devices. These observations were then correlated with the measured electrical characteristics to gain an insight into the operation of the cell.

9.2 Structural Studies of Copper Telluride

In its natural form copper telluride is found as either Rikardite (Cu_3Te) or Weissite (Cu_2Te)[9]. The latter has a crystal structure which is predominantly hexagonal[10] with c:7.27 Å and a = 4.23 Å. In copper deficient (tellurium rich) samples ($\sim Cu_{1.95}Te$) the values of c and a are found to decrease slightly to 7.24 Å and 4.19 Å respectively. As described in Section (2.3.3) the atom-to-atom distances in Cu_2Te are estimated to be Cu-Cu=2.33 Å, Te-Te=2.82 Å and Cu -Te=2.67 Å. From these studies it is reasonable to believe that copper telluride has phases which are analogous to those of cuprous sulphide. Cu_2Te also has a cubic modification (a = 6.11 Å) (ASTMS) known to exist at higher temperatures ($\sim$ 640°C).

In order to study the crystallinity and phase structure of copper telluride, layers were deposited on single crystal CdTe substrates grown from the vapour phase (Section 4.2.3) and oriented along the (111) planes. The substrates were doped n-type, then cut (5x5x2 mm^3 dice) and polished, and their orientation checked by RHEED. To grow a topotaxial layer of copper telluride, a polished dice was first covered with lacomit varnish on all sides except for the surface to be chemiplated. The dice was then dipped into a hot (95°C) cuprous ion solution for various intervals of time during which a Cd-Cu exchange reaction took place, to produce a thin layer of Cu_2Te in the CdTe surface.

Fig (9.1) shows an electron diffraction pattern from a freshly polished (111) oriented CdTe substrate with the beam along the [110] direction. The diffraction pattern of the substrate with a topotaxial layer of copper telluride with the electron beam along the three different azimuths is shown in Fig (9.2). Of interest is the asymmetry in the distribution of spots in the columns on opposite sides of the substrate normal in the RHEED pattern, taken with the electron beam incident along [110] direction (Fig 9.2a). The pattern is reversed when the substrate is rotated through 60° so that the electron beam lies along the [101] azimuth (Fig 9.2c). Rotation through 30°, i.e. the [211] beam direction, yields a completely symmetrical pattern (Fig 9.2b). There is no evidence for the presence of any polycrystalline phase as has been observed in, for example, Cu_2Se formed by a similar chemiplating technique[11].

These observations indicate that there is a close topotaxial relationship between the (111) CdTe substrate and the layer of copper telluride formed on it. The spot patterns are however, complex and are probably composite containing diffraction spots from both the CdTe substrate and one or more phases of Cu_2Te. Nevertheless, the predominant phase would appear to be the cubic Cu_2Te as the following observations imply:

(1) The three largest measured interplanar spacings, 3.42 Å, 2.2 Å and 1.87 Å are in good agreement with the published values for the cubic phase of Cu_2Te; 3.51 Å (111), 2.16 Å (220) and 1.84 Å (311) (ASTMS).

(2) The asymmetry referred to above cannot be explained in terms of the hexagonal phase of Cu_2Te, and provides conclusive evidence that the Cu_2Te is predominantly cubic.

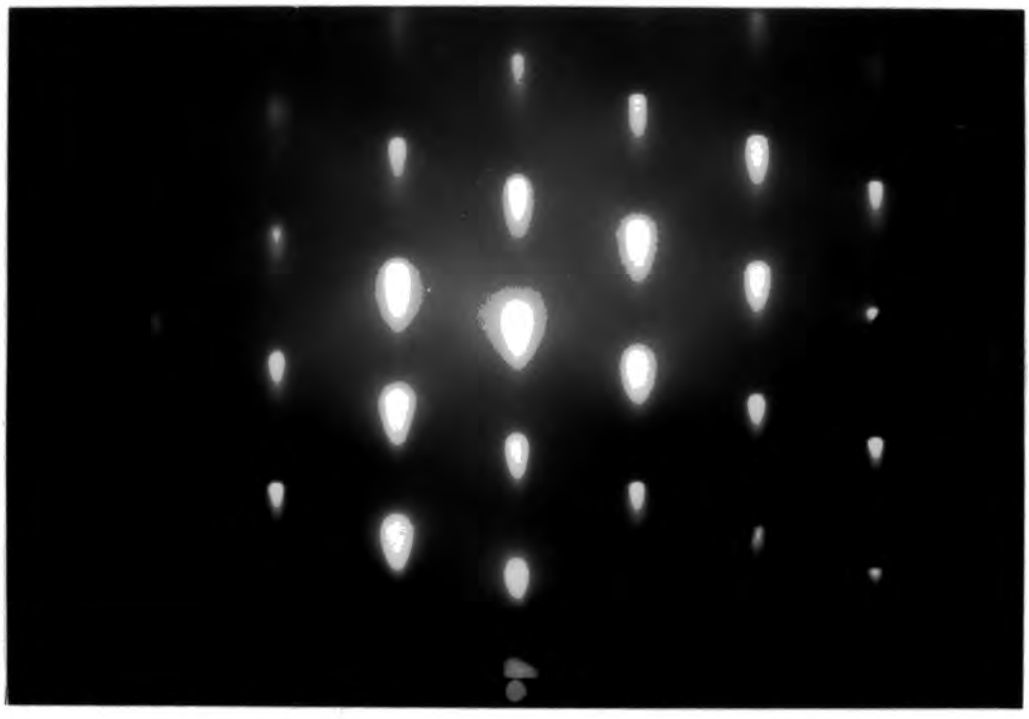
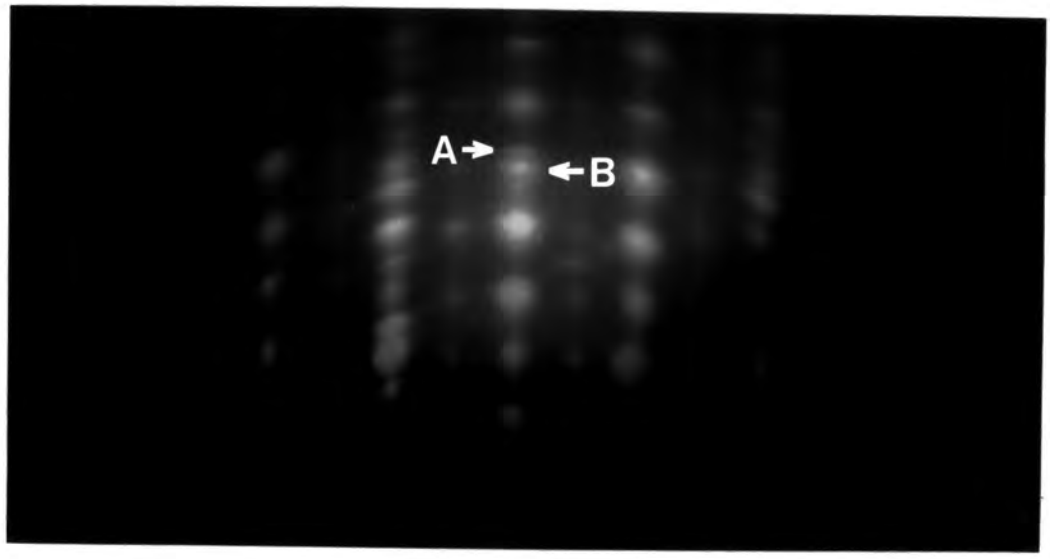
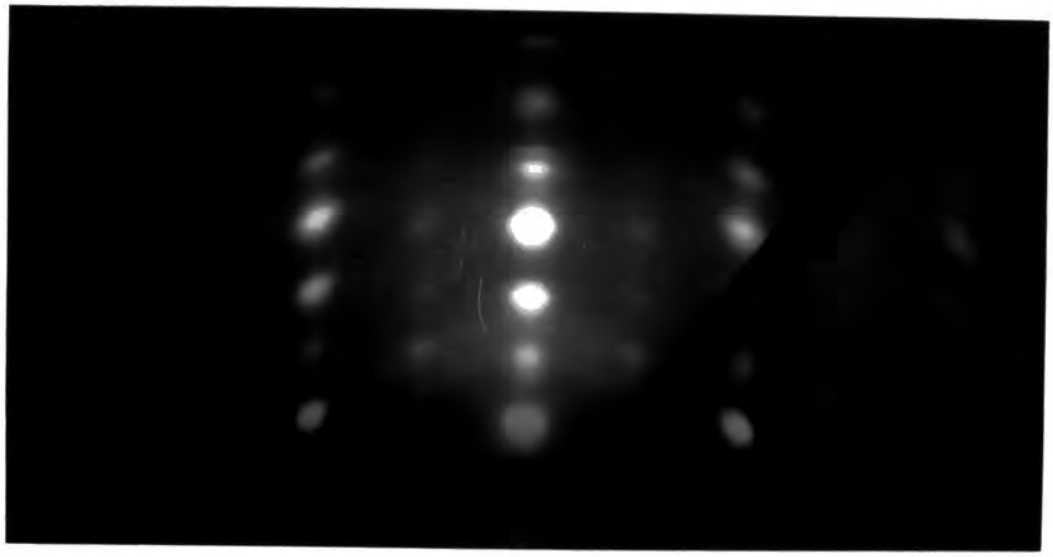


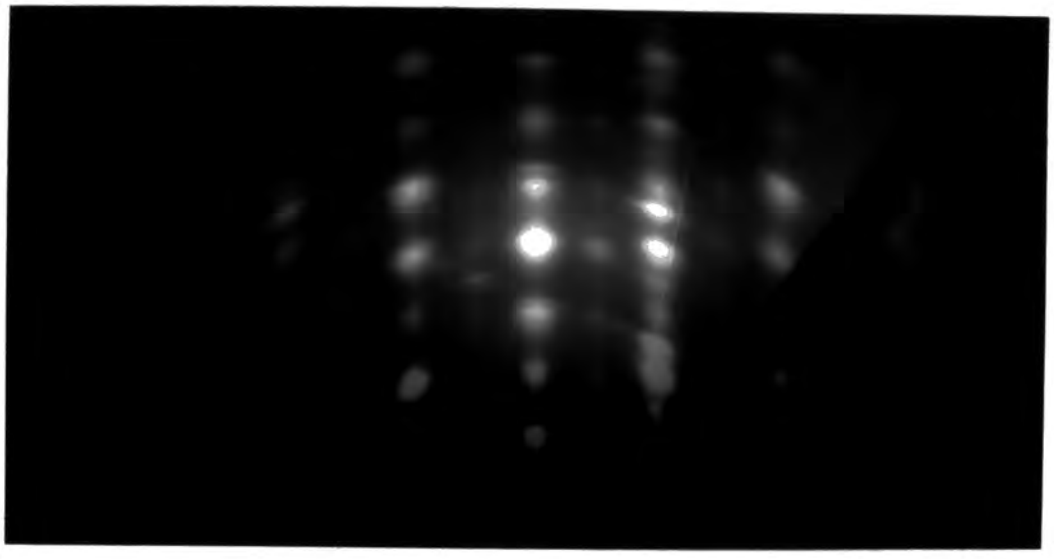
Fig. 9.1 : RHEED pattern from a freshly polished (111) oriented CdTe substrate with the electron beam along a <110> direction.



(a) [110]



(b) [211]



(c) [101]

Fig. 9.2 : RHEED patterns from a topotaxial layer of Cu_2Te with the electron beam along directions: (a) [110]; (b) [211]; and (c) [101].

Clearly, the pattern (Fig 9.2a) is very complex and contains more spots than can be explained in terms of a cubic phase alone. No attempt has been made to index all the diffraction spots present, and in fact many of them may well have arisen from double diffraction effects. It is possible that the complexity indicates the presence of some hexagonal material. However, there are a number of indications which suggest that some of the spots are due to diffraction from the substrate, particularly the additional reflections seen at A in Fig (9.2a). The interplanar spacings, calculated for the diffraction spot at A and for that at B, yield a ratio of $\sim$ 1.05 which is in good agreement with the ratio of 1.06 for the lattice parameters of CdTe and cubic Cu_2Te.

The observation of a dominant cubic phase contrasts with the results of similar chemiplating experiments with single crystals[1] which indicated the growth of a hexagonal phase of Cu_2Te. As mentioned earlier, the only cubic phase of copper telluride recorded in the ASTM powder index data is a high temperature modification at 640°C. The growth of the cubic phase at lower temperature (95°C) could have resulted from the cubic CdTe substrate which compelled the cubic growth of Cu_2Te. Moreover, it should be emphasized that topotaxial growth of Cu_2Te implies that only the cubic phase can form without any disruption of the tellurium sublattice.

Topotaxial layers grown on (111) CdTe substrates were heat treated in vacuum for 10-15 mins and then also investigated using RHEED. The electron diffraction patterns of the heat treated samples were indistinguishable from those obtained from as-made Cu_2Te layers. The heat treated samples were then left to age in the laboratory for a period of up to 2 months, after which time again showed no change in the diffraction pattern. These studies suggest that the phase of Cu_2Te is stable, although it has been reported in the literature that Cu_2Te films change with time[12,13].

9.3 Electrical Properties of Copper Telluride/Cadmium Telluride Heterojunctions

9.3.1 Diode Characteristics

Oriented (111) CdTe substrates were cut and annealed in molten Cd (Section 4.3.4) to make them conducting n-type and pad-polished in Br-methanol solution (Section 4.4.2) to obtain a damage free mirror-like surface. Typically, devices were fabricated by dipping the substrates into the cuprous chloride solution for 40 sec to form a topotaxial layer of Cu_2Te. An indium dot was then evaporated onto the CdTe side of the device, while an Au grid pattern was evaporated onto the Cu_2Te face.

The diode characteristics of a typical device are given in Fig 9.3 while the logJ vs V plots of the cell in the forward and reverse bias condition are shown in Fig 9.4. The diodes were found to be highly rectifying with a rectification ratio at 0.5V of $\sim 6 \times 10^3$. The value of the ideality factor was 1.5.

The lattice mismatch (difference in lattice constants) between the components of a heterojunction produces, in principle, a periodic array of dangling bonds or edge dislocations. These ideally form a net at the interface and each dislocation will be associated with a region of lattice strain. Such a dislocation may or may not be electrically active. It has been found that a large amount of compensation takes place and so only a small fraction of these bonds remain active and accounts for the observed electrical phenomena[14]. Similarly, impurities or defects introduced during fabrication may result in energy states in the vicinity of the interface. The presence of large density of interface states provides a high density of recombination centres near the interface. So unlike homojunctions, the carrier transport properties of HJs are generally dominated by phenomena in the interface region. The current transport in the depletion layer is variously attributed to recombination, to tunneling or to combination of tunneling and recombination involving energy levels near the interface[15].

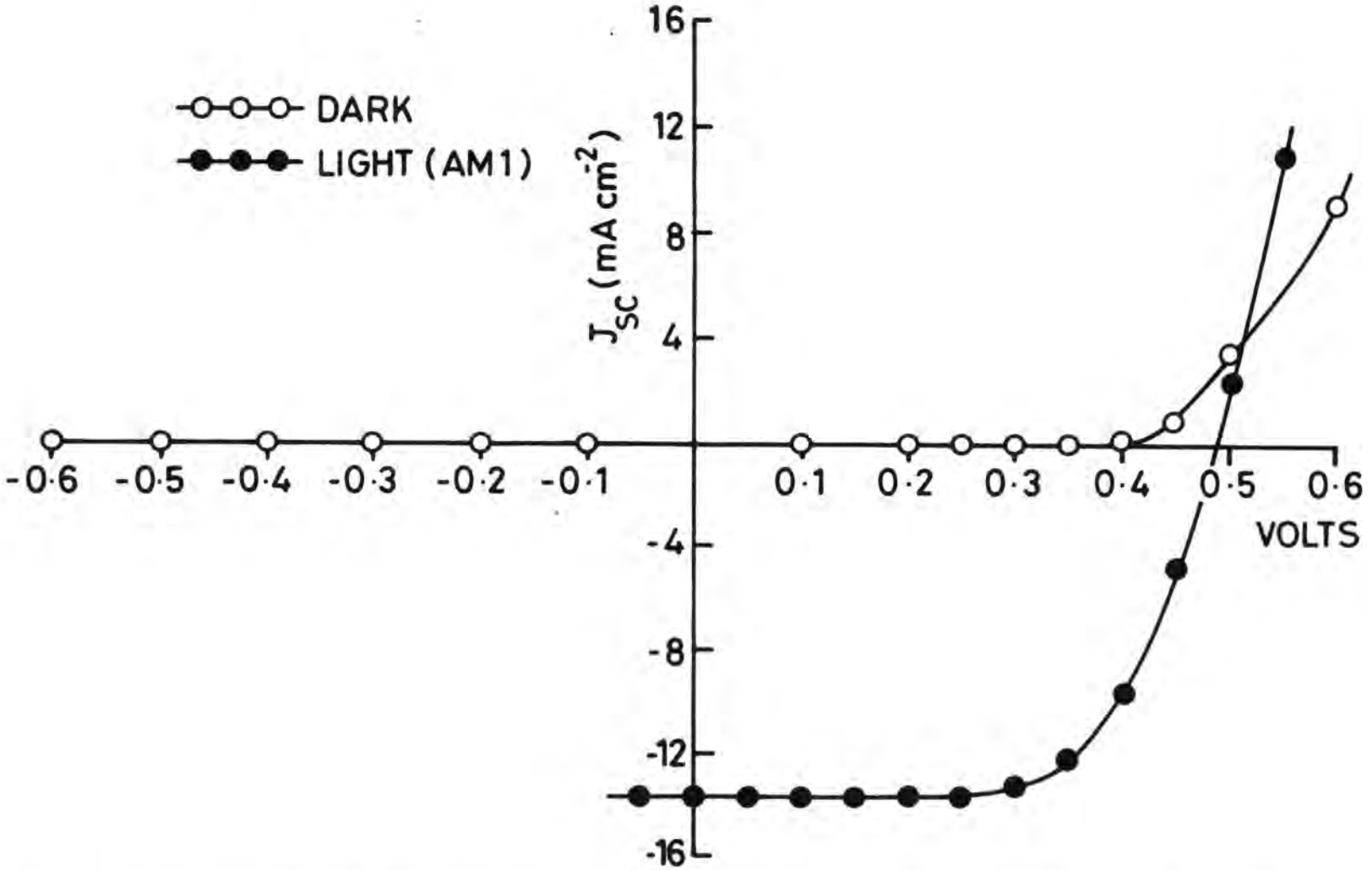


Fig. 9.3 : Current-voltage characteristics for a $Cu_2Te/CdTe$ solar cell chemiplated for 40 sec.

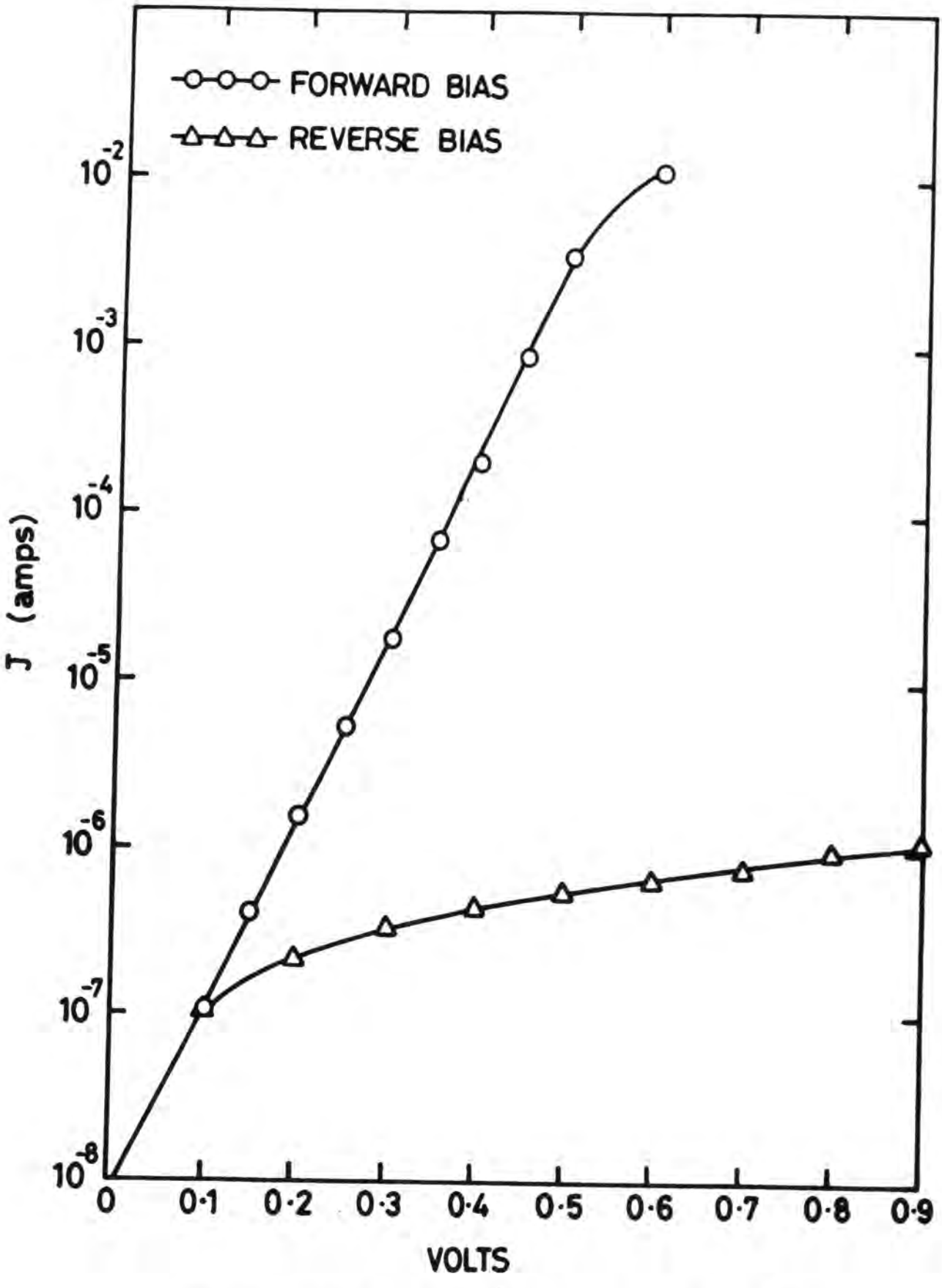


Fig. 9.4 : LogJ vs V plots of the same cell (Fig. 9.3)

In the present CdTe/Cu_2Te heterojunctions the Cu_2Te layer was found to consist of more than one phase (i.e. cubic and hexagonal) and this would also lead to an increase in defect states with a loss of performance. The lattice mismatch between CdTe and the cubic Cu_2Te is $\sim$ 6.2% and would be expected to generate a small density of misfit dislocations with an accompanying reduction in interfacial recombination. The carrier transport should therefore be controlled by the recombination and a value for the ideality factor $\sim$ 1.5 is consistent with this argument. The lower value of the ideality factor (A) as compared to Cusano[1] could have resulted from the predominant cubic phase of Cu_2Te.

Cu_2Te/CdTe heterojunctions have been previously fabricated by Cusano[1] using a similar wet barrier process. The diode characteristics of Cusano's cells appeared to be less ideal, with a diode factor of 2.7 and rectification ratio at 0.5V of several hundreds. One important difference between the present cells and those of Cusano is that in his cells the structure of the Cu_2Te layer was largely hexagonal. This might well have led to increased interfacial disorder with correspondingly greater recombination losses and hence a higher ideality factor.

9.3.2 Photovoltaic Output Characteristics

The photovoltaic output characteristics for a typical Cu_2Te/CdTe heterojunction cell are given in Fig 9.3 for AM1 illumination. For this particular device shown, the OCV, SCC, FF and efficiency were 0.49 volts, 14 mA/cm^2, 62.5% and 4.1% respectively. While the SCC is acceptable, the OCV is disappointingly low. In part, this reflects the fact that the cell is not a window-absorber structure. However, the fill factor is relatively high. Considering that no steps had been taken to optimise the device efficiency (i.e. there were no A.R.coatings, etc), this value compares favourably with the best

performance obtained with CdS/CdTe cells[4]. This may be attributed to two factors. Firstly, the n-type CdTe can be made more highly conducting than its p-type counterpart. Secondly, the use of indium is expected to provide a lower resistance ohmic contact to n-CdTe than can normally be obtained to p-type material.

The cross-over of the dark and illuminated characteristic in the first quadrant indicates a change in parameters from dark to light[16]. It suggests that some photoconductive process is in operation. When the light generated current is increased, the current increases more rapidly with V and cross-over occurs. Such a cross-over has been observed in Cu_2S/CdS[16] and CdS/CdTe cells[17] but not in crystalline silicon devices.

9.3.3 Spectral Response

The SCC and OCV spectral responses were measured at 85 and 300K, and are shown together with the lamp response in Fig 9.5 for a typical device. The threshold for the OCV response starts at about 0.95 eV and a second sharp rise occurs at 1.37 eV (at room temperature) with the peak at 1.50 eV. At 85K, the onset of the second rise is shifted to higher photon energies and correspondingly the peak value is $\sim$ 1.65 eV. Similar behaviour was observed in the SCC response, although here there was no detectable increase until about 1.04 eV. At 85K the principal change was in the width of the peak which had become much broader.

As indicated in Fig 9.5b, the principal response in the dependence of OCV occurred at about 1.5 eV at 300K. This corresponds to the bandgap of CdTe and is consistent with Cusano's[1] observations. The new feature of the response in Fig (9.5b) is the presence of a second peak which is only clearly resolved at 85K, at which temperature it exhibits a maximum value at $\sim$ 1.2 eV. The origin of this second peak is not yet clear, but could be related either to the presence of copper levels in the CdTe or alternately to band-to-band transitions in the

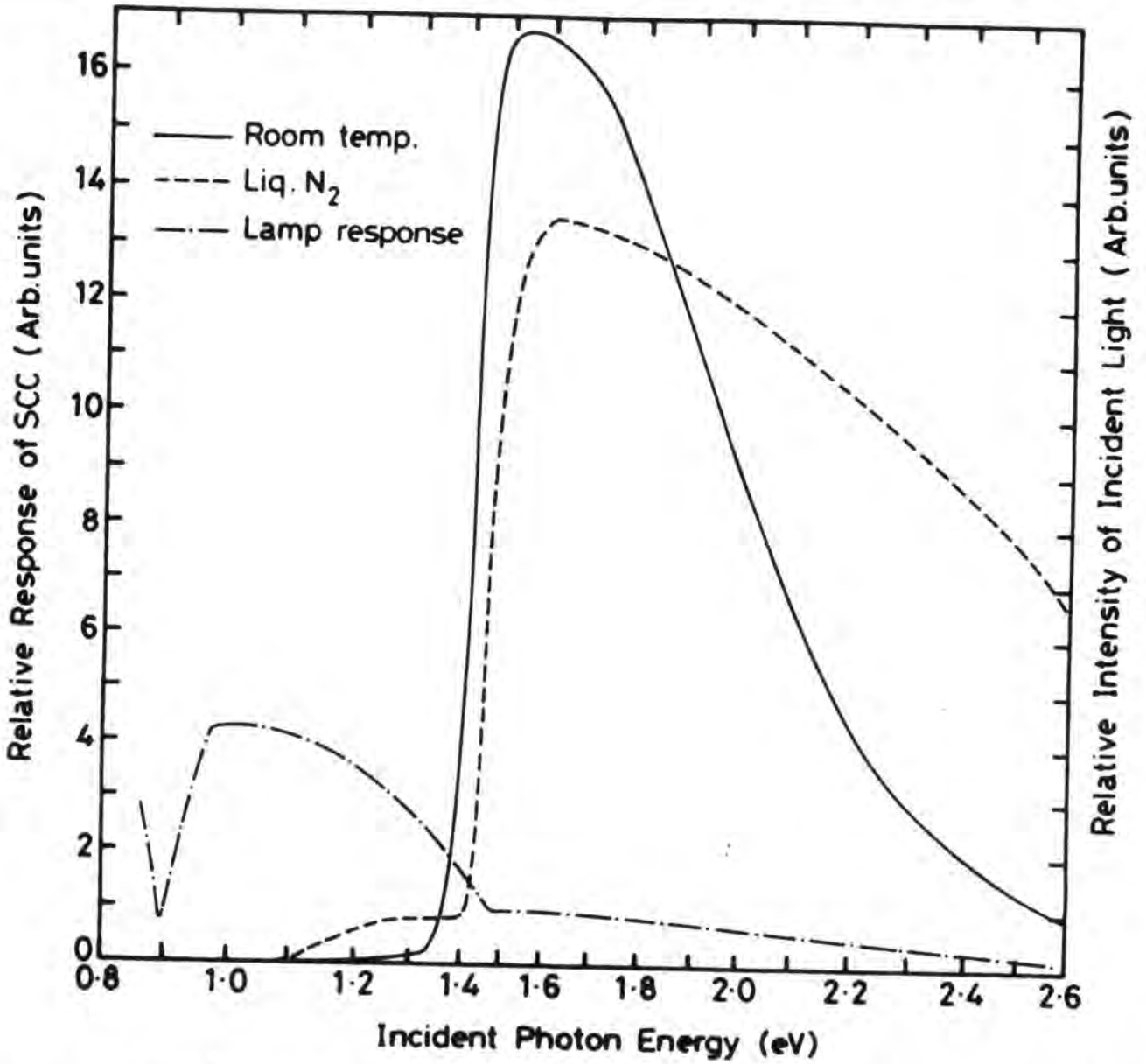


Fig. 9.5(a) : SCC spectral response of the same $Cu_2Te/CdTe$ solar cell (Fig. 9.3) measured at different temperatures.

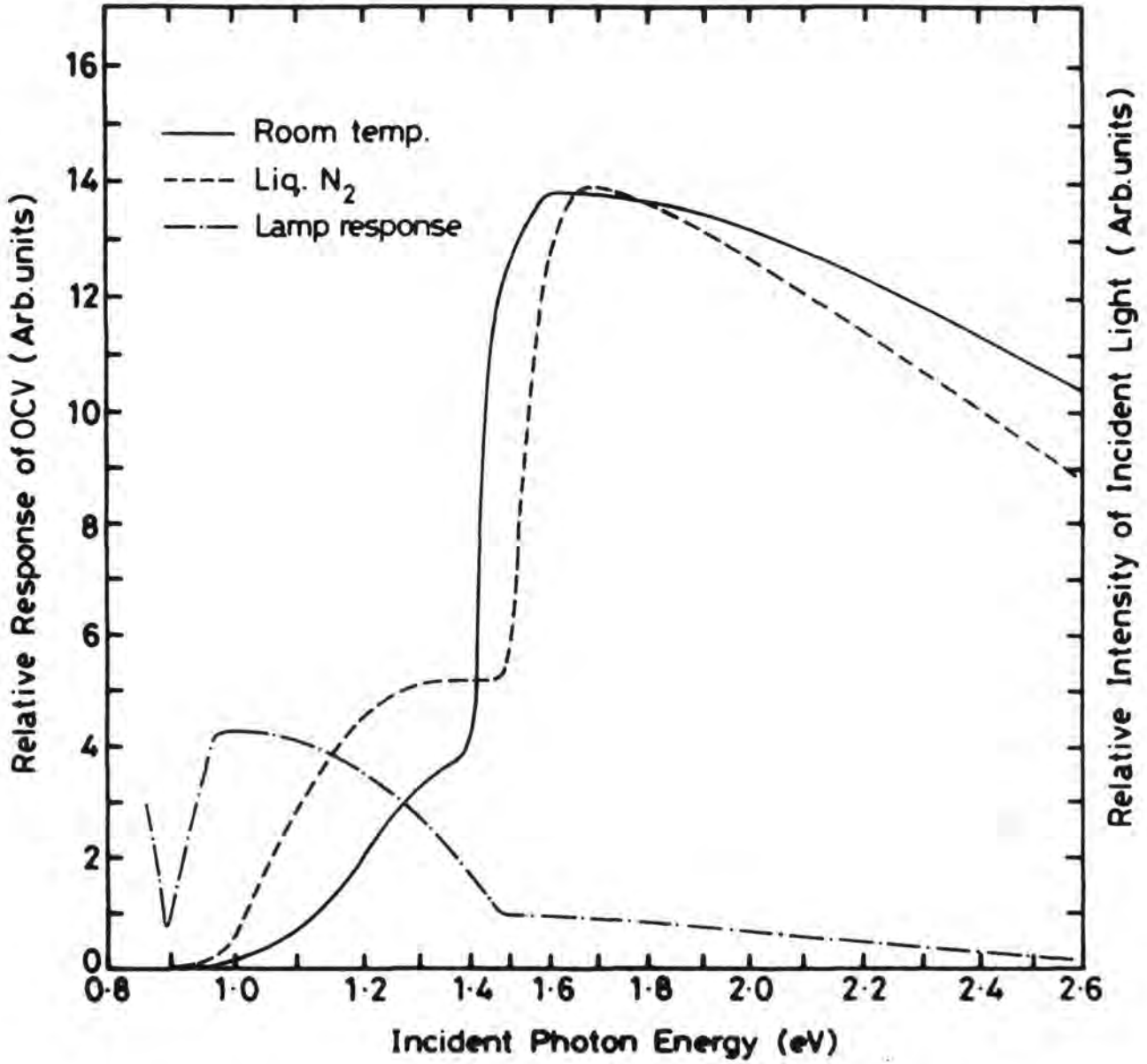


Fig. 9.5(b) : OCV spectral response for the same cell (Fig. 9.5(a))

cubic phase of Cu_2Te. However, in the literature Cu substituted on Cd sites is reported to have energy levels at ∿ 0.35 eV[18,19] and 0.15 eV[20]. In the latter case the copper level would be expected to give a response at ∿ 1.5 eV at 85K (or at 1.35 eV at 300K) which could be too high to explain the presence of the second peak in Fig 9.5b. Similarly, a value for the Cu level of ∿ 0.35 eV also fails to explain this response which would then be at ∿ 1.3 eV. Thus, it appears that cross diffusion of copper is not responsible for this second peak. It is therefore suggested that this response arises from absorption in the Cu_2Te. Unfortunately, the bandgap of the cubic phase of Cu_2Te is not known. However, it is interesting to note that Cusano did not observe this second peak and concluded that Cu_2Te was opto-electronically inactive.

9.3.4 Capacitance-Voltage Characteristics

The capacitance-voltage measurements were made at 1 MHz frequency using the technique described in Section 5.6. A C^{-2} vs V characteristic for a typical device is shown in Fig 9.6. It is a straight line in the reverse bias range up to 2.0 V with an intercept of ∿ 2.8 V on the voltage axis. The donor density deduced from the slope of the C^{-2} vs V plot was 1.9×10^{16} cm^{-3}.

Although the C^{-2} vs V plots were straight lines for lower values of reverse bias, there was a departure from linearity at large reverse bias. This behaviour is very similar to that frequently observed in the CdS/CdTe[21] devices. It may be attributed to inter-diffusion at the junction interface, or from the tailing into the bulk of defect states created during fabrication, or from lattice mismatch[21]. Inter-diffusion is believed to introduce a more highly compensated layer at the interface. Such an effect has also been reported in CdS/Cu_2S and $ZnCdS/Cu_2S$ heterojunctions[22]. In the present case this could well

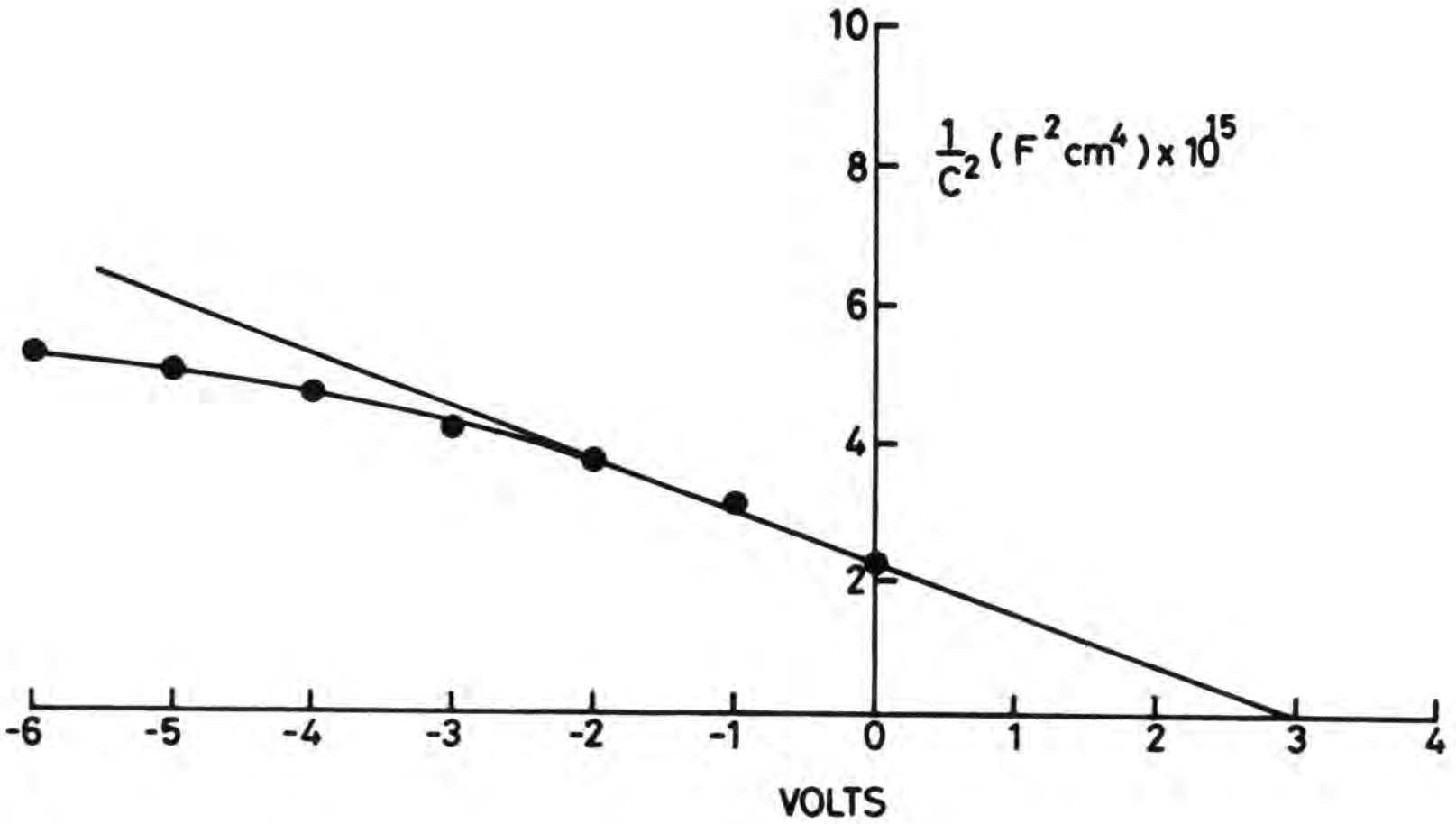


Fig. 9.6 : C^{-2} vs V characteristic for the cell described in fig. 9.3.

result from the cross-diffusion of copper into the n-CdTe substrate which would lead to a decrease in the conductivity of the CdTe. The large value of the intercept on the voltage axis may indicate the presence of an interfacial layer as observed with Schottky devices[23]. The interfacial layer may be produced during processing and can arise due to chemical reactions, cross-diffusion, out-diffusion, oxide layers etc.[24]. (ZnCd)S/Cu_2S heterojunctions fabricated by the chemiplating process have been reported to have very high values of voltage intercepts[22].

9.3.5 Photocapacitance Studies

The photocapacitance of the diodes was measured at room and liquid nitrogen temperature using the experimental arrangement described in section 4.6. Fig 9.7 shows the photocapacitance spectra of a typical device chemiplated for 40 sec. In general, the photon energy was scanned from ∿ 0.59 eV to 2.5 eV. Between 0.59 eV and the first positive going threshold at ∿ 0.88 eV the capacitance was found to decrease uniformly, though not steeply, suggesting the existence of a negative going threshold at some photon energy less than 0.59 eV. A second more pronounced increase was observed near 1.36 eV (room temperature) and 1.44 eV (liquid nitrogen temperature). The photocapacitance decreased sharply at L.N. temperature for photon energies above 1.58 eV.

The initial decrease in photocapacitance as the photon energy was increased was difficult to interpret since the capacitance was not investigated at photon energies below 0.59 eV. It is likely therefore that the true threshold would have occurred at lower energy. Ordinarily a decrease in capacitance would indicate a net increase in stored negative charge possibly through the filling of acceptor-like levels, with electrons[5].

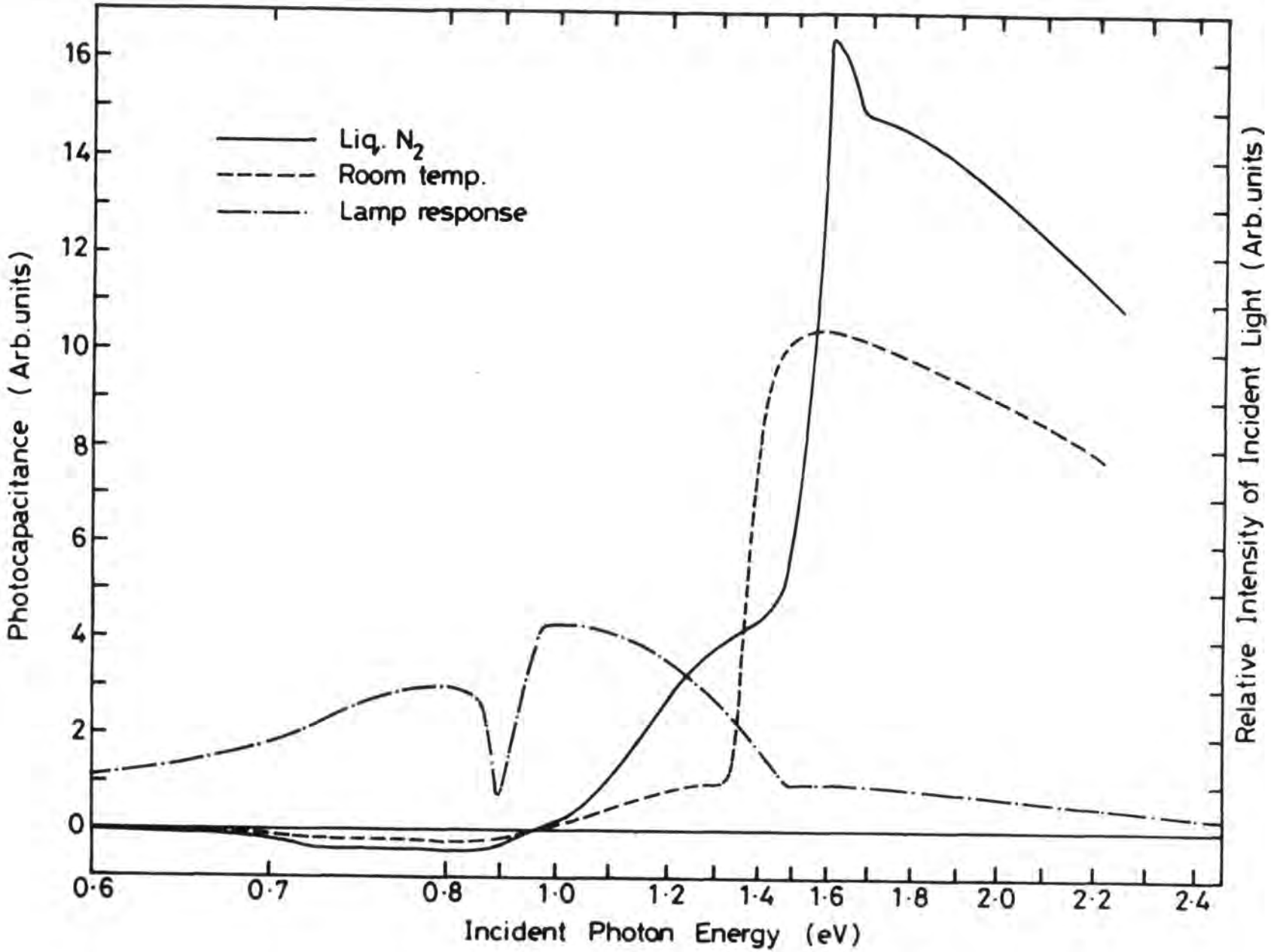


Fig. 9.7 : Photocapacitance spectra of a typical device chemiplated for 40 secs measured at different temperatures

The sharp rise in capacitance at about 1.44 eV (at L.N) is due to junction field assisted interband transitions. The steep negative going threshold at ∿ 1.58eV may be related to transitions across the bandgap. However, the bandgap of CdTe at 80K is 1.595 eV[25] and it is possible that this peak indicates the presence of a shallow donor level approximately 0.015 eV below the conduction band. This feature was not observed at room temperature. The donor levels with ionization energies of 0.014 eV below the conduction band have been reported in the literature[26]. Moreover, the positive going threshold around 0.88 eV is not easy to explain. The increase in photocapacitance is associated with the transition of electrons from the level to the conduction band so this threshold could be related to emptying of a level with ionization energy less than 0.88 eV and buried in the background. It is important to note that defect levels with energy 0.6-0.9 eV have been reported by Zanio[26].

9.4 Effect of Substrate Properties

In this section, the effects of the substrate properties on the behaviour of heterojunctions are reported. The substrate properties such as resistivity, minority carrier diffusion length and surface preparation strongly affect the final behaviour of the device[27], and consequently, their effects on device performance were investigated.

9.4.1 Measurements of Diffusion Length

The diffusion length can be measured in several ways. Optical methods[28-35] and surface photovoltage measurements[36,37] generally require a knowledge of the absorption coefficient of the material at the wavelength of radiation used for excitation. The absorption is strongly dependent on impurity concentration in the semiconductor[38]. Another method of finding the diffusion length employs a modulated electron

beam[39] in a scanning electron microscope. Unfortunately, beam modulation was not available with the Cambridge Instrument Stereoscan 600 microscope used in the present study. An alternative method described by Wittry and Kyser[40], makes use of the voltage dependence of cathodoluminescence to determine the diffusion length. There are problems with this method, however. Firstly, it requires the structural and chemical state of the sample surface to be known and this is not always the case. Secondly, the contribution to the measured current from the self absorption of recombination radiation[41] is in general not determined. Consequently, there is frequently some uncertainty in the measurements. By comparison, the EBIC method outlined in Section 5.3.3 is relatively easy to interpret (providing the assumptions are fulfilled) and since it was available, it was used in the present study.

As described in Section 5.3.3 the short circuit electron beam induced current collected by a planar p-n junction is given by[38]

$$J = J(o) \exp(-x/L) \qquad 9.1$$

where $J(o)$ is the total current contributed by the minority carriers generated by the incident electron beam, x is the distance of the point of incidence of the electron beam from the junction, and L is the minority carrier diffusion length. From equation (9.1) the value of L can be determined from a semi-logarithmic plot of I(x)/I(o) vs x provided the following conditions are satisfied[38].

(1) The electron-hole pairs are generated from a point source, that is far from the junction ;

(2) Surface effects (i.e. excessive surface recombinations may be neglected, and excess carriers are assumed to travel only by diffusion ;

(3) The intensity of the current generated by the multiple process (electron-hole pair generation near the impact point, radiative recombination and photocurrent generation near the junction) is small

compared with the intensity of the minority carrier current generated by the incident electron beam.

The minority carrier diffusion length was measured in the as-made Cu_2Te/CdTe solar cells fabricated on n-type CdTe substrates which had been either doped with chlorine or annealed in cadmium. Devices were studied in both the SE and EBIC modes of the SEM. For diffusion length measurements the devices were cleaved through the junction and perpendicular to it. The sample was then mounted in the SEM such that the beam was incident normally to the cleaved edge so that the EBIC signal across the junction could be monitored. A typical linescan showing the variation of the electron-beam induced current with beam position across the junction is shown in Fig 9.8. There is a maximum response at the junction which decays on either side. Measurements of the current relative to the peak as a function of the distance from the junction were made and a plot of log $I(x)/I_o$ vs x were plotted and fitted to equation (9.1). A typical example for a device on a Cd doped substrate is shown in Fig 9.9 in which the diffusion lengths were 0.76 μm and 3.80 μm on the Cu_2Te and CdTe sides of the junction respectively. The minority hole diffusion length in Cd annealed CdTe (3.8 μm) was larger compared with 0.78 μm in Cl-doped substrates. However, like Cu_2S/CdS cells the minority electron diffusion length in Cu_2Te was less than minority hole diffusion length.

The diffusion length of minority-holes in Cl-doped CdTe was smaller than that for minority holes in cadmium doped CdTe. This difference is attributed to the nature of the dopant used. Bell et al[42] have explored the dependence of the hole diffusion length in CdTe with the kind of n-type dopant used. They made measurements on Bridgman-grown CdTe doped with I, Br, and Cl and found that the shortest diffusion lengths were observed with Cl-doped CdTe, while the largest occurred with I doped material.

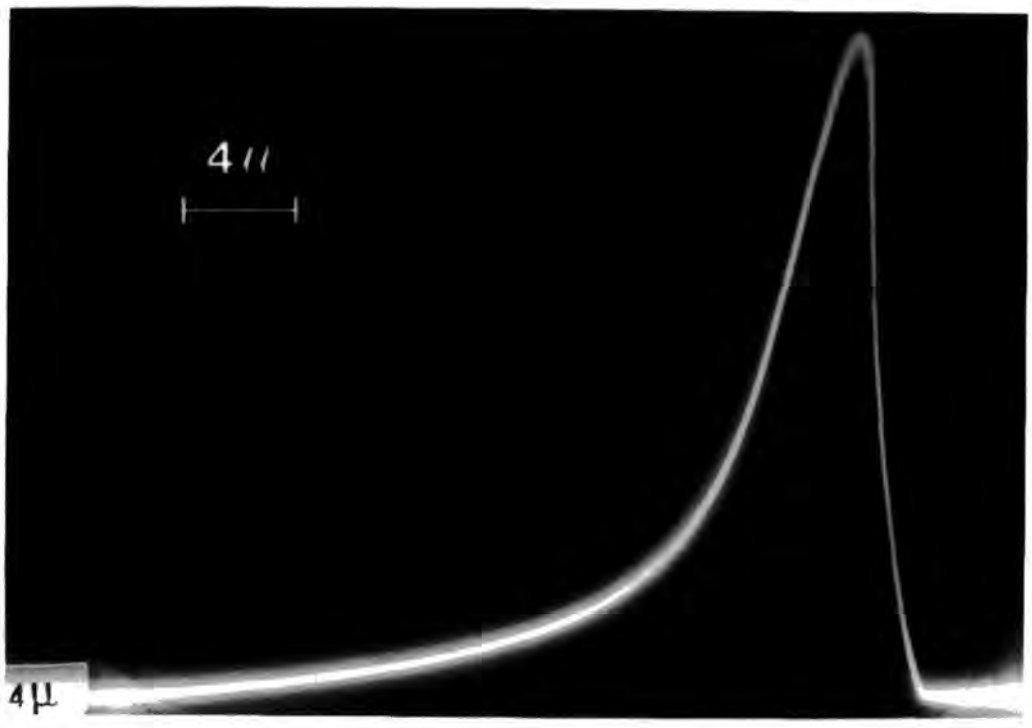


Fig. 9.8 : A typical linescan taken across a cleaved $Cu_2Te/CdTe$ junction fabricated on a Cd annealed substrate.

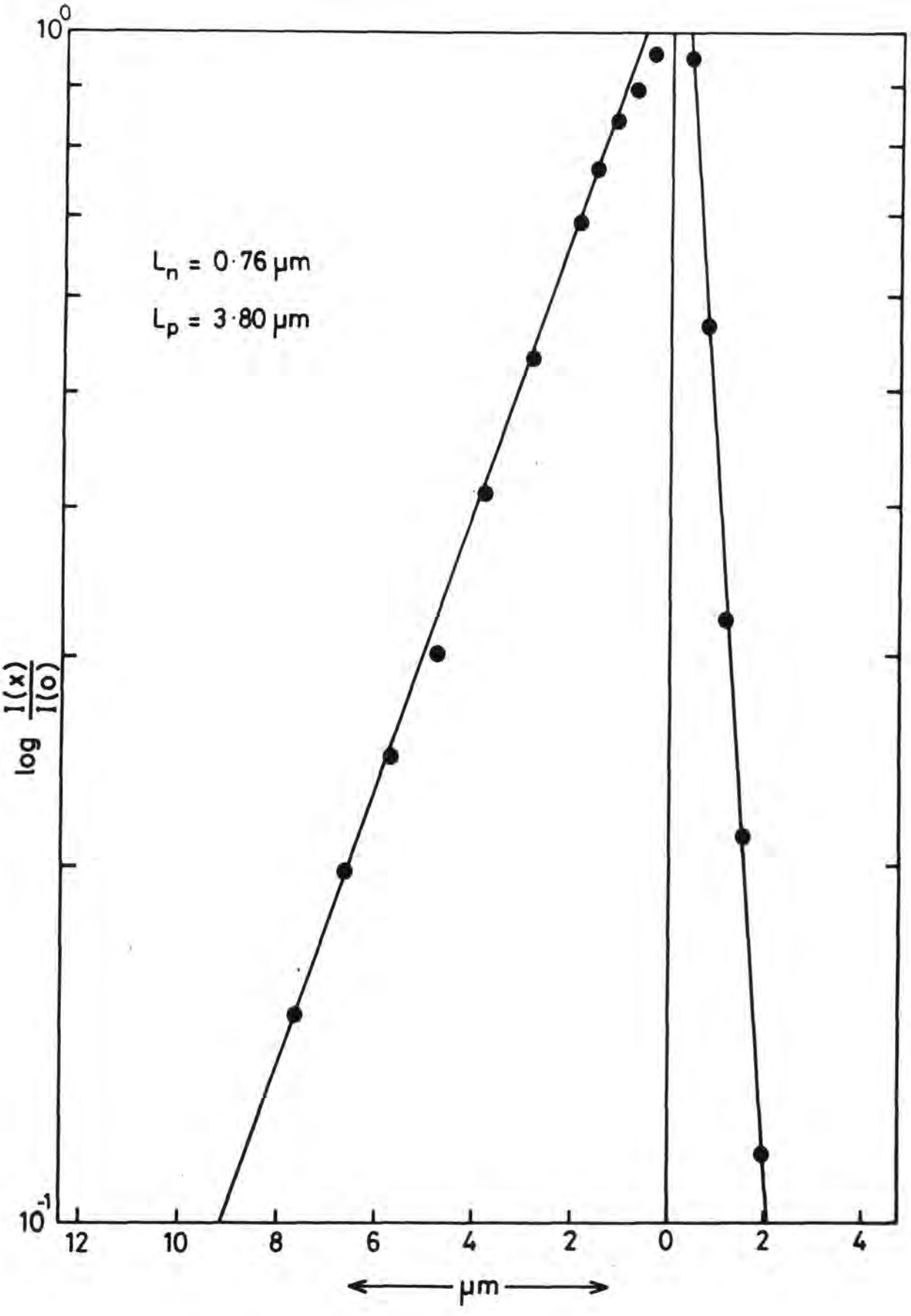


Fig. 9.9 : A plot of logI(x)/I(o) VS distance from the junction for the linescan shown in Fig. 9.8.

This suggests that to produce efficient solar cells using CdTe some means of controlling the resistivity must be found, that does not cause short diffusion lengths. This was true of our CdTe/Cu_2Te heterojunctions. Devices made on Cl-doped substrates gave consistently low values of SCC whereas cells on cadmium treted CdTe resulted in much higher values.

9.4.2 Resistivity Effects

The effect of substrate resistivity on device characteristics was studied using CdTe substrates with a range of resistivities. Three devices were fabricated on cadmium annealed n-CdTe with resistivities of 20 Ω cm, 7 Ω cm and 0.1 Ω cm. These devices were designated as a, b and c respectively. The substrates were chemiplated for 40 sec in hot (90°C) cuprous chloride solution.

The photovoltaic output characteristics of the cells measured under AM1 illumination are shown in Fig 9.10. The values of SCC, OCV, FF and η for the cells are given in Table 9.1.

TABLE 9.1: Solar Cell Parameters with Different Substrate Resistivities

Device	Substrate Resistivity ρ (Ω cm)	OCV volts	SCC mA/cm^2	FF (%)	η
a	20	0.48	18	46	3.3
b	7	0.5	13.4	62	4.1
c	∿ 0.1	0.34	8.5	41	1.1

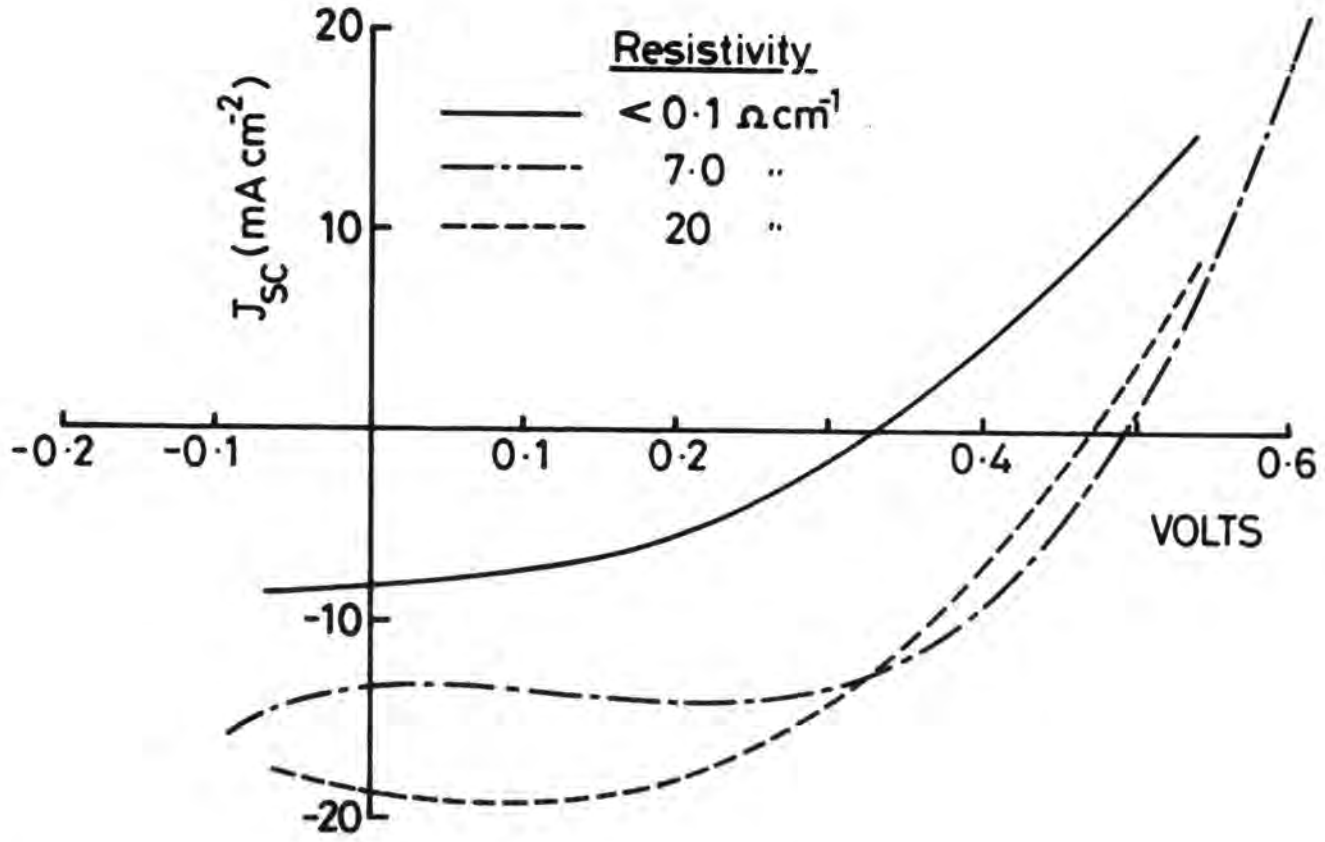


Fig. 9.10 : Photovoltaic characteristics of cells fabricated on substrates with different resistivities

The resistivities of the semiconductors forming a p-n junction photovoltaic device can affect its operation in two ways: firstly, when the resistivity is very low (i.e. high doping concentration) the depletion region is reduced ; secondly, the minority carrier diffusion length is also reduced. Copper telluride is a highly conducting near degenerate semiconductor, and the junction between it and a low resistivity substrate would result in a very narrow depletion region. This in turn would give large values of reverse saturation current I_o and a correspondingly low open circuit voltage (Section 2.1.3). This was precisely what was observed for device C ($\rho \sim 0.1$ Ω-cm). Low values of SCC may also be explained in terms of reduced diffusion length and narrow depletion region associated with very low resistivity values[43]. In this situation, the SCC is reduced because the active region of the device (i.e. depletion region + one diffusion length) is correspondingly narrow, and a smaller proportion of the absorbed radiation is able to contribute to the current.

The heterojunction on 20 Ω-cm material (device a) exhibited the highest short circuit current of 18 mA/cm^2. In this case the width of the depletion region was significantly increased so that the contribution to the short circuit current from generation within the depletion region was also highly increased. The low fill factor, however, for this heterojunction (device a) was possibly the result of increased series resistance.

Cusano[1] also studied the effect of resistivity and similarly established that highly doped material (with its consequently narrow junction width) leads to poor efficiency. Although our results are not conclusive in determining the optimum value of resistivity they do demonstrate the undesirable effects of too low a resistivity.

9.4.3 Effect of Surface Preparation

The substrate surface preparation conditions can exert a strong influence on the performacne of the heterojunctions[27]. Two methods of substrate preparation were compared, namely contactless pad polishing in Br-methanol (Section 4.4.2), and a procedure involving an initial mechanical polish using alumina followed by a chemical polish in Br-methanol solution (Section 4.4.1). The n-CdTe substrates with identical resistivities (∿ 7 Ω-cm) were prepared using polishing techniques described above and chemiplated for about forty seconds in cuprous ion solution to fabricate CdTe/Cu_2Te heterojunctions.

The photovoltaic output characteristics of two typical devices fabricated on CdTe substrates prepared by; (a) the contactless pad polish and (b) the mechanical/chemical procedure are compared in Fig 9.11. The OCV and fill factor were low for device (b) [alumina polished surface] although the SCC was slightly higher. The efficiency (4.0%) of device (a) [pad polished surface] was ∿ 30% greater than that of device (b) (3.0%) as a result of the greater OCV and FF. The superior performance of the pad polished device was also revealed by the diode characteristics which showed rectification ratio at 0.5 V bias that were ∿ 6 times higher than for the chemical/mechanical polished devices ($6x10^3$,10^3). The spectral responses of the OCVs are shown in Fig 9.12. The SCC response also had similar behaviour. Fig 9.12 clearly shows that the spectral response for the pad polished device is greater in magnitude at all wavelengths.

The current-voltage characteristics described in Fig 9.11 reflect the quality of the surface produced by the two preparational methods. As described in Section (4.4.2), pad polishing produces a very clean and smooth surface, whereas surfaces polished by the mechanical-chemical method had small particles of alumina embedded in the surface in

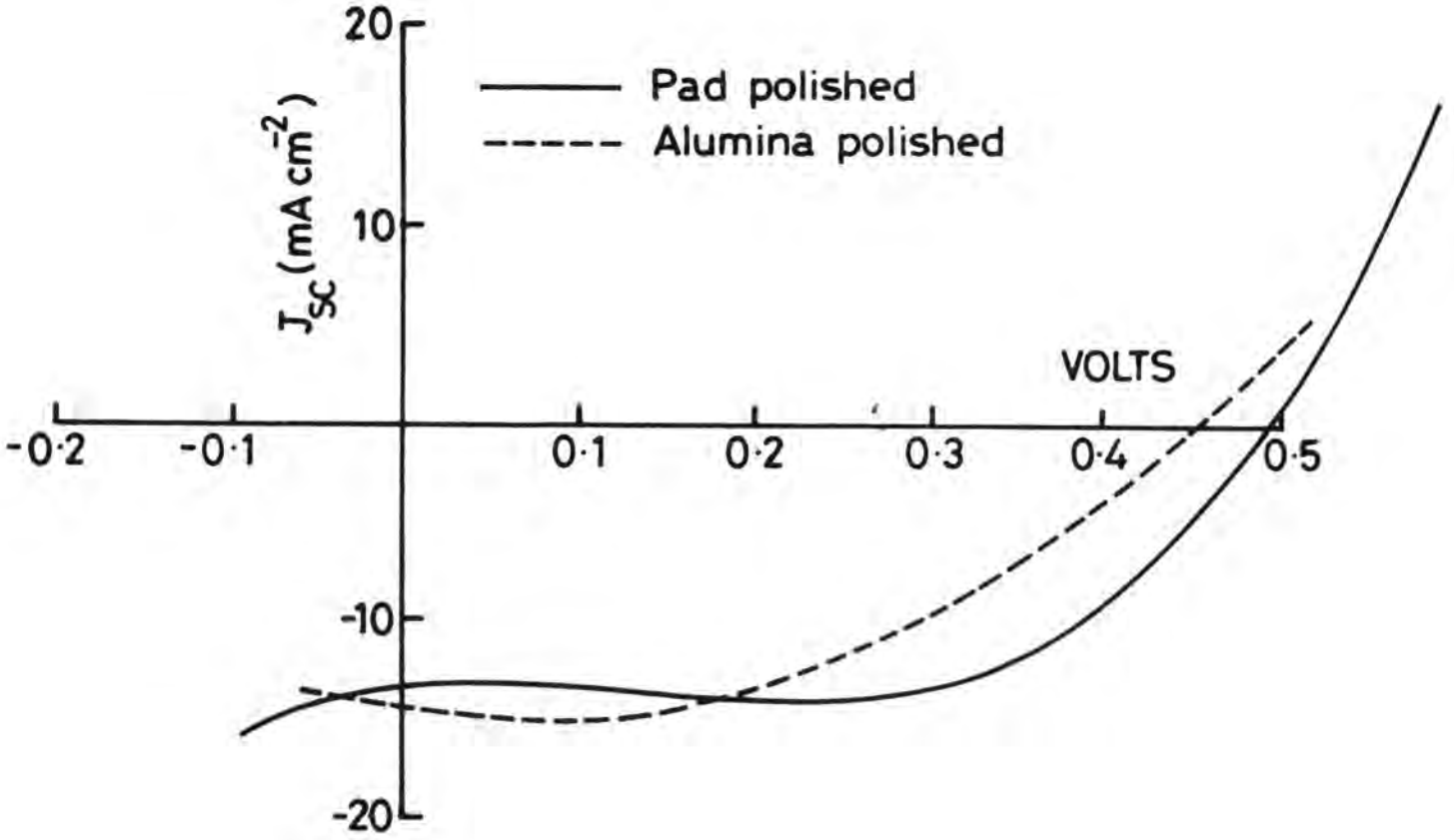


Fig. 9.11 : Photovoltaic characteristics of cells fabricated on pad polished and alumina polished substrates

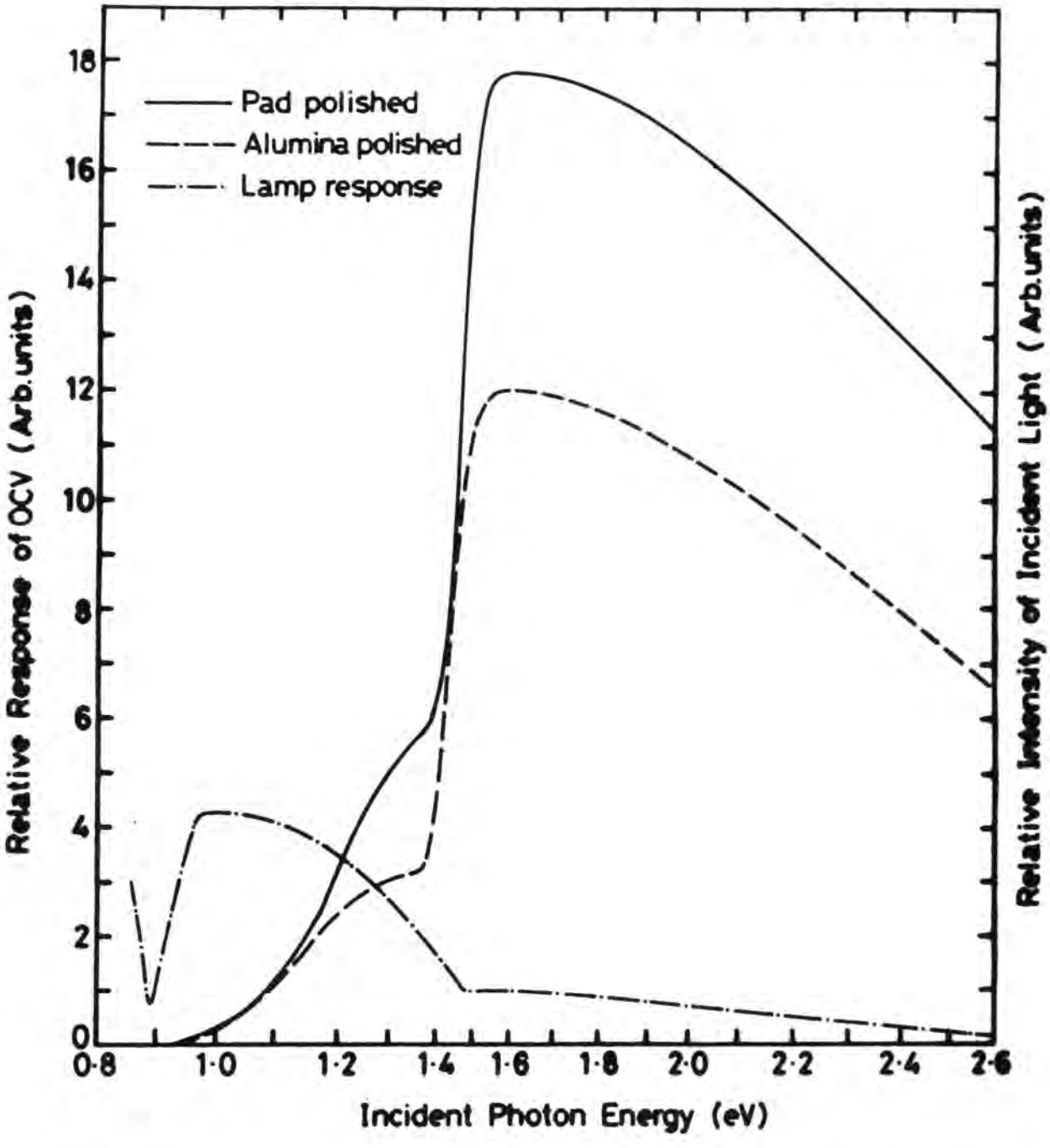


Fig. 9.12 : Spectral responses of the open circuit voltages for the same devices (Fig. 9.11)

addition to a considerable amount of surface damage. Mechanical polishing is known to produce a heavily damaged surface[44]. The function of the Br-methanol polish is to remove the damaged surface layers. Although it does reduce mechanical damage to a large extent, CdTe surfaces were still not damage free. The surface damage would be expected to lead to a higher density of interface states in the heterojunction and hence an interfacial recombination. This, in turn, would lead to an increase in I_o and consequently, lower values of OCV as observed in these devices.

Alumina particles embedded in the surface would also hinder the formation of a good epitaxial layer of Cu_2Te and ultimately poor performance of the device.

9.5 Effect of Chemiplating Time

9.5.1 Introduction

Clearly, the time for which the CdTe substrates are immersed in the cuprous ion chemiplating bath will affect the thickness of the Cu_2Te layers. A systematic investigation of the effects of varying the chemiplating time was therefore, carried out. In order to try and isolate the effects of chemiplating time from those of substrate resistivity, only CdTe substrates cut from a boule doped with Cl were used for this exercise. In fact, Cl doped substrates are not ideal, as discussed above (Section 9.4), but they do have the merit of uniformity. Thus, it was possible to ensure that the substrate resistivity did not vary from device to device, so that differences in cell performance could be attributed with greater certainty to the Cu_2Te layer.

The devices were all fabricated in conditions identical to those described in Section 9.3 except, of course, for the chemiplating time. This was varied from 20 sec to 120 sec. The current-voltage, photoresponse characteristics were then investigated.

9.5.2 Current-Voltage Characteristics

The diode characteristics of five devices made with different chemiplating times are shown in Fig 9.13. All had little reverse bias leakage although the rectification ratios were found to vary with plating time (Table 9.2). The rectification ratio at 0.5 V was highest ($\sim$ 2000) for a plating time of about 30 seconds. It decreased significantly for shorter and longer plating times. Similar behaviour was observed with Cd annealed substrates, when a rectification ratio at 0.5 V of $\sim$ 6000 was measured for devices plated for 40 seconds. On increasing the plating time to 50 seconds the rectification ratio fell to 600.

The photovoltaic output characteristics measured under AM1 illumination are shown in Fig 9.14. Devices plated for 30-40 secs yielded short circuit currents twice as large as those for cells plated for 20 and 90 secs. The OCV for these devices was low and did not vary significantly nor systematically with plating time. A summary of the variation of device parameters with plating time is given in Table 9.2.

TABLE 9.2: Device parameters for different plating times

Chemiplating Time (sec)	OCV (mV)	SCC mA/cm^2	FF %	Rectification Factor at 0.5 V	η
20	407	4.5	26	620	0.8
30	330	8.34	39	2000	1.1
50	422	8.78	33	589	1.3
90	420	4.74	30	389	0.7
120	423	1.21	26	90	0.2

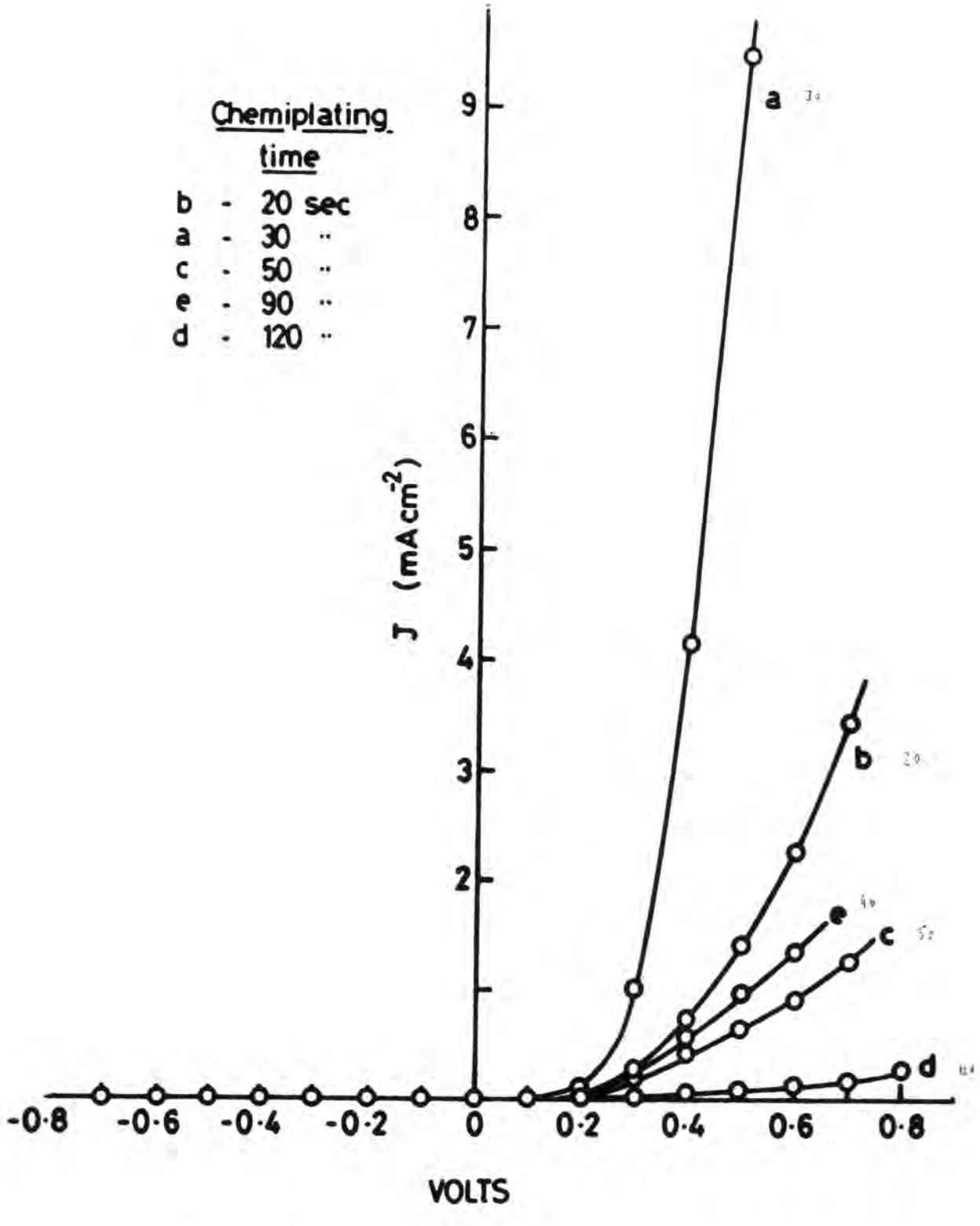


Fig. 9.13 : Effect of chemiplating time on diode characteristics of solar cells

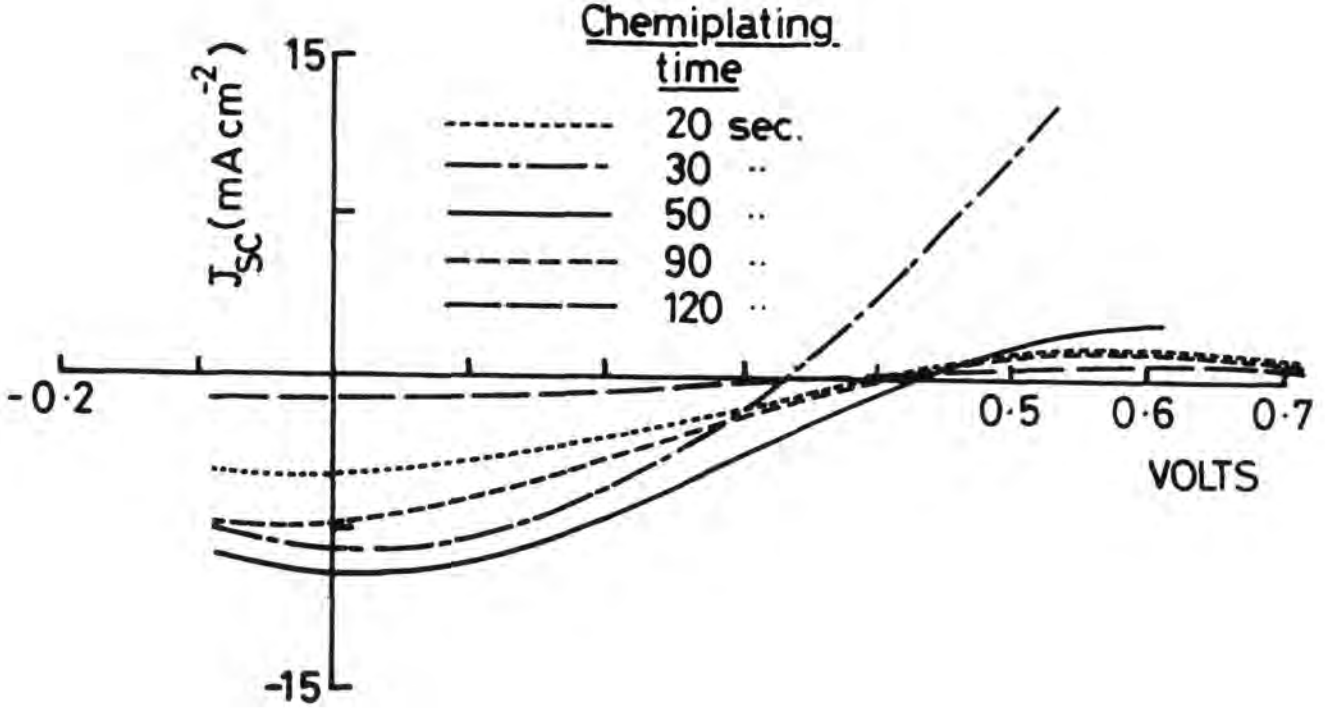


Fig. 9.14 : Effect of chemiplating time on photovoltaic characteristics

The variation of the SCC with plating time can be explained in terms of the thickness of Cu_2Te layer. For 20 sec plating the copper telluride layer was clearly too thin and contributed to the series resistance as evident from Fig 9.14. At the same time, if the Cu_2Te film is very thin, its transparency will be too high and low energy photons will contribute proportionately less towards the SCC. The decrease in the SCC with increasing time beyond 50 seconds is probably due to the greater thickness of Cu_2Te. If the layer thickness exceeds the minority carrier diffusion length then the carriers generated near the surface will not be separated at the junction and will not therefore, contribute to the short circuit current. In this respect, it should be remembered that Cu_2Te is not a window material like CdS in CdS/CdTe heterojunctions.

The generally low values of SCC and OCV were probably related to the substrates (Cl-doped) which were very highly conducting with low minority carrier diffusion lengths (Section 9.4.2). At low resistivities the transition region becomes very narrow[43] with a consequential reduction in SCC and OCV. A similar observation has been made by Cusano for In-doped CdTe with very low resistivity, where the junction width was thin and carriers generated beyond the small depletion region were not collected. These studies imply that the optimum plating time is about 30-40 secs.

9.5.3 Spectral Response

The spectral response of the devices was measured at room temperature. The OCV reponses for devices chemiplated for different periods of time are shown in Fig 9.15. The spectral responses for the short circuit currents were similar. All these cells showed a photovoltaic response at photon energies less than the bandgap of CdTe that increased in magnitude with increasing plating time.

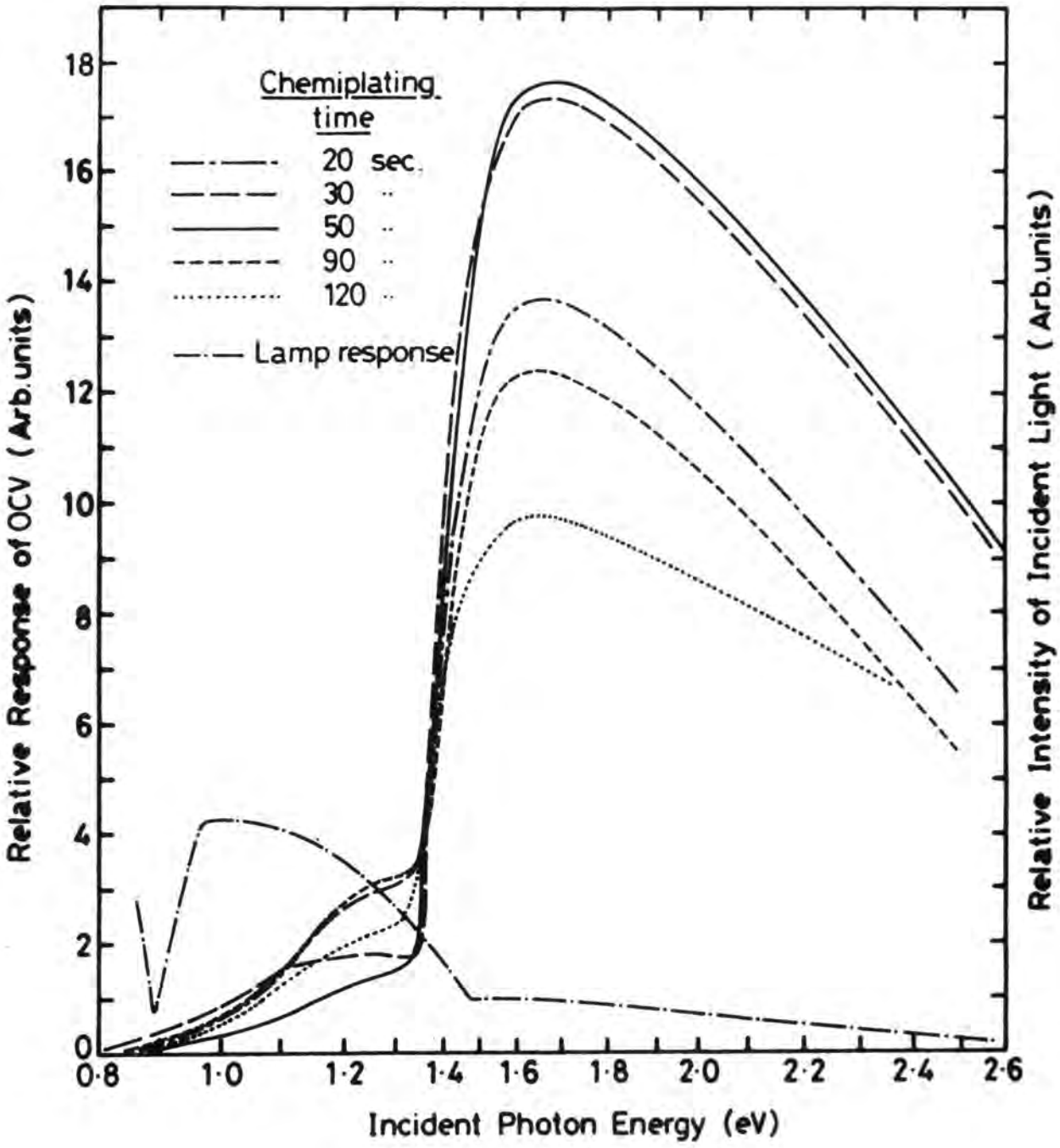


Fig. 9.15 : Effect of chemiplating time on the open circuit voltage spectral response for the same cells as Fig. 9.14.

This response probably arises from absorption in the Cu_2Te layer and the change in its magnitude would be expected to follow the variation in thickness. Clearly, for short chemiplating times, the Cu_2Te layer would be thin and so highly transparent (particularly near infrared)[45] with a corresponding small response. For very long plating times, the layer becomes very thick so that the electron hole pairs, generated near the surface, do not reach the junction and the response is again reduced.

9.6 Effect of Heat Treatment

In order to study the effect of heat treatment on the characteristics of Cu_2Te/CdTe devices, they were heated in vacuum at $\sim$ 200°C for about 7 minutes. The characteristics of the as-made and heat treated devices were measured under similar illumination (AM1) conditions. The I-V characteristics were found to be affected strongly by the heat treatment. The photovoltaic output characteristics of an as-made, and a heat treated device are shown in Fig 9.16. After heat treatment the SCC was greatly reduced while the OCV was slightly increased.

To investigate the effect of heat treatment on the minority carrier diffusion length, the diffusion length was measured before and after heat treatment at $\sim$ 200°C for 5-7 minutes. The heat treatment reduced the hole diffusion length in CdTe from 3.8μm to 1.3 μm, while the electron diffusion length in Cu_2Te improved from 0.76 μm to 1.2 μm.

The spectral responses of the SCC and OCV were also recorded to observe any changes due to this annealing. The appropriate SCC and OCV responses are shown in Fig 9.17. It is clear that the spectral response from the Cu_2Te totally disappeared on heating. Moreover, the SCC response of the heat treated devices showed a steep decrease at photon energies slightly greater than the bandgap of CdTe. A similar situation was observed with the OCV (Fig 9.17b).

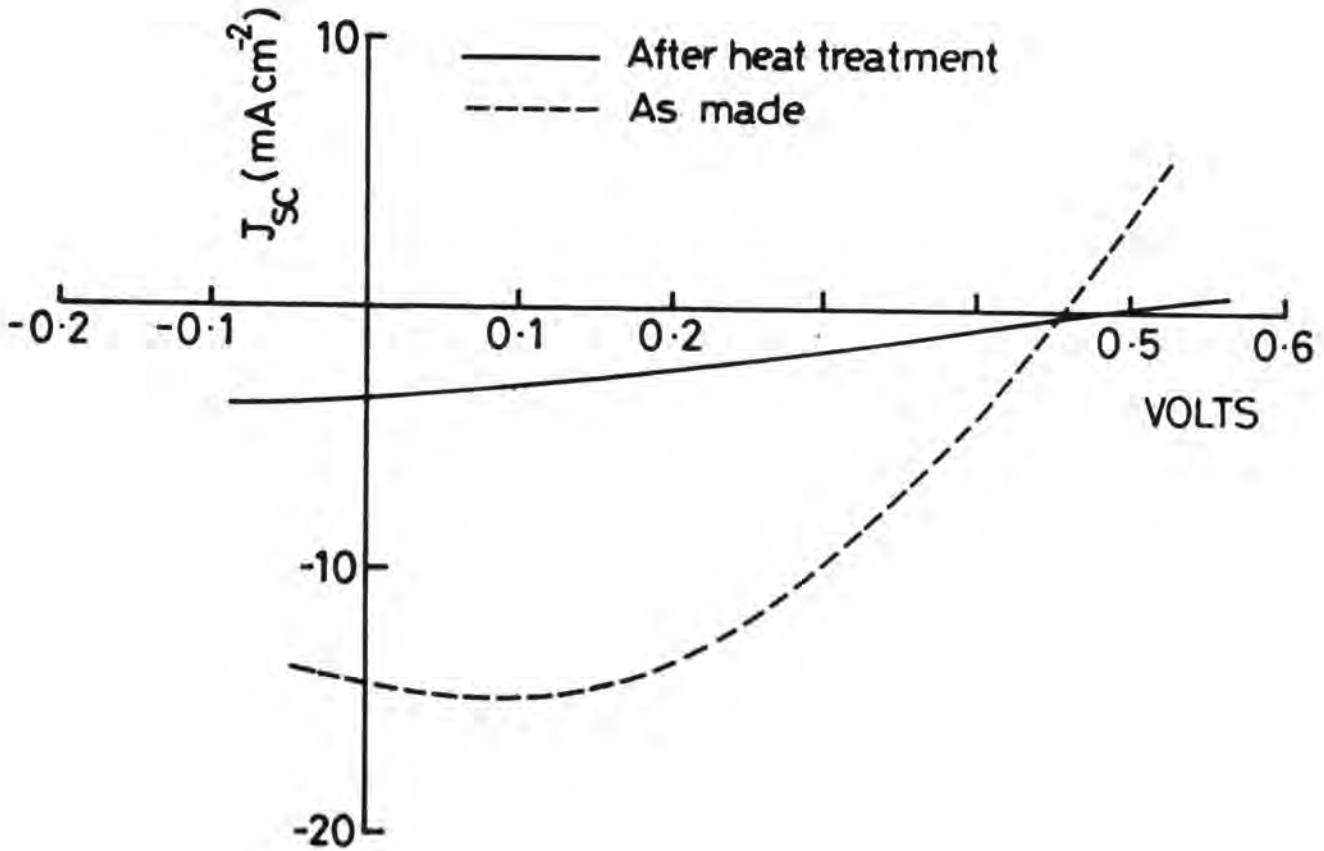


Fig. 9.16 : Photovoltaic output characteristics of an as-made and a heat treated device

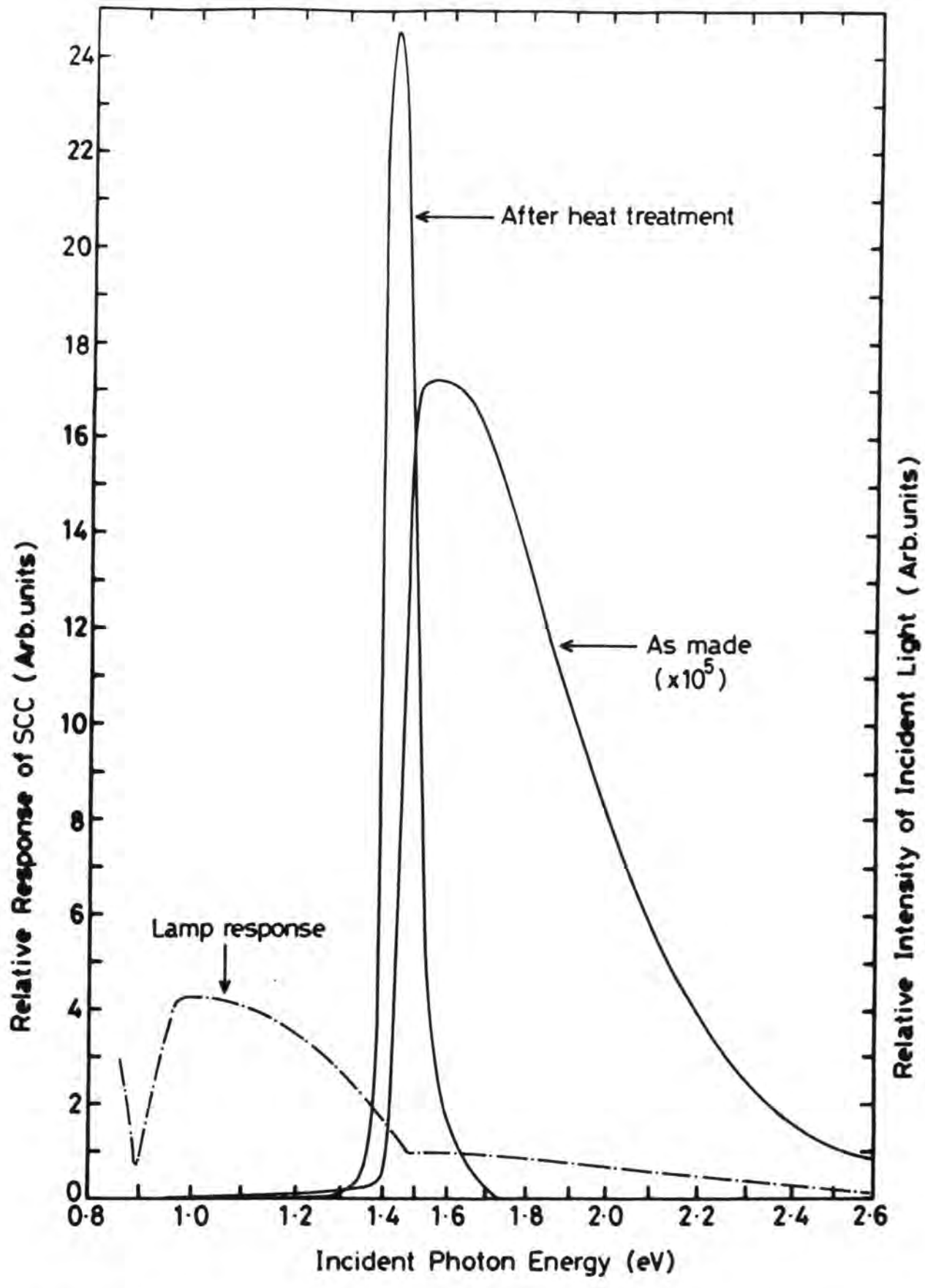


Fig. 9.17(a) : SCC spectral responses of an as-made and a heat treated cell.

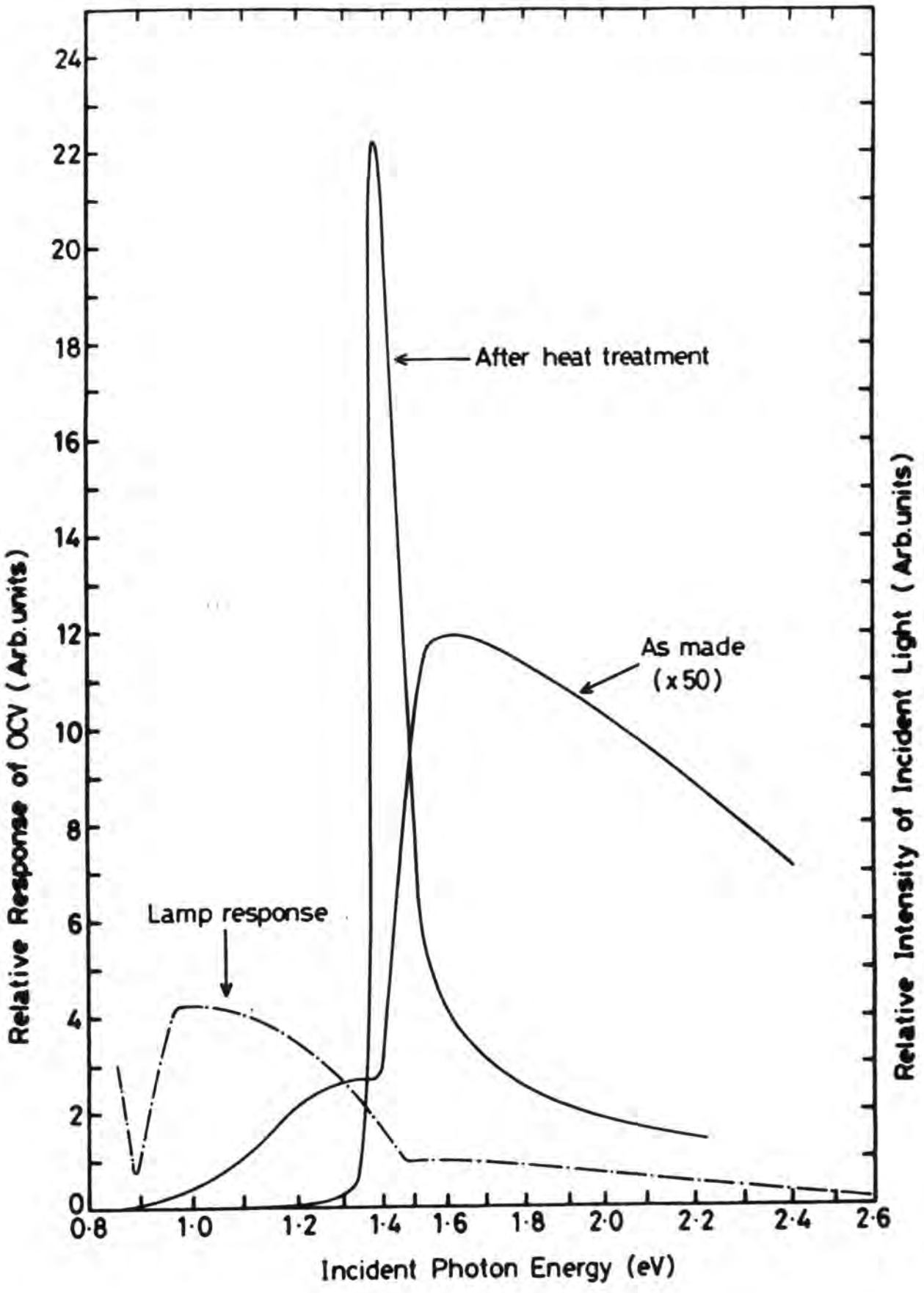


Fig. 9.17(b) : OCV spectral responses of an as-made and a heat treated cell.

The observed degradation in the performance of the annealed devices cannot be related to changes of structure since there were none (Section 9.2). However, it is likely that cross diffusion of Cu from the Cu_2Te into the n-CdTe substrate would have taken place. It is known to occur in the Cu_2S/CdS cell and the effects on the I-V characteristics of the heat treatment are well documented. Gill and Bube[46] have pointed out that copper diffusion would introduce deep acceptor-like states in a region near the junction. This would have a number of effects, but in particular would raise the CdS resistivity and thus the series resistance of the device. Similar arguments seem plausible in the present case. Copper diffusion into the n-CdTe substrate would also introduce deep acceptor levels and thus reduce the n-CdTe conductivity. This would raise the series resistance which in turn would reduce the SCC of the device. In addition the diffusion of copper into the CdTe would move the junction deeper into the substrate, leading to greater losses, and some carriers generated by absorption near the surface of Cu_2Te would be less likely to reach the junction. This is evident from the absence of any contribution to the spectral response of OCV and SCC from the light of energy greater than the CdTe band gap. A small rise in OCV after heating can be attributed to a photoconductive i-layer produced by copper diffusion in CdTe.

Similarly, changes observed in the hole diffusion length after heating would be expected because of the migration of copper into CdTe. The improvement in the minority electron diffusion length in Cu_2Te could be explained in terms of a reduction in the concentration of Cd^{++} ions in Cu_2Te on heat treatment. When devices are fabricated by the chemiplating, Cd^{++} ions are replaced by Cu^{+} ions. As the Cu_2Te layer grows in thickness, Cd^{++} ions fail to diffuse to the surface to be dissolved in the bath solution and are trapped in the Cu_2Te layer where

they may act as recombination centres, hence giving smaller diffusion lengths. But on heating these ions may diffuse to the surface and reduce the density of recombination centres in Cu_2Te, thereby improving the minority electron diffusion length. It is known that with CdS substrates, about 0.27 mol % cadmium exists in the Cu_2S layer formed by aqueous ion exchange[47].

9.7 Effect of Ageing

In order to study the effects of ageing, the photovoltaic output characteristics and the spectral response were measured periodically during storage in the laboratory. In general, the devices did not show degradation over a period of 6 to 8 weeks. However, in some cells the device parameters improved with ageing. These devices were fabricated on Cd annealed substrates and were chemiplated for about 50 secs.

The photovoltaic output characteristics of such a device in the as-made condition and after 6 months ageing are shown in Fig 9.18. The output characteristics of the as-made device indicated a high series resistance as well as non-ohmic behaviour of the contact. The I-V characteristic (under AM1 illumination) after 6 months showed a marked reduction in series resistance and an improved ohmic contact. The values of the SCC, OCV and FF for the as-made and aged device are shown in Table 9.3.

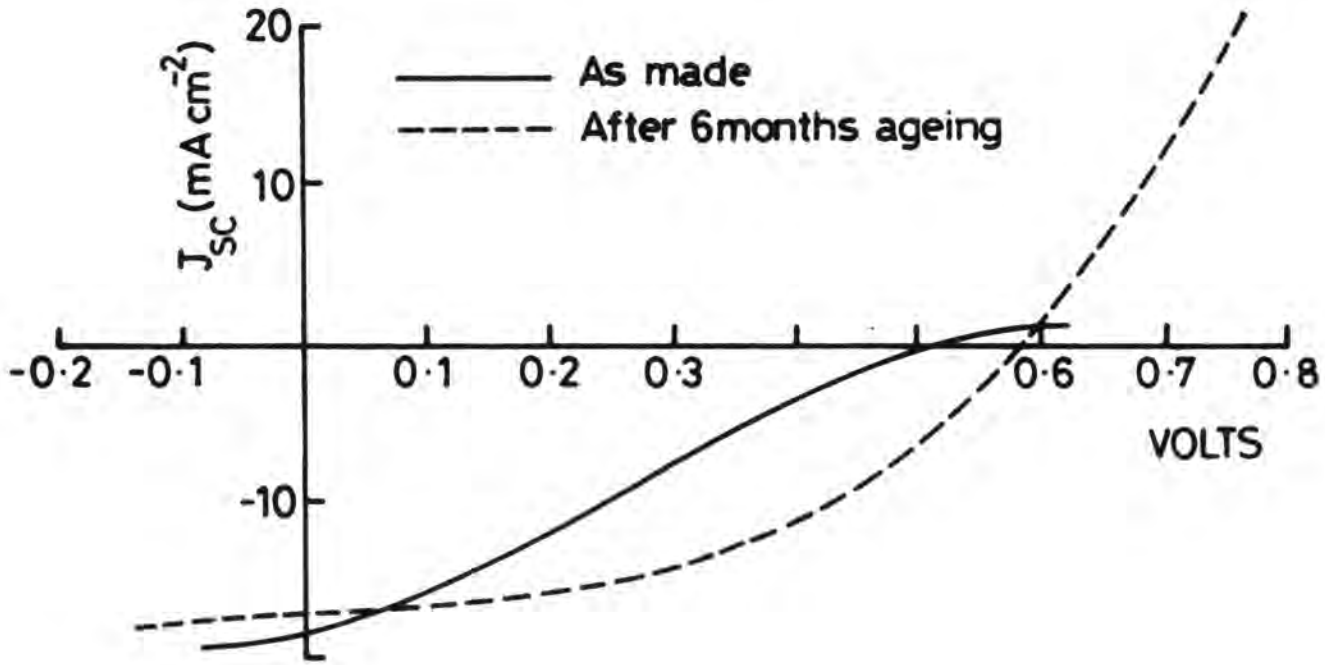


Fig. 9.18 : Photovoltaic characteristics of an as-made and an aged device

TABLE 9.3: Performance parameters for an as-made and aged device

Device	OCV (volts)	SCC mA/cm^2	FF (%)	η (%)
As-made	0.53	18.23	26.36	2.55
Aged (6 months) $\sim$	0.60	17.29	43.56	4.51

The spectral responses of the OCV and SCC for the as-made and aged device are shown in Fig 9.19. Fig 9.19b indicates that the SCC spectral response from the copper telluride was low in magnitude, and was more pronounced in the OCV response, as has been observed for most of the devices investigated. However, the overall magnitude of the SCC response decreased with time. The OCV spectral response also showed a reduction in the contribution from the Cu_2Te after 6 months.

Copper telluride films are believed to change with time[12,13] due to the effects of moisture, absorbed oxygen and diffusion of copper. This ultimately results in the degradation of $CdTe/Cu_2Te$ solar cells. However, in some of our cells the efficiency improved by a factor of two. This behaviour was probably a contact effect which improved with time.

The exact nature of any changes that might have occurred over this period is unclear. RHEED studies of Cu_2Te after ageing showed that no structural changes had taken place. However, the spectral response of the device after 6 months did show a reduction in the spectral

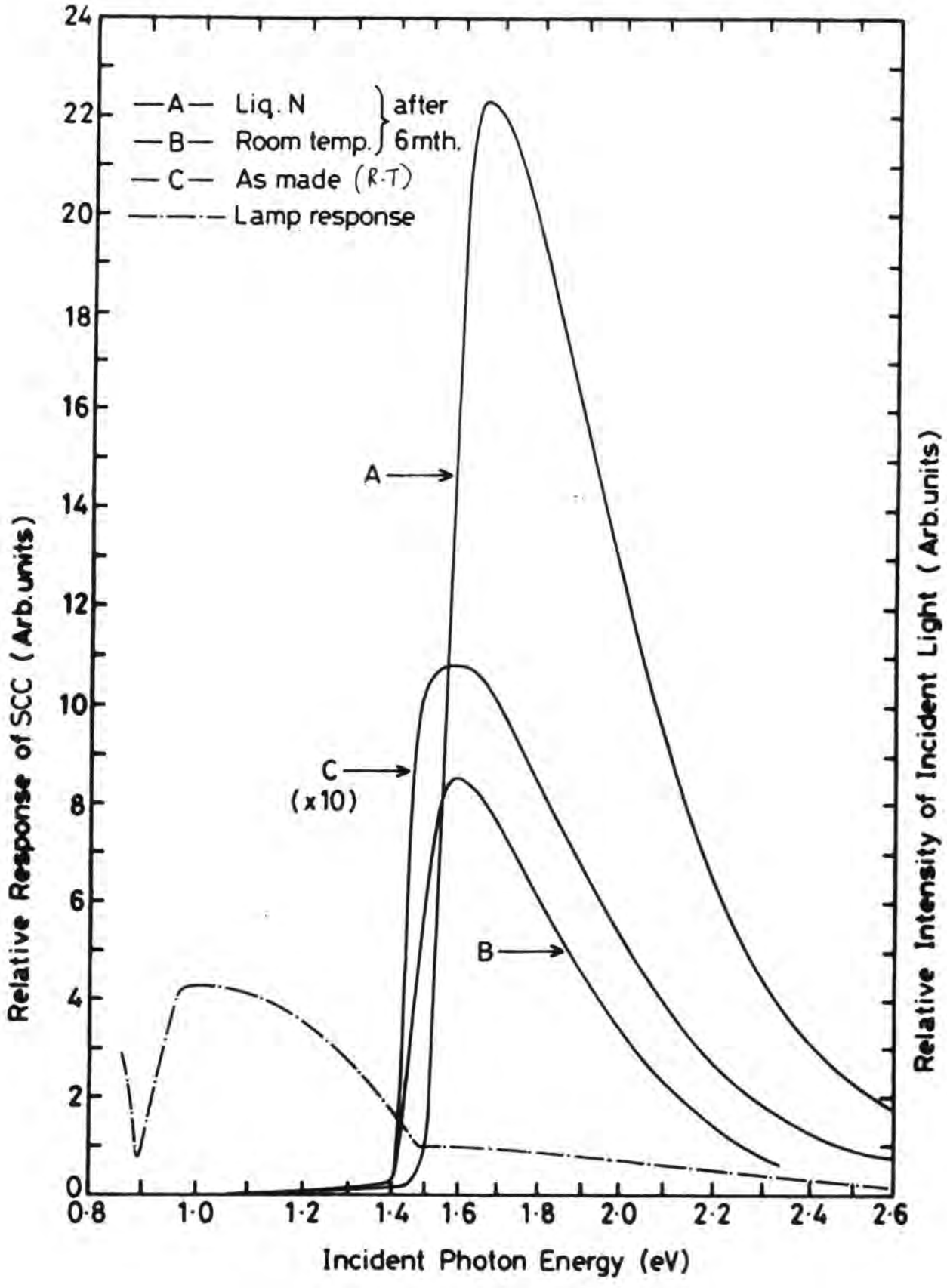


Fig. 9.19(a) : SCC spectral responses of an as-made device and after 6 months ageing

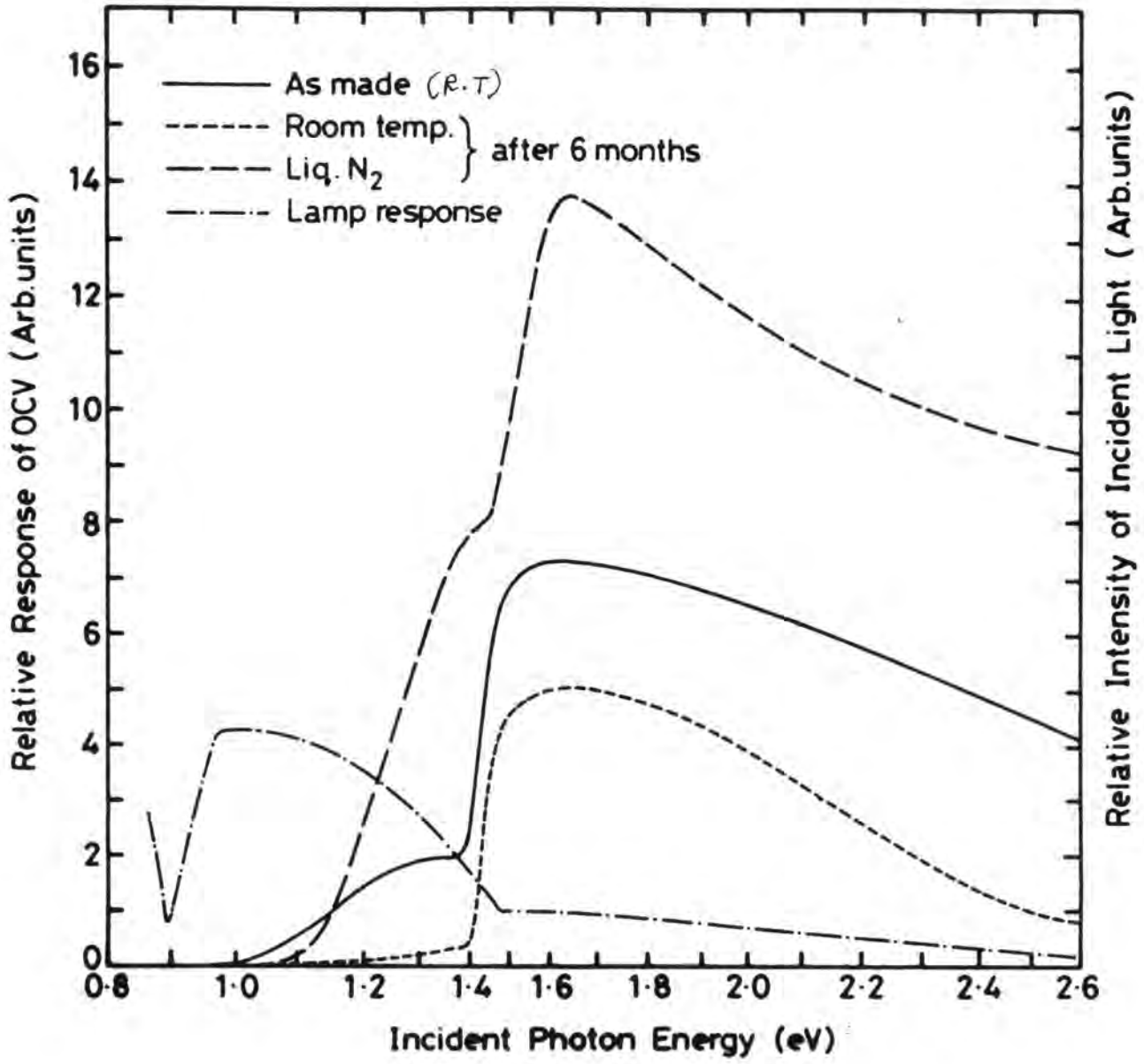


Fig. 9.19(b) : OCV spectral responses of an as-made device and after 6 months ageing

sensitivity of the Cu_2Te layer. This suggests that copper had diffused into the CdTe resulting in a reduction in the contribution from the Cu_2Te. The higher values of OCV at L.N. temperature are due to reduction in I_o which gave higher OCV. The reduction in the SCC with time could be due to a reduced diffusion length in the CdTe due to copper diffusion.

9.8 Conclusions

A study of Cu_2Te/CdTe heterojunctions in single crystal form has been carried out. Structural properties of Cu_2Te grown on single crystal (111) CdTe were investigated. The Cu_2Te was predominantly cubic and the structure was stable with no change of phase observed with heating in vacuum at 200°C for 10-15 mins, or with ageing over a period of two months.

Single crystal devices displayed good diode characteristics with a rectification ratio of $\sim 6 \times 10^3$ at 0.5 V and an ideality factor of 1.5. The values of SCC, OCV, FF and efficiency η for a device chemiplated for the optimum time ($\sim$ 40 sec) were 14 mA/cm^2, 0.5 V, 63% and 4.1% respectively. The spectral response measurements revealed that Cu_2Te appeared to be opto-electronically active. There was some evidence from steady state photocapacitance studies of an acceptor-like level lying close to the valence band. Its precise position could not be determined, but an upper limit of 0.59 eV was found. A donor level situated at a 0.015 eV below the conduction band was also observed in the low temperature spectra. There also appeared to be an additional level midway in the bandgap.

The effect of the substrate on the cell behaviour in terms of resistivity, surface preparation procedure and dopant used to control the resistivity was investigated. Diffusion length measurements indicated that Cl-doped substrates were undesirable, while Cd annealed

substrates gave improved diffusion lengths. This was fully reflected in the device performance. Solar cells prepared on pad polished substrates gave a 30% improvement in efficiency as compared to alumina polished. Studies relating to the effect of substrate resistivity showed that devices with very low resistivity (< 0.1 Ω-cm) gave narrow junctions which resulted in poor performance of the devices.

The effect of chemiplating time on device efficiency was also investigated. With short dipping times (∿ 20 sec) the devices were not very efficient. Similarly, longer chemiplating times (> 50 sec) gave reduced performance. The optimum dipping time was found to be ∿ 40 sec.

The effect of heat treatment and ageing on the electrical properties of the devices was also studied. Heat treatment for about 7 mins in vacuum at ∿ 200°C did not lead to improved efficiency. Rather it reduced the SCC drastically. Ageing studies showed that devices were stable over at least two months shelf storage.

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CHAPTER 10

EPITAXIAL GROWTH OF CdS ON CdTe

10.1 Introduction

The fabrication of CdS/CdTe solar cells usually entails the deposition of thin polycrystalline CdS on CdTe substrates or vice-versa. The two materials have a lattice mismatch of $\sim 9.8\%$[1] and also belong to different crystal systems, i.e. CdTe is cubic sphalerite whereas CdS is hexagonal wurtzite. Consequently, epitaxial structures have not generally been considered viable, however, we report in this chapter on the epitaxial growth of CdS onto CdTe.

Crystalline defects and non-uniformities can often trap free charge carriers or act as recombination centres and so affect carrier lifetimes, with deleterious effects on cell performance. With CdS/CdTe heterojunctions the interface between CdS and CdTe, and grain boundaries in the polycrystalline CdS films lead to high recombination rates for carriers. To achieve maximum efficiency, it is essential to minimize the recombination losses at the interface and at grain boundaries. One possible solution to these problems would be to find orientations of the substrates which might result in epitaxial growth of one material on the other, thus reducing the density of defects responsible for recombination losses.

Yamaguchi et al[2,3] have reported the epitaxial growth of CdS onto {111} CdTe by sublimation of the compound in a flow of hydrogen. They achieved an efficiency of 10.5% in their devices and also predicted that an epitaxial n-CdS/p-CdTe cell could in principle yield an efficiency of 19.7% under AMO conditions. They concluded that their cells were buried

homojunctions, probably due to the high substrate temperatures involved. In the present study (Chapter 7) the junctions were formed at a substrate temperature of ∿ 180°C and were true heterojunctions. The epitaxial deposition of CdS on CdTe reported in this Chapter was carried out at the same low substrate temperature. Unfortunately, the CdTe substrates were semi-insulating so that the resulting heterojunctions could be used for structural studies only. However, it is hoped to extend this work with a more systematic study of the photovoltaic properties of these types of cell later.

10.2 Growth of CdS on {221} CdTe Surfaces

The epitaxial growth of CdS on {221} CdTe was first observed during a wider investigation of CdS/CdTe heterojunctions, using evaporated thin films of CdS deposited onto oriented single crystal CdTe substrates[4]. Initially, the latter were cut parallel to the {100} plane from single crystal boules grown in house from the vapour phase (Sect.4.3.3). The CdTe slices were then manually pad polished (Sect.4.2.2) in a 2% solution of Br in methanol before being loaded into the CdS evaporation system. CdS was evaporated onto the CdTe with a source temperature of ∿ 900°C and substrate temperature ∿ 180°C.

Growth on the {100} face always resulted in polycrystalline layers, though these layers often exhibited a high degree of preferred orientation as shown by the 100 KV RHEED pattern in Fig 10.1. On one occasion, it was observed that in a region of the (100) CdTe substrate where a narrow lamellar twin band had intersected the substrate surface, the CdS was qualitatively different in appearance from the rest of the film. In particular, the CdS in the twinned region was smooth and shiny, while that in the untwinned part had a matt appearance. More importantly, further investigation in RHEED showed that the CdS

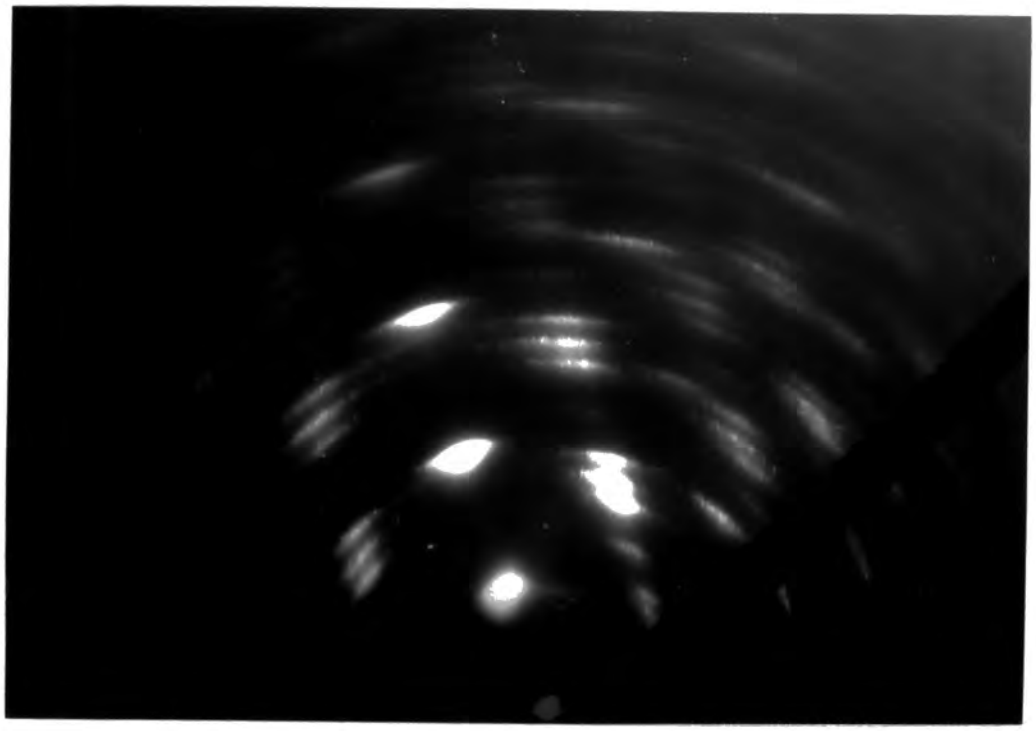

Fig. 10.1 : RHEED pattern taken from a CdS film deposited onto an untwinned region of a {100} oriented CdTe substrate.

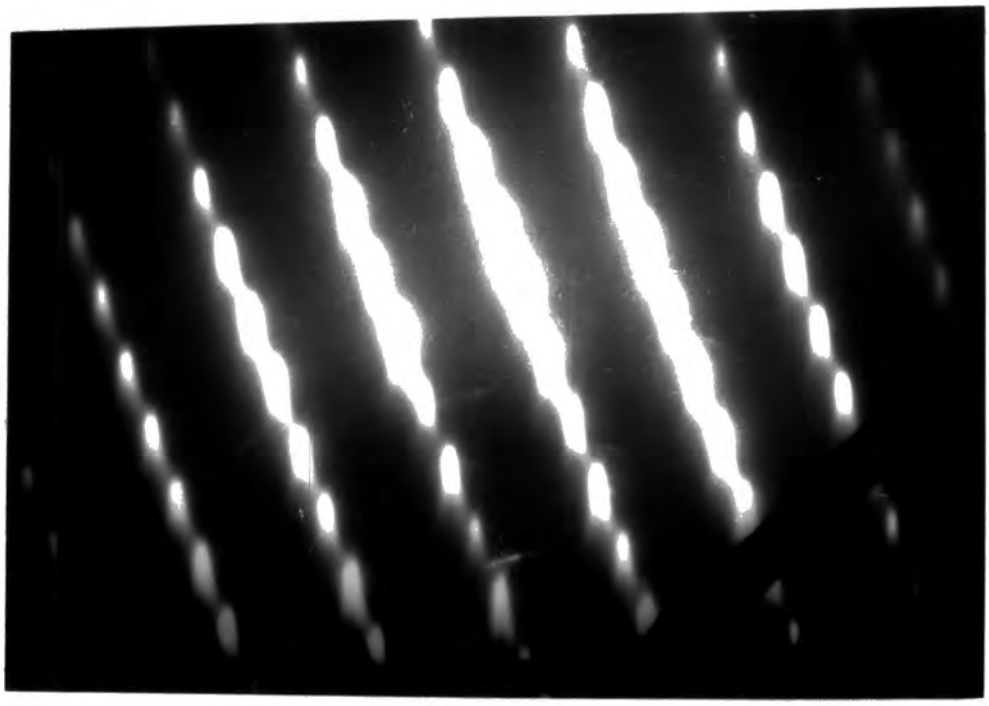

Fig. 10.2 : RHEED pattern recorded from a CdS layer deposited onto a twinned region of the same substrate

deposited on the twinned area was single crystal as demonstrated by the diffraction pattern in Fig.10.2. This pattern was recorded from the same layer which yielded the pattern of Fig.10.1, after simply translating the sample across the beam without changing its orientation. An attempt was then made to determine the orientation of the twinned region and to reproduce the epitaxial growth on deliberately oriented substrates.

10.3 Determination of Twin Orientation

Crystals were generally oriented, using Laue X-ray back reflection and subsequently the orientation was confirmed in RHEED. The orientation of the twinned region was first determined with Laue X-ray back reflection. The CdTe with the twin was fixed onto the goniometer such that the X-ray beam from the X-ray source was incident normally on the surface. The X-ray micrograph obtained from the twin region showed that the twin surface was tilted away from the {111} plane through an angle of $\sim 16^\circ$ towards {001}. Reference to standard tables of angles between crystal planes[5] in cubic crystals indicated that this was probably the {221} orientation. Unfortunately, this could not be confirmed by RHEED because of the small width of the twin band.

This identification however, was confirmed by calculating the twin matrix transformation. For twinning on a {111} plane the twinning matrix is [6,7]

$$= 1/9 \begin{vmatrix} -1 & -2 & -2 \\ -2 & -1 & 2 \\ -2 & 2 & -1 \end{vmatrix}$$

and multiplying this matrix by the surface plane in the untwinned part of the crystal (i.e. the {100} plane) will give the corresponding plane

in the twinned region, as follows:

$$\text{Twin plane} = 1/9 \begin{vmatrix} -1 & -2 & -2 \\ -2 & -1 & 2 \\ -2 & 2 & -1 \end{vmatrix} \begin{vmatrix} 1 \\ 0 \\ 0 \end{vmatrix} = -1/9 \begin{vmatrix} 1 \\ 2 \\ 2 \end{vmatrix}$$

10.4 Epitaxial Deposition of CdS on Oriented {221} CdTe

A single crystal boule of CdTe was deliberately oriented parallel to the (221) plane. Substrates ∿ 2mm thick were cut, pad polished in 2% Br in methanol solution and loaded into the CdS evaporator. About 15 g of purified CdS (Section 4.2.2) was placed in the evaporation source and a layer of CdS was then deposited onto the substrate under nominally identical conditions (substrate temperature 180°C, source temperature 900°C).

The CdS films were characterized by RHEED and SEM. The diffraction pattern recorded from a typical film grown on {221} CdTe is shown in Fig 10.3. It is evident from the spot pattern (Fig 10.3) that the CdS layer had grown epitaxially on the {221} CdTe, and there was no evidence of any polycrystallinity in these films. Analysis of the RHEED pattern showed it to be characteristic of the $[10\bar{1}0]$ zone axis tilted such that the $[01\bar{1}6]$ spot lay on the perpendicular to the shadow edge from the origin. This indicates that the epitaxial relationships were close to:

$$(221)_{CdTe} \; // (01\bar{1}6)_{CdS}$$

$$[110]_{CdTe} \; // \; [10\bar{1}0]_{CdS}$$

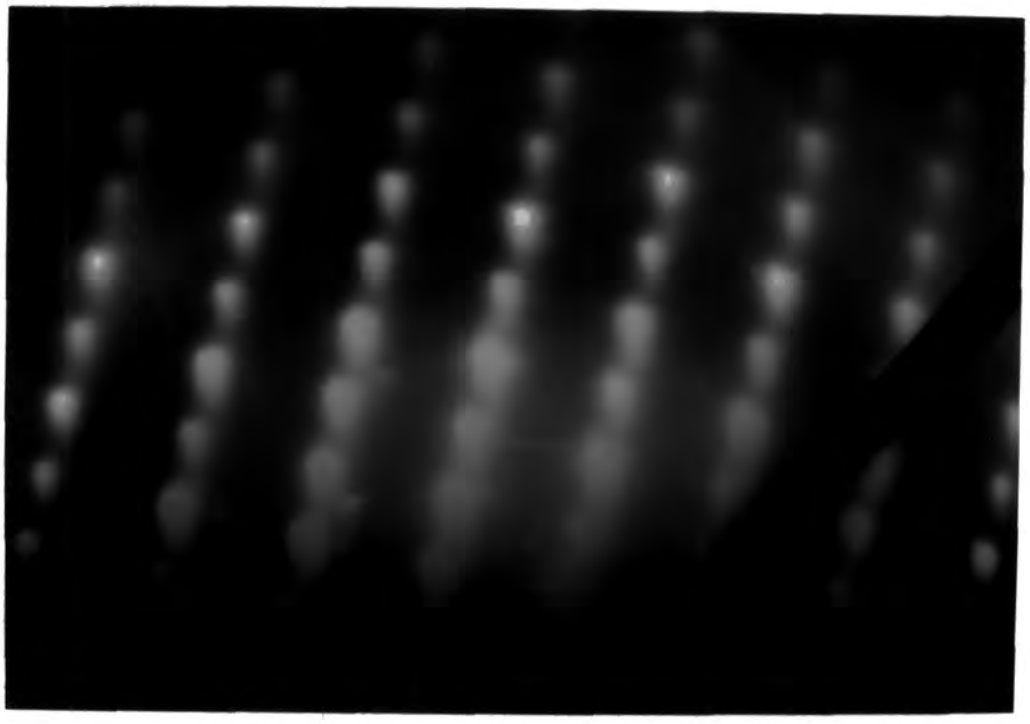

Fig. 10.3 : RHEED pattern from a CdS layer grown onto a {221} oriented CdTe substrate. The electron beam lay along <110> zone axis.

Surface morphology studies in the SEM, and by optical microscopy, indicated the presence of small hillocks (< 1 μm) with a density of 10^5 cm^{-2}. Apart from the hillocks these layers were relatively smooth and free from any other surface features.

10.5 Epitaxial Growth on {111} Oriented CdTe Substrates

As described earlier, Yamaguchi et al deposited epitaxial CdS on {111} CdTe by a vapour phase process. The CdTe substrates were cut from {111} oriented single crystal boules and hydroplane polished (Sect.4.4.3 CdS was deposited on {111}A and $\{\bar{1}\bar{1}\bar{1}\}$B faces using a substrate temperature of 180°C and source temperature of 900°C.

Layers of CdS deposited onto {111}A CdTe were visually matt and uneven in texture. Nevertheless, these layers were largely single crystal as evidenced by the RHEED diffraction pattern in Fig 10.4. This was recorded with the beam along the $\langle 110 \rangle_{cubic}$ or $\langle 10\bar{1}0 \rangle_{hexagonal}$ direction and shows a well formed, distinct spot pattern. The epitaxial relations were found to be

$$(111)_{CdTe} \; // \; (0002)_{CdS}$$

$$[01\bar{1}]_{CdTe} \; // \; [10\bar{1}0]_{CdS}$$

In addition to the spot pattern, however, there is a faint pattern of rings passing through the spots, indicating the presence of some polycrystalline material.

Examination of the surface morphology in the SEM and by optical microscopy revealed the presence of a high density of hillocks on the surface of the film as shown in Fig 10.5. Typically, these were

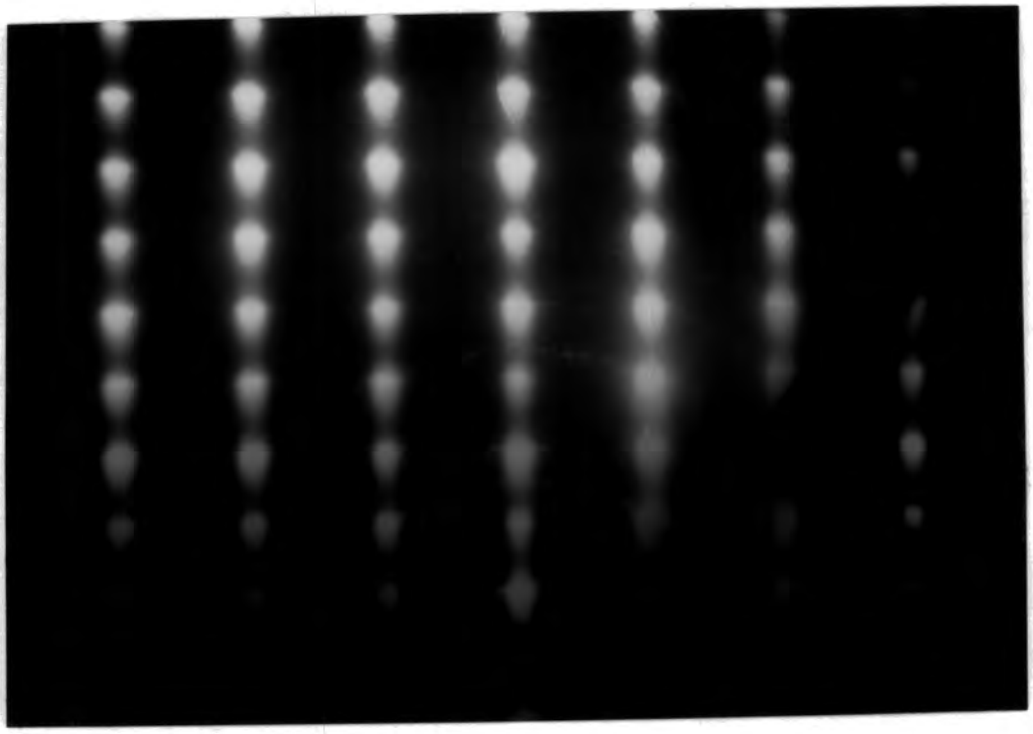

Fig. 10.4 : RHEED pattern recorded from a CdS layer deposited onto a {111}A CdTe substrate with the electron beam along <110> zone axis.

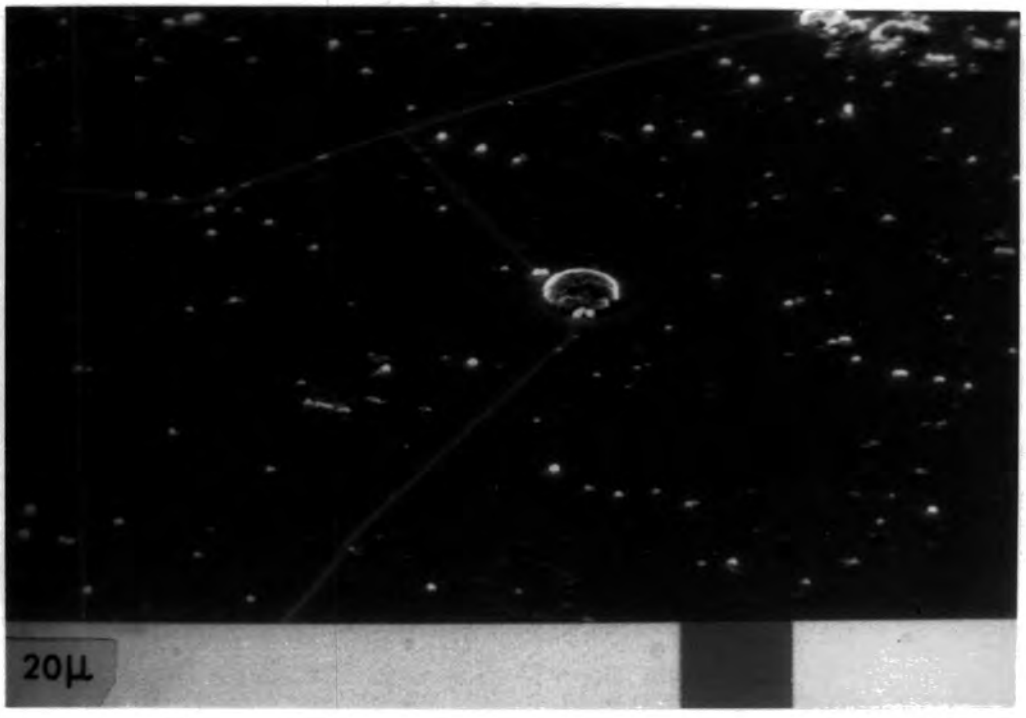

Fig. 10.5 : Surface morphology of the epitaxial CdS grown on a {111}A CdTe substrate.

observed to have a density of 10^6 cm^{-2} and were generally a few μm across. In between the hillocks the surface was very flat and featureless, although long cracks, often found to be centred on one of the larger surface hillocks, were observed along crystallographic directions (Fig 10.5). The cracks were generally found to run in parallel lines across the surface at spacings of a few tens of μm.

Layers of CdS grown on $\{\bar{1}\bar{1}\bar{1}\}$B CdTe possessed a mirror-like surface. When examined in the SEM these layers were still found to be characterized by the small hillocks but at a very much reduced density of 5×10^4 cm^{-2}. However, these films also displayed long straight cracks similar to those in the films grown on the A face. Again, these often seemed to be associated with the hillock-like features and ran along crystallographic directions (Fig 10.6).

RHEED studies indicated that these layers were structurally superior to those grown on the A face. A RHEED pattern recorded from a typical film grown on the B face is shown in Fig 10.7. There is no evidence of any polycrystalline material and streaks perpendicular to the shadow-edge indicate that the surface was very flat and smooth.

10.6 Discussion

The epitaxial deposition of II-VI compounds onto foreign substrates with a substantial lattice mismatch has been reported for several systems, most notably (Hg,Cd)Te/GaAs[8] and CdTe/GaAs[9], where the lattice mismatch is ∿ 14% and ZnS/GaAs[10] where the mismatch is 5%. Cross-sectional TEM studies of these systems have shown that the strain is accommodated in a variety of ways, depending on the material and substrate orientation. When CdTe is grown epitaxially onto {100}GaAs surfaces, the CdTe may adopt either the {111} or the {100} orientation[11,12]. In the latter case the lattice mismatch is taken up

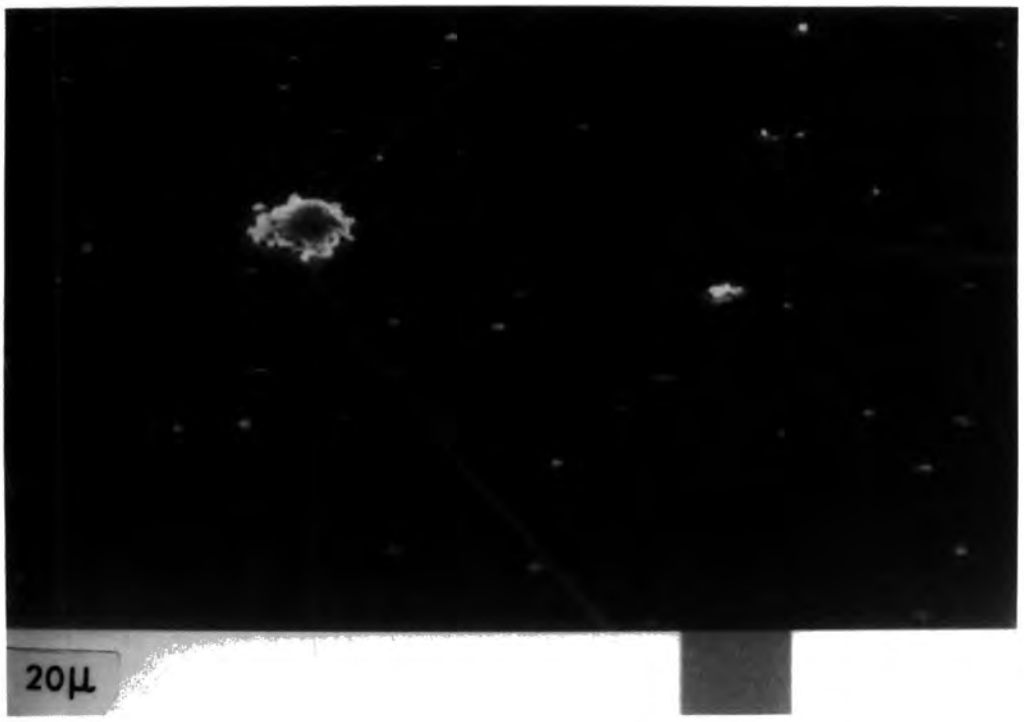

Fig. 10.6 : Surface morphology of epitaxial CdS grown on $\{\bar{1}\bar{1}\bar{1}\}$B CdTe substrate.

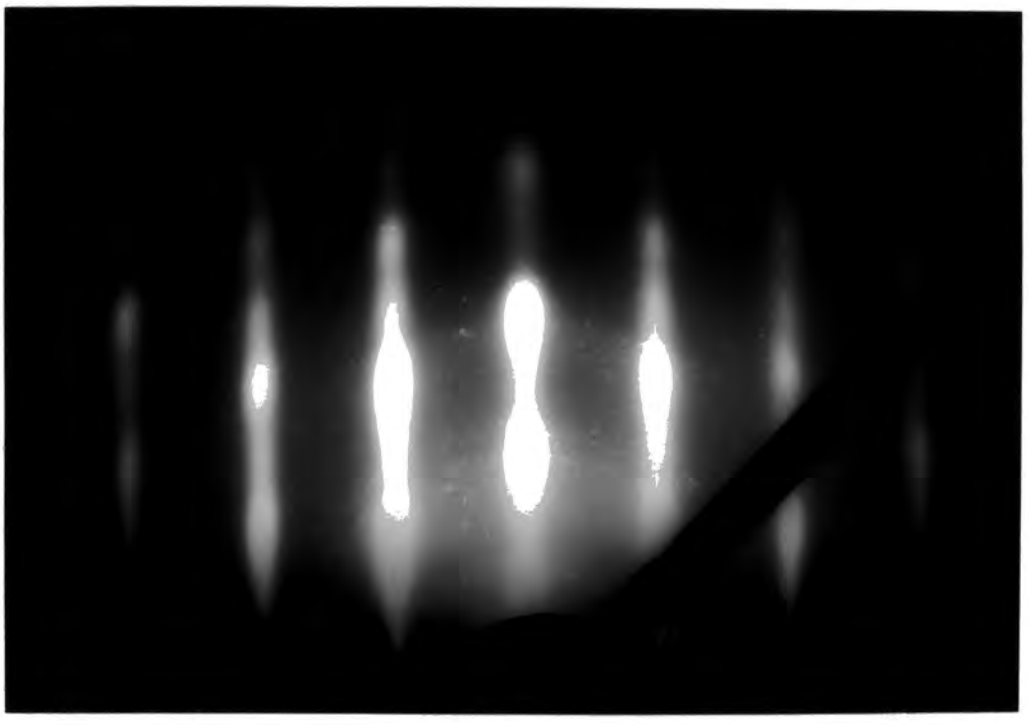

Fig. 10.7 : RHEED pattern taken from an epitaxial layer of CdS deposited onto a $\{\bar{1}\bar{1}\bar{1}\}$B CdTe substrate with the electron beam along <110> axis.

by a dense array of misfit dislocations which extend to a depth of $\sim$ 0.5 μm into the epitaxial layer[11,13]. Epitaxial layers of CdTe displaying the {111} orientation, whether grown on {100} or {111} GaAs substrates, are generally found to contain thin lamellar twins lying parallel to the interface[11], which may help to accommodate the lattice mismatch. Similar studies with the ZnS/GaAs heterojunctions have shown that there is a high density of microtwins which nucleate at the interface and propagate through the epilayer[14]. In the present case, there appears to be no evidence from RHEED of any twinning, nor any significant density of planar defects (these would give rise to characteristic streaking in the RHEED pattern along <111> directions. However, the large scale cracking which is observed is typical of highly strained layers.

The epitaxial growth of CdS on CdTe although unexpected, is most conceivable on the $(111)_{cubic}$ and $(0002)_{hexagonal}$ planes, since these are the close packed planes in both structures. Atomic positions are therefore similar, although the lattice parameters are of course different. The fact that the CdS layers grown on the $\{\bar{1}\bar{1}\bar{1}\}$B (Te) face of CdTe were superior to those deposited on the {111}A (Cd) face, is consistent with experience in other epitaxial systems involving CdTe. For example, the morphology of CdTe and (Hg,Cd)Te layers deposited epitaxially on CdTe substrates is significantly worse where growth takes place on the A face rather than the B face[15]. This may indicate that the A(or Cd) faces are more prone to contamination (i.e. oxide formation) than the B(or Te) faces with consequent implications for the nucleation behaviour of the deposited material.

The epitaxial growth of CdS on {221} CdTe is more unexpected. It is not immediately clear that the $\{221\}_{CdTe}$ and $\{01\bar{1}6\}_{CdS}$ planes are

equivalent in the same sense that the $(111)_{cubic}$ and $(0002)_{hexagonal}$ planes are. However, it is interesting to note that the {221} planes are inclined to the {111} by 15.79° and the $\{01\bar{1}6\}$ planes are inclined to the {0002} by 17.35°. The difference of 1.56° is within the experimental error (∿ 2°) inherent in the RHEED measurements. Thus it is possible that the CdS planes which lay parallel to the {221} substrate planes were actually ∿ 1.5° off the $\{01\bar{1}6\}$, since such a difference would be difficult to detect.

10.7 Conclusion

It has been demonstrated that deposition of epitaxial CdS onto {111}A, $\{\bar{1}\bar{1}\bar{1}\}$B and {221} oriented CdTe substrates by thermal evaporation in vacuum is feasible. It was found that the structural quality of the layers grown on the $\{\bar{1}\bar{1}\bar{1}\}$B CdTe face was superior to that of layers deposited on to the A(Cd) face, and were comparable to films produced on the {221}CdTe substrates. However, growth on the {111}A and $\{\bar{1}\bar{1}\bar{1}\}$B faces led to highly strained layers that cracked along well defined crystallographic directions. The layers deposited on all three types of surfaces displayed an even distribution of small hillocks although the density was much greater on the layers deposited on {111}A (CdTe) surfaces.

Currently, the main problems with the CdS/CdTe heterojunction relate to the high resistivity of CdTe resulting in a high series resistance and difficulties in the fabrication of stable, low resistance ohmic contacts to P-CdTe. However, improving the quality of the CdS layer, through the removal of grain boundaries which improve carrier lifetimes, would of course result in better device performance. Of more

technical importance, however, would be the reverse procedure of epitaxial deposition of CdTe onto oriented CdS substrates. If this can be achieved, it raises the possibility of producing more highly conducting p-type CdTe and hence of reducing some of the current difficulties with this particular solar structure.

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CHAPTER 10

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CHAPTER 11

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

11.1 Introduction

The major thrust of the work described in this thesis was to investigate the material and device fabrication aspects of CdTe based solar cells. During the development of the project the work was subdivided into material characterization, fabrication and characterization of the photovoltaic devices. Different versions of CdTe cells investigated included:

(1) Bulk single crystal CdTe/CdS heterojunctions.

(2) Thin film CdS/CdTe solar cells.

(3) Bulk single crystal CdTe/Cu_2Te devices.

These studies led to the important observation of epitaxial growth of CdS on CdTe substrates using thermal evaporation. The project was therefore, further extended to an investigation of epitaxial deposition of CdS on oriented CdTe substrates, particularly on {221} and {111} planes.

11.2 Summary of Results

11.2.1 Characterization of Material

The high resistivity as-grown CdTe was investigated by analysing space charge limited currents (SCLC). It was found that the material was extrinsic (Section 6.2) in the temperature range 200-360K and an activation energy of 0.5 eV was measured.

DLTS measuremnets were made on Schottky barrier devices, fabricated on Te-annealed CdTe substrates, and thin film CdS/CdTe heterojunctions with Cu doped CdTe films. The electrically dominant deep levels in the Te-annealed material were at 0.53, 0.71 and 0.84 eV above the valance

band. The energy level at 0.53 eV is believed to be due to a native defect, possibly a Cd vacancy. The level at 0.71 eV is considered to be due either to impurities or to defects introduced during the annealing process, while the level 0.84 eV may be due to either doubly ionized Cd vacancies or Te interstitials. With thin film CdS/CdTe cells with a Cu doped CdTe layer, an energy level at 0.35 eV above the valence band was observed. This is most possibly related to the copper impurity.

11.2.2 Bulk Single Crystal CdS/CdTe Solar Cells

In these devices carbon contacts on p-CdTe resulted in improved device parameters, particularly the fill factor and efficiency which increased by factors of $\sim$ 2 compared with identical devices employing evaporated Au contacts. Carbon contact devices had a significantly lower series resistance. This was attributed to the diffusion of acceptor impurities from the C paste into the surface of CdTe, creating a p^+ doped region under the contact. As a result, there was probably a narrower Schottky barrier (between CdTe and C) through which the carriers were able to tunnel. Minority electron diffusion lengths were also larger in the C-contact devices, which is thought to be due to the back surface field (BSF) effect resulting from impurity concentration gradient under the contact.

The optimum annealing temperature for C-contacts was found to be $\sim$ 300°C. These contacts were stable with time. In comparison, heat treatment of Au contacts did not improve cell performance significantly, although a 10 min anneal at 180°C in Ar was found to be optimum. Au contacts degraded with time.

Phosphorus doping was found to be best for low resistivity CdTe substrates as compared with Cu and Te doping. Solar cells on p-doped substrates were the most efficient, having higher FF and SCC than those made on undoped, Cu and Te doped substrates. Minority carrier

(electron) diffusion lengths were however, larger in the nominally undoped CdTe, probably due to better crystallinity and absence of defects introduced during post-growth doping.

Substrates prepared by the pad polishing technique had a damage free surface as compared to mechano-chemically polished surfaces. After polishing with alumina and cerium oxide paste, followed by Br-methanol etch, it was found that the polishing material became embedded in the CdTe surface. In consequence, devices fabricated on pad polished substrates gave the best results. The best devices had SCC, FF, OCV and η of 21 mA cm^{-2}, 47%, 0.72 V and 7.2% respectively.

11.2.3 Thin Film CdS/CdTe Solar Cells

The deposition conditions strongly affected the electrical and structural properties of both CdS and CdTe films, which in turn influenced the final device efficiency. The optimum substrate temperature for CdS films was 180°C, while for CdTe layers it was 200°C. Layers produced at the optimum temperatures displayed a high degree of preferred orientation and excellent columnar growth, although with the CdTe this did not result in a reduction in the resistivity (in fact the CdTe resistivity remained relatively insensitive to the growth temperature, being primarily a function of the doping). The resistivity of the as-grown undoped CdTe layers was very high and efforts to reduce it by doping with Cu, Te and Sb during deposition were unsuccessful. However, post-growth doping with Cu did result in a low resistivity. The resistivity of the CdS films, which was relatively low, was found to increase with increasing substrate temperature from 120-300°C, although increasing the evaporation rate had the reverse effect.

The CdTe layer thickness, copper concentration, contact sintering temperature, cell dimensions and crystallinity of the films all had important roles to play in producing efficient cells. The most

efficient device ($\eta > 3\%$) was obtained with a 6 μm thick CdTe layer, 300 ppm copper concentration and contact annealing temperature of ∿ 330°C. The optimum cell dimensions were 12 x 4 mm (Area = 0.48 cm^2). The value of SCC (∿ 17 mA cm^{-2}) was respectable but the OCV and FF were low. These devices were very stable (SCC rather improved).

Photocapacitance studies were used to identify deep levels. The dominant level in the Cu doped CdTe layers was ∿ 0.35 eV above the valence band and was probably related to Cu. Three other levels at 0.64 eV above the valence band in CdS, and 0.26 eV and 0.12 eV below the conduction band in CdS were also observed.

Devices with C-Cu/CdTe/CdS/In (screen printed carbon contact) and Cr-Au/CdTe/CdS/In structure had very poor performances as compared to reverse structure on tin oxide coated slides. In particular, heat treating the latter at 375°C for 30 minutes degraded the device and resulted in the formation of two junctions with reverse polarity.

11.2.4 Bulk Single Crystal Cadmium Telluride/Copper Telluride Cells

The Cu_2Te was grown topotaxially onto (111) oriented n-CdTe substrates by dipping into a hot aqueous solution of cuprous chloride. The substrates were converted from their as-grown semi-insulating state to highly conducting n-type by annealing in Cd. Some devices were also fabricated on substrates that had been doped with Cl during growth. The Cu_2Te was found to be predominantly cubic in structure and stable with time. No change of phase was observed after heating in vacuum to 200°C for 10-15 minutes or after ageing over a period of two months. The resulting devices were, not surprisingly, also found to be stable.

The n-CdTe/Cu_2Te devices were highly rectifying with a rectification ratios of 6 x 10^3 at 0.5 V and ideality factors of 1.5. Solar cell parameters, SCC, OCV, FF and η for a device chemiplated for an optimum time of 40 sec were 14 mA cm^{-2}, 0.5V, 63% and 4.1%

respectively. In contrast to the observations of other research workers, Cu_2Te was found to be opto-electronically active. The spectral dependence of PHCAP revealed that an acceptor level some 0.59 eV above the valence band of CdTe was present (this was possibly due to the copper centre); a donor level was also observed at 0.015 eV below the conduction band.

Minority carrier diffusion length in the Cd annealed substrates was almost three times higher than in the Cl-doped material and consequently devices prepared on Cd treated samples were much more efficient. As for the CdS/CdTe single crystal heterojunctions, cells prepared on pad polished substrates gave about 30% better efficiency than those on alumina polished. Heterojunctions on very low resistivity ($\rho < 0.1$ Ω-cm) substrates gave narrow junctions which resulted in poor performance.

The optimum chemiplating time was 30-40 sec. Heat treatment for 7 mins in vacuum at 200°C did not improve device efficiency; rather it reduced the SCC.

11.2.5 Epitaxial Growth of CdS on CdTe

It was demonstrated that it is possible to grow epitaxial layers of CdS onto {111} and {221} oriented CdTe substrates by thermal evaporation in vacuum. The structural quality of the films grown on {111}B faces was superior to that of films deposited onto the {111}A faces, and comparable to that of films grown on {221} planes. Layers produced on all three types of surface displayed an even distribution of small hillocks although the density was greater on the layers deposited on the {111}A CdTe.

Growth on the {111}A and {111}B faces led to highly strained layers that cracked along well defined crystallographic directions. Importantly, no cracks were observed for CdS layers grown on {221} CdTe substrates, suggesting that growth on this plane may be advantageous.

11.3 Suggestions for Future Work

In order to extend the scope of the work described in this thesis, the following suggestions are made:

(1) Following the success in depositing epitaxial CdS layers onto CdTe substrates, and the suitability of the phosphorus doping technique in reducing the resistivity of bulk CdTe crystals, it would be appropriate to continue the phosphorus doping of CdTe in order to obtain a resistivity in the 1-10 Ω-cm range. This material would be ideal for the production of fully epitaxial CdS/CdTe heterojunctions which should have reduced recombination losses at the interface and at grain boundaries in the CdS. Efforts to dope CdS layers should also be fruitful to reduce series resistance and hence improve solar cell efficiency.

(2) Since thin film CdS/CdTe devices are the potential candidates for low cost cells, it is essential to pursue further research on these devices. In the thin film cells the SCC was reasonably high (17 mA cm^{-2}) while the OCV and FF were low. This may have resulted mainly from a high series resistance (contribution from the CdS and CdTe layers), particularly the high resistivity at the interface. It would be interesting to optimize the fabrication of devices with thin CdTe layers to avoid diffusion of Cu into the CdS and consequently improve device performance. Attempts to reduce the resistivity of the window layer should also contribute to the fabrication of an efficient low cost thin film CdS/CdTe solar cell.

(3) With CdTe/Cu_2Te cells the OCV was again low, although the FF was respectable (63%) and hence efforts to optimize the n-CdTe resistivity may help improving the OCV and so produce solar cells with a higher efficiency. Moreover, this work could be extended to a thin film version of n-CdTe/p-Cu_2Te devices.

Finally, the photocapacitance and DLTS techniques may be used to characterise traps involved in different versions of CdTe solar cells.