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Studies of CdTe Thin Films and Solar Cells Grown by MOCVD

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By

Guillaume ZOPPI, BSc, MSc

A thesis presented in candidature for the degree of Doctor of Philosophy in the University of Durham

Department of Physics
October 2005

07 DEC 2005

ABSTRACT

This thesis presents the results of investigation of arsenic doped CdTe thin films and CdTe/CdS solar cells grown by MOCVD. Particular emphasis has been placed on the electrical and microstructural characterisation of layers and structures, and the effects of the post-deposition heat treatment of the materials and devices.

For a growth temperature of 400°C, using dimethylcadmium, di-isopropyltelluride and dimethylamino arsine as precursors, the incorporation of arsenic in thin films of CdTe is dependent on the ratio of organometallics partial pressures in the growth ambient (VI/II ratio) with concentration of up to 2×10^{19} at.cm^{-3} for a VI/II ratio of 0.73. The dependency of the lateral resistivity upon arsenic incorporation was investigated and found to increase for higher arsenic concentrations. The influence of the growth temperature and VI/II ratio on the texture and lattice parameter of the films is also examined.

Investigations of the microstructure of absorber layers of CdTe/CdS bi-layers revealed that grain size and preferred orientation are dependent on the thickness of the films which is itself a function of the substrate position on the susceptor block. The influence of the post-deposition heat treatment with and without $CdCl_2$ was investigated by means of XRD and SEM. In both cases annealing causes a recrystallisation from the [111] into the [422] direction and a reduction in the in-plane lattice stress of the CdTe layers. The grain size increases from 0.7 to 1.3 μm only in the presence of $CdCl_2$ and Burke and Turnbull's grain growth exponents of 7 and ~4 are derived for ~8 μm thick films treated at 440°C and 400°C.

The activation of CdTe/CdS bi-layers using the $CdCl_2$ heat treatment shows that only devices with ~4 μm CdTe can be made into efficient solar cells. Thinner and thicker structures produce cells exhibiting no photoresponse due to the lack of sustainability of the thin layers during treatment and the particularly low conductivity of the thicker layers. Optimisation of the $CdCl_2$ treatment indicates that best devices are produced following an 18 min annealing at 420°C for structures coated with a 30 nm layer of $CdCl_2$. The cells are limited by a poor fill factor arising from low shunt and high series resistances indicated by a high reverse saturation current and diode quality factor.

DECLARATION

I declare that with the exception of those procedures listed below all the work presented in this thesis was carried out by the candidate. I also declare that none of this work has previously been submitted for any degree and that it is not being submitted for any other degree.

Samples were provided by Dr A. Stafford and Dr V. Barrioz, Department of Chemistry, University of Wales, Bangor.

SIMS measurements included in Chapter 5 were performed by MATS-UK.

K Durose .....

Dr K. Durose

Supervisor

.....

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I wish to extend my gratitude to the technical staff of the physics department, especially Norman Thompson and David Pattinson for their expertise and friendly technical support. I also acknowledge Dr Tom Hase from this department and Dr John Evans from the department of chemistry for allowing me to carry out the XRD work.

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CONTENTS

ABSTRACT ii

DECLARATION iii

ACKNOWLEDGMENTS iv

LIST OF SYMBOLS x

---

1 Introduction 1

1.1 References for Chapter 1 5

---

2 Fundamentals of Solar Cell Devices 6

2.1 Introduction 6

2.1.1 Historical Development 6

2.1.2 The Photovoltaic Effect 7

2.2 Solar Cell Configurations 8

2.2.1 Schottky Junction 8

2.2.2 Homojunction 9

2.2.3 Heterojunction 10

2.3 Diode Physics and Cell Parameters 12

2.3.1 The Diode Equation 12

2.3.2 Current-Voltage Characteristic and Cell Parameters 14

2.3.3 Efficiency Limits and Losses 17

2.3.3.1 Short Circuit Current 18

2.3.3.2 Open Circuit Voltage 19

2.3.3.3 Fill Factor 19

2.4 Types of Solar Cells 20

2.4.1 Single Crystal and Polycrystalline Silicon 20

2.4.2 Group III-V Technologies 21

2.4.2.1 Gallium Arsenide 21

2.4.2.2 Indium Phosphide 22
2.4.3 Thin Film Solar Cell 22
2.4.3.1 Hydrogenated Amorphous Silicon a-Si:H 22
2.4.3.2 Copper Indium Diselenide ($CuInSe_2$) 23
2.4.3.3 Cadmium Telluride (CdTe) 24
2.5 References for Chapter 2 **25**

3 Thin Film CdTe/CdS Solar Cells **29**

3.1 Introduction **29**
3.2 Solar Cell Structure **30**
3.2.1 The substrate 31
3.2.2 The Front Contact 31
3.2.3 The CdS Window Layer 32
3.2.4 The CdTe Absorber Layer 32
3.2.5 The Back Contact 33
3.3 Material Deposition Techniques **35**
3.3.1 Chemical Vapour Deposition 35
3.3.2 Other Deposition Techniques 39
3.4 Post-Deposition Treatment **42**
3.5 Typical Device Characteristics **45**
3.6 Defects and Doping in CdTe Materials **47**
3.7 Concluding Remarks **50**
3.8 References for Chapter 3 **52**

4 Sample Preparation and Characterisation Techniques **60**

4.1 Introduction **60**
4.2 MOCVD Growth of CdS, CdTe and CdTe:As **61**
4.3 Post-Deposition Treatment **65**
4.4 Solar Cell Characterisation **66**
4.4.1 Solar Radiation and Solar Simulator 66
4.4.2 Current-Voltage Measurements 69

4.4.3 Spectral Response Measurements 70
4.5 Electrical Measurements for Individual Layers 71
4.5.1 Carrier Type Determination 71
4.5.2 Resistivity and Sheet Resistance 73
4.6 Scanning Electron Microscopy 75
4.7 X-Ray Diffraction 77
4.7.1 Determination of the Lattice Parameter 79
4.7.2 Grain Size and Deformation Strain 79
4.7.3 Crystallographic Orientation 80
4.8 Thickness Measurements 81
4.9 Secondary Ion Mass Spectroscopy 81
4.10 References for Chapter 4 83

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5 Doping Studies of CdTe:As on Sapphire Substrates 85

5.1 Introduction 85
5.2 Description of the Samples Used in this Study 86
5.3 General Effects of Growth Temperature 89
5.3.1 On Electrical Properties 89
5.3.2 On Crystal Structure 90
5.4 Effect of VI/II Ratio and Dopant Incorporation on the Properties of Layers Grown at 400°C 91
5.5 Structural Analysis 96
5.6 Discussion 99
5.7 Conclusion 102
5.8 References for Chapter 5 104

---

6 Influence of the Post-Growth Treatment on the Absorber Layer Microstructure 107

6.1 Introduction 107
6.2 Description of the Samples Used in this Study 108

6.3 Results for As-Grown Material 109
6.4 Heat Treated Samples (No $CdCl_2$) 114
6.5 $CdCl_2$ Treated Samples 119
6.5.1 Effect on Crystal Structure 119
6.5.2 Effect on Crystallite Size 123
6.6 Discussion 125
6.7 Conclusion 129
6.8 References for Chapter 6 131

7 Characterisation of $CdCl_2$-Treated Solar Cell Devices 134
7.1 Introduction 134
7.2 Description of the Samples Used in this Study 135
7.2.1 The Samples 135
7.2.2 Post-Growth Treatment and Parameters 137
7.3 Performance of Cells with ~2 and ~8 μm Thick CdTe Absorber 137
7.4 Results for Cells with ~4 μm Thick CdTe Absorber 142
7.4.1 Influence of $CdCl_2$ Thickness 142
7.4.2 Influence of Annealing Temperature 143
7.4.3 Influence of Annealing Time 145
7.4.4 Limiting Factors for Higher Efficiencies 146
7.5 EBIC Measurements (Cells with ~4 μm CdTe) 156
7.5.1 Front-Wall EBIC 156
7.5.2 Variation of Back-Wall EBIC Signal with Beam Voltage 157
7.5.2.1 Theory and Experimental Procedure 158
7.5.2.2 Monte Carlo Simulation of Carrier Generation 158
7.5.2.3 Experimental Results 160
7.6 Influence of CdS Thickness and the ITO Substrate Type 164
7.7 Discussion 166
7.8 Conclusion 169
7.9 References for Chapter 7 171

8 AC Impedance Measurements 174

8.1 Introduction 174
8.2 Theoretical Approach 175
8.3 Experimental Details 178
8.4 Thermal Admittance Results 179
8.5 Conclusion 185
8.6 References for Chapter 8 186

9 Conclusions 188

9.1 Summary of Conclusions 188
9.2 Suggestions for Future Work 192

LIST OF SYMBOLS

a	Lattice parameter	Å
A	Diode quality factor	-
α	Absorption coefficient	cm^{-1}
C	Capacitance	F
C_{hkl}	Texture coefficient	-
d_{hkl}	Interatomic distance	Å
d	Thickness	m
E_b	Electron beam energy	keV
E_C	Energy of bottom of conduction band	eV
E_F	Fermi level energy	eV
E_g	Energy bandgap	eV
E_i	Ionisation energy	eV
E_t	Defect characteristic energy	eV
E_V	Energy of top of valence band	eV
D_n, D_p	Electron and hole diffusion coefficients	$cm^2.s^{-1}$
$F(z)$	Collection probability	-
FF	Fill Factor	%
G	Conductance	S
$g(E_b,z)$	Generation function for minority carrier	m^{-1}
h	Planck's constant	J.s
h, k, l	Miller's indices	-
I_c	Electron beam current	A
J	Current density	$mA.cm^{-2}$
J_0	Saturation current density	$mA.cm^{-2}$
J_L	Light generated current density	$mA.cm^{-2}$
J_{mp}	Maximum power current density	$mA.cm^{-2}$
J_{sc}	Short circuit current density	$mA.cm^{-2}$
k	Boltzmann's constant	$J.K^{-1}$

L_n, L_p	Electron and hole diffusion lengths	cm
n	Refractive index	-
n	Number of reflection	-
n	Grain growth exponent	-
n, p	Electron and hole densities	cm^{-3}
n_p, p_n	Minority carrier densities	cm^{-3}
n_{p_0}, p_{n_0}	Equilibrium carrier densities	cm^{-3}
N_V	Valence band density of states	cm^{-3}
N_t	Defect density of states	cm^{-3}
P_{in}	Incident illumination intensity	$W.m^{-2}$
q	Electronic charge	C
r	Grain radius	µm
R_A, R_B	Van der Pauw characteristic resistances	Ω
R_s	Series resistance	$\Omega.cm^{-2}$
R_s	Sheet resistance	Ω.□
R_{sh}	Shunt resistance	$\Omega.cm^{-2}$
S_{xy}	Component of compliance	$dyn.cm^{-2}$
t	Time	s
T	Temperature	K
V	Voltage	V
V_{oc}	Open circuit voltage	V
V_{bi}	Built-in voltage	V
V_{mp}	Maximum power voltage	V
z	Depth	µm
x_d	Depletion width	cm
β_p	Hole capture coefficient	$cm^3.s^{-1}$
ε	Strain	-
η	Efficiency	%
λ	Wavelength	nm
μ_n, μ_p	Electron and hole motilities	$cm^2.V^{-1}.s^{-1}$
ν	Frequency	Hz

ρ	Resistivity	Ω.cm
σ	Degree of preferred orientation	-
σ_i	Conductivity	$S.cm^{-1}$
σ_p	Hole capture cross section	cm^2
σ_s	In-plane stress	$dyn.cm^{-2}$
υ_0	Attempt-to-escape frequency	s^{-1}
υ_{th}	Thermal velocity	$cm.s^{-1}$
ω	Angular frequency	s^{-1}
ω_t	Defect characteristic frequency	s^{-1}
$\Sigma(E_b)$	Charge collection efficiency	-
ϕ_B	Barrier height	eV
ϕ_m, ϕ_s	Work function of metal, semiconductor	eV
χ_s	Electron affinity	eV

Chapter 1

Introduction

Global energy consumption has increased at a rate of around 2% each year, doubling, on average, every 30 to 40 years [1]. Today world energy consumption is highly dependent on fossil fuel-based sources, i.e. oil, natural gas and coal, these sources accounting for over 80% of the global market [2]. The remainder is provided predominantly from nuclear resources but also from renewable energy, such as hydro-power (Figure 1-1). However, this ever-growing global demand for energy cannot be sustained indefinitely as primary resources are rapidly running out. Projections based on known reserves and predicted consumption extrapolations have been made regarding the different time scales over which, through depletion, each fuel source will become increasingly scarce and therefore their expense will increase considerably. It is estimated that coal production can continue for the next 200 years while resources of natural gas and oil will extinguish in 40 and 60 years, respectively [3].

The environmental impact of the burning of fossil fuels for energy production is also of high considerations and concerns. Green house gases and ozone depleting gases are among the product of such combustion. Long term effects of this include smog build up in urban areas, acid rain deforestation and global climate changes. The latter being considered as a high priority matter for many governmental institutions. Regarding nuclear power, safety, disposal, storage, material handling and reactor

decommissioning are some of the questions that make the future of nuclear energy uncertain.

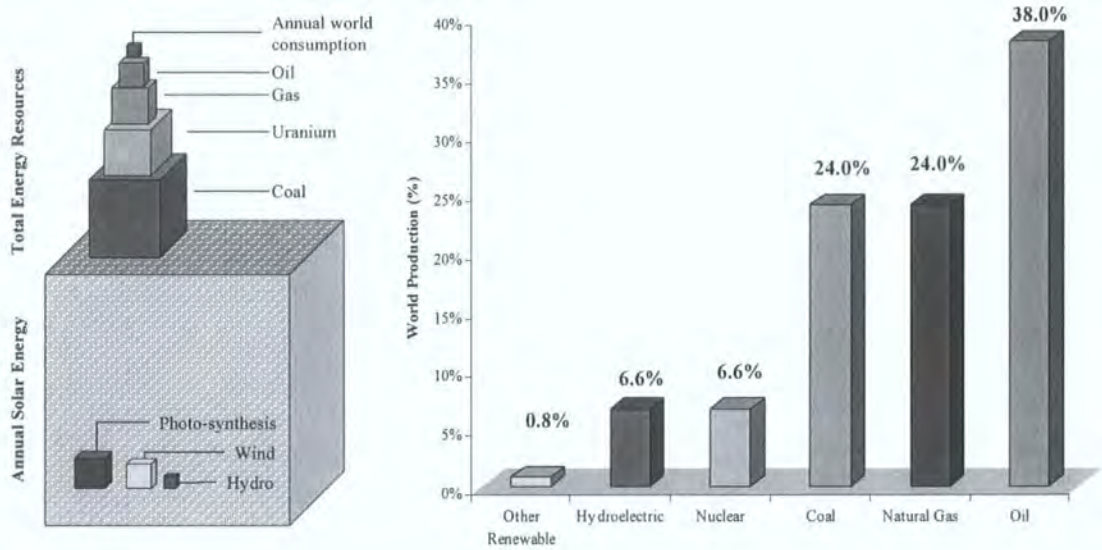

Figure 1-1 Order of magnitude of primary energy resources (left) [3] and world production of primary energy (right) [2].

Since the 1970's a diverse range of technologies have emerged as potential alternatives for renewable energies from natural resources. These include wind, geothermal, tidal wave, hydroelectric and biomass, solar thermal and solar photovoltaic energies. As seen in Figure 1-1, the sun is responsible for most of the earth's exploitable energy, producing the exploitable resources of wind, wave, photosynthesis and hydroelectric power. It is also solar radiation in its immediate form that can be exploited through solar thermal heating and photovoltaic conversion. The latter is the subject of this work.

Photovoltaic (PV) conversion is the direct conversion of the solar energy into electrical power, providing a promising renewable, almost unlimited, affordable and environmentally friendly energy source as well as being economically viable. Among the different photovoltaic materials available, the cadmium telluride – cadmium sulphide solar cell has attracted considerable attention. The use of cadmium telluride (CdTe) as a light absorbing material in solar cells is attractive, because it possesses a nearly optimal bandgap of 1.5 eV for conversion efficiency [4]. The direct band gap of this semiconductor allows considerable light absorption for film thicknesses of

only 2 μm, resulting in low material usage. Moreover, CdTe is a robust material open to a wide variety of deposition techniques.

One of these techniques is metal-organic chemical vapour deposition (MOCVD) and has been used throughout the course of this work to produce the different layers and structures studied. MOCVD is a well established technique for producing optoelectronic devices based on III-V materials [5]. The use of MOCVD for solar cell applications has mainly been limited to the development of GaAs-based devices for space applications. In the case of II-VI materials such as CdTe and CdS, progress on controlling point defects, doping and alloy composition have been slower compared to III-V technology. At a research level, MOCVD is utilised for the growth of CdTe/CdS solar cells in an attempt to improve the quality of the CdTe layer compared to other deposition techniques and hence improving the collecting power of the film. Although the growth conditions can be optimised to produced *p*-type CdTe films with micron sized grains [6], the resulting polycrystalline films are, however, often too resistive for photovoltaic applications arising from the high density of grain boundaries.

The opportunities offered by the MOCVD technique for reproducible high efficiency photovoltaic devices are (i) control in the growth of the CdTe/CdS structures, (ii) doping consistently in all areas of the device and (iii) annealing in a controlled atmosphere during and after growth cycles. Improvement in heterojunction and metal-semiconductor junction formation, maximisation of grain size and controlled passivation of grain boundary provide the major challenges for MOCVD if it is to become a reliable and cost-effective technique for the production of thin film solar cells.

Initially this thesis discusses the principles and fundamentals of solar cell devices and also the diverse structures and materials used (Chapter 2). Following this, Chapter 3 will focus on the CdTe/CdS polycrystalline thin film solar cell by reviewing the technologies and properties of the materials and also the effects of processing. Then the range of experimental techniques used through the course of this work is described in details in Chapter 4. The experimental results are then described and analysed in the following chapters:

(i) In Chapter 5, the structural and electrical properties of arsenic doped thin film CdTe are investigated in order to assess the influence of the dopant incorporation.

(ii) In Chapter 6, the microstructure of the absorber layer of CdTe/CdS bi-layers is studied with regards to the post-deposition treatment of the structures.

(iii) The processing and characterisation of solar cell structures are then detailed in Chapter 7 by means of current-voltage characteristics and microscopy techniques.

(iv) Finally, the junction properties of two devices with thin and thick CdTe are analysed by means of impedance spectroscopy in order to assess the particular differences between the two junctions (Chapter 8).

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Chapter 2

Fundamentals of Solar Cell Devices

2.1 Introduction

Solar cells are semiconductor devices that convert sunlight directly into electrical energy using the photovoltaic process. Not only is the efficiency of the cell important, but also its ability to perform well over a long period of time under real atmospheric conditions. This chapter presents a review of the features of solar cells, their band structures, their working parameters and the main materials.

2.1.1 Historical Development

Solar cells depend upon the photovoltaic effect for their operation. Becquerel, who observed a light-dependent voltage between electrodes immersed in an electrolyte, reported this effect initially in 1839 [1]. It was also observed in an all-solid-state system in 1876 for the case of selenium [2]. This was followed by the development of photocells based on both this material and cuprous oxide. Although a silicon cell was reported in 1941, it was not until 1954 [3] that the forerunner of present silicon cells was announced. This device represented a major development because it was the first photovoltaic structure that converted light to electricity with reasonable efficiency. These cells found application as power sources in spacecrafts

as early as 1958. By the early 1960's, the design of cells for space use had stabilized and over the next decade this was their major application.

The early 1970's saw an innovative period in silicon cell development with marked increases in realisable energy conversion efficiencies. At about the same time, there was a reawakening of interest in terrestrial use of these devices. By the end of the 1970's, the volume of cells produced for terrestrial use had completely outstripped that for space use. This increase in production volume was accompanied by a significant reduction in solar cell costs. The early 1980's saw newer device technologies being evaluated at the pilot production stage, poised to enable further reduction in costs over the coming decade such as copper indium diselenide and cadmium telluride based devices. Today, attention is concentrated on implementing new devices such as organic solar cells or multijunction cells and also on improving performances of current devices.

2.1.2 The Photovoltaic Effect

The photovoltaic (PV) effect in a semiconductor is the combined result of two processes. The first one is the generation of carriers by interaction of incident photons with the semiconductor. The second process consists of the collection of those generated carriers in order to create an electrical current. Those two stages are now explained.

Carrier generation depends upon the photon energy $h\nu$ and the energy bandgap E_g of the semiconductor. If $h\nu < E_g$ then nothing will happen as the energy provided by the photon is too small to excite an electron from the valence band to the conduction band of the semiconductor. If $E_g \leq h\nu < 2E_g$ an electron-hole pair is created by the promotion of an electron across the bandgap of the semiconductor. In a third case, if $h\nu \geq 2E_g$ the electron promoted across the bandgap gain enough energy so that it can excite electron-holes pairs by the process known as impact ionisation.

Carrier collection is achieved by separating an electron and hole pair through the creation of a built-in electric field. In a solar cell, such a field arises when a semiconductor is put in contact with a metal, i.e. Schottky barrier, or to another semiconductor. In the latter case, the two semiconductors can be of different

compounds (heterojunction) or from the same material but differently doped (homojunction).

In this chapter, the three different solar cell configurations mentioned above are described followed by the derivation of the diode equation for an ideal *p-n* junction and the description of solar cell parameters from the current-voltage *J-V* curve. Finally, losses and limitations affecting cell parameters are introduced followed by a review of the different types of photovoltaic devices and the materials used for them.

2.2 Solar Cell Configurations

2.2.1 Schottky Junction

The potential barrier, which forms when a metal is in contact with a semiconductor, arises from the separation of charges at the metal-semiconductor interface. The energy band diagrams in Figure 2-1 illustrate the process of barrier formation. Figure 2-1 a) shows the electron energy band diagram of a metal having a work function ϕ_m and an *n*-type semiconductor of work function ϕ_s and electron affinity χ_s.

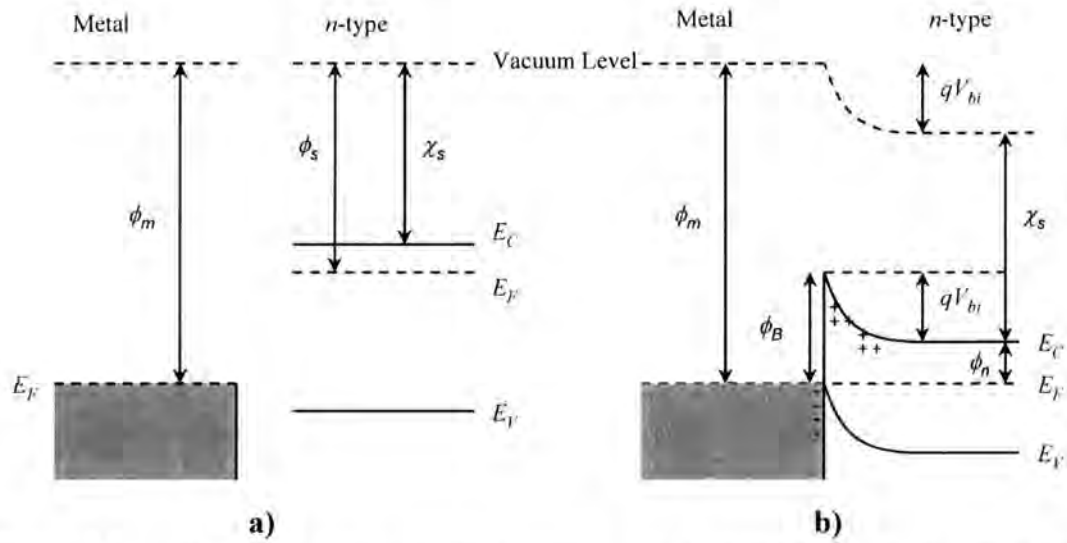

Figure 2-1 Electron energy band diagrams of a metal contact to an *n*-type semiconductor with $\phi_m > \phi_s$. a) Neutral materials separated from each other and b) thermal equilibrium situation after the contact has been made.

Figure 2-1 b) shows the energy band diagram after the contact is made and equilibrium has been reached. When the two materials are brought into intimate contact, electrons from the conduction band of the semiconductor, which have higher energy than the metal electrons, flow into the metal until the Fermi level on the two sides is brought into coincidence. As the electrons move out of the semiconductor into the metal, the free electron concentration in the semiconductor region near the boundary decreases. Since the separation between the conduction band edge E_C and the Fermi level E_F of the semiconductor increases with decreasing electron concentration, the conduction band edge bends up as shown in Figure 2-1 b).

The conduction band electrons which cross over into the metal leave a positive charge of ionised donors behind, so the semiconductor region near the metal gets depleted of mobile electrons. Thus a positive charge is established on the semiconductor side of the interface and the electrons which cross over into the metal form a thin sheet of negative charges. Consequently an electric field is established from the semiconductor to the metal.

The amount of band bending is equal to the difference between the two vacuum levels and is $qV_{bi} = \phi_m - \phi_s$ where V_{bi} is the built-in potential of the junction. qV_{bi} is the potential barrier which an electron, moving from the semiconductor into the metal, has to surmount. However, the barrier looking from the metal towards the semiconductor is different and is given by $\phi_B = \phi_m - \chi_s = qV_{bi} + \phi_n$ where $\phi_n = E_C - E_F$ represents the penetration of the Fermi level in the bandgap of the semiconductor.

2.2.2 Homojunction

We now consider the case of a formation of a barrier between two semiconductors of the same material, doped differently to ensure they have opposite conductivity. The energy band diagram of the isolated pieces of semiconductor is shown in Figure 2-2 a). When contacted together, the Fermi level of the two semiconductors are brought into coincidence at the equilibrium condition so some electrons have migrated from the *n*-type into the *p*-type and a dipole layer of charge exists near the contact surface creating a barrier. This is shown in Figure 2-2 b).

Again the amount of band bending is equal to the difference between the two vacuum levels, $qV_{bi} = \phi_p - \phi_n$.

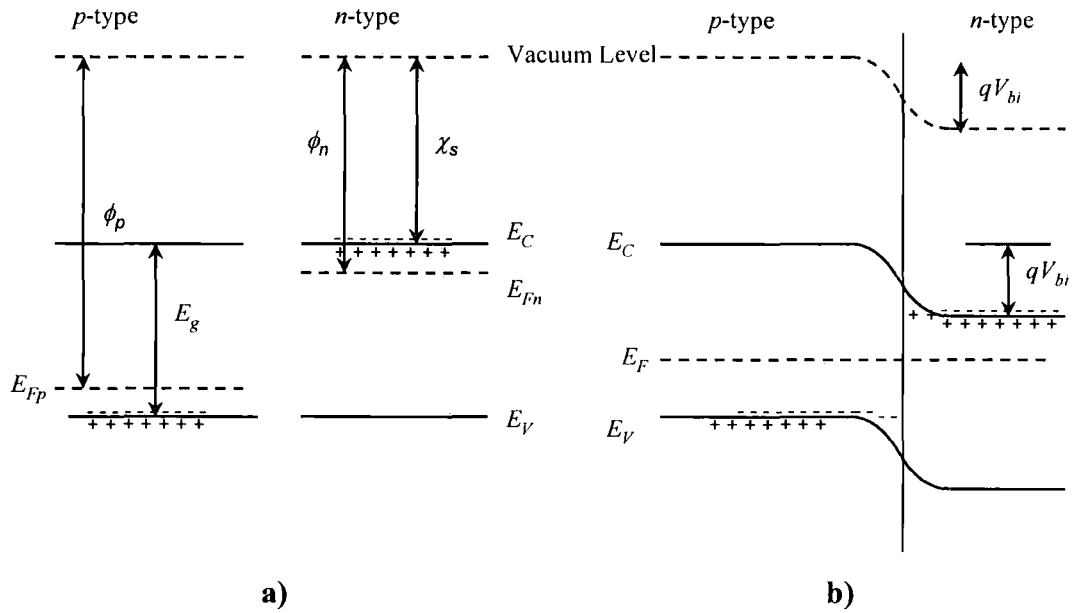

Figure 2-2 Electron energy band diagram of a homojunction: a) Neutral materials separated from each other and b) thermal equilibrium situation after the contact has been made.

2.2.3 Heterojunction

A heterojunction is a junction formed between semiconductors having different energy bandgaps. The energy band model of the two isolated semiconductors is shown in Figure 2-3 a). When the junction is formed between these semiconductors, the energy band profile at equilibrium is shown in Figure 2-3 b) and based upon the Anderson model [4].

The differences in energy bandgap and electron affinity require discontinuities in the conduction band and valence band, ΔE_C and ΔE_V that can be seen on the diagram. These discontinuities act as barriers to the flow of electrons and limit the performance of the solar cell.

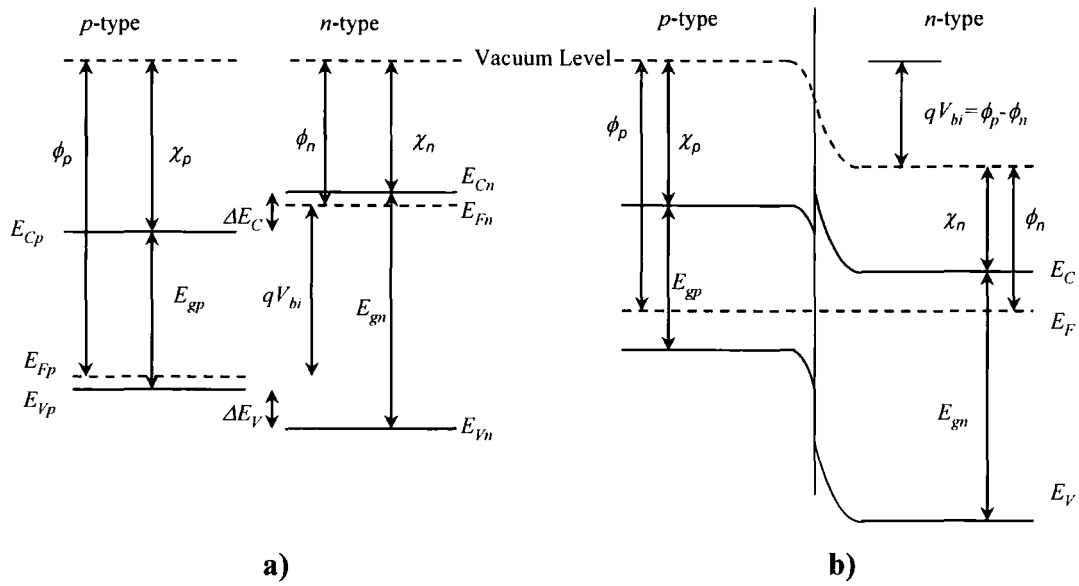

Figure 2-3 Electron energy band diagram of a heterojunction. a) Neutral materials separated from each other and b) thermal equilibrium situation after the contact has been made.

The heterojunction structure is the configuration that concerns the CdTe/CdS structures used in this work. The wide bandgap CdS material is referred to as the window layer and the narrow bandgap CdTe semiconductor as the absorber or active layer. Although the homojunction offers no possibility of discontinuities in the band diagram at the interface, a working constraint of homojunction is that the active junction must be located near the surface in order to avoid strong absorption loss in the layer which receives the light. This can significantly reduce the generated current due to surface recombination in absorbers with high absorption coefficients. However, some of the most efficient cells to date use this type of junction. Indeed, silicon homojunction are eminently practical in contrast to those made from compound semiconductors for which the absorption coefficients are higher. The Schottky junction is also of concern in this work: one of the inherent difficulties in device processing is the inability, due to the high work function of CdTe (5.8 eV), to prepare ohmic contacts to *p*-CdTe. If the metallization layer has a smaller work function, a Schottky barrier will form when the two materials are contacted.

2.3 Diode Physics and Cell Parameters

2.3.1 The Diode Equation

The current voltage characteristic for an ideal *p-n* junction was first derived by Shockley in 1949 [5]. The derivation assumed that the doped regions are uniformly doped and that the transition between the two regions is abrupt. It also assumed low level injection, i.e. the injected minority carrier densities are small compared to the majority carrier densities. A diagram of the junction is presented in Figure 2-4.

The minority carrier densities at the edges of the depletion width x_d are defined for the holes as:

$$p_n(x = x_n) = p_{n_0} \exp\left(\frac{qV}{kT}\right) \tag{2-1}$$

and for the electrons

$$n_p(x = -x_p) = n_{p_0} \exp\left(\frac{qV}{kT}\right) \tag{2-2}$$

where V is the applied voltage, T the temperature, k the Boltzman constant, q the electronic charge, p_{n_0} and n_{p_0} are the equilibrium hole and electron density respectively on the *n*-side and *p*-side.

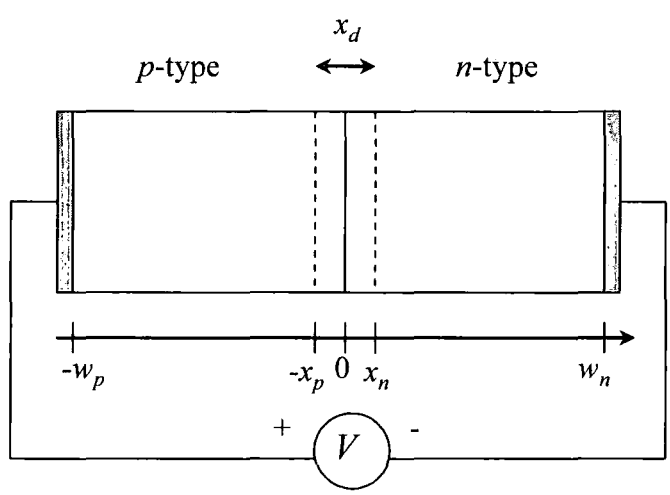

Figure 2-4 Diagram of a *p-n* junction cross section.

The carrier density at the metal contacts is assumed to be equal to the thermal equilibrium carrier density. This assumption implies that excess carriers immediately recombine when reaching either of the two metal-semiconductor contacts. This results in the following set of boundary conditions:

$$p_n(x = w_n) = p_{n_0} \tag{2-3}$$

and

$$n_p(x = -w_p) = n_{p_0} \tag{2-4}$$

The general expression for the ideal diode current is obtained by applying the boundary conditions to the general solution of the diffusion equation for each of the quasi neutral regions:

$$p_n(x \geq x_n) = p_{n_0} + A\exp\left(-\frac{x - x_n}{L_p}\right) + B\exp\left(\frac{x - x_n}{L_p}\right) \tag{2-5}$$

$$n_p(x \leq -x_p) = n_{p_0} + C\exp\left(-\frac{x + x_p}{L_n}\right) + D\exp\left(\frac{x + x_n}{L_n}\right) \tag{2-6}$$

where L_n and L_p are the diffusion lengths of electrons and holes, respectively and A, B, C and D are constants.

Applying the boundary conditions after rearranging equations 2-5 and 2-6 into hyperbolic terms and assuming $\frac{1}{\tanh x} \cong \frac{1}{x}$ for $x << 1$ yields:

$$p_n(x \geq x_n) = p_{n_0} + p_{n_0}\left(\exp\left(\frac{qV}{kT}\right) - 1\right)\exp\frac{-(x - x_n)}{L_p} \tag{2-7}$$

$$n_p(x \leq -x_p) = n_{p_0} + n_{p_0}\left(\exp\left(\frac{qV}{kT}\right) - 1\right)\exp\frac{x + x_p}{L_n} \tag{2-8}$$

The current density in each region is obtained by calculating the diffusion current density [6]:

$$J_p(x \geq x_n) = qD_p\frac{\delta p_n}{\delta x}$$

$$= \frac{qD_p p_{n_0}}{L_p}\left(\exp\left(\frac{qV}{kT}\right) - 1\right)\exp\frac{-(x - x_n)}{L_p} \tag{2-9}$$

and

$$J_n(x \le -x_p) = qD_n \frac{\delta n_p}{\delta x}$$

$$= \frac{qD_n n_{p_0}}{L_n}\left(\exp\left(\frac{qV}{kT}\right)-1\right)\exp\frac{x+x_p}{L_n} \tag{2-10}$$

where D_n and D_p are the diffusion coefficients for electrons and holes, respectively.

The total current must be constant throughout the structure since a steady state case is assumed. No charge can accumulate or disappear somewhere in the structure so that the charge flow must be constant throughout the diode. The total current then equals the sum of the maximum electron current in the *p*-type region and the maximum hole current in the *n*-type region. The maximum currents in the quasi-neutral regions occur at either side of the depletion region and can therefore be calculated from equations 2-9 and 2-10. The total current is then given by:

$$J = J_n + J_p = J_0\left(\exp\left(\frac{qV}{kT}\right)-1\right) \tag{2-11}$$

where $$J_0 = \frac{qD_n n_{p_0}}{L_n} + \frac{qD_p p_{n_0}}{L_p} \tag{2-12}$$

Equation 2-11 is the diode equation for an ideal *p-n* junction with J_0 the saturation current density.

2.3.2 Current-Voltage Characteristic and Cell Parameters

The diode equation for an ideal homojunction was previously derived in the dark (equation 2-11). Under illumination the dark current-voltage (*J-V*) characteristic is translated downward by the magnitude of the light generated current density J_L without change in shape (equation 2-13). These ideal characteristics for a solar cell operating in the dark and under illumination are shown in Figure 2-5.

$$J = J_0\left(\exp\left(\frac{qV}{AkT}\right)-1\right) - J_L \tag{2-13}$$

where J_0 is the reverse saturation current density, J_L the light generated current density and A the diode quality factor. For an ideal junction, the diode factor is equal to 1 and in real devices it is almost always between one and two.

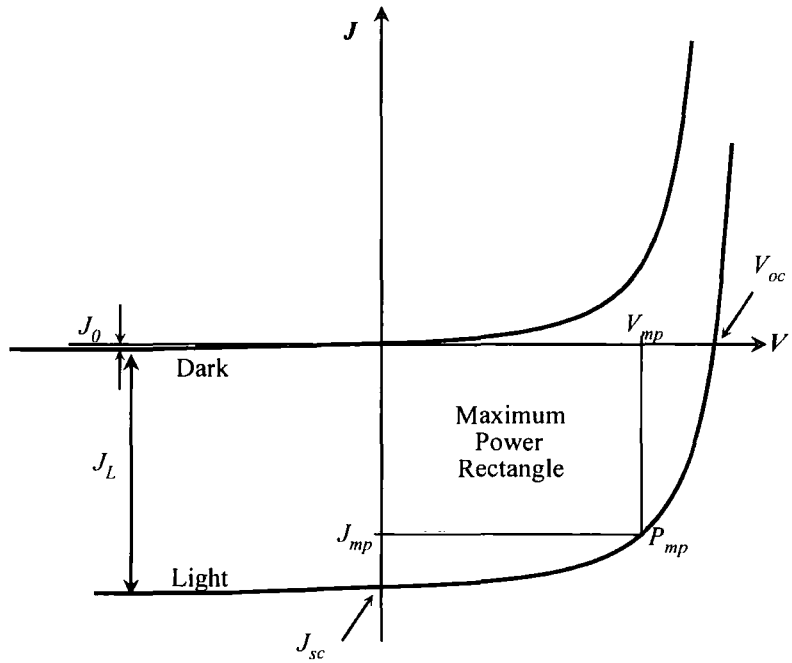

Figure 2-5 Typical current-voltage (J-V) curves for a solar cell operating in the dark and under illumination. The important points are marked on the plot and are explained in the text.

From the light J-V characteristic, the primary parameters of the solar cell under investigation may be extracted. These are open circuit voltage V_{oc}, short circuit current density J_{sc}, efficiency η and fill factor FF, and are defined as:

Open circuit voltage The open circuit voltage V_{oc} is defined as the applied voltage at which no current is flowing through the junction. For an ideal cell the open circuit voltage value is obtained by setting the total current to zero and has a value of:

$$V_{oc} = \frac{AkT}{q} \ln\left(\frac{J_L}{J_0} + 1\right) \tag{2-14}$$

Short circuit current The short circuit current density J_{sc} is the current density measured when no bias is applied to the device and in an ideal case it is equal to the light generated current density J_L.

Fill Factor The fill factor is given by:

$$FF = \frac{J_{mp} \times V_{mp}}{J_{sc} \times V_{oc}} \tag{2-15}$$

where J_{mp} and V_{mp} are the current density and voltage describing the maximum output power P_{mp} of the cell and is computed from the area of the rectangle indicated in the fourth quadrant of the *J-V* curve. The fill factor is a measure of the "squareness" of the *J-V* curve in forward bias.

Efficiency The efficiency gives the power conversion of the device and is defined as the ratio of the maximum power over the incident illumination intensity P_{in}:

$$\eta = \frac{J_{mp} \times V_{mp}}{P_{in}} \tag{2-16}$$

Typical values for a 16.5% efficient CdTe/CdS cell are: V_{oc} = 850 mV, J_{sc} = 25 mA/cm^2 and FF = 75% [7].

Although these four parameters have been used throughout this work, in the case of real devices, the diode equation must be modified to take into account the resistance losses due to the different layers. Two resistances are introduced, the series resistance R_s and the shunt resistance R_{sh}. The series resistance arises from the resistance of the different layers of the device, and hence limits the total output current available. The shunt or parallel resistance is attributed to short circuit paths through the device. The ideal single diode equation can be modified to describe real devices:

$$J = J_0\left[\exp\left(\frac{q(V - JR_s)}{AkT}\right) - 1\right] + \frac{V - JR_s}{R_{sh}} - J_L \tag{2-17}$$

The equivalent circuit is shown in Figure 2-6. It consists of a current source in parallel with a non-ideal diode, i.e. with a diode quality factor $\neq 1$. In addition are included a shunt resistor to model the current flowing through pin-holes in the window layer and a resistor in series to take into account the resistance of the films.

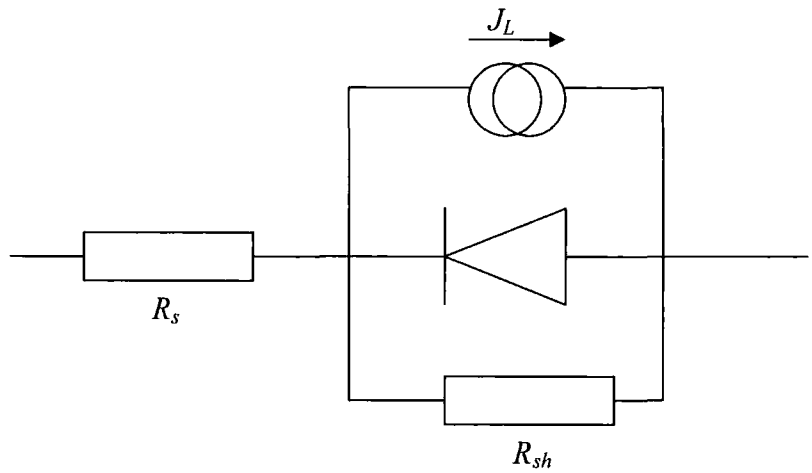

Figure 2-6 Equivalent single diode circuit for a real solar cell.

2.3.3 Efficiency Limits and Losses

The major constraints on photovoltaic efficiency come from the poor match between the broad spectral distribution of the sunlight and the single bandgap E_g of a given semiconductor. The bandgap of a photoactive semiconductor determines the upper bound of both the open circuit voltage V_{oc} and short circuit current density J_{sc}. A narrow bandgap cell such as a silicon based device has a larger V_{oc} than a wider bandgap cell, e.g. CdTe device, but it absorbs fewer photons so it has a smaller J_{sc}. The theoretical limit for a single junction cell is a power conversion efficiency of ~30% for a bandgap of ~1.4 eV [8].

As mentioned earlier for the case of real devices, power losses are also due to the presence of series and shunt resistances. Series resistance arises both from the resistance of the semiconductor bulk and from the contact resistance to the semiconductor to complete the circuit. Shunt resistance arises from imperfections on the devices surface or in the bulk as well as leakage currents across the edge of the cell. The experimental determination of series and shunt resistance from the *J-V* curve is explained in Chapter 7. In this section, origins of losses are considered with regard to the main parameters of the cells, J_{sc}, V_{oc} and *FF*.

2.3.3.1 Short Circuit Current

Under ideal conditions, each incident photon of greater energy than the bandgap gives rise to one electron flowing in the external circuit. Hence, to calculate the maximum short circuit current, the photon flux of the sunlight must be known. This can be calculated from the energy distribution of the sunlight by dividing the energy content at a given wavelength by the energy of an individual photon. The maximum J_{sc} is then found by integrating these distributions from low wavelengths up to the maximum wavelength for which electron hole pairs can be generated for a given semiconductor. Types of optical losses can be described as follows:

(i) Reflection losses at the front surface of the glass substrate in superstrate configuration cell. Reflection losses also occur at the interfaces between the different layers constituting the cell [9]. To reduce this, an anti-reflective coating such as MgF_2 is used in some applications [10-12].

(ii) Absorption losses occur in the glass substrate, front contact and window layer. The substrate and the front contact can account for a loss of 5-10% of the incoming sunlight [13].

(iii) If the cell is not thick enough, some of the light will pass right through before being absorbed. This problem is not significant for direct bandgap materials like CdTe as it has a large absorption coefficient, $\sim 10^5$ cm^{-1} [14, 15].

(iv) In the case of large area modules, a conductive grid is used to retrieve the current at the front contact, grid that can cover 5 to 15% [13] of the structure area generating considerable optical losses.

Because of the wavelength dependence of the absorption coefficient, it is expected that the shorter wavelength photons will be absorbed close to the surface, while those with longer wavelengths are absorbed deeper in the bulk. Surface recombination will therefore be more important for short wavelengths while recombination in the quasi-neutral region is more important for long wavelengths. Short circuit current losses can also occur due to the recombination at the surfaces and/or in the bulk of semiconductor materials. Only electron-hole pairs generated in the depletion region of the *p-n* junction contribute towards J_{sc}.

2.3.3.2 Open Circuit Voltage

The ideal open circuit voltage value (equation 2-14) can be simplified for $J_L/J_0 >> 1$ as:

$$V_{oc} = \frac{AkT}{q}\ln\left(\frac{J_L}{J_0}+1\right) \approx \frac{AkT}{q}\ln\left(\frac{J_L}{J_0}\right) \tag{2-18}$$

For a good cell performance, V_{oc} and hence J_L must be as large as possible. The maximum value of J_L would be obtained if all photo-generated electron hole pairs are collected as photocurrent. J_L can achieve 80-90% of this limit if light absorption and minority carrier collection are both highly efficient [16]. The limiting value of V_{oc} is the built-in voltage barrier qV_{bi} and usually V_{oc} is no more than $0.7 \times qV_{bi}$. Inspection of equation 2-18 shows that V_{oc} increases as the saturation current J_0 decreases. Interestingly, J_0 has no absolute minimum value. In thin film solar cells with well passivated surfaces, J_0 can be reduced to zero and V_{oc} increased to its upper limit of qV_{bi}. In thicker cells where volume recombination occurs, the lower limit on J_0 is determined by the rate of radiative recombination of minority carriers. Usually non-radiative recombination also occurs and this raises J_0 by some orders of magnitude and lowers V_{oc} accordingly.

2.3.3.3 Fill Factor

The fill factor is strongly affected by series and shunt resistances due to their influence on J_{sc} and V_{oc}. Series resistance in high efficiency polycrystalline cells is usually small ($R_s < 1\ \Omega$.cm) and probably dominated by the TCO layer [4].

The fill factor is also influenced by the voltage dependence of the light generated current. This can be easily observed on the *J-V* curve, by the fact that the dark and light curves cannot be superimposed. At reverse and small forward bias the light generated current decreases with increasing voltage hence reducing the fill factor value.

2.4 Types of Solar Cells

The first solar cell was developed at Bell laboratories in 1954 [3]. At that time, solar cells were made from semiconductor grade single crystalline silicon and were used as power source for space applications such like on satellites. The systems were very reliable, and the cost was of little concern with regard to huge space program budgets. At present, solar cells can be single junction devices or multijunction structures and new technologies are employed for making solar cells. Nanotechnology have helped producing a 8.2% efficient nanocrystalline dye-sensitized solar cell [17] while organic cells with 3-4% efficiencies have been reported [18]. However, most efficient devices have been produced using inorganic materials and the technology of these solar cells is outlined next.

2.4.1 Single Crystal and Polycrystalline Silicon

Silicon is still the most popular solar cell material for commercial application because it is so readily abundant (it is actually the second most abundant element in the earth's crust second only to oxygen [19]). Another reason why silicon is a popular choice for photovoltaic energy generation is the large technology base that has built up over the past 50 years for silicon used in the semiconductor industry [19]. The source material for extraction of silicon is silicon dioxide, the major constituent of sand. Single crystalline and polycrystalline silicon have an indirect bandgap of 1.1 eV and low absorption coefficient (1.1×10^3 cm^{-1} at 1.63 eV [4]). This means that over a large range of the visible spectrum, light absorption occurs only with the assistance of phonons. Phonons provide the additional wave vector needed for momentum conservation in any energy transition in an indirect bandgap semiconductor.

Single crystal silicon devices have attained an efficiency of 24.4% [20] on the laboratory scale. Commercial crystalline silicon solar cell modules are available with conversion efficiencies as high as 22.7% [21]. The major disadvantages of single crystal silicon solar cells are the requirements of high grade material and the problems associated with producing single crystals over large areas. Recently, there have been some imaginative attempts to make single crystal ribbon silicon, which is

lower in cost than high quality single crystals and today, accounts for 10% of the world PV total [22, 23].

The production of polycrystalline silicon cells is more cost effective than single crystal silicon. Silicon is poured into blocks that are subsequently sawn into plates. During solidification of the material, crystal structures of varying sizes are formed. Polycrystalline silicon has the disadvantage that large grain sizes are required to reduce the negative influence caused by grain boundaries. In polycrystalline silicon the smaller crystals or "grains" introduce boundaries that impede the flow of electrons and encourage them to recombine with holes, thereby reducing the output power of the cell. However, polycrystalline silicon is much cheaper to produce than single crystal silicon, hence researchers are working on new innovative ways of minimizing the effects of grain boundaries.

2.4.2 Group III-V Technologies

Photovoltaic technologies based on group III and V elements in the periodic table show very high efficiencies under either normal or concentrated sunlight. Although expensive, their cost can be compensated for by using concentrators, which increase the energy conversion efficiency under higher illumination [24, 25]. Concentrators focus light from a large area to a small area, thereby increasing illumination to many times the terrestrial sunlight. The most important solar cells in this category are gallium arsenide (GaAs) and indium phosphide (InP).

2.4.2.1 Gallium Arsenide

Gallium arsenide is a compound semiconductor for which the use in solar cells has been developing synergistically with its use in light emitting diodes, lasers, and other optical devices. It has a direct bandgap of 1.43 eV, nearly ideal for single junction solar cells [8]. The absorption coefficient of GaAs is relatively high ($> 10^4$ cm^{-1} for $h\nu > 1.45$ eV [26]) and causes sufficient absorption of photons in only a few microns of material. It is also very resistant to radiation damage. This, along with its high efficiency, makes GaAs very desirable for space applications. The most efficient solar cell to date has been based on this material and cells of 25.1% efficiency have already been confirmed [21]. When used in concentrator application,

the efficiency increases to 27.6% [27]. The greatest barrier to the success of GaAs cells has been the high cost of single crystalline GaAs substrates. For this reason, GaAs cells are used primarily in concentrator system. For mass production of GaAs solar cells, gallium element availability and the toxic nature of the arsenic are considered as major limitations of this technology.

2.4.2.2 Indium Phosphide

Indium phosphide (InP) has a direct bandgap of 1.34 eV, close to the optimum for solar energy conversion [8]. Research on InP heterojunctions did not start until about 1974, probably because of the unavailability of high quality single crystals of *p*-type InP. InP crystals are grown by the Czochraski method at high pressures using the liquid encapsulation technique to preserve the stoichiometry [28]. A 21.9% efficient InP crystalline solar cell was reported 15 years ago [29]. When a 99-sun concentrator is used, the efficiency increases to 24.3% [30]. A 31.8% multijunction InP/GaInAs cell, operating at 50 suns concentration has been achieved [31]. The major limitation of this technology is the high cost due to limited resources for indium and purification of phosphorous.

2.4.3 Thin Film Solar Cell

In an effort to reduce the fabrication costs of the present technology based on silicon, and to increase material utilisation, thin film materials have been the subject of intensive research. Three main types of materials have emerged as the most promising candidates for the next generation of solar cells. These are hydrogenated amorphous silicon (a-Si:H), cadmium telluride (CdTe) and copper indium diselenide ($CuInSe_2$) and its related alloys.

2.4.3.1 Hydrogenated Amorphous Silicon a-Si:H

Amorphous silicon films exhibit very different characteristics than crystalline silicon. The main difference between the two materials is that there is no long-range order in the amorphous film. There is also a large number of dangling bonds in amorphous films that create trap states throughout the bandgap region. In order to remove the dangling bonds, amorphous silicon films are hydrogenated during deposition. This results in the occupation of dangling bonds by hydrogen atoms.

Hydrogenated amorphous silicon (a-Si:H) exhibits a bandgap that is not well defined. Its value may vary from approximately 1.6 to 1.8 eV depending on deposition conditions. For plasma chemical vapour deposited a-Si:H, the variation depends on the deposition conditions including substrate temperature, RF power and gas pressure [32]. This material can be doped either *p*- or *n*-type by introduction, during deposition, of boron or phosphorous, respectively.

Solar cells fabricated from a-Si:H are based on a *p-i-n* structure rather than a *p-n* junction. This is because the doping necessary to generate the field across the junction results in a very high defect density, greatly reducing carrier lifetime. The deposition of an insulating intrinsic layer between thin *p*-type and *n*-type layers circumvents this problem. A nominally 100 nm thick *p*-type layer and a 20-30 nm thick *n*-type layer generate a field across the 100-400 nm intrinsic layer. The intrinsic layer becomes the absorber in this configuration, with the collection of the generated carriers enabled by the externally generated field. Textured surfaces are typically used in this type of device to induce light trapping, thereby effectively increasing the optical path length within the device. This results in an increased probability of collecting each photon and generating an electron-hole pair. A primary problem associated with these devices is a photo-induced increase in defect density resulting in degraded device performance [33]. The effect can be reversed by annealing the device after degradation, but the process repeats when the device is again illuminated. Elimination of this effect is a topic of current research.

2.4.3.2 Copper Indium Diselenide ($CuInSe_2$)

One of the most promising thin film solar cell devices is based on $CuInSe_2$ (CIS) absorber films. Conversion efficiencies of between 12 and 15% have already been achieved for devices based on a $CuInSe_2$/CdS/ZnO heterojunction [34-36]. The bandgap of CIS can be modified continuously over a wide range (i.e. 1.0-1.65 eV) by substituting Ga for In. Similarly, one can also increase the bandgap by the substitution of Se for S.

Recent trends in $CuInSe_2$ research and development focus on these high bandgap chalcopyrite alloys, and preliminary results indicated that conversion efficiencies above 18% can be achieved when using these specific absorber films

[37]. Gallium incorporation is also believed to improve adhesion between the CIS and the molybdenum electrical back contact [38] and also increases the open circuit voltage of the cell. Record efficiency of 19.2% has been demonstrated using this type of devices [39]. Beside basic investigations at various university laboratories, commercialisation of CIS based solar cell technology has already been realised. To compete with silicon solar cells, conversion efficiency above 10% is required on large areas and currently, the best modules can achieve 13.4% efficiency for an active area of 3460 cm^2 [40].

2.4.3.3 Cadmium Telluride (CdTe)

Cadmium telluride was very early seen as one of the best materials for solar cell applications with a theoretical efficiency limit of ~27% [8], CdTe is the nearly ideal material for absorbing the maximum amount of the solar spectrum with minimal losses. CdTe is typically used in conjunction with cadmium sulphide (CdS) for the formation of heterojunctions. The first CdTe/CdS solar cell device was developed by Bonnet and Rabenhorst in the early 1970's and achieved a power conversion of ~5% [41]. Today the best cell reaches an efficiency of 16.5% in laboratories [7] whilst large area modules perform at ~11% [42].

The development of CdTe/CdS cells has been dominated by empirical methodology. For example, the 99.999% purity standard used in industry has not been defined by systematic investigations. Hence doping by residual impurities and the $CdCl_2$ post-growth heat treatment is an optimised if not fully understood process. One feature of the present work is to investigate the feasibility of intentional arsenic doping of CdTe as a new route to controllable CdTe/CdS solar cells.

In order to perform well CdTe solar cells require a post-deposition heat treatment in a $CdCl_2$ environment (see for example [43]). One of the critical issues for CdTe-based devices is the formation of an ohmic back contact, which requires in most case a chemical treatment of the surface [44]. This $CdCl_2$ treatment and back contact formation as well as the CdTe/CdS solar cell as a whole are studied in more depth in the next chapter as it is the type of solar cell concerned in this work.

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Chapter 3

Thin Film CdTe/CdS Solar Cells

3.1 Introduction

The potential of cadmium telluride (CdTe) for use as absorber in a solar cell has long been recognised, as with a bandgap of 1.45 eV it is close to the theoretical ideal that could produce devices up to 27% efficient [1]. Homojunction cells were first investigated to make use of the ability to produce both *p* and *n*-type CdTe, but efficiencies were limited to 6% [2] due to surface recombination arising from the strong absorption coefficient of the CdTe and the collecting junction being located near the surface. The first efficient polycrystalline thin film CdTe-based solar cells was *p*-Cu_2Te/*n*-CdTe heterojunction and demonstrated a conversion efficiency of 6% [3]. However, due to instabilities associated with the Cu_2Te layer, alternative *p*-type window layers were sought. Ultimately, this proved unsuccessful and consequently attention turned to device structures employing *p*-CdTe.

As a result, a *p*-CdTe/*n*-CdS heterojunction solar cell with 1% efficiency was fabricated in 1969 by evaporating CdS then CdTe films on a glass substrate coated with a transparent conductive oxide (TCO) [4]. This type of configuration is referred to as "superstrate" configuration and is shown in Figure 3-1. In 1972 an all thin film CdTe/CdS solar cell was reported by Bonnet and Rabenhorst [5] by evaporation of a

CdS layer over a CdTe absorber film, in "substrate" configuration. This device demonstrated an efficiency of 5% under 50 $mW.cm^{-2}$ illumination. In both "substrate" and "superstrate" configurations, light enters through the TCO and CdS films. In a superstrate cell, the TCO, CdS and CdTe layers are sequentially deposited onto a glass substrate. However, in a substrate configuration the CdTe film is typically deposited first onto a suitable metal substrate followed by the deposition of CdS and TCO.

In this chapter the functions and properties of each layer that constitutes the CdTe/CdS thin film solar cell are reviewed. In section 3.3, some of the growth techniques are described with particular emphasis on chemical vapour deposition, the deposition method used for the fabrication of the layers and devices investigated in this work. Then, the effects of the $CdCl_2$ post-growth treatment are detailed (section 3.4), followed by a review of defect chemistry in CdTe.

3.2 Solar Cell Structure

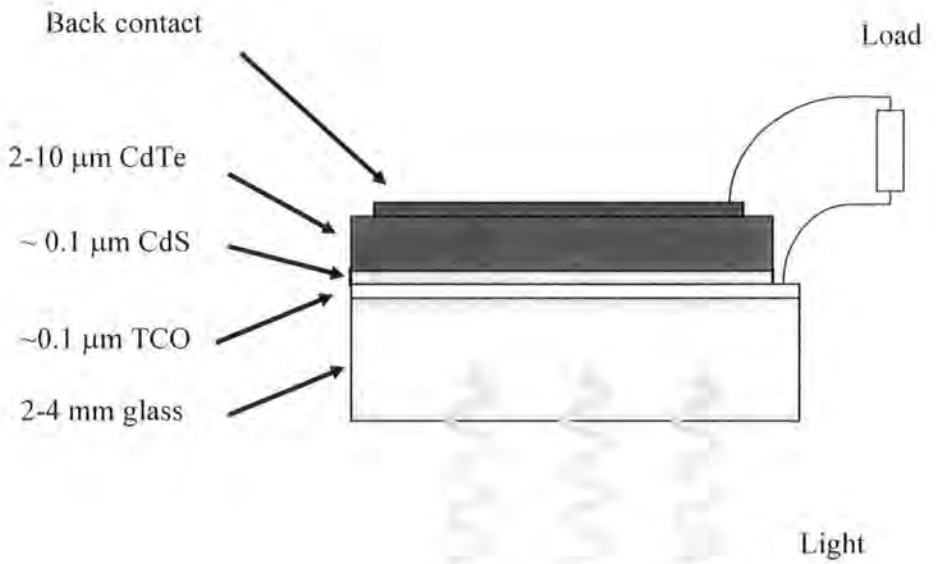

Figure 3-1 Basic structure of a typical CdTe/CdS solar cell in superstrate configuration.

3.2.1 The substrate

The choice of an appropriate substrate is very important. It should withstand the cell fabrication process temperature and must not contaminate the layers that are subsequently grown. CdTe/CdS solar cells in superstrate configuration require a transparent substrate because incident light has to pass through it before reaching the CdS and the CdTe layers, any absorption in the substrate would be detrimental to the current generation in the cell. The general choice is glass because it is transparent, cheap and withstands relatively high temperature. Common types of glass used include soda-lime glass which is inexpensive and borosilicate glass. The latter has a higher softening temperature, and for this reason it is often used for the higher temperature deposition methods, but since it is ten times more expensive, soda-lime glass is generally preferred for low-cost production. However, it should be mentioned that cells fabricated on low ion or borosilicate glass are ~3% more efficient than those made on soda-lime glass. Presumably this is due to a reduced contamination of the layers. The substrate is usually 2-4 mm thick, with sometimes an anti-reflection coating such as MgF_2 on its surface to minimise reflection losses.

3.2.2 The Front Contact

The front contact must be transparent and highly conducting. In general transparent conductive oxides (TCO) are used as front contact. For high efficiency cells, it is required that the sheet resistance of the front contact is no more than 10 Ω/□. The most widely used material is tin oxide (SnO_2) usually 100 nm thick, deposited by sputtering or atmospheric pressure chemical vapour deposition. Since tin oxide has a low conductivity, it is often doped with indium, forming indium tin oxide (ITO), or sometimes with fluorine (FTO). The choice between ITO and SnO_2 is primarily determined by the deposition temperature of CdS and CdTe films [6]. For low temperature deposition processes, ITO is the material of choice, because it has a high optical transmission for a given sheet resistance. For higher temperature deposition, SnO_2 is the material preferred since it is more stable. However, to avoid diffusion of indium from the ITO used in high temperature deposition techniques, a layer of undoped SnO_2 is often included between the ITO and CdS layers. Recently, the use of cadmium stannate (Cd_2SnO_4, CTO) as front contact has shown

improvements in power conversion [7] due to the higher conductivity of CTO compared to ITO and also to a higher transmittance.

3.2.3 The CdS Window Layer

The bandgap of the window layer must be large compared to the absorber layer bandgap to enable a maximum light absorption in CdTe. Also, the window layer should be of relatively high electrical conductivity (i) to ensure that the field region is largely located in the CdTe layer to maximise carrier collection and (ii) to minimise resistance losses in the transport of carriers to the external circuit. The polycrystalline CdS is grown *n*-type and can be deposited by vacuum evaporation (physical vapour deposition) [8], close space sublimation (CSS) [9], chemical bath deposition (CBD) [10], radio frequency (RF) sputtering [11] and MOCVD [12].

As a wide bandgap semiconductor (E_g = 2.42 eV at 300 K), CdS is largely transparent down to a wavelength of around 510 nm. Depending on the thickness of the CdS layer which is usually ~100 nm, some of the light below the 510 nm wavelength can still pass through to the CdTe giving additional current in the device. The reduction of layer thickness is then important to allow greater transmission into the CdTe, but on the other hand the uniform coverage of the TCO and the consumption of CdS into the CdTe layer during annealing treatment require that the thickness is not reduced below a certain limit, otherwise the cell is shunted or gives low voltage [13].

CdS grown by low temperature deposition techniques (e.g. CBD) generally requires an annealing in air or in chlorine ambient to increase grain size and reduce defect density [14]. This treatment has been found to be less influential for layers deposited by methods such as CSS, spray pyrolysis and screen printing where temperature, in excess of 500°C are used during the deposition.

3.2.4 The CdTe Absorber Layer

CdTe is, in principal, an ideal thin film photovoltaic absorber material as ~99% of the solar radiation is absorbed within a thickness of 2 μm. The polycrystalline CdTe layer should be *p*-type to form the *p-n* junction with the *n*-CdS layer. Since CdTe has a lower carrier concentration than the CdS layer, the depletion

region is mostly located within the CdTe layer and in this region most of the carrier generation and collection occur.

The conductivity and grain size of the layer depend on the deposition technique and post-deposition treatment used. Typically the thickness of this layer is between 2 and 10 μm, with grain size ranging from 0.5 to 5 μm. As-deposited, the CdTe layer is either *n*-type or highly resistive *p*-type. However, a suitable heat treatment in chlorine or oxygen ambient can convert the layer to *p*-type and also increase its conductivity. This will be further detailed in section 3.3.

3.2.5 The Back Contact

Producing ohmic contacts on most semiconductors is a difficult problem. With *p*-type material, an ohmic contact is only created when the work function of the conducting layer is larger than that of the semiconductor. When this condition is not satisfied, a Schottky barrier is formed which can reduce device performance. For *p*-type CdTe, forming an ohmic contact is exceptionally hard due to the high work function of CdTe ($\phi_p \sim 5.7$ eV) [15]. This can be seen in Figure 3-2, which shows a band diagram of a metal contact on *p*-type CdTe.

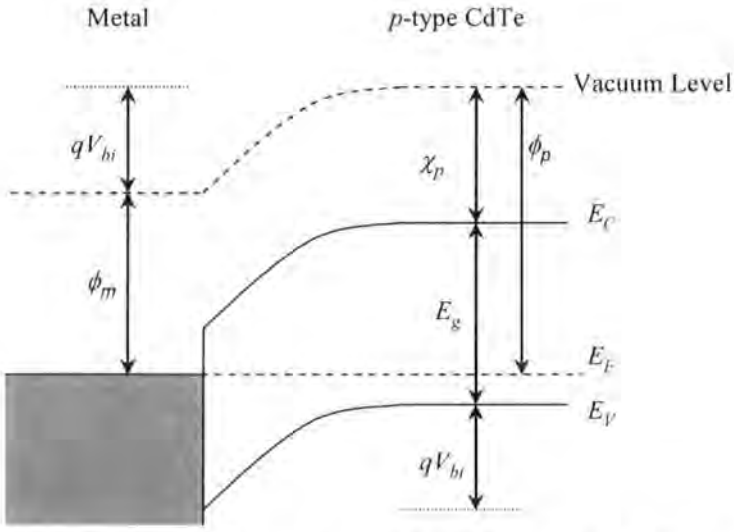

Figure 3-2 Band diagram of a metal/*p*-type CdTe contact at equilibrium.

The Schottky barrier height, defined as the difference of the two work functions $qV_{bi} = \phi_p - \phi_m$, can be reduced by increasing the carrier concentration in the CdTe in the vicinity of the back contact. Numerous chemical recipes are employed with more or less success to make a back contact to CdTe/CdS solar cells. One possibility is to prepare a p^+-type layer which can decrease the work function of the top part of the absorber in order to make a quasi-ohmic contact with the metal. Various chemical etchants may be used and include acidified dichromate [16], bromine methanol [17] and nitric phosphoric acid [18]. The principle of this etching is to leave a tellurium rich layer at the surface of the CdTe by reduction of the tellurium ions, hence creating a more *p*-type layer at the surface of the absorber.

A second technique involves direct doping of the top surface of the absorber using a graphite paste with the required dopant such as Cu_xTe in HgTe. Subsequent annealing allows the dopant to diffuse in the CdTe [19]. Doping can also be performed during growth. Both methods increase the acceptor concentration near the surface and this results in a narrower depletion region when the metal is subsequently applied. This allows the thermally assisted tunnelling of holes through the barrier.

Finally deposition of an intermediate layer of *p*-type semiconductor with a lower work function than CdTe, such as ZnTe [20], HgTe [21] or Sb_2Te_3 [8] can be used sometimes in complement with one of the first two methods.

A different approach, suggested by Irvine *et al.* [22], for contacting CdTe/CdS solar cell would be to make contact to a n^+-CdS layer instead of the usual *p*-CdTe layer by modifying the cell structure to n^+-CdS/p^+-CdTe/*p*-CdTe/*n*-CdS/ITO/glass. Contacting to n^+-CdS would be achieved through the formation of a low resistive tunnel junction between the p^+-CdTe absorber layer and the n^+-CdS window layer. The electron affinity of CdS is ~4.2 eV, hence a number of metals with smaller work function are available for contacting to the n^+-CdS layer: In, Al, W, Ti, Cr and Mo. Part of this work is based on this new approach, with investigation of conductive CdTe layers doped with arsenic to create the p^+ region of the tunnel junction.

3.3 Material Deposition Techniques

Numerous methods have been employed to deposit CdTe and CdS thin films for solar cells. Some of the methods that have demonstrated viability for the commercial manufacture of CdTe/CdS solar cells and modules are reviewed in this section with some aspects of the microstructure of the absorber layer being also described.

3.3.1 Chemical Vapour Deposition

Chemical deposition from the vapour phase is a well developed technique for the growth of epitaxial or polycrystalline material. Since Manasevit's pioneering work [23], chemical vapour deposition (CVD) has been extended so that nearly all III-V and II-VI compounds can be produced using this and other vapour methods. Metal-organic vapour phase epitaxy (MOVPE) is defined as the growth on the surface of a crystal so that the layer grown has the same structure as the underlying substrate. The main advantages of the CVD technique are:

(i) a wide range of thickness can be achieved and controlled;

(ii) the dopant concentration and distribution in the film can also be controlled;

(iii) multilayer structures are obtainable in a single deposition run;

(iv) the technique is scalable to manufacturing.

CVD is a non vacuum technique operating over a broad range of temperature (200-1200°C) from organic precursors in hydrogen carrier gas. The substrates are supported on a graphite susceptor and can be heated radiatively or by coupling a RF generator. The CVD principle involves a series of gas phase and surface reactions, and this is schematically shown in Figure 3-3. The process can be divided into several steps:

(A) Mass transport of reagents in the bulk gas flow region to the deposition zone.

(B) Gas phase reactions in the boundary layer which produce film precursors and by-products.

(C) Mass transport of film precursors through the boundary layer to the surface growth.

(D) Adsorption of film precursors on the growth surface.

(E) Surface diffusion of precursors to growth sites.

(F) Surface chemical reactions leading to film deposition and to by-products, which subsequently desorb.

(G) Mass transport of by-products into the bulk gas flow region and out of the reactor.

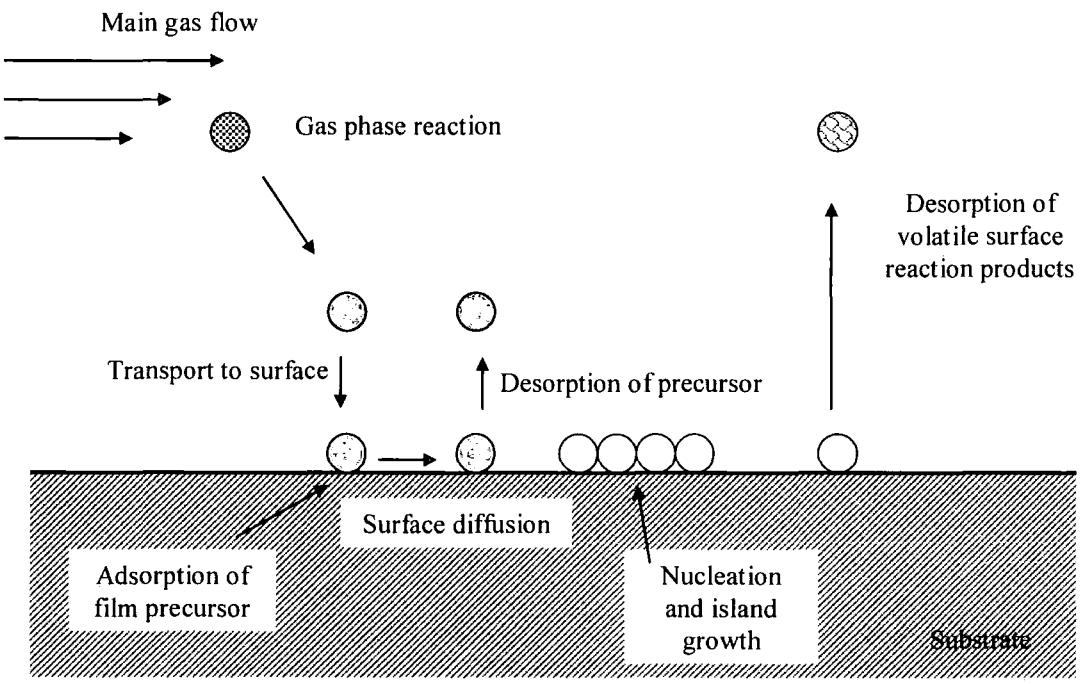

Figure 3-3 Transport and reaction processes in chemical vapour deposition [24].

The choice of organometallics for the growth of II-VI compounds has been one of the issues in the development of MOCVD, to fulfil an increasing demand for lower decomposition temperatures and higher purity. Low growth temperatures are desirable since they reduce solid state inter-diffusional processes, sharpening interfaces and decreasing the possibility of unwanted doping from foreign substrates. Tellurium precursors have always been the limiting factor as temperatures higher than 400°C were required for the decomposition of diethyltelluride, one of the early gases used. With the advent of di-isopropyltelluride (DIPTe) the growth temperature could then be lowered down to 320°C [25]. On the other hand, dimethylcadmium

(DMCd) decomposes at 150°C and is therefore well suited. The organometallic of choice for the production of sulphur atoms is ditertiarybutylsulphide (DTBS) that allows growth temperatures of 290°C. The choice of growth conditions is an important part of the overall process design. Independent parameters such as substrate temperature, VI/II ratio and total flow rate have to be carefully chosen to give the desired material properties.

High quality MOVPE-grown CdTe is best grown on lattice matched or nearly lattice matched substrates. But despite a 14.6% lattice mismatch, CdTe crystals have been produced on GaAs substrates with comparable quality to that of bulk CdTe. This substrate has for long been preferred due to its availability in high quality at low cost and large area. Alternative substrates such as sapphire or InSb have also been employed [26]. As a prospect for solar cell applications, the first epitaxial growth of CdS onto CdTe was reported by Igarashi in 1971 [27], but it was not until 1976 that heterostructures for photovoltaic devices were produced, achieving over 10% conversion efficiencies [28, 29] using the substrate configuration. It was shown by Simmons *et al.* that it is also possible to grow epitaxial CdTe onto single crystal CdS in a superstrate configuration using MOVPE [30, 31]. Devices made from these structures achieved ~7% efficiency. Since then the effort expended on the development of photovoltaic devices grown by MOVPE has been rather less than that put into direct vapour transport fabrication of CdTe/CdS solar cells: the latter has given more efficient devices.

MOCVD, widely used for the epitaxial growth of compound semiconductors, has also been applied to the deposition of polycrystalline CdTe thin films [32] and CdS films [33]. CdS can be deposited onto ITO/glass at rates of up to 5 nm/min for substrate temperature of 300°C, while CdTe can be deposited at temperatures of 320-450°C at rates of 85 nm/min. The conductivity type of CdTe films can be controlled via the VI/II molar ratio in the growth ambient, that modifies the density of intrinsic defects [34]. At low ratios (VI/II < 2), the deposited films are *p*-type and become *n*-type at higher ratios. However, the material produced is usually highly resistive (lateral resistivity of ~10^7 Ω.cm in the dark). The resistivity can be reduced by *in situ* doping using, for example, gallium or arsenic sources for *n*- and *p*-type dopant,

respectively, and by choosing the appropriate VI/II ratio. Defects and doping in CdTe material are reviewed in section 3.6.

The use of MOCVD-grown polycrystalline CdTe for producing solar cells was initially reported by Rohatgi *et al.*[35], Sudharsanan *et al.* [36] and Chu *et al.* [37]. Devices with conversion efficiency up to 10% were reported for CdTe grown by MOCVD onto CdS/SnO_2/glass substrates. Growth was performed in a tellurium rich ambient at substrate temperature of 300-400°C. A post-deposition treatment in $CdCl_2$ solution followed by anneal at 400°C for 15-30 min proved necessary to activate the structure. Annealed films were etched in bromine methanol solution prior to contact deposition. Best devices produced had open circuit voltage of 0.73 V, fill factor of 60% and short circuit current of 22 mA/cm^2. An *in situ* heat treatment of the substrate prior to CdTe deposition showed improvements on both V_{oc} and FF. Devices were characterised by a strong bias dependence but a wavelength independent quantum efficiency response, suggesting that recombination of carriers occurs at the interface.

Chou *et al.* [38] investigated the influence of the VI/II ratio in the growth ambient on the performance of the cells. The cell fabrication was similar to the one described above. Quantum efficiency measurements of the as-grown structures with illumination from both sides of the devices were used to confirm that cadmium rich growth (VI/II = 0.02) produces essentially *n*-type films and for tellurium rich growth (VI/II = 6) films are *p*-type. After $CdCl_2$ treatment, cells grown in Te-rich condition achieved 11.9% efficiency, while those grown in Cd-rich condition reached only 6-7%.

Kumazawa *et al.* [39], Aramoto *et al.* [12] and Tsuji *et al.* [40] have all used the MOCVD technique to grow the CdS window layer coupled with CSS growth of the absorber layer. Kamuzawa *et al.* [39] investigated the effect of CdS thickness reduction on device performance. As the film thickness was decreased from 80 to 40 nm, the open circuit voltage also decreased from 0.8 to 0.6 V. However, a slight increase in short circuit current was observed. A maximum power conversion of 15.1% was obtained for a CdS thickness of 60 nm with very reproducible results. Following this, Aramoto *et al.* [12] produced a 50 nm MOCVD-CdS/3.5 μm CSS-CdTe cell with 16% conversion efficiency (FF = 73%, V_{oc} = 0.84 V, J_{sc} = 26

mA/cm^2). The use of an ultra thin window layer allows higher quantum efficiency in the 300-500 nm region thus improving the performance of the devices. This technique was also applied to the fabrication of modules with success as Tsuji *et al.* [40] reported MOCVD-CdS/CSS-CdTe 1376 cm^2 modules with efficiency up to 10.5%.

Full polycrystalline MOCVD structure have also been reported by Rohatgi *et al.* [41] and Irvine *et al.* [42, 43]. Full advantage of the opportunity offered by the MOCVD technique to control doping during growth was taken by Irvine. *In situ* chlorine doped-CdS and arsenic doped-CdTe produced photovoltaic devices with limited efficiency. Improved performance was observed when undoped CdS was used. In this condition, the CdTe growth ambient was optimised for a VI/II ratio of ~0.6 at which devices exhibit a 2% power conversion, without the use of the post-deposition heat treatment. ~11% conversion efficiency was achieved by Rohatgi using full MOCVD structures with the use of the $CdCl_2$ heat treatment.

3.3.2 Other Deposition Techniques

Physical Vapour Deposition PVD can be used to deposit either CdS or CdTe. Deposition occurs by evaporation from elemental sources, by direct sublimation from a CdTe source or by vapour transport using a carrier gas to entrain and deliver Cd and Te_2 vapours from either elemental or CdTe source. For deposition in moderate vacuum, ~10^{-6} Torr, a deposition rate of 1 μm/min is obtained at 800°C for substrate temperature sufficiently low (~100°C). Higher substrate temperatures result in lower deposition rate. As-deposited films often exhibit a [111] preferred orientation [44] and also a columnar grain structure [45]. Grain size strongly depends on film thickness and substrate temperature, but as an example, for a 2 μm thick film, grain sizes range from 100 nm for a substrate temperature of 100°C to 1 μm at 350°C.

Close-Space Sublimation CSS is a widely used technique for depositing CdTe but CdS can also be grown using this technique. To date, the most efficient cells use CSS deposited CdTe [7, 12, 46, 47]. The technique is based on reversible dissociation of both CdTe and CdS at high temperature. The source material is maintained at a higher temperature (e.g. 650°C) than the substrate (e.g. 550°C), a few

mm away from it. The source dissociates into its elements which recombine on the substrate surface. In the case of CdTe, this technique is characterised by a high deposition rate (~1 μm/min), nearly random orientation of the as-deposited film [44] and large grain size (several μm) [48].

Electrodeposition Electrodeposition of CdTe and CdS has been developed to become a promising method for producing efficient thin film solar cells. It consists of the galvanic reduction of cadmium and tellurium from Cd^{2+} and $HTeO_2^+$ ions in acidic aqueous electrolyte. The reduction of these ions utilises six electrons in the following reactions taking place simultaneously:

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O,\ E_0 = +0.559\ V$$

$$Cd^{2+} + 2e^- \rightarrow Cd,\ E_0 = -0.4\ V$$

$$Cd + Te \rightarrow CdTe$$

Thickness and deposition rate are limited to the ability to maintain deposition potential over the entire surface of the growing film. As-deposited CdTe film on CdS exhibit strong [111] orientation [49] with columnar grains having a mean lateral diameter of 100-200 nm [50].

Radio Frequency Sputtering CdTe and CdS films can be deposited by RF magnetron sputtering from compound targets. In the case of CdTe, mass transfer of Cd and Te occurs via ablation of the CdTe target by Ar^+ ions, followed by diffusion to the substrate and condensation. As-deposited films (2 μm thick) exhibit grain size of ~300 nm and nearly random orientation [51].

Screen Printing Screen printing deposition can be used to deposit both CdS and CdTe layers. High purity elements are combined together with a suitable binder into a paste that is applied to the substrate through a screen. Following a drying step to remove binder solvents, the layer is baked at temperature up to 700°C to recrystallise the film and activate the junction. For CdTe films, CdO_2 is combined together with Cd and Te to act as a sintering flux and to avoid the usual post-deposition heat treatment. Films fabricated by this method typically have a thickness of 10 to 20 μm with lateral grain dimension of ~5 μm and random orientation.

Spray Pyrolysis Pyrolytic spraying is a low-cost technique for the fabrication of large area CdTe/CdS solar cells. It is a non vacuum technique for depositing films from a solution. Droplets of liquid are sprayed onto unheated or heated substrates after which a reaction/recrystallisation treatment is performed. CdTe films deposited by this technique have usually large grains and random orientation.

Chemical Bath Deposition CBD is used to deposit CdS with success, as this is the method employed to produce the best cell [7]. The CBD CdS process involves the use of aqueous alkaline solutions containing a cadmium salt, a complexing agent (e.g. aqueous ammonia) and a sulphur compound such as thiourea. The release of Cd^{2+} ions occurs through the dissociation of a complex species formed from the cadmium salt and complexing agent:

$$Cd(NH_3)_4^{2+} \leftrightarrow Cd^{2+} + 4NH_3(aq)$$

Sulphide ions are supplied by the hydrolysis of thiourea:

$$S{=}C(NH_2)_2 + OH^- \rightarrow S^{2-} + H_2NC{\equiv}N + 2H_2O$$

Finally CdS precipitates when the concentration product of Cd^{2+} and S^{2-} in solution exceeds the solubility product of CdS. This method results in uniform film deposition even with very thin layer (50 nm) due to a slow deposition rate, typically 10 nm/min.

The following table summarises the best CdTe/CdS thin film solar cells produced to date for each of the technique described previously. This table reports only structures that have both CdS and CdTe grown using the same deposition method.

Growth Technique	Efficiency (%)	Cell Area (cm^2)	Laboratory
CSS	16	1	Matsushita Battery Industrial [47]
PVD	16	0.25	Central Research Laboratory [52]
Electrodeposition	13.1	0.02	University of Queensland [53]
RF Sputtering	14	-	University of Toledo [54]
Spray Pyrolysis	12.7	0.3	Golden Photon Inc. [55]
Screen Printing	11.3	1	Matsushita Battery Industrial [56]
MOCVD	11.9	0.077	Georgia Institute of Technology [41]

Table 3-1 CdTe/CdS thin film solar cells. Best devices reported for each of the deposition techniques presented. Window and absorber layers of each device reported are grown by the same technique.

3.4 Post-Deposition Treatment

A large number of successful techniques for depositing quality CdS and CdTe films have been previously described. However, in the case of chloride free deposition technique, the deposition itself has been found to be less critical than the post-deposition processing. It generally involves a high temperature processing step with exposure to a chlorine containing species and/or oxygen. This treatment changes the electrical and structural properties not only of the absorber layer but also of the junction itself, and enables the solar cell to increase its efficiency from 2-5% in the as-grown state to 10-16% after treatment.

The treatment steps can be performed in a variety of ways such as:

(i) *In situ* incorporation of chlorine species during CdTe film deposition;

(ii) Dipping the CdTe layer in a $CdCl_2$ aqueous solution followed by drying in order to precipitate a $CdCl_2$ film and then annealing [57];

(iii) Annealing in $CdCl_2$ vapour [58], HCl [59] or Cl_2 gas [60, 61];

(iv) Deposition of a $CdCl_2$ layer onto the absorber followed by annealing.

The typical temperature-time range for the thermal cycle for chlorine incorporation is from 380 to 450°C for 15 to 30 min depending on the CdTe film thickness, with thicker films requiring longer treatment time.

The post-deposition treatment modifies the electronic properties of the CdTe layer. In its as-deposited state, CdTe is usually *n*-type or highly resistive *p*-type, making it unsuitable for solar cell applications. The $CdCl_2$ treatment is thought to introduce *p*-type dopant centres into the absorber layer and this is referred to as a "type conversion" process because most CdTe film are grown *n*-type.

The incorporation of chlorine is considered to form an acceptor complex with cadmium vacancies, $[V_{Cd}Cl_{Te}]^-$. This relatively shallow acceptor state has an ionisation energy of 0.12 eV [62] compared to 0.6 eV for $[V_{Cd}]^{2-}$ [63] which makes the complex a more effective dopant than the cadmium vacancies alone. However, excess chlorine can lead to compensating $[Cl_{Te}]^+$ donors. This will be further developed in section 3.6. This, as well as converting the conductivity of the CdTe layer from *n* to *p*-type, decreases the sheet resistance of the absorber layer up to three orders of magnitude [64].

The $CdCl_2$ treatment also modifies the structural properties of the CdTe films. The treatment can promote recrystallisation and grain growth in small grained films [65]. Levi *et al.* [66] observed a five time increase of the initial crystallite size following treatment on small grained PVD-grown films, but not for larger grained CSS-deposited layers. This was confirmed by Cousins *et al.* who observed that no grain growth occurs following chloride treatment on 10 μm thick CSS-deposited structures [67]. The predominant recrystallisation effect common to almost all deposition techniques giving small grains is the randomisation of the orientation of the CdTe films, showing the intragrain influence of the $CdCl_2$ on lattice arrangement. The effect of the $CdCl_2$ treatment on CdTe films grown by different techniques on crystallite size and orientation is summarised in Table 3-2.

Growth Technique	Film Thickness (μm)	Grain size (μm) Initial → After treatment	Orientation Initial → After treatment
CSS	8	8 → 8	Random → Random
PVD	4	0.1 → 1	(111) → (220)
Electrodeposition	2	0.1 → 0.3	(111) → (110)
RF Sputtering	2	0.3 → 0.5	(111) → (?)
Spray Pyrolysis	10	10 → 10	Random
Screen Printing	12	~10	Random
MOCVD	2	0.2 → 1	(111) → Random

Table 3-2 Structural changes that CdTe deposited by different methods, undergoes following $CdCl_2$ treatment (after McCandless *et al.* [68]).

The post-deposition treatment is usually performed at temperatures greater than 350°C. During this phase, a physical reaction between CdTe and CdS can occur and interdiffusion between the two semiconductors forms a $CdTe_{1-x}S_x$ solid solution in the absorber layer but also a $CdS_{1-x}Te_x$ solid solution in the window layer. These solid solutions have both beneficial and detrimental effects on the performance of solar cell. The interdiffusion process narrows the bandgap of the absorber layer for lower sulphur concentration ($x < 0.4$), resulting in higher long wavelength quantum efficiency [69]. Intermixing of CdS and CdTe reduces interfacial strain by reduction of the lattice mismatch at the CdTe/CdS junction [70] and may reduce the dark current recombination [71]. Alloy formation also consumes the CdS layer which can be beneficial for window transmission, but non-uniform consumption can result in lateral discontinuities at the junction [72].

Finally, one of the important effects of the $CdCl_2$ treatment is the passivation of the grain boundaries of the polycrystalline absorber layer. This has been evidenced by Edwards *et al.* [73, 74] using electron beam induced current (EBIC) imaging. The technique, which basically consists of mapping the short circuit current collected by the *p-n* junction after carrier excitation by the electron beam, is further detailed in section 4-6 and 7-5. Using the front-wall configuration, i.e. junction irradiated from

the front surface after chemically removal of the glass substrate, Edwards showed that the collected images were beam current dependent and that for $CdCl_2$-treated CSS-grown structures, no image contrast was observed between grains and grain boundaries at low beam current. Further investigations under high beam injection, i.e. higher beam current, gave rise to a newer band structure diagram of grain boundaries this being consistent with previously derived model using conductivity experiments indicating an upwards band bending at the grain boundaries [75, 76].

3.5 Typical Device Characteristics

To date, the most efficient CdTe/CdS thin film solar cell produced on a laboratory scale achieved 16.5% power conversion under standard AM1.5 illumination conditions [7]. The cell parameters were FF = 75.5%, J_{sc} = 25.9 mA/cm^2 and V_{oc} = 845 mV. The structure was glass/CTO/Zn_2SnO_4/CBD-CdS (0.1 μm)/CSS-CdTe (10 μm)/back contact (C:Hg:CuTe). By comparison, Aramoto *et al.* [12] have produced a 16% efficient MgF_2/glass/ITO/MOCVD-CdS (50 nm)/CSS-CdTe (3.5 μm)/Carbon/Ag cell. High efficiency was achieved because of an increase in the quantum efficiency to 50% for wavelengths around 400 nm due to the reduced CdS thickness. This shows the wide range of opportunities available for improving the performances of CdTe/CdS solar cells.

A common feature of CdTe cells, but also of solar cells to which it is difficult to form an ohmic back contact, is a current limiting effect in forward bias, which becomes progressively more important as temperature decreases. This is shown in Figure 3-4 where the current-voltage (J-V) curve for a CSS-grown solar cell is plotted as a function of temperature [77]. The influence of temperature on the open-circuit voltage can be seen as well as a flattening of the J-V curve at high forward bias and is referred to as the rollover effect.

The current-voltage equation for a solar cell was derived in section 2.3. In the particular case of CdTe thin film solar cells, the single diode equation is not sufficient to fully describe the behaviour of the device. Stollwerck and Sites [78] described this phenomenon as due to a second diode barrier located at the back contact of the solar cell. The equivalent circuit model corresponding to this is shown in Figure 3-5.

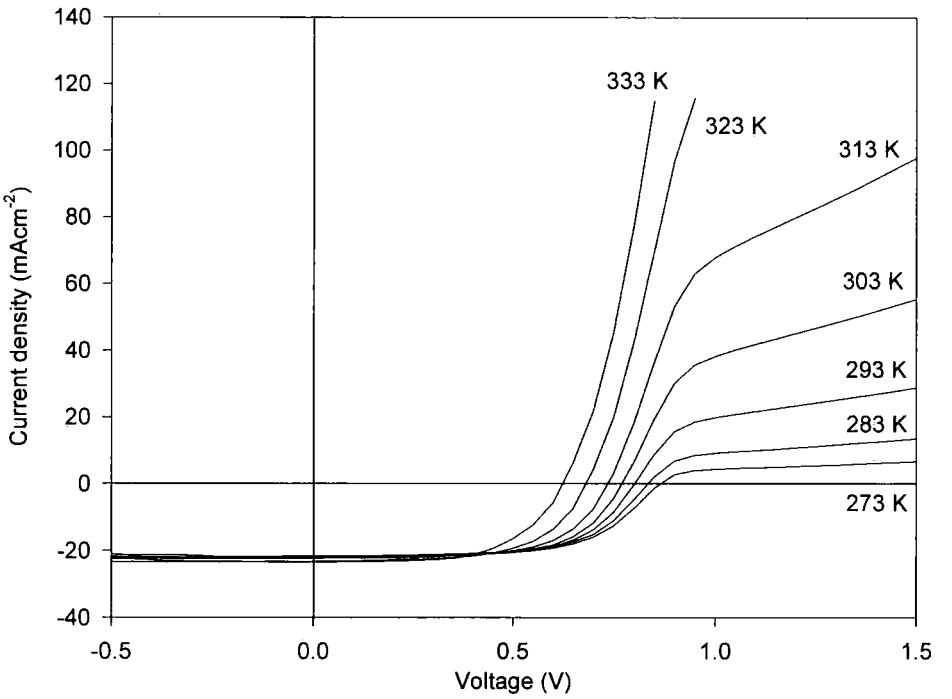

Figure 3-4 Current-voltage characteristics under illumination as a function of temperature for a CdTe/CdS solar cell (reproduced from [77]).

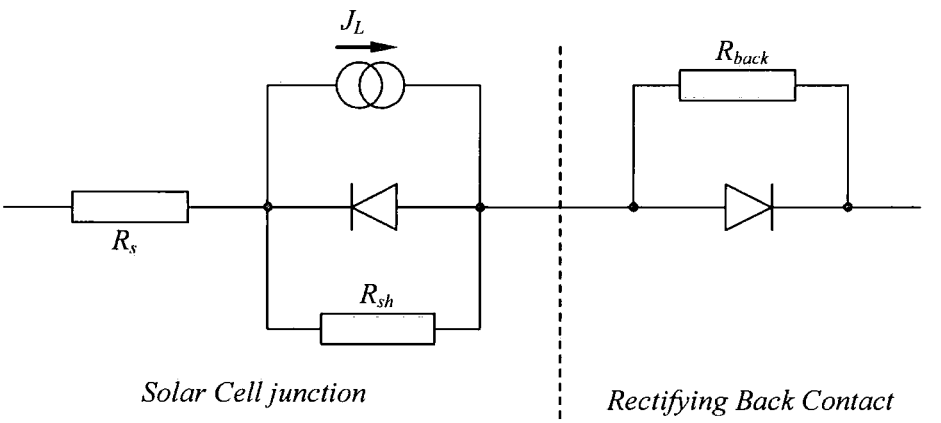

Figure 3-5 Equivalent circuit for a solar cell with rectifying back contact: this comprises two diodes associated with the main solar cell and the Schottky junction located at the back contact, respectively.

This barrier is also thought to be responsible for the crossover effect between the dark and light *J-V* curves because of non negligible minority carrier current. This feature also demonstrates the poor conductivity of the absorber layer in the dark. However, it has been suggested by Agostinelli *et al.* [79] that the crossover observed between the current-voltage characteristics measured in the dark and under

illumination could be associated with a barrier located at the front region of the device due to an increased compensation of donors in the CdS window layer and the presence of a buried junction located deeper in the absorber layer.

3.6 Defects and Doping in CdTe Materials

The development of preparing high quality single crystals in II-VI technology has been slower than in other technologies because of the ease of defect formation within the crystal lattice. This is particularly true for CdTe materials. Due to the large number of CdTe film deposition methods, control of impurities is difficult. The multi-stage processing of the solar cell brings even more impurity elements into the system. It has been shown recently using quantitative SIMS (secondary ion mass spectroscopy) and ICPMS (inductively coupled plasma mass spectrometry) analysis by Emziane *et al.* [80-82] that numerous impurities are introduced into the structure originating from the starting materials, even when using high purity ones.

The defects are classified into categories depending on their dimension. Point defects are zero dimensional defects involving a single atom or a complex of a few atoms. These can be vacancies, i.e. a missing atom from the lattice, interstitials, i.e. an extra atom between normal lattice sites, or substitutions, i.e. an atom on another element's lattice site. Vacancies and self-interstitials are called intrinsic defects, while substitutions and extraneous interstitials are labelled extrinsic defects. Figure 3-6 shows the positions of common defect levels in CdTe and will be discussed in more detail later in this section.

One dimensional defect such as dislocations, involves a line of continuous defects. Two dimensional defects include grain boundaries, stacking faults, interfaces and twin boundaries. Grain boundaries are a source of high defect densities in polycrystalline CdTe. High concentrations of two dimensional defects can be found near the interface of a CdTe/CdS heterojunction because of the important lattice mismatch (~10%) between the two semiconductors. Finally, three dimensional defects can exist in a crystal in the form of voids or precipitates of point defects. Part of this work is concerned with impurity doping of CdTe, thus involving point defects.

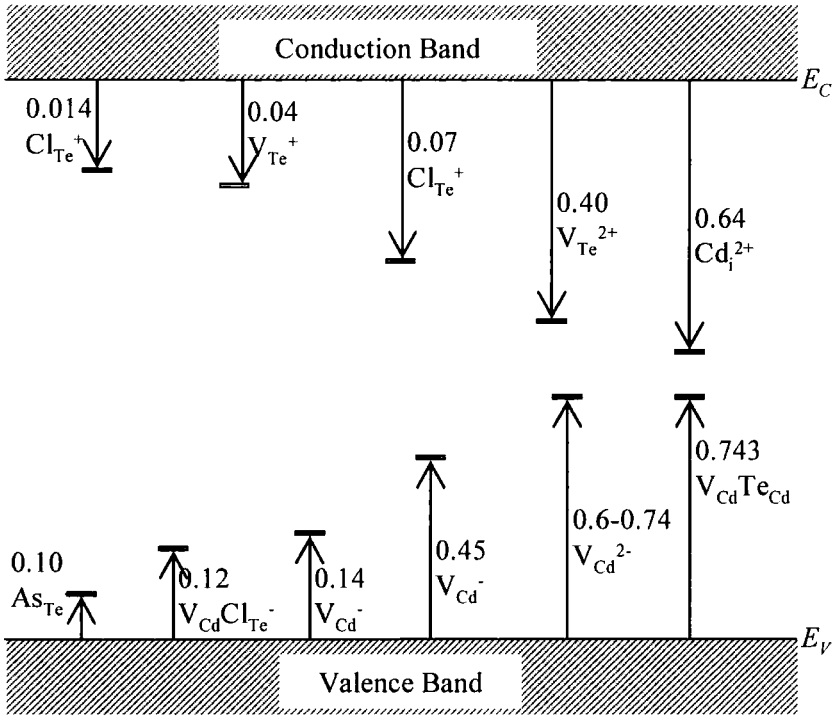

Figure 3-6 Ionisation energy in eV of common defects and impurities in CdTe. References for each level are given in the text.

Doping in CdTe is achieved by making use of point defects, either intrinsic or extrinsic. Processing steps for the fabrication of a solar cell involve the addition of various impurities to the structure and especially to the absorber layer. Some of these impurities such as chlorine are intentionally added while others are unintentionally introduced, such as indium or sodium. Other processing steps include annealing at various temperatures for different durations and these annealings can create or annihilate many types of defects due to an enhanced diffusion at increased temperatures.

Intrinsic Defects and Doping The case of tellurium rich growth of CdTe implies an excess of tellurium and hence a deficiency of cadmium in the crystal lattice. Thus the dominating defect is cadmium vacancy, singly $[V_{Cd}]^-$ or doubly $[V_{Cd}]^{2-}$ ionised, both acting as acceptors. Their energies have been reported at 0.1 eV [83] and 0.45 eV [84] above the upper limit of the valence band for the single acceptor, and 0.6-0.74 eV+E_V [63, 85] for the double acceptor. The density of cadmium vacancies is commonly in the range of 10^{17}-10^{18} cm^{-3} [86], with an estimation of up to 10^{19} cm^{-3} [63]. High concentration of compensating anti-site

$[Te_{Cd}]^+$ donors can also be found in tellurium rich grown CdTe [86]. Compensation occurs with the existence of both cadmium vacancies and $[Te_{Cd}]^+$ donors. Neutral or singly ionised acceptor complex $[V_{Cd}Te_{Cd}]$ are also commonly form during material growth. The neutral defect was reported as having an energy level of 0.743 eV above the valence band [85].

When the material is grown cadmium rich, there is an increase in tellurium vacancy concentration. Tellurium vacancies can be doubly ionised $[V_{Te}]^{2+}$ and act as donors. They reside 0.4-0.5 eV below the bottom of the conduction band. Also possible but less common are tellurium interstitial acceptors, $[Te_i]^-$, having a formation energy of 3.44 eV [62].

Intrinsic doping is achieved by controlling the concentration of native defects in the undoped material. The cadmium rich growth enhances the formation of tellurium vacancies which can become positively charged. These defects act as donors, therefore the material is grown *n*-type. On the other hand, a tellurium rich film will be *p*-type owing to an increase in cadmium vacancy (acceptor) concentration. This type of doping is limited by strong compensation of donors and acceptors in CdTe. Doping can be applied to both CdS and CdTe layers in order to increase carrier concentrations. Usually doping occurs during the $CdCl_2$ heat treatment of the respective layers (see section 3.4). Impurity doping also occurs during the preparation of the back contact as explained in section 3.2.5.

Extrinsic Defects and Doping Abundant literature is available on extrinsic defects arising from the introduction of impurities in CdTe due to the long history of the material in the detector industry. The discussion will be restricted to chlorine and arsenic as they are the main impurities used in this work.

Chlorine defects are introduced when depositing the CdTe layer or during the post-deposition treatment when processing the solar cells. Typically, chlorine resides on a tellurium site $[Cl_{Te}]^+$, acting as a shallow donor. This defect is located 0.014 eV below the conduction band [2] and is present in concentrations of up to 10^{18} cm^{-3} [87]. Many complexes may form in the presence of chlorine in CdTe. The $[V_{Cd}Cl_{Te}]$ complex can be neutral for a singly ionised cadmium vacancy or an acceptor for a doubly ionised cadmium vacancy. The latter resides 0.12 eV above the valence band

[62]. Chlorine self-compensation occurs through the existence of both $[Cl_{Te}]^+$ and $[V_{Cd}Cl_{Te}]^-$ [88].

Arsenic, a group V element, acts as an acceptor on a tellurium site $[As_{Te}]^-$. This is a shallow acceptor located between 0.06 eV [89] and 0.10 eV [90] above the valence band. Compensation of the shallow acceptors occurs at high doping with tellurium vacancies. Arsenic can also be incorporated in cadmium sites as a triply ionized donor [89]. Thus the doping level of arsenic is function of the partial pressures of cadmium and tellurium used during layer growth.

Extrinsic doping is achieved using a variety of impurities, but carrier concentration may be limited by compensation effects. This has made possible the fabrication of highly resistive CdTe crystals but this can be problematic for conductive CdTe. Doping is limited by the solubility of the dopant atoms in the host semiconductor lattice. For example, when the quantity of arsenic acceptor exceeds the solubility of arsenic in CdTe, the excess acceptor atoms create tellurium vacancies forming a complex centre that acts as a donor and hence annihilates the *p*-doping effect of the process.

3.7 Concluding Remarks

The science and technology of CdTe/CdS thin film solar cells have been reviewed. It has been shown that the optical and electrical properties of CdS and CdTe are well-suited for photovoltaic applications, and that the flexibility of the system in terms of the wide range of deposition methods available, make the technology highly promising for large-scale production. Several companies are currently commercialising thin film CdTe/CdS modules (First Solar, Matsushita and ANTEC Solar) which can reach 11% conversion efficiency for a 0.54 m^2 area.

On a laboratory scale, several groups can produce in a reproducible way, devices with efficiencies in the range of 14-16%. A realistic target in the near future is an efficiency over 20% [91]. In order to further increase the efficiency of current CdTe solar cells, the research focuses on several main issues:

(i) Determining the exact mechanisms behind the effect of the $CdCl_2$ treatment. This should allow greater control over the post-deposition processing, without relying on empirical methods;

(ii) Examining the extent and effect of the sulphur and tellurium interdiffusion at the device junction;

(iii) Development of a cheap, stable and low-resistance back contact;

(iv) Increasing the carrier concentration in the absorber layer which is today limited to $1\text{-}4\times10^{14}$ cm^{-3} [92];

(v) Routes for novel materials, for the front contact to reduce optical losses and control the out-diffusion of impurities from the substrate.

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Chapter 4

Sample Preparation and Characterisation Techniques

4.1 Introduction

This chapter describes the sample preparation and characterisation methods used throughout this work. Both individual layers and cell structures were prepared by metal-organic chemical vapour deposition (MOCVD), the principles of which are described in section 4.2. The post-growth processing steps required to make working devices are outlined in section 4.3. The reminder of the chapter is dedicated to characterisation techniques used for both layers and devices. They include optical, electrical, structural and chemical methods namely, response to solar radiation, current-voltage measurements, spectral response, carrier type and resistivity measurements for single layer, SEM and electron beam induced current (EBIC) plus x-ray diffraction (XRD) and secondary ion mass spectroscopy (SIMS).

4.2 MOCVD Growth of CdS, CdTe and CdTe:As

All the layers and structures used in this work were grown by MOCVD at the University of Wales, Bangor. A review of CdTe based solar cells and materials was presented in section 3.3.1 and a schematic of the actual growth system is now shown in Figure 4-1.

The substrates used in this work were of two kinds. Films of CdTe:As were grown onto insulating sapphire and CdTe/CdS solar cell structures were grown onto ITO/glass substrates. Two kinds of glass substrates with different TCO were used. The first one was supplied by Merck Display Technology (MDT) and consisted of 0.7 mm soda lime glass coated with a bilayer of SiO_2 (~20 nm) and ITO (~100 nm). The indium doped tin oxide has the high conductivity required to provide a low sheet resistance front contact, whereas the silicon dioxide layer acts as a barrier to the diffusion of impurities from the glass. The second ITO/glass substrate was provided by ANTEC GmbH. This substrate is somewhat different from the first one as it comprises ~4 mm soda lime glass coated with a bilayer of ITO (~250 nm) and SnO_2 (~30 nm). In this case the tin oxide layer is used to reduce the diffusion of indium atoms from the ITO layer into the rest of the cell. This layer, with higher resistivity than ITO, is less prone to pinholes. This type of substrate is commercially used by ANTEC GmbH to produce CdTe based photovoltaic modules.

The precursor vapours for MOCVD used were dimethylcadmium (DMCd) and ditertiarybutylsulphide (DTBS) for the growth of CdS, and DMCd and di-isopropyltelluride (DIPTe) for CdTe growth. *In situ* doping was achieved using tris-dimethylamino arsine (DMAAs). All organometallic vapours were supplied by Epichem Ltd. The layers were deposited at atmospheric pressure in a Thomas Swan horizontal reactor with a graphite substrate holder. The substrate holder was heated with a graphite resistance heater capable of reaching a working temperature of up to 600°C. Prior to growth, the organometallic concentrations were calibrated using an Epison (Thomas Swan Ltd) ultrasonic concentration monitor. This is a gas concentration analyser that measures the speed of sound in a binary ambient. The sound velocity is related to the composition via analytical calculations using the temperature, molecular weight of each component and specific heat ratio. This is also

used during the growth to ensure that the organometallic mixture is maintained at a constant concentration.

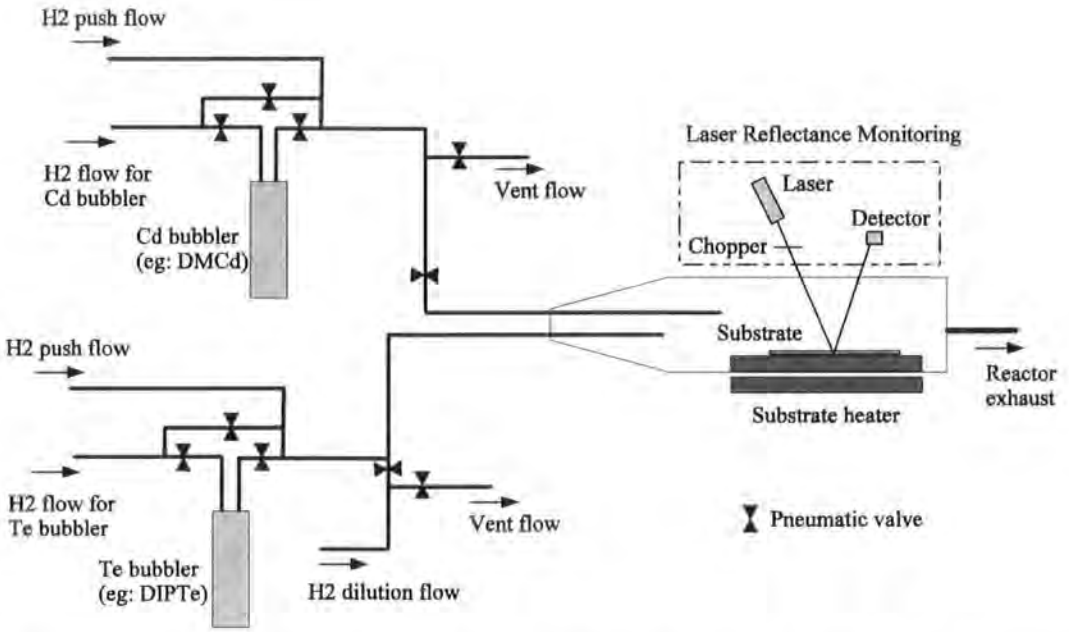

Figure 4-1 Horizontal reactor with gas supply for MOCVD growth [1]. The actual system contains six bubblers for Te, Cd, S, As, Cl and Zn organometallics.

The top walls of the reactor and liner tube are modified to permit the reflectance of a 635 nm diode laser beam for *in situ* optical monitoring [2]. *In situ* monitoring helps in understanding kinetic mechanism and in providing parameters suitable for feedback control of the layers during growth. The monitoring technique used was laser reflectometry that measures the thin film interference between the surface of a growing film and the film/substrate interface. The technique gives information on film thickness, growth rate, surface roughening and some indication of film composition and this is briefly outlined now.

When a monochromatic light beam hits the surface of a growing film a succession of reflection/transmission phenomena occurs. All reflected beams leaving the sample are detected yielding an overall reflected intensity. Because there is a phase difference between the multiple reflected beams, constructive or destructive interferences will occur, leading to an intensity modulation of the overall reflected light. This is also known as Fabry-Perot etalon or interferometer [3]. The phase difference and therefore the intensity of the reflected light depends upon the

thickness of the growing layer as well as on the optical constants of the materials and beam wavelength. Thus the thickness is determined by measuring the period of the oscillations and the growth rate can thereafter be deduced. Hence low growth rates are characterised by long oscillation periods while higher growth rate will yield shorter ones.

Changes in the reflected signal also arise from surface roughness and optical waviness. The former being referred to as thickness fluctuations on a nanometre scale while the latter on a micron scale. Increasing optical waviness is detected by reduced oscillation amplitudes but a constant average value. On the other hand increasing roughness is detected by a reduced total reflected intensity. When roughness is negligible only specular reflectance is detected while as roughness increases more and more light is scattered, i.e. diffuse reflectance, and therefore the total signal detected is smaller. Changes in film composition can also be detected by reflectance measurements due to changes in the refractive index associated for each composition. Optimum sensitivity of such a system is achieved when more than one wavelength of incoming light is used.

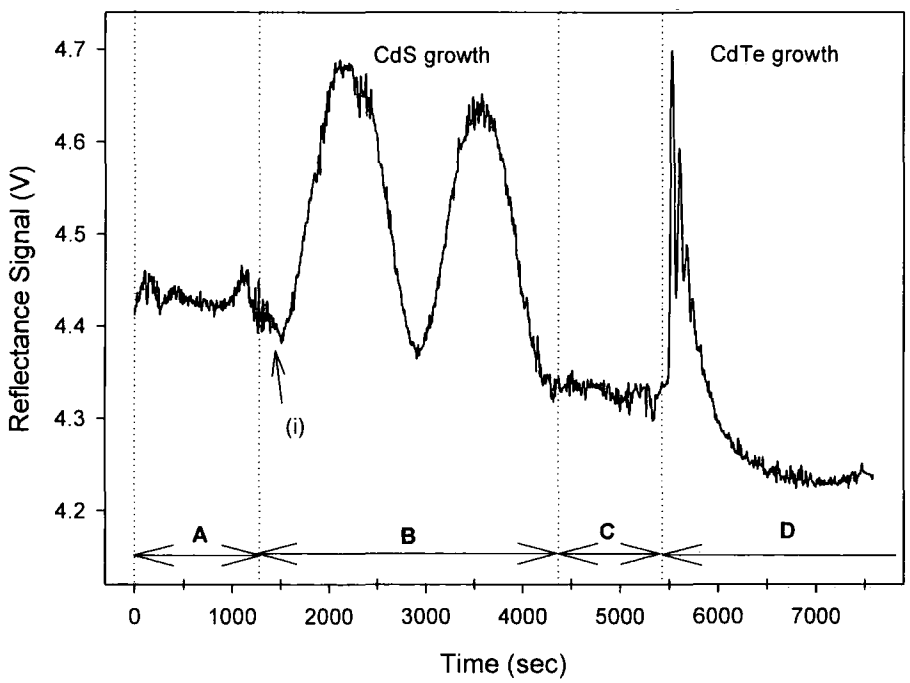

Figure 4-2 Optical interferogram recorded during the growth of 240 nm of CdS grown at 300°C and 8 μm of CdTe at 350°C.

An example of an optical interferogram recorded for the growth of CdS (240 nm) and CdTe (8 μm) on ITO/glass substrate is given in Figure 4-2. This time resolved reflectance gives the growth history. The interferogram can be divided into four parts marked A, B, C and D on the figure which are explained next.

A Time t = 0-1230 s. The heating phase starts. The temperature is raised to 300°C and stabilised for ~1200 s.

B Time t = 1230-4240 s. This is the CdS growth phase. The organometallics DMCd and DTBS are allowed into the reactor and this is marked by a small decrease in reflectance marked (i) on the figure. Then a short period of stagnation (~300 s) corresponding to nucleation process [4] is observed before the CdS growth starts. Growth is marked by two oscillations. During this time 240 nm of CdS are grown at a rate of ~5 nm/min.

C Time t = 4240-5496 s. The CdS growth is stopped, the organometallics are switched to vent and the temperature is reset to 350°C in preparation for the growth of the CdTe absorber layer.

D Time t = 5496-11500 s. The DMCd and DIPTe organometallics are switched into the reactor to start the CdTe growth. No delay is observed and the growth starts immediately. More rapid oscillations are observed compared to the CdS growth which indicate a higher growth rate for CdTe compared to CdS. The interferogram shows strong attenuation of the CdTe oscillations due to the absorption at the laser wavelength. 8 μm of CdTe were grown in ~6000 s, i.e. at a growth rate of ~80 nm/min.

Growth parameters for the samples used in the different studies will be given in the respective chapters, but the ranges are as follows. The CdS layers were grown at 300°C while the CdTe layers were deposited at 300-400°C. The precursor ratio (Te:Cd or VI/II ratio) for the CdS growth ranged between 1.2 and 1.5, and between 0.6 and 1.7 for the CdTe growth. For the study of arsenic doped CdTe films the flow of arsenic organometallic in the growth system varied between 3 and 9 sccm (standard cubic centimetres per minute). Note that throughout this work the precursor ratio refers to the concentrations in the reactor and not in the material grown. For a

stoichiometric MOCVD-grown CdTe film it is generally considered that a VI/II ratio of ~1.96 is required, while a 1:1 reactant mixture gives cadmium rich (*n*-type) films [5].

4.3 Post-Deposition Treatment

To enhance the performance of a CdTe/CdS solar cell a post-deposition heat treatment in a cadmium chloride ($CdCl_2$) environment must be performed. Following this a special chemical surface preparation must carried out on the CdTe prior to application of a back contact to the CdTe absorber layer. Post-growth treatment of the as-grown layers usually takes the form of a four step process that includes (i) a deposition of a $CdCl_2$ layer, (ii) a bake in air or nitrogen, (iii) a chemical etch and then (iv) contact deposition.

A thin film of $CdCl_2$ (up to ~140 nm) was deposited onto the back surface of the CdTe/CdS structures (~1 cm^2) by evaporation of $CdCl_2$ powder under vacuum. At this stage, the substrate was not heated. The thickness of the deposited coating was controlled *in situ* by a crystal quartz monitoring. The sample was subsequently annealed in nitrogen in a tube furnace. Baking temperatures were in the range of 340-500°C for 5-50 min. Once the annealing was completed, the sample was thoroughly rinsed in deionised water in order to remove any $CdCl_2$ residue from the surface, and then blow dry with nitrogen. For contacting the CdTe layer, an intermediate Te rich layer was formed at the surface before applying a back contact. This was achieved by chemically etching the back surface in either a solution of bromine methanol (Br_2/MeOH) or nitric and phosphoric acid (NP).

In most cases, the samples were dipped in a solution of 1% HNO_3 (70%)+ 70% H_3PO_4 (85%) + 29% H_2O [6] until bubbles appeared at the back surface and left for ~10 s before rinsing in water and drying in nitrogen. When dipped in the Br_2/MeOH solution (0.03-0.5% bromine concentrated), the cells were etched for 5 s before rinsing in methanol and drying in nitrogen. In both cases the solution was maintained at room temperature.

Immediately after the etching step the cells were placed in an evaporator where four ~100 nm thick gold dots of 2.5 mm diameter each were deposited to form back contacts. Finally, a contact to the ITO was made. To allow this, part of the

CdTe layer was removed mechanically and the underlying CdS etched off with hydrochloric acid. Contact to the ITO could then be made using indium-gallium amalgam. Hence most of the devices measured comprised 4 gold dots on a ~1 cm^2 area. The contact dots were not scribed to define their area and the active area was defined by the area of a single gold dot.

4.4 Solar Cell Characterisation

4.4.1 Solar Radiation and Solar Simulator

The sun is essentially a self-sustained nuclear fusion reactor transforming hydrogen into helium at temperatures of around 2×10^7 K within its core. This produces around 4×10^{20} W. This energy is liberated as spectrally continuous electromagnetic radiation between ~1 Å (x-ray) and 30 m (RF) and can be closely approximated by a black body radiator at 5800 K, the surface temperature of the sun.

The intensity of solar radiation in the free space at the average distance of the earth from the sun is defined by the solar constant, the value of which is 1367 $W.m^{-2}$ [7]. As solar radiation passes through the earth's atmosphere it is scattered by atmospheric molecules. These attenuate the whole spectrum but are more effective at shorter wavelength. In addition the spectrum is also attenuated in particular spectral bands through absorption by constituent atmospheric gases and water. The degree of which the atmosphere attenuates the solar radiation reaching the earth's surface is defined as the air mass (AM).

The AM0 spectrum represents the solar spectrum outside the earth's atmosphere where intensity is given by the solar constant. The shortest path through the atmosphere is that taken when the sun is directly overhead. This is known as AM1. When the sun is at an angle θ from the vertical, air mass is given by $1/\cos\theta$. For example, an angle of 45° corresponds to AM1.5. For temperate latitudes AM1.5 is used to represent the average spectrum. In this case the incident power density is 777 $W.m^{-2}$ for direct irradiation and 960 $W.m^{-2}$ with the inclusion of diffuse and scattered light to give a total or global intensity. Both AM0 and AM1.5 direct spectra are shown in Figure 4-3. In this work, the 100 $mW.cm^{-2}$ AM1.5 direct spectrum was used throughout for all the measurements.

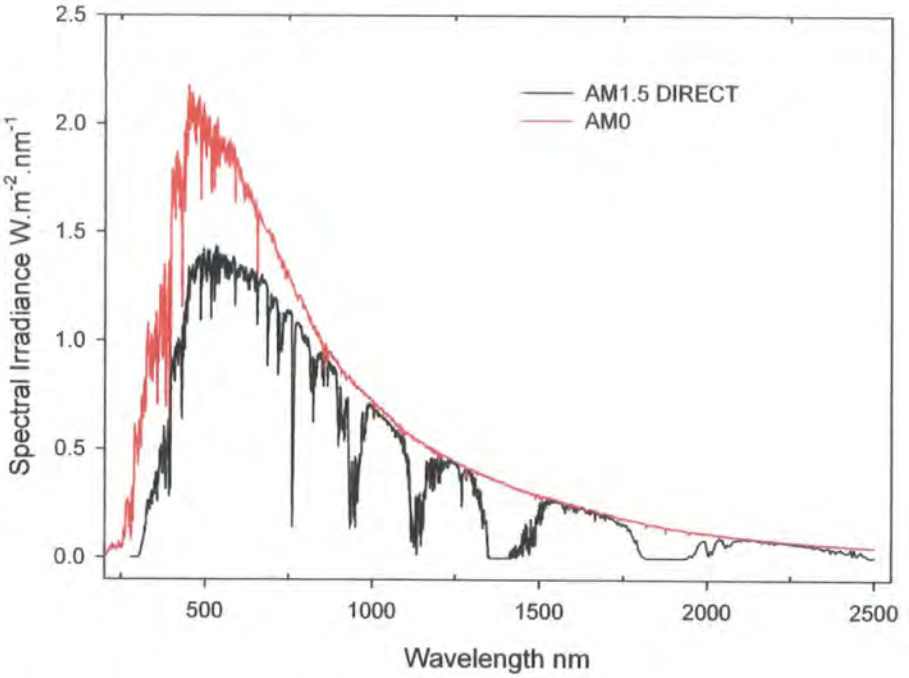

Figure 4-3 AM0 (red line) [8] and AM1.5 Direct (black line) [9] spectra.

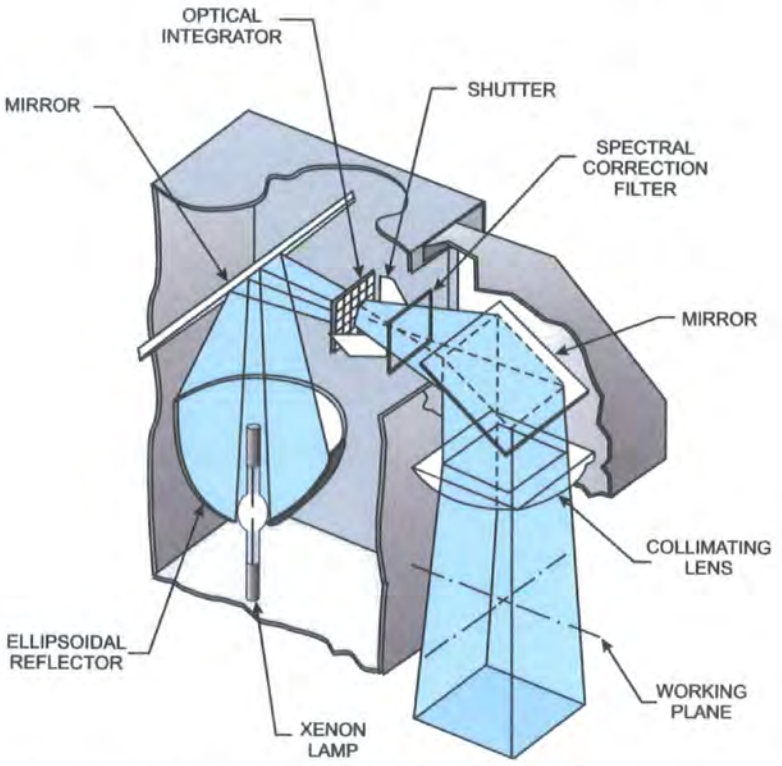

Figure 4-4 Light path of the ORIEL 300 W solar simulator [10].

In order to achieve standard illumination conditions, a commercial 300 W xenon arc-lamp solar simulator from ORIEL (model 81160) was used [10]. The light path inside the housing is shown in Figure 4-4. The simulator produces a uniform, collimated 51×51 mm output beam. The uniformity in intensity is within ±5% over the area and the equivalent output power produced by the xenon arc-lamp is ~2 suns. The xenon lamp differs from the solar spectrum in the 800 to 1100 nm region because of the intense line output of the lamp. A primary filter is used to reduce the mismatch in this region, and a second filter modifies the visible and ultraviolet portion of the spectrum to match the AM1.5 one. This is shown in Figure 4-5 where both the unfiltered output and the output with AM1.5 filters are plotted.

Finally a light intensity controller is used to ensure long-term stability of the output. It compares the recorded signal to the set level and changes the power supply setting accordingly. Intensity fluctuations of less than 0.03% are achieved with this system. Calibration of the light intensity to 100 $mW.cm^{-2}$ was done using an ORIEL thermopile and a Kipp & Zonen SP Lite pyranometer.

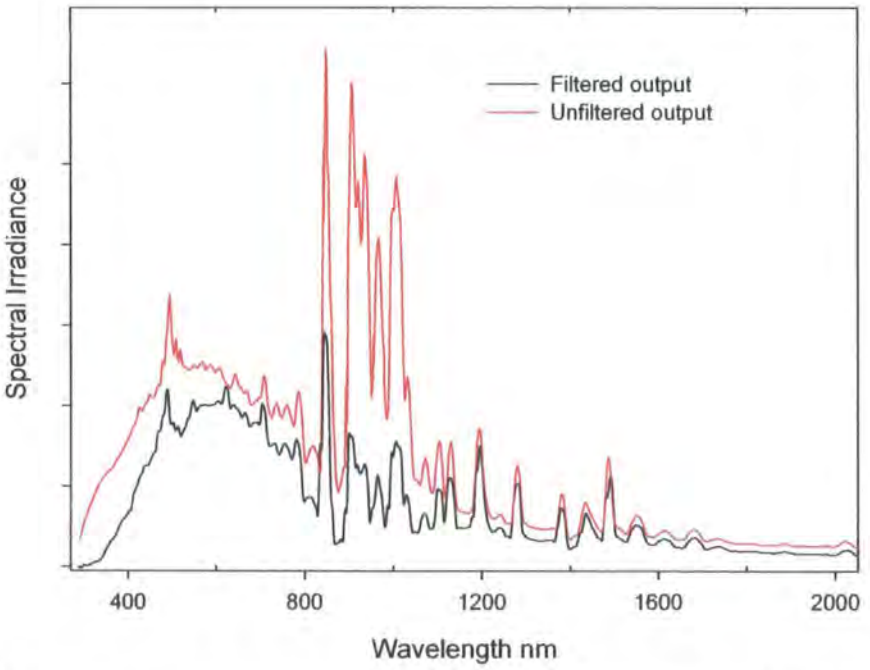

Figure 4-5 ORIEL solar simulator output. Unfiltered (red line) and filtered (black line) output to give an approximate AM1.5 spectrum [11].

4.4.2 Current-Voltage Measurements

Current-voltage (*J-V*) measurements are necessary to evaluate primary characteristics of solar cells that determine the energy conversion performance as described in section 2.3.2. *J-V* measurements also allow the measurement of more basic *p-n* junction parameters such as diode quality factor and series and parallel resistances. A further description of these parameters is given in section 2.3.2 and the method used to extract parameters from the *J-V* curves is given with the results in Chapter 7.

To perform the test, the solar cell was mounted on a sample holder specially designed and built for this experiment that allows the use of samples in either the substrate or superstrate configuration. The design was based on an earlier setup from the Solar Cells group at the University of Ghent in Belgium. A picture of a specimen mounted on the holder is displayed in Figure 4-6. Measurements were done using two magnetic PH100 probes from SUSS MicroTec connected to a Keithley sourcemeter controlled by a computer through an IEEE GPIB interface to allow data acquisition. The control software was written as part of this work in Visual Basic. The software includes both current and voltage sweeps, although current sweeps were generally used in practice. Other features include the facility to repeat and average each data point, and the display of the sample response in real time.

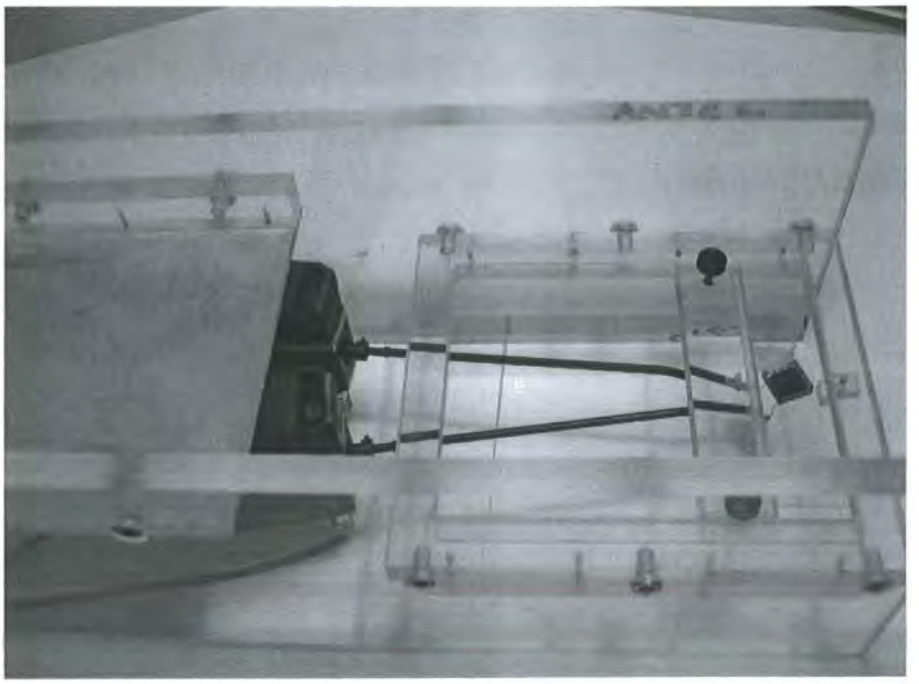

Figure 4-6 Solar cell and sample holder.

4.4.3 Spectral Response Measurements

Spectral response measurements entail the determination of the quantum efficiency (QE) of a sample as a function of wavelength. QE is defined as the number of electron-hole pairs created and collected by the solar cell per incident photon and is usually less than unity. QE has a strong wavelength dependence due to the spectral behaviour of the optical absorption coefficients of CdS and CdTe, and also due to the depth dependence of the carrier collection probability. The as-measured QE is referred to as *external* quantum efficiency. In contrast the *internal* quantum efficiency is used when corrections are made to allow for reflection losses at the front of the cell. For this work, new spectral response experiment was built from components according to the schematic shown in Figure 4-7.

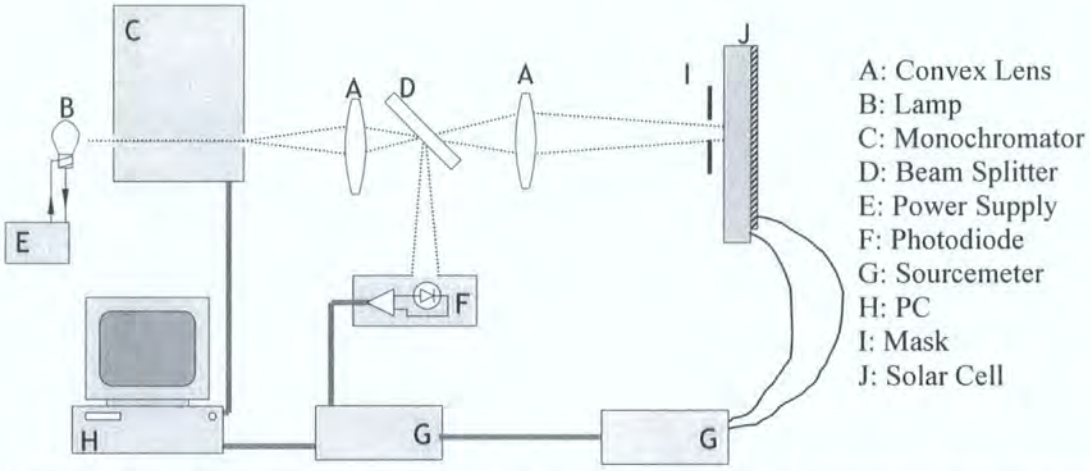

Figure 4-7 Experimental arrangement used for spectral response measurements (adapted from [12]).

The system was based on a Bentham M300 monochromator having a Czerny-Turner configuration and a Bentham 100 W quartz halogen lamp controlled by a constant current stabilised power supply. The output intensity was monitored by a fully calibrated silicon PIN photodiode from Hamamatsu Photonics Ltd in order to determine the photon flux. Order sorting filters were used to eliminate second order harmonics and were integrated in the entrance slit of the monochromator. A built-in stepping motor allowed wavelength scanning controlled from a remote stepping motor drive unit equipped with an IEEE-488 bus interface. Wavelength increments

as well as the currents recorded from the photodiode and the sample response were computer controlled using GPIB links and Keithley sourcemeters.

A QE spectrum is an important source of device performance-related information. It is possible to extract material information from QE spectra such as the intermixing of the CdS and CdTe layers for a CdTe/CdS cell [13-15]. It is also possible to determine the position where the highest carrier collection occurs and therefore to distinguish between a heterojunction and a buried homojunction [16]. For example, for an ideal heterojunction the QE is high and constant between the bandgaps of the two materials. If the minority carrier diffusion length is small in the absorbing material, the QE decreases towards lower photon energies for which the optical absorption coefficient is also lower. On the other hand, if the particular device is a buried homojunction, the QE will increase at long wavelength due to deep penetration of photons into the buried junction.

4.5 Electrical Measurements for Individual Layers

Electrical measurements were also employed to investigate the effectiveness of doping layers of CdTe with arsenic. Apparatus used to determine the conductivity type and the resistivity of these layers was set up and is described in the next two sections.

4.5.1 Carrier Type Determination

The determination of the conductivity type of the films provided is essential to assess the effectiveness of growing *p*-type CdTe absorbers that are required for solar cell applications. Two different methods were used for the conductivity type determination of thin film CdTe and are outlined next.

Thermoelectric probe method The conductivity type is determined by the sign of the thermal emf or Seeback voltage generated by a temperature gradient. Two probes contact the sample surface: one is "hot" and the other one is "cold" as illustrated in Figure 4-8 a). The hot probe heats the *n*-type semiconductor immediately below it, thereby causing the donor atoms to release their extra electrons. Thus, the concentration of free electrons near the hot probe is increased. In

order to maintain a uniform free carrier concentration throughout the sample, these carriers tend to diffuse away from the heated region, which becomes positively charged since the electrons are negatively charged. This creates an electric field that opposes the diffusion, producing a potential detected by the voltmeter. Analogous reasoning leads to the opposite potential for *p*-type samples.

Hot probe techniques are effective over the 10^{-3} to 10^{3} Ω.cm resistivity range. The voltmeter tends to indicate *n*-type for high resistivity material even if the sample is weakly *p*-type. As some of the material measured in this study appeared to be of high resistivity, the rectification method was also used and is now explained.

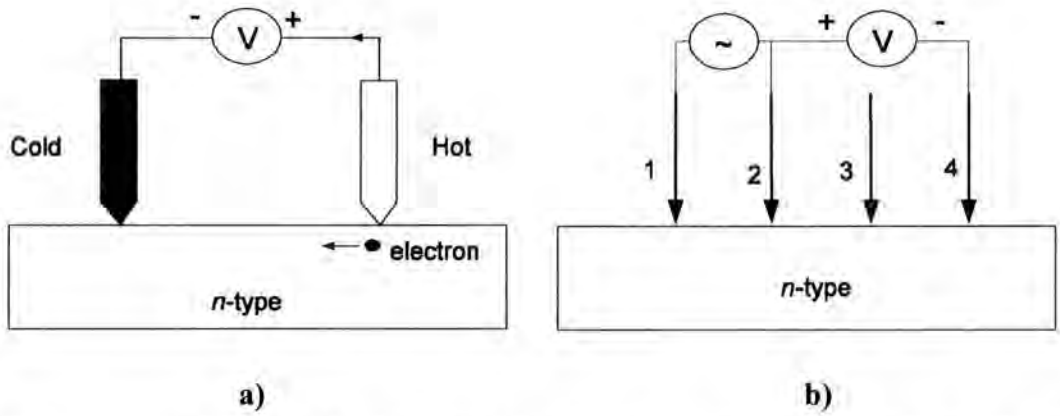

Figure 4-8 Hot probe (a)) and rectifying probe (b)) methods for conductivity type measurements.

Rectification method The sign of the conductivity is determined by the polarity of a rectified AC signal at a point contact to the semiconductor [17, 18]. When two probes are used, one should be rectifying and the other should be ohmic. Current flows through a rectifying contact to *n*-type material if the contact probe is positive and for *p*-type if it is negative. Rectifying and ohmic contacts are difficult to implement with two-point contacts. Fortunately four-point probes experiment can be used with appropriate connections not requiring ohmic contacts. An AC voltage is applied between probes 1 and 2, and the resulting potential is measured between probes 4 (or 3) and 2 as shown in Figure 4-8 b). The metal-semiconductor Schottky diode at probe 2 will therefore be either forward or reverse biased depending on the polarity of the current and the film conductivity type. The DC voltage measured between probes 2 and 4 will be positive for a *p*-type material and negative for an *n*-

type material. The use of an oscilloscope in place of the voltmeter allows direct observation of the biasing of the metal-semiconductor junction and the average voltage gives the conductivity of the film.

4.5.2 Resistivity and Sheet Resistance

Arsenic doped CdTe films were grown in an attempt to provide low resistivity material with a high concentration of carriers. A resistivity experiment was set up to test the grown films. The objectives were to determine the sheet resistance R_s and the resistivity ρ of the layers studied. The geometry of such an experiment is shown in Figure 4-9 and is referred to as the Van der Pauw technique. This method requires four contacts on the periphery of the sample, rather than depending on miscellaneous corrections for finite sheets as used in the more classical four-point probe technique. Van der Pauw demonstrated that there are actually two characteristic resistances R_A and R_B associated with the corresponding terminals shown in Figure 4-9 [19].

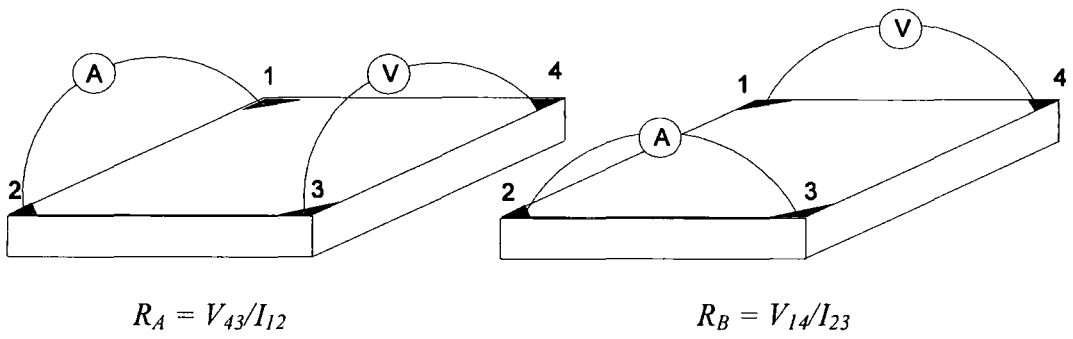

Figure 4-9 Schematic of a Van der Pauw configuration used in the determination of the two characteristic resistances R_A and R_B for a thin film sample.

R_A and R_B are related to the sheet resistance through the Van der Pauw equation which can be solved numerically for R_s:

$$\exp\left(-\frac{\pi R_A}{R_s}\right)+\exp\left(-\frac{\pi R_B}{R_s}\right)=1 \tag{4.3}$$

Then the bulk electrical resistivity ρ can be calculated using $\rho=R_s\times d$ where d is the thickness of the material. To obtain the two characteristic resistances, one applies a DC current I_{12} into contact 1 and out of contact 2 and measures the voltage V_{43} from contact 4 to contact 3 as shown in Figure 4-9. Reversing the polarity of the current

(I_{21}) allows measuring V_{34} and then this procedure is repeated to measure the six remaining currents and voltages (V_{41}, V_{14}, V_{12}, V_{21}, V_{23}, V_{32}). Because some measurements are redundant they allow consistency checks on measurement reproducibility, ohmic contact quality and sample uniformity. These eight voltages and current measurements yield eight values of resistance such as $R_{21,34} = V_{34}/I_{21}$. The sheet resistance can now be determined via the Van der Pauw equation (Equation 4.3) using the two characteristic resistances:

$$R_A = \frac{1}{4}\left(R_{21,43} + R_{12,34} + R_{34,12} + R_{43,21}\right) \tag{4.4}$$

and $$R_B = \frac{1}{4}\left(R_{23,41} + R_{32,14} + R_{41,23} + R_{14,32}\right) \tag{4.5}$$

In order to facilitate the measurements and to avoid confusion in wiring the eight different voltage-current couples, a unit box was built to allow switching between each one of the combinations by simply turning a knob and is pictured in Figure 4-10. This unit also allows two-point measurements between each of the four contacts to control the contact quality and to evaluate two-point resistance. Finally, this unit box is wired to support Hall effect measurements but as the technique has not been used in this work it will not be described here. Rapid processing of the experimental data was done using solvers and spreadsheets in Microsoft Excel.

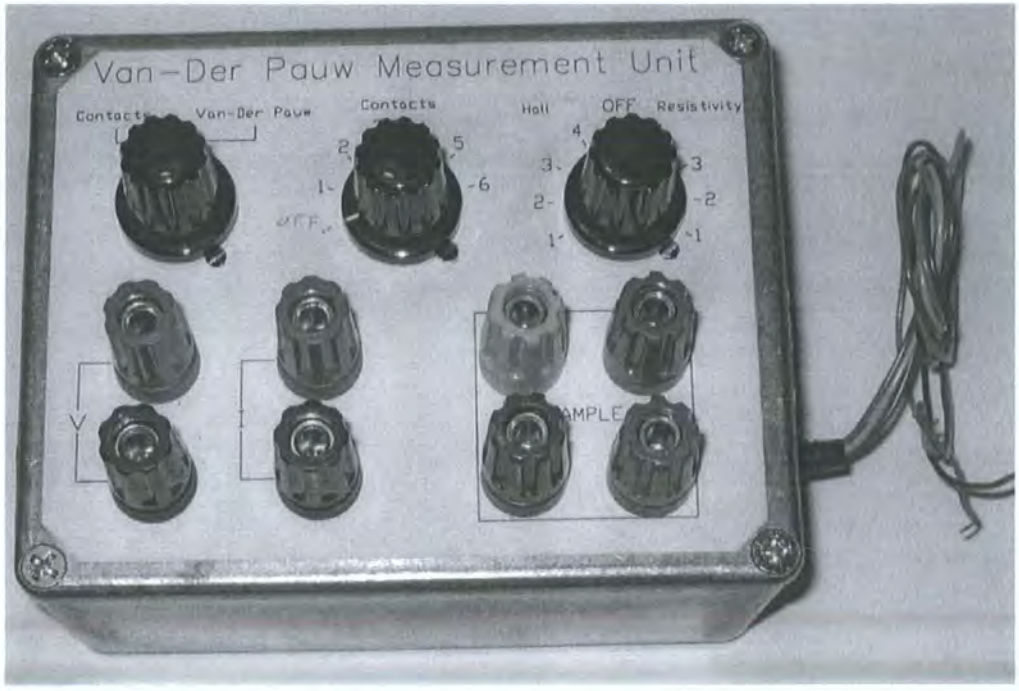

Figure 4-10 Van der Pauw and Hall effect measurement unit box.

4.6 Scanning Electron Microscopy

This section outlines the principles of the scanning electron microscope (SEM) and the different modes in which they have been used in this work.

Principles of the SEM The scanning electron microscope scans the surface of a specimen with an electron beam. When the electron beam hits the sample, the interaction between high energy primary electrons from the filament and the sample atoms generates a variety of signals. The effects are shown schematically in Figure 4-11.

Not all of these effects are necessarily significant enough to be detectable from a given sample. However, virtually all materials exhibit useful large primary and secondary electron emission currents as well as x-ray emissions [20]. During this work, the SEM investigation was performed on a JEOL JSM-IC848 used in two different modes as outlined next.

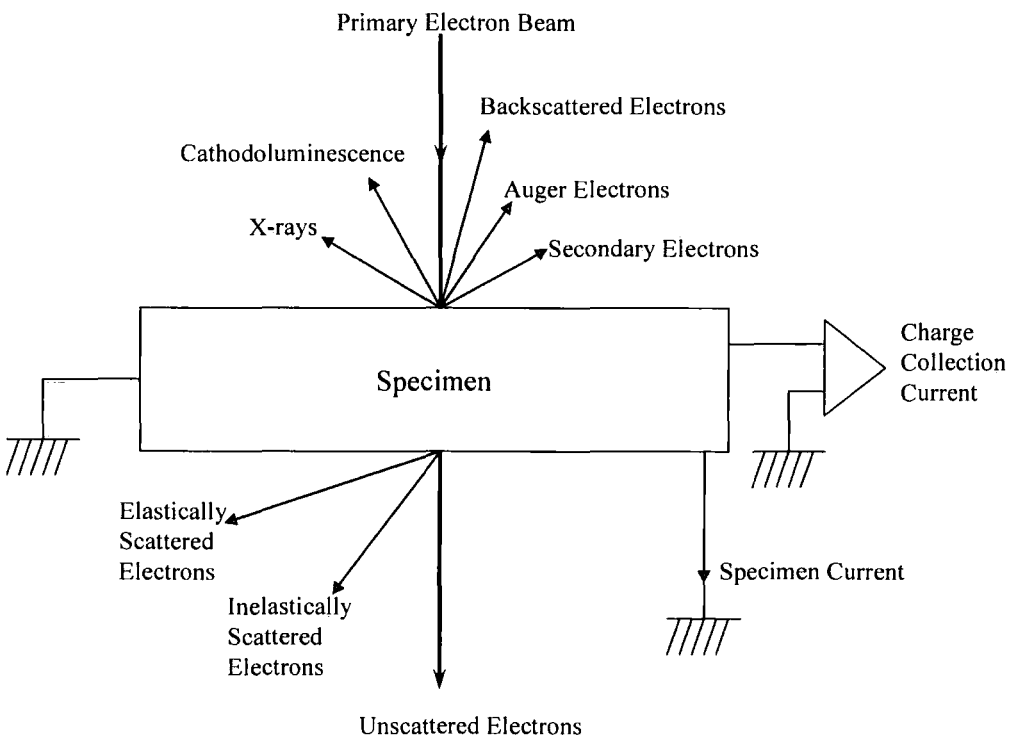

Figure 4-11 Schematic diagram of the types of interaction produced as a result of electron beam interaction with a solid material.

The secondary electron mode is the most common mode used for surface topology investigations. The incident electron can interact with the loosely bound conduction band electrons in the specimen. Only those electrons excited within a short distance of the surface have sufficient energy to leave the sample. Topographic contrast arises from shadowing of the line of sight to the detector by surface features.

In electron beam induced current (EBIC) mode, electrical connections are made to the specimen to be studied and the measured current is amplified and used for SEM display. Using EBIC, it is possible to observe electrical barrier contrast at *p-n* junctions, Schottky barriers or heterojunctions, and bulk contrast at, for instance, impurity growth striations or grain boundaries. The EBIC technique was used with two different configurations. The first one is in the planar geometry of the cell referred to as back-wall EBIC in which the electron beam irradiates the back surface of the cell. The second configuration used is when the beam irradiates the active region of the cell, i.e. the side that is illuminated under normal device operation. This configuration is referred to as plan view or front-wall EBIC. In order to allow the electron to penetrate the active region of the cell, the glass substrate must be removed prior to the EBIC experiment. This was achieved by mechanical polishing of the glass to reduce the thickness of the substrate to a few hundreds of nm, followed by a chemical etch using hydrofluoric acid (HF), the ITO acting as an etch stop layer [21].

The spatial resolution of an SEM depends on the mode used. It is determined by the electron-probe size, the size of the generation volume which is related to the electron beam penetration range in the material, and the minority carrier diffusion length. Spatial resolution is the highest in the secondary electron mode (30-50 Å). This is because the low energy secondary electrons can only escape from the material from less than 100 Å of the specimen surface and since the electron-probe size can be made much smaller than the size of the generation volume. In the other modes such as cathodoluminescence, x-ray and charge collection microscopy, the spatial resolution is on the order of 1 μm depending on the material and beam voltage.

4.7 X-Ray Diffraction

X-ray diffraction (XRD) is a well documented method for specimen characterisation [22, 23], and is one of the most important characterisation tools in solid state chemistry and materials science. X-rays are electromagnetic radiation with a wavelength ranging from 0.1 Å to 100 Å. This technique allows crystalline structures to be probed at the atomic level. X-ray diffraction has been in use for two main purposes, namely the fingerprint characterisation of crystalline materials and the determination of their structure. This includes the determination of the lattice parameter, the preferred orientation as well as the size of the grains in polycrystalline materials, and the deformation strain. It will be explained how these parameters are determined later in this section. Each crystalline material has its unique characteristic x-ray powder diffraction pattern which may be used as a fingerprint for its identification. Materials may be identified from diffraction patterns, using databases from the ICDD (International Centre for Diffraction Data). Using such references for known materials, x-ray crystallography provides rapid access to information about the lattice type, interatomic distances and angles between planes.

The diffraction condition is described by Bragg's law (Equation 4.6):

$$n\lambda = 2d_{hkl}\sin\theta \tag{4.6}$$

where λ is the x-rays' wavelength, θ the angle between the reflected beam and the diffracted plane, d_{hkl} the interatomic distance between *hkl* planes and n is the order of diffraction and is always assumed to be equal to 1. This is illustrated in Figure 4-12.

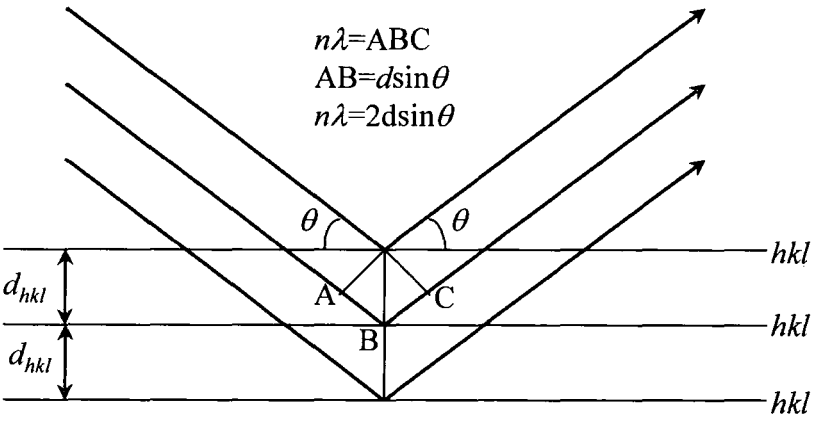

Figure 4-12 Diffraction of x-rays from atomic plane in a crystal.

Powder diffraction is the XRD method that was used in this work. It uses a monochromatic beam of x-rays and a polycrystalline specimen. If we consider part of the irradiated sample, every time the Bragg condition is fulfilled then the incident beam is reflected to the detector by the *hkl* planes. We then easily have access to the diffracted intensity (counts per second) as a function of the angular position of the detector. This principle was used in the θ-2θ (also called Bragg-Brentano) mode which is illustrated in Figure 4-13. The first aperture positioned in the incident path determines the irradiated zone on the specimen. The second aperture placed in the diffracted beam path, allows attenuation of the unwanted diffused radiation. Then a monochromatic radiation is obtained by filtering the Kβ line prior to detection.

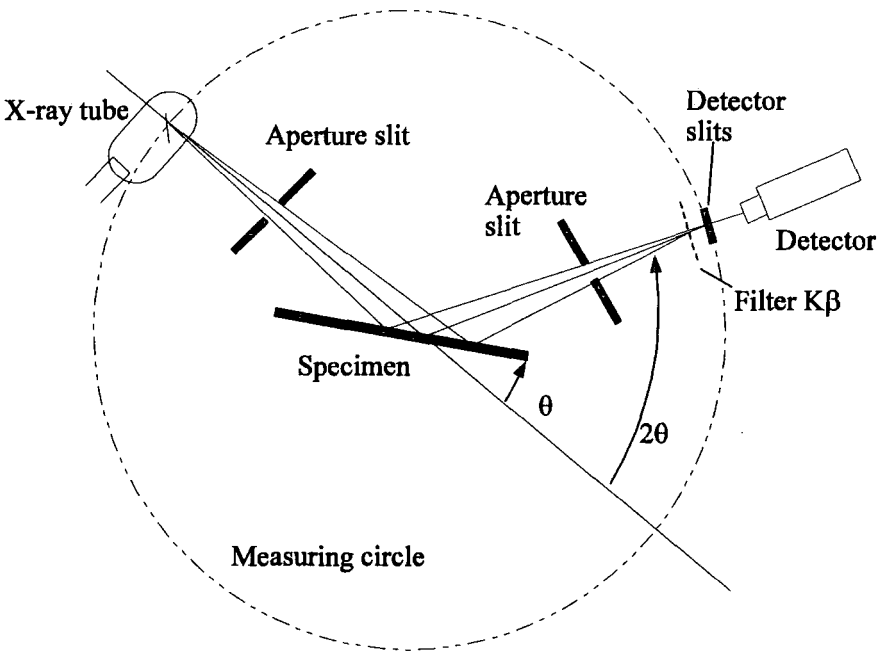

Figure 4-13 Schematic of an x-ray diffractometer in θ-2θ mode.

In this study two systems were used for XRD measurements, a Philips PW1800 and a Siemens D5000 diffractometers both using the Cu Kα (1.5406 Å) line. Typical wide angle scans from 20° to 135° at 0.02° step integrated for 4 seconds per step were taken using x-ray tube settings of 40 kV and 20 mA for most samples in order to carry out phase analysis.

4.7.1 Determination of the Lattice Parameter

This section describes the accurate determination of lattice spacing of a cubic structure such as that of CdTe with cell parameter a. This parameter can be determined using Bragg's law:

$$\lambda = 2d_{hkl} \sin\theta$$

$$\text{with } d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{4.7}$$

As a consequence it is possible to determine a for each reflection. The accuracy in determining a is essentially the accuracy with which θ and λ can be determined. Differentiating Bragg's law with respect to θ shows that the error in a is proportional to $cot\ \theta$. Therefore, the error in a, generated by a defined $\Delta\theta$ is smaller when a reflection at a higher 2θ angle is used.

Although there are different causes of systematic errors in determining a, the predominant one is displacement of the specimen from the diffractometer axis. This results in an error in the lattice spacing defined by:

$$\frac{\Delta a}{a} = -\frac{D}{R}\frac{\cos^2\theta}{\sin\theta} \tag{4.8}$$

where D is the horizontal displacement of the specimen from the diffractometer axis and R is the distance from the specimen to the detector. The procedure for an accurate determination of the lattice parameter a is as follows:

- Determine a for the different hkl planes with Equation 4.7.
- Plot the data as a function of $f(\theta) = (\cos^2\theta)/\sin\theta + (\cos^2\theta)/\theta$, function extrapolated by Taylor and Sinclair [24] and by Nelson and Riley [25].
- Linear extrapolation to $f(\theta) = 0$ gives a lattice spacing which takes account of the systematic errors from θ.

4.7.2 Grain Size and Deformation Strain

Information on grain size and strain is obtained from the shapes and positions of the diffraction peaks respectively. The strain within a crystal affects the d spacing and therefore the position of the diffraction peaks and the grain size has an effect of broadening the peaks.

The effect of grain size on the width of the diffraction peak is given by the Scherrer equation [22]:

$$\Delta_{size}(2\theta) = \frac{\kappa\lambda}{D\cos\theta} \tag{4.9}$$

where $\Delta_{size}(2\theta)$ is the width of the peak in radians, λ the wavelength, D the grain size, θ the Bragg angle and κ a constant approximately equal to unity depending both on the line shape profile of the peaks and the crystallite shape. It must be noted that the grain size determined by x-ray diffraction experiments is that perpendicular to the plane of the specimen.

The peak can also be broadened by micro-strains, ε, within the crystal or powder. These strains cause variations in the d spacing, Δd, and consequently cause a broadening of the diffraction peak. Differentiating Bragg's law yields:

$$\Delta_{strain}(2\theta) = 2\varepsilon\tan\theta \tag{4.10}$$

where $\Delta_{strain}(2\theta)$ is the width of the peak in radians due to strain.

If both strain and size effects occur within the sample, the width of the diffraction peak is the sum of equations 4.9 and 4.10 and by rearranging the equation:

$$\Delta_{total}(2\theta)\cos\theta = \frac{\kappa\lambda}{D} + 2\varepsilon\sin\theta \tag{4.11}$$

A plot of $\Delta_{total}(2\theta)\cos\theta$ against $\sin\theta$ allows the two broadening terms to be separated and measured and is referred to as a Williamson-Hall plot [26].

4.7.3 Crystallographic Orientation

The other major parameter that can be obtained from powder diffraction studies is the intensity of the individual peaks. The intensity can be affected by the non random orientation of the crystallites. The preferential orientation along a specific direction is termed "texture" and can give useful information about the sample itself. For this, the method of Harris is used [27] and the fraction of the crystals that have *hkl* plane normals lying parallel to the fibre axis, C_{hkl}, is defined by [27, 28]:

$$C_{hkl} = \frac{\frac{I_{hkl}}{I_{r,hkl}}}{\frac{1}{n}\sum_{n}\frac{I_{hkl}}{I_{r,hkl}}} \tag{4.12}$$

where n is the number of reflections, I_{hkl} the intensity of the hkl reflection and $I_{r,\,hkl}$ the intensity of the hkl reflection for a completely random sample. C_{hkl} is also referred to as texture coefficient.

The preferred orientation of each film, as a whole, was analysed from the standard deviation σ of all C_{hkl} values as compared with randomly oriented samples as:

$$\sigma = \sqrt{\sum \frac{1}{n}(C_{hkl} - 1)^2} \tag{4.13}$$

σ values are used to compare the degree of orientation between different samples, so that lower σ values indicate more randomly oriented samples.

4.8 Thickness Measurements

The thickness of the CdS and CdTe layers grown was estimated using *in situ* laser reflectometry. Exact measurement was done using a Tencor Instruments Alpha Step 200 step profiler. The equipment provides routine measurements of step heights less than 200Å and can identify discontinuities in the tens of Angstroms. It works by accurately monitoring the displacement of a stylus placed in contact with the sample as the specimen is scanned beneath it.

4.9 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is a widely used technique for analysis of trace element and compositional studies of solid materials, including thin films and semiconductors [29]. In this work, SIMS was applied to thin film CdTe doped with arsenic. The analyses were performed by MATS-UK using a 7 kV Cameca IMS with Cs^+ primary ions and a probe current of approximately 80 nA rastered over a 1 mm^2 area. The SIMS technique involves a focused ion beam, which sputters the surface region of the sample. The bombarding ion beam produces monoatomic and polyatomic particles of sample material, along with electrons and

photons. The secondary particles carry positive, negative and neutral charges, with kinetic energies that range from zero to several hundred eV. Neutral species are typically the most abundant of the secondary particles. Mass spectroscopy is applied to measure the mass to charge ratios of the emitted secondary ions. This provides the basis for compositional analysis. Monitoring the secondary ion count rate of selected elements as a function of time provides a depth profile of an elemental species within the sample. To convert this axis into a depth scale, a stylus profile meter is typically used to measure the sputter crater depth. The signal count is converted into concentration using standards.

This chapter gave an overview of the range of experimental methods used for this work. The next chapters will now present and discuss the results for studies on MOCVD CdTe-based grown materials, including doping studies by impurities incorporation and processing material for solar cells. The first study concerns the arsenic doping of CdTe thin films.

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Chapter 5

Doping Studies of CdTe:As on Sapphire Substrates

5.1 Introduction

In order to perform well a CdTe/CdS solar cell must undergo an *ex situ* post growth heat treatment in a chlorine environment. The effects of this treatment have been reviewed in section 3.4 and include among them a conversion type of the absorber layer from *n*- to *p*-type due to chlorine inclusion. The effects of this treatment are not fully understood and it is vital to investigate other possible routes for the activation of the CdTe/CdS structure.

It is possible to obtain *p*-type material grown by MOCVD in a Te-rich growth ambient, thus relying on intrinsic defects such as cadmium vacancies to produce the required conductivity type [1]. However, because only slight deviations from stoichiometry can occur, the carrier concentration remains relatively low. Another possible route is via acceptor doping, for example using arsenic. This has previously been applied to produce solar cells with limited efficiencies (1-2%) but without the use of a post-deposition annealing step [2]. However, efficient incorporation of the dopant species is of primary concern. The difficulty in doping *p*-type CdTe stems

from both strong compensation effects and the low solubility of the dopant species. A doping review of CdTe was previously detailed in section 3.6.

The results presented in this chapter aim at gaining a better understanding of the behaviour of the As dopant under various growth conditions, with a view to optimising the *p*-type conductivity and hence finding a route to improve the photovoltaic performances of the CdTe/CdS structure.

5.2 Description of the Samples Used in this Study

Thin layers of CdTe doped with arsenic were grown onto insulating sapphire by MOCVD. The MOCVD growth technique and apparatus have been described earlier in sections 3.3.1 and 4.2. The organometallic precursors were dimethylcadmium (DMCd), di-isopropyltelluride (DIPTe) and dimethylamino arsine (DMAAs). The concentrations of DMCd and DIPTe in the growth ambient were measured using an Epison ultrasonic monitor (see section 4.2). Dopant concentration was controlled by the flow of the carrier gas through the bubbler as the ultrasonic monitor equipment was not sensitive enough to measure the partial pressure of DMAAs in the growth mixture. This is due to the small flow of the dopant gas varied between 0-9 sccm (standard cubic centimetre per minute) at a bubbler temperature of 20°C in a total gas flow of 3355 sccm.

As mentioned above the CdTe layers were grown onto insulating c-plane sapphire. Sapphire was chosen since (i) it is an insulator and allows the resistivity of the CdTe layers to be unambiguously checked and (ii) it is chemically stable to the growth of CdTe upon it. Sapphire is composed of hexagonal close packed (HCP) planes of oxygen intercalated with HCP planes of aluminium. The aluminium planes have vacancies on one third of the sites so that each aluminium atom is surrounded by six oxygen atoms, and each oxygen atom is surrounded by four aluminium atoms. The lattice mismatch between CdTe and sapphire is large, > 10%. Despite this large mismatch, epitaxial growth of CdTe in the [111] direction on the sapphire basal plane can be achieved [3]. However, because of interface strain relaxation, CdTe layers grown by MOVPE are affected by a rough surface whose microrelief features depend on several parameters like growth conditions, layer thickness, substrate

nature or substrate orientation. The surface roughness usually exceeds 1-2 μm for 5-15 μm thick MOVPE-grown CdTe layers on sapphire substrate at relatively low temperature (300-400°C) [4]. Nevertheless sapphire was utilised because of its high temperature stability and its availability at low price in wafers of good quality.

For this study the variable parameters are the growth temperature, the dopant flow and the VI/II ratio, which is the ratio of the tellurium and cadmium partial pressures in the growth ambient.

Table 5-1 lists the samples grown and the growth parameters used. The temperature was varied between 320 and 400°C whilst varying the VI/II ratio from 0.59 to 2.4 and the DMAAs dopant line flow from 0 to 9 sccm. Samples were grown on wafers of 5 cm diameter and then cleaved into pieces of ~2 cm^2. Gold contacts were evaporated at the periphery of the sample using a mask for electrical measurements. The thickness of the layers grown was monitored during growth by laser interferometry and measured *ex situ* using the Alpha Step. This was not intentionally varied during growth.

Table 5-1 also summarises the electrical properties (conductivity type, resistivity and arsenic concentration) and structural properties (degree of preferred orientation, texture coefficient, lattice parameter and grain size) obtained for the layers investigated.

The conductivity type of each sample was verified using either the thermoelectric probe or the rectification method (see section 4.5.1). Resistivity measurements were performed under dark and AM1.5 illumination conditions using the Van der Pauw technique as explained in section 4.5.2. The structural properties of the thin CdTe:As layers grown were investigated using x-ray diffraction (XRD) in a Philips PW800 diffractometer using the Cu Kα (1.5406 Å) line. Peak determination was performed using Topas Software from Bruker AXS [5]. The arsenic concentration in the layers was determined by SIMS using a Cameca IMS with 7 kV and 80 nA Cs^+ primary ions rastered over a 1 mm^2 area. Finally, atomic force microscopy (AFM) was performed on selected specimens using a Digital Instrument Nanoscope IV in order to reveal the surface morphology of the layers.

Table 5-1 Summary of the growth parameters and the results for the CdTe films doped with As. (X) indicates that the measurement was not possible and (-) indicates that the measurement was not performed. Sheet resistance and resistivity were measured under AM 1.5 illumination.

Sample Number	33	34	36	40	41	42	43	44	47	49	63	64	67
Growth T (°C)	320	320	320	350	350	400	400	400	400	400	400	400	400
VI/II ratio	2.4	2.4	2.4	0.59	0.95	1.0	0.6	0.9	1.2	1.7	0.95	0.73	1.2
DMAAs flow (sccm)	9	3	6	9	9	0	9	9	9	9	9	9	9
Thickness (μm)	3.0	1.8	2.1	2.1	2.3	1.6	1.7	1.3	1.4	1.5	1.3	1.2	1.6
Conductivity type	*p*	*p*	*p*	*p*	*p*	*n*	*p*	*p*	*p*	*p*	*p*	*p*	*p*
[As] by SIMS ($at.cm^{-3}$)	-	-	-	2×10^{19}	-	5×10^{16}	6×10^{18}	4×10^{18}	-	-	2×10^{18}	2×10^{19}	1×10^{18}
Sheet resistance ($\times10^3$ kΩ.□)	X	X	X	51	X	205	5.6	3.8	1.3	3.1	1.9	89	X
Resistivity (kΩ.cm)	X	X	X	10.9	X	34.0	0.78	0.48	0.17	0.47	0.24	11.0	X
Degree of orientation σ	0.3	0.6	0.4	1.7	-	2.7	1.7	1.0	2.7	-	2.7	1.7	2.2
Texture coefficient C_{111}	0.7	0.9	0.7	4.0	-	7.0	4.0	2.0	7.0	-	7.0	5.2	6.5
Grain size (nm)	49	62	47	56	-	48	72	67	58	-	67	51	65
Lattice parameter (Å)	6.4831	6.4841	6.4816	6.4832	-	6.4820	6.4833	6.4836	-	-	6.4857	6.4854	6.4851

5.3 General Effects of Growth Temperature

In this section the effects of the growth temperature on the structural and electrical properties of the CdTe:As layers are described. Since the layers grown at the highest temperature investigated (400°C) showed the highest *p*-type conductivity they were investigated in more detail and a full description of them is deferred until section 5.4.

5.3.1 On Electrical Properties

Three Te-rich (VI/II = 2.4) CdTe samples were grown at 320°C, with dopant flows of 3, 6 and 9 sccm respectively. These *p*-type samples proved to be too resistive to be measured using the Van der Pauw technique, i.e. the resistance between two contacts was greater than 200×10^6 Ω. When the growth temperature was increased to 350°C, with high As concentration (bubbler flow of 9 sccm) the conductivity was measurable under AM1.5 conditions for a VI/II ratio of 0.6 (i.e. Cd-rich) but not for a ratio of 0.95. The lateral resistivity was relatively high at around 10.9 kΩ.cm. At a growth temperature of 400°C the resistivity was measurable for a range of VI/II ratios and dopant flows as can be seen in Table 5-1.

For undoped material, *p*-type conductivity occurs in samples grown in a Te-rich ambient (i.e. a VI/II ratio > 1) since the intrinsic defects which give rise to conductivity of this type are cadmium vacancies and act as acceptor species for CdTe [6]. However, in the case of Cd-rich growth with As, the Cd-rich growth ambient is thought to promote *p*-type conductivity via encouraging the occupation of Te sites by the As dopant. For the layers grown at 320°C in a Te-rich ambient it may only be concluded that the carrier concentration and/or mobility are very low, too low to allow successful measurements. For a growth temperature of 350°C the results are consistent with the fact that for solar cells doped with arsenic grown at 350°C, efficiency was optimised by using a Cd-rich growth ambient [2]. Increasing the growth temperature to 400°C allowed measurement on a variety of samples grown with different VI/II ratios.

SIMS analysis indicated that the actual chemical concentration of As in the layer grown at 350°C was higher than in the one grown at 400°C (for the same VI/II ratio and As flow), i.e. 2×10^{19} at.cm^{-3} compared with 6×10^{18} at.cm^{-3} (see Table 5-1). However, the resistivity was also higher, 10.9 kΩ.cm compared to 0.78 kΩ.cm. This may be understood in terms of the increased presence of more compensating defects such as $[V_{Te}]^{2+}$ or $[Cd_i]^{2+}$ in the lower temperature material, resulting in a reduced concentration of active carriers [7]. An increase in adsorption of As species onto Cd species was also observed by Capper *et al.* when the growth temperature was lowered [8]. In addition, lowering the growth temperature had the effect of reducing the effective Te/Cd atomic ratio at the growing surface because the pyrolytic efficiency of DIPTe is significantly reduced below 400°C [9], whereas that of DMCd is less affected. This is because the decomposition temperature of DIPTe is 320°C compared to 150°C for DMCd. This decrease in the Te/Cd atomic ratio enhances the arsenic incorporation onto Te species.

5.3.2 On Crystal Structure

Figure 5-1 shows the XRD data for representative samples grown at 320 and 400°C where the intensity (in square root unit) is plotted against the position of the detector in 2θ angle. All samples showed peaks corresponding to the cubic structure of CdTe and also to the substrate. Reflections from oxides such as TeO_2 and $CdTeO_3$ were also observed in some cases.

The experimental data were analysed using the values of texture coefficients C_{hkl} for each CdTe peak in the XRD pattern and the degree of preferred orientation σ (as described in section 4.7.3). Note that the peaks corresponding to the (333) and (511) reflections have been excluded in the analysis due to their overlapping in the XRD pattern - it is not possible to obtain values of intensity for each of these peaks individually. The results are included in Table 5-1. For the sample grown at 320°C the σ values ranged between 0.3 and 0.6 and for samples grown at higher temperature they ranged from 1.4 to 2.7. This indicates that a lower growth temperature will produce samples that are more randomly oriented compared to those grown at higher temperature. The spread of σ values for samples grown at 400°C is due to the variation of the VI/II ratio.

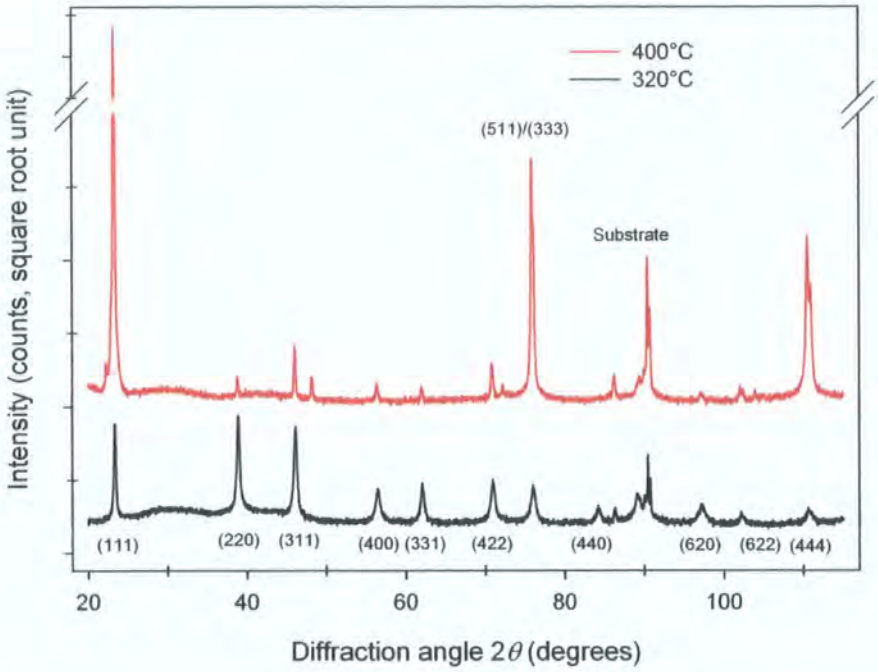


Figure 5-1 X-ray diffraction scans of two characteristic samples grown at 320°C (black line) and 400°C (red line).

This was also confirmed by the variation in C_{111} values, as for the samples grown at 320°C lower values of texture coefficients were determined compared to those for samples grown at 350-400°C (see Table 5-1). Both σ and C_{111} values indicate that the samples grown at 320°C are almost randomly oriented, while some samples grown at 400°C are completely textured in the [111] direction. From our measurements it was not possible to determine the position of the temperature threshold above which the samples become [111] oriented with great precision, but was estimated to be around 350°C depending on the ratio of the organometallics used.

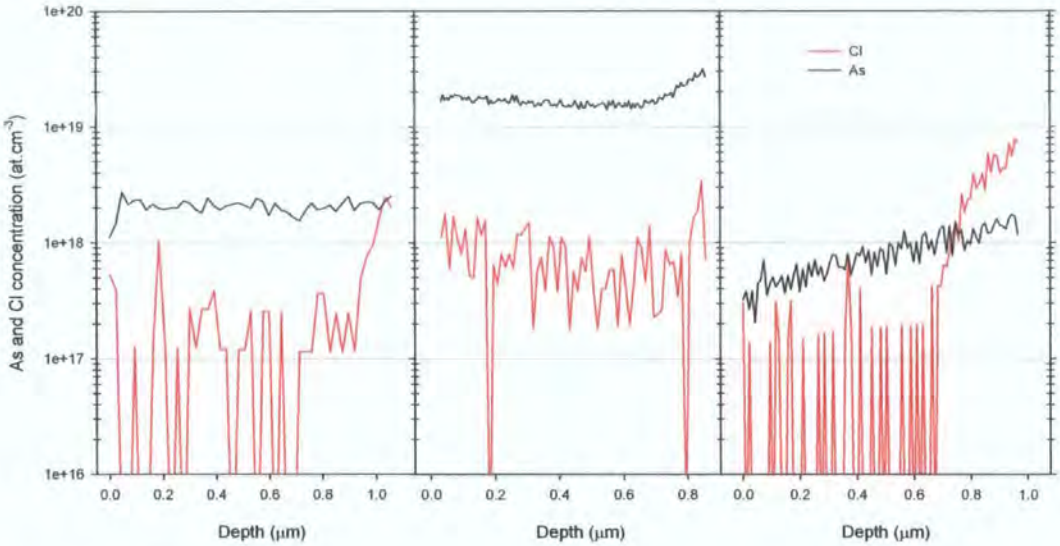
5.4 Effect of VI/II Ratio and Dopant Incorporation on the Properties of Layers Grown at 400°C

The results for the samples grown at 400°C with an arsenic precursor gas flow of 9 sccm are now described in detail. All the films grown, regardless of the

growth temperature, were found to be of *p*-type conductivity except the undoped sample (42) which was found to be *n*-type. This confirms that MOCVD-CdTe films grown in a stoichiometric growth ambient are of *n*-type conductivity. When possible, resistivity measurements were also performed in the dark. Strong photoconductivity of the material was observed as the dark resistivity was found to be two orders of magnitude higher compared to light resistivity.

Depth profiles of arsenic and chlorine content were recorded by SIMS measurements. Arsenic calibration was done using implanted CdTe material and for chlorine only a CdS reference sample was available, so the chlorine level in CdTe is only known approximately. Profiles for samples number 63, 64 and 67 are shown in Figure 5-2. The profiles stop at the point where the sapphire substrate became visible. A uniform concentration in arsenic is observed throughout the CdTe films for sample 63 and 64. This is also true for the other samples analysed but not shown here, i.e. specimen number 43 and 44. This was not the case for sample 67, as a constant increase in concentration is observed over the entire layer increasing from 3×10^{17} to 1.5×10^{18} at.cm^{-3} in 1 μm. No explanation for this is known but it is suspected that a change in the dopant flow is the cause of this variation. The SIMS profiles show the great advantage of MOCVD for controlling the dopant concentration within the layer. By comparison, the ion implantation technique can only form an extremely thin *p*-doped layer at the surface [10].

For most samples, very noisy chlorine SIMS signal can be noticed and this marks the background level of the detection. This is confirmed by the fact that no chlorine species were used during growth. However for sample 67, a background level is recorded for the first ~600 nm but then there is a strong increase in chlorine concentration near the interface with the substrate. This strong offset is due to memory effects in the pipework and originates from the previous growth run (not part of this work) which involved chlorine doping.



Sample 63 Sample 64 Sample 67

Figure 5-2 Sims depth profile for sample 63, 64 and 67 showing the total concentration of As (black line) and Cl (red line) in the sample as a function of depth.

Figure 5-3 a) shows a plot of the lateral resistivity of the polycrystalline CdTe films against the VI/II ratio of the organometallics in the growth ambient. It must be noted that the lateral resistivity measured may be different from the resistivity in the thickness direction due to grain boundary effects. This is particularly true in high resistivity films, since the potential barrier across the grain boundaries contributes to the resistivity measured by the Van der Pauw technique, and this contribution decreases with increasing carrier concentration in the film. At sufficiently high carrier concentrations, the potential barrier at grain boundaries becomes negligible, and the Van der Pauw measurements provide the average resistivity of the grains. On the other hand, the resistivity measured in the thickness direction of the film potentially consists of contributions from the columnar arrangement of the grains and grain boundaries. Their relative importance depends on the carrier concentration in the grains and the chemical and structural properties of the grain boundary.

Figure 5-3 a) shows that as the DMCd partial pressure in the precursor mixture is reduced, i.e. VI/II ratio increased, the resistivity of the film first increases up to 10^4 Ω.cm for a VI/II ratio of 0.7. At higher tellurium to cadmium ratios the resistivity decreases owing to the increase in cadmium vacancy concentration and reaches a minimum of ~200 Ω.cm for a VI/II ratio of ~1.1. As the cadmium partial

pressure in the growth ambient is further reduced, the resistivity increases presumably owing to defect complexes and/or self-compensation.

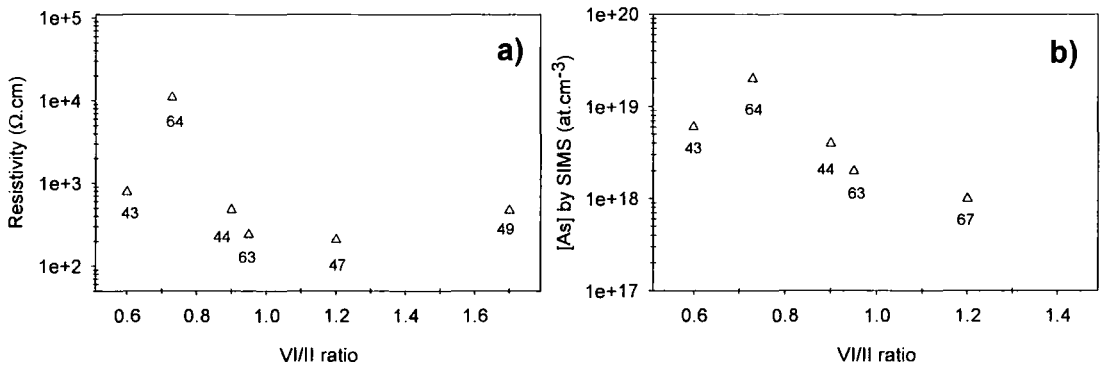


Figure 5-3 a) Lateral resistivity and b) arsenic concentration as a function of VI/II ratio in the growth ambient, for samples grown at 400°C, with constant As precursor flow rate of 9 sccm. Sample numbers used in Table 5-1 are marked for each point.

The same data distribution is observed between the actual arsenic incorporation in the CdTe films measured by SIMS and the organometallic ratio. Arsenic incorporation does appear to be affected to some extent by VI/II ratio in the growth ambient. Figure 5-3 b) shows this relationship for five samples all of which were grown with a DMAAs flow of 9 sccm. An increase in arsenic concentration can be seen as the VI/II ratio decreases, up to an apparent maximum arsenic concentration at VI/II~0.7, which correspond to a Cd-rich growth. Insufficient data is available at the low VI/II ratios to draw any conclusions about a possible optimum VI/II ratio for arsenic incorporation. However, Ghandhi *et al.* [10] also reported higher arsenic incorporation at a VI/II ratio of 0.6 than at a ratio of 1 and Taskar *et al.* [11] observed higher As incorporation for lower tellurium to cadmium ratios. If it is assumed that the arsenic incorporation is dependent upon the VI/II ratio as shown in Figure 5-3 b), then the high resistivity of sample 64 can be explained by the high incorporation of the dopant species. The maximum uncompensated acceptor doping concentration using As in CdTe grown by liquid phase epitaxy is ~2.8×10^{18} at.cm^{-3} [12]. Above this threshold strong self-compensation occurs in the case of a cadmium rich growth with $[V_{Te}]^{2+}$ but also with $[Cd_i]^{2+}$.

Sample 67 (VI/II = 1.2), included in Figure 5-3 b), was not included in Figure 5-3 a) due to the high chlorine concentration measured in this particular film. For growth under certain conditions, chlorine is known to play a role in creating highly resistive CdTe material due to the formation of [Te_i-$2Cl_{Te}$] and [V_{Cd}-$2Cl_{Te}$] complexes [13, 14], and indeed the resistivity of this particular sample was much higher than expected. It was too resistive to be measured with the setup used. However, it is unlikely that the chlorine content would have affected the arsenic concentration significantly, so the inclusion of this sample in Figure 5-3 b) is believed to be valid. Sample 42, on the other hand, is not included in Figure 5-3 a) and b) as this sample was not intentionally doped and is *n*-type.

As expected, arsenic incorporation is enhanced for tellurium deficient growth conditions because of the decrease of the surface coverage rate of Te species over Cd species at the growing surface. This offers more opportunities for As species to bond to Cd species, which would lead to an increase in effective As incorporation onto Te sites. However, in the present case this explanation may be over-simplistic since the dopant incorporation is expected to be influenced by grain boundaries and other structural defects.

A correlation was found between the actual arsenic incorporation measured by SIMS and the resistivity of the films for samples grown at 400°C with the same dopant flow of 9 sccm. This is shown in Figure 5-4 where the resistivity decreases with decreasing arsenic content, down to ~1×10^{18} at.cm^{-3}. Note that in Figure 5-4, sample 42 was nominally undoped. The assigned arsenic concentration for this particular sample is close to the SIMS background signal of around 5×10^{16} at.cm^{-3}. Furthermore, sample 67 was also disregarded in this plot due to the high chlorine content present in the layer. This means that the arsenic content in the films which depends on the tellurium and cadmium partial pressures in the growth ambient is not electrically active at high concentration.

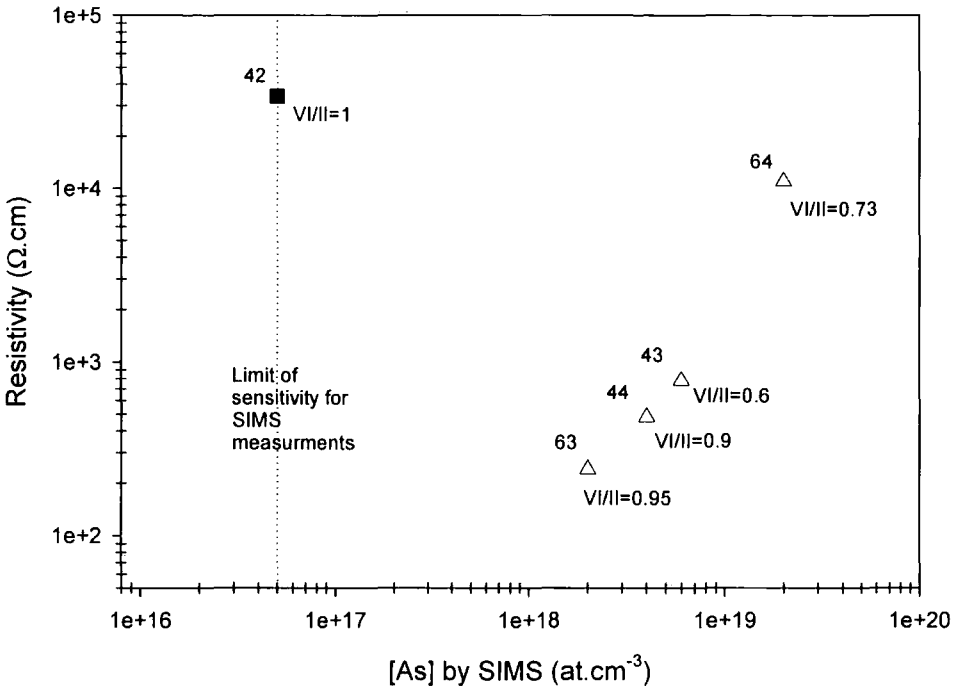


Figure 5-4 Lateral resistivity (Van der Pauw) as a function of arsenic concentration as measured by SIMS for samples grown at 400°C. Sample number and VI/II ratio in the growth ambient are marked for each data point. The ■ marker indicates undoped layer and △ markers indicate doped layers.

5.5 Structural Analysis

Figure 5-5 a) shows the variations of the lattice parameter (obtained from Nelson-Riley plots, see section 4.7.1) as a function of the VI/II ratio. Only data points corresponding to samples grown at 400°C with an As gas flow of 9 sccm are plotted. For the samples measured, lattice parameter values fall between 6.4833 and 6.4857 Å, which is larger than the value for a randomly oriented powder sample (6.481 Å). The lattice parameter of the undoped sample grown in a stoichiometric ambient is 6.4820 Å. This suggests that the film is submitted to a compressive stress in the plane parallel to the substrate surface. This stress is caused by a lattice mismatch and difference in thermal expansion coefficients between CdTe and the sapphire substrate. No trend is observed in Figure 5-5 a) between the lattice parameter and the gas phase VI/II ratio. This might be explained by the fact that the VI/II ratio is not the only parameter affecting the lattice spacing and that the arsenic incorporation would probably affect the interatomic distance. This is shown in Figure

5-5 b) where the lattice parameter is plotted against the arsenic concentration measured by SIMS. No definite trend can be seen but the lattice parameter has a tendency to increase with arsenic incorporation.

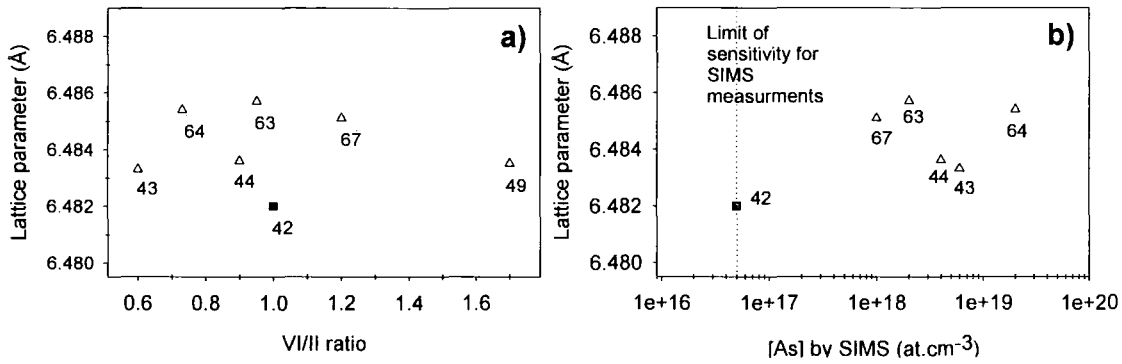


Figure 5-5 Lattice parameter for samples grown at 400°C as a function of a) the VI/II ratio in the growth ambient and b) As concentration measured by SIMS. Sample number is marked for each point. The ■ marker indicates undoped layers and △ markers indicate doped layers.

The smallest lattice spacing value was measured for the undoped sample, grown in a stoichiometric ambient and indicates a possible influence of impurity incorporation. For example, sample 67 has a high content of chlorine which atomic radius (189 pm) is larger than the ones of Cd (151 pm) and Te (142 pm), so its incorporation will increase the lattice parameter of the structure. Indeed this sample has one of the largest lattice parameter values measured. This sample and the other doped samples have a high concentration in arsenic throughout the layers and this will introduce more compressive stress yielding a larger lattice parameter.

The preferred orientation of the layers was discussed in section 5.3.2 with respect to the growth temperature. The samples grown at temperatures in the range 350-400°C had a [111] preferred orientation, some samples being nearly completely [111] oriented. This could be attributed to the substrate which provided sites of low energy and also provided a reference plane during the growth of the CdTe film. At lower growth temperature, the films had almost no texture, i.e. were almost randomly oriented.

Grain sizes were also determined from the XRD data o using the Williamson-Hall method and Scherrer's equation (see section 4.7.3). Note that the data was not corrected to take into account the instrument broadening as it was considered to be negligible compared to strain and size effects. Some Williamson-Hall plots examples are shown in Figure 5-6 for samples 42, 44, 63, 64 and 67. The slope of each graph indicates the strain in the film and the intercept with the ordinate axis yields the crystallite size. A great scatter in the plots can be seen and this is characteristic of the Williamson-Hall plots. Moreover, due to the highly oriented film structure, some plots have limited number of data points as seen in Figure 5-6 b).

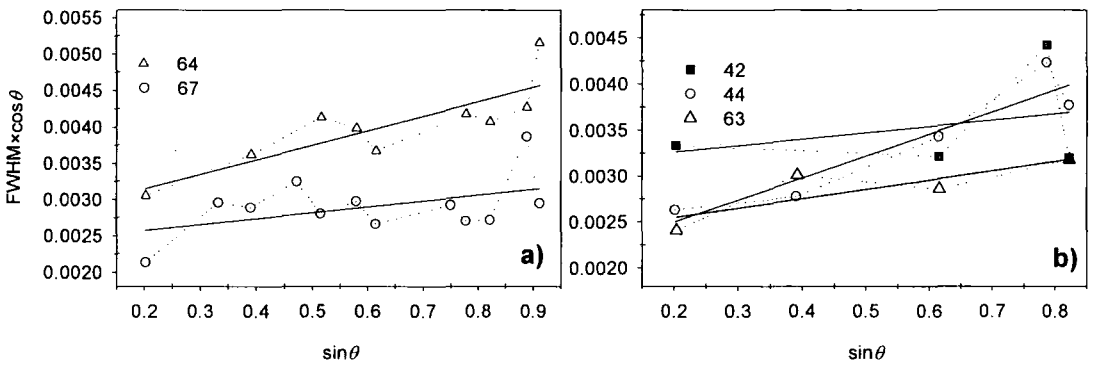
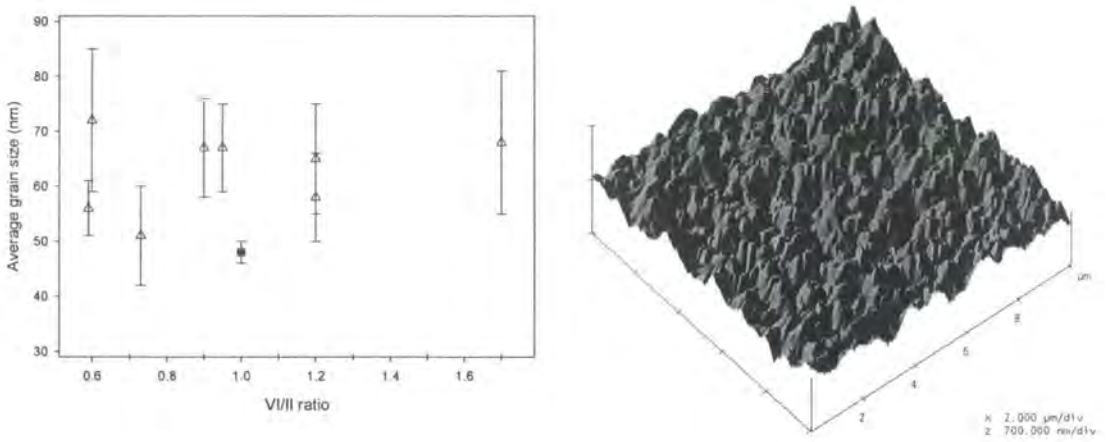


Figure 5-6 Williamson-Hall plots for samples grown at 400°C with different growth ambient (VI/II ratio).The total broadening of the peak due to strain and size is measured as the full width at half maximum (FWHM). a) Samples 64 and 67 and b) samples 42, 44 and 63.

The crystallite sizes were also extracted from the XRD data using Scherrer's equation applied to the (111) peak. This is the most widely used technique for grain size determination from XRD analysis when neglecting micro-strain effects. It must be reminded that grain size values quoted from XRD measurements are in the direction perpendicular to the reflected plane. The crystallite sizes for the range of samples grown at 400°C are plotted in Figure 5-7 a) as a function of the VI/II ratio. The data points represent the mean values for each sample extracted using both techniques. The error is given by the standard deviation between the two measurements. No influence of the tellurium and cadmium partial pressures is observed, and also the arsenic incorporation seems to have no effect.



a) b)

Figure 5-7 a) Variation of calculated grain sizes with VI/II ratio in the growth ambient for samples grown at 400°C and b) AFM micrograph of sample 64 revealing hillock structure. The ■ marker indicates undoped layers and △ markers indicate doped layers.

However it can be noted that the absolute grain sizes are very small ranging from ~45 to ~75 nm. The MOCVD growth technique is know for growing small grained polycrystalline structures by comparison with films grown by PVD (400 nm at 250°C) and films grown by CSS (2-10 μm at 600°C) [15]. This small grain structure was confirmed by the SEM images that revealed morphological details smaller than 100 nm and AFM images revealed hillock structured surface as seen in Figure 5-7 b). Although the grain sizes measured are fundamentally different -SEM and AFM give grain size indications in the plane of the substrate while XRD informs on grain sizes in the plane perpendicular to the substrate- comparison between the three measurements give information on the grain development in both directions.

5.6 Discussion

It is important at this point to recall that the conductivity of a semiconductor, σ_i, is given by:

$$\sigma_i = \frac{1}{\rho} = q(n\mu_n + p\mu_p) \tag{5-1}$$

where ρ is the resistivity, q the electron charge, n and p the concentrations of electrons and holes, respectively, and μ_n and μ_p their mobilities. Therefore high conductivity is achieved for higher carrier concentrations and mobilities.

Prior to discussing the doping mechanism in MOCVD-grown thin film CdTe, the understanding of CdTe growth kinetics is essential. Among several growth parameters, the growth temperature and the flow rates of organometallics are considered to have the greatest influence on the growth kinetics. It has been observed that (i) the growth rate increases with the VI/II ratio and saturates for ratios greater than 1 [16, 17] and that (ii) the growth rate also increases with the substrate temperature [17, 18]. Theses dependences of the growth rate show that the growth is dominated by the surface kinetically controlled reactions, the so-called Lambmuir-Hinshelwood type growth [19]. The effect of temperature is attributed to an enhancement in the Te/Cd atomic ratio at the growing surface, because the pyrolysis of DIPTe is significantly increased above 320°C whereas that of DMCd is less affected [20].

In the present study, higher As incorporation was achieved when the growth temperature was lowered: 2×10^{19} at.cm^{-3} at 350°C compared to 6×10^{18} at.cm^{-3} at 400°C for a VI/II = 0.6. Lowering the growth temperature is considered effective in increasing the adsorption of As species onto Cd species because of the reduced Te/Cd atomic ratio at the growing surface at lower substrate temperature. Lowering the VI/II ratio has an effect on the decrease of the surface coverage rate of Te species over Cd species at the growing surface. This offers more opportunities for As species to stick on Cd species, which would lead to an effective incorporation of As into Te sites. This was shown in Figure 5-3 b) where increased As concentration was measured when the VI/II ratio was lowered from 1 to 0.7. This suggests that the As incorporation is not dominated by the pyrolytic efficiency of the dopant species but by the sticking efficiency of the dopant species. However, the increased As incorporation increased the lateral resistivity of the CdTe films yielding ineffective doping.

It has been suggested by some authors that the solubility limit of As in epitaxial CdTe film grown by MOVPE is around ~2×10^{17} at.cm^{-3} [10, 21, 22], when using arsine as the dopant species. For the samples presented in Figure 5-3 the

measured As concentration is higher than the limit suggested above and it is thought that above this limit the conductivity in the films is governed by intrinsic defects. The film resistivity was shown to increase for decreasing VI/II ratios owing to the increased concentration of cadmium vacancies. Although cadmium vacancies act as acceptors, the increased resistivity is thought to be due to the formation of complexes such as [V_{Cd}-As_{Te}] but could also be due to the incorporation of As into Cd sites acting as compensating donors [10].

Preliminary Hall measurements performed at room temperature and light conditions on sample 47 (ρ = 0.17 kΩ.cm under AM 1.5 illumination) revealed a low carrier concentration of ~10^{14} cm^{-3} and a hole mobility of 62 $cm^2.V^{-1}.s^{-1}$. Other authors [21, 22] have measured such hole concentrations for As doped epitaxial CdTe films and concluded that thermal anneals were necessary to activate the As acceptors. Indeed hole carrier concentration could be increased to ~2×10^{17} cm^{-3} after a heat treatment at 500°C. However, because the As has been incorporated in such high concentrations (2×10^{18}-2×10^{19} cm^{-3}) part of it must be incorporated in the form of precipitates or at grain boundaries due to the polycrystalline nature of the films. The effect of grain boundaries on the conductivity is now exposed. Because the solubility of As in CdTe is low, it is suggested that most of the As is incorporated at grain boundaries. If it is assumed that for all samples grown the density of grain boundaries is of a similar order of magnitude, then this would explain the fact that increasing arsenic incorporation yielded more resistive films because the incorporated As is located at grain boundaries.

It is known that grain boundaries influence the electrical behaviour of polycrystalline semiconductor by favouring recombination at grain boundaries and limiting current transport through potential barriers and hence influencing grain boundaries diffusion, segregation and compensation effects [23]. Thorpe *et al.* [24] and Gilmore *et al.* [25] showed that the resistances associated with grain boundaries are 3-5 orders of magnitude larger than that of the bulk material, and that the potential barrier present at the grain boundary decreases with increasing light intensity. This explains the differences between light and dark resistivity measurements described earlier, the mobility of the carriers being limited by the increased barrier in dark conditions. A reduced density of states in polycrystalline *p*-

CdTe compared to bulk CdTe [24] and a high density of grain boundary trapping states (~10^{19} cm^{-3}) [26] induce a reduced mobility and hence the conductivity in polycrystalline films. The carrier mobility in the polycrystalline layer is dominated by the potential barriers associated with grain boundaries and thus controls the resistivity of the films. In this case the conductivity does not depend linearly on the carrier density; the influence of carrier density is manifested most strongly through its effect on barrier height. The resistivity in the parallel direction of the film such as measured by the Van der Pauw technique is thus strongly affected by the grain boundaries whereas the transverse resistivity is less affected. However the mobility in *p*-CdTe usually decreases with increasing carrier concentration yielding higher conductivity [27] and therefore in the study presented here the conductivity is limited by the low active carrier concentration.

5.7 Conclusion

The resistivity of arsenic doped CdTe thin films is dependent on growth temperature and upon arsenic incorporation. For a growth temperature of 400°C, arsenic incorporation is affected not only by the proportion of arsenic precursor in the gas flow, but also by the VI/II precursor ratio. This offers two potential means of controlling the resistivity. A uniform incorporation of the dopant species throughout the layer was confirmed by SIMS showing the advantages of the *in situ* doping. For this growth temperature there appears to be a minimum in the resistivity (200 Ω.cm) at a total arsenic concentration of ~2×10^{18} at.cm^{-3}.

Structural analysis of the layers showed that higher growth temperature favours the [111] preferred orientation. The growth of CdTe films onto sapphire substrates is characterised by a lattice under compressive stress and a small grained structure (~70 nm) with dopant incorporation having almost no effect on the structural properties of the specimens.

Furthermore the incorporated arsenic seemed to be not wholly electrically active. While there was a relationship between conductivity and As incorporation, it was not possible to achieve high *p*-type conductivity in CdTe using the MOCVD conditions investigated in this work. Indeed the samples were generally very resistive. These findings caused a major change of direction in the work presented in

this thesis. It was decided to investigate the more widely used $CdCl_2$ post-growth treatment. This has rarely been investigated as a route to making cells from MOCVD-grown CdTe/CdS structures and offers a potential high-purity route to cell production. The remainder of this thesis describes the work on this topic.

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Chapter 6

Influence of the Post-Growth Treatment on the Absorber Layer Microstructure

6.1 Introduction

One of the key steps in optimising the photovoltaic performance of CdTe/CdS solar cells is the post-deposition heat treatment of the structure. There are reports regarding the effects of the post-deposition heat treatments on the structural changes of CdTe thin films and their influence on the cell performance [1-6]. It is known that the annealing in O_2 (air) or $CdCl_2$ containing environments have a significant impact on morphology of the films, promoting grain growth or sometimes reconstructing grains and reducing internal stress – depending on the growth deposition technique (see section 3.3). It has also been observed that the recrystallisation process influences the preferred orientation of the crystallites. This chapter reports the investigation into the post-deposition heat treatment conditions on

the morphology and microstructure of thick absorber layers (8-13 μm) of CdTe/CdS solar cell structures grown by MOCVD.

6.2 Description of the Samples Used in this Study

CdTe/CdS solar cell structures were grown by MOCVD on ITO/glass substrates supplied by Merck Display Technology. The MOCVD technique was described earlier in section 4.2 and details on the ITO/glass substrates can be found in section 4.2. Substrates were cleaved into 35×50 mm pieces and cleaned using the process described in [7] prior to growth. The structures were grown in an original manner which consisted of three substrates placed along the graphite susceptor block instead of the usual single substrate. The arrangement of this is shown in Figure 6-1. Three positions are defined: the *inlet*, *centre* and *outlet* positions with reference to the entry and exhaust sides of the reactor tube. The centre position has a facility for sample rotation that was not used in this part of the work.

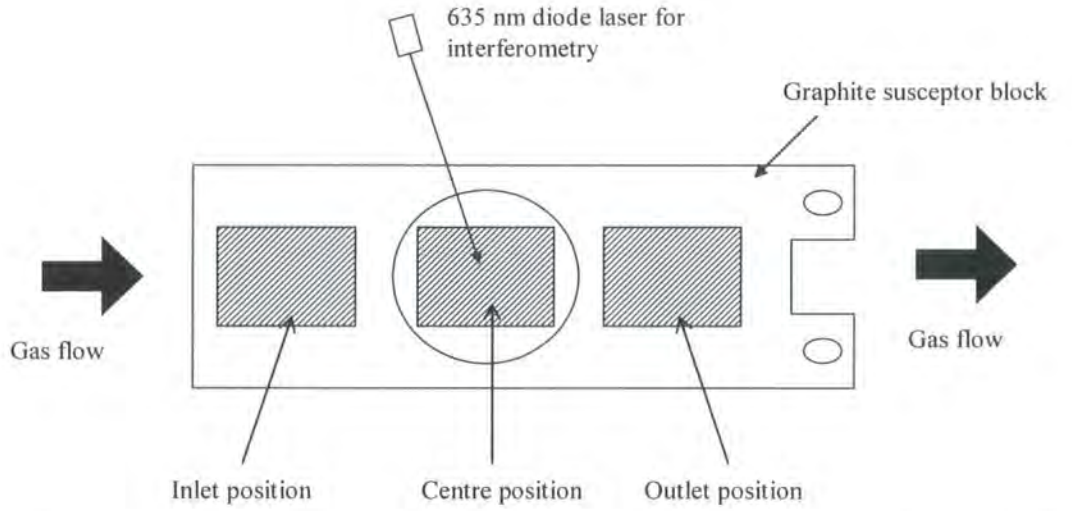


Figure 6-1 Diagram showing the arrangement of the ITO/glass substrates on the graphite susceptor block for the growth of CdTe/CdS solar cell structures.

The CdS window layers were grown at a temperature of 300°C in a total flow of 3355 sccm. The flows of ditertiarybutylsulphide (DTBS) and dimethylcadmium (DMCd) were 551 and 101 sccm respectively (VI/II ratio of 1.25) diluted in 2703

sccm of hydrogen. The final thicknesses were estimated at the centre position from interferometry and were 120, 240 and 500 nm for three growth runs performed. The CdTe absorber layers were grown at 350°C on top of the CdS using a DMCd and di-isopropyltelluride (DIPTe) flows of 101 and 500 sccm respectively (VI/II = 1) diluted in 2755 sccm of H_2. The nominal thickness of the CdTe layer for all three growths was 8 μm. Nine structures were grown in total, three for each run, with the CdS layer thickness being the only parameter changed intentionally.

Specimens were characterised by means of x-ray diffraction (XRD) and scanning electron microscopy (SEM). XRD was performed using a Siemens D5000 diffractometer using the Cu Kα line (1.5406 Å). Peak determination and phase identification was accomplished using the DIFFRAC^{plus} software suite from Bruker AXS [8]. SEM was performed in a JEOL IC-848 instrument. All the scanning electron micrographs presented in this chapter were taken at a beam voltage of 20 keV unless stated otherwise.

6.3 Results for As-Grown Material

Figure 6-2 a) shows the variation of the thickness of the structure measured by the alpha step, as function of the position of the substrate on the graphite block. Data for the three different growth runs is plotted. The zero position is arbitrary and referred to as the position on the susceptor block where the laser beam for interferometry is directed. Great variations in thickness were observed. The nominal thickness of 8 μm deduced from laser interferometry was confirmed for the *centre* sample as the values measured at $x = 0$ were between 8.5 and 9.5 μm. The *inlet* samples were thicker than expected, ~12.5 μm while the *outlet* ones were much thinner, ~4.8 μm. Thickness variation within the same sample was also observed with best uniformity measured for the *inlet* samples at ~1.5%. Variations of 15% were measured for the *centre* samples and 40% for the *outlet* samples. These variations within the same substrate and as a function of the substrate position reflect a change in the growth rate. The growth rate can be estimated from the thickness measurements and is plotted in Figure 6-2 b). Note that the growth rate is plotted on a logarithmic scale and that errors arise from the uncertainty of the exact position of the substrate along the susceptor block. The growth rate increases exponentially as

the substrate is moved closer to the reactor gas inlet and seems to reach an upper limit.

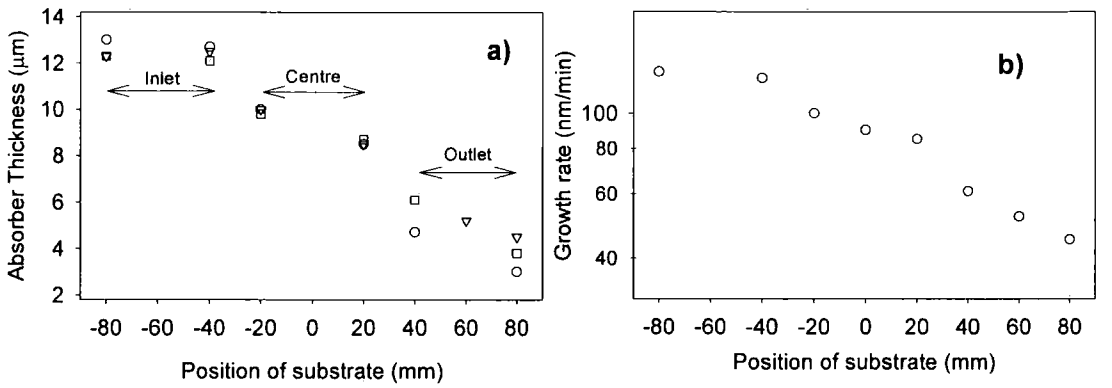


Figure 6-2 a) Thickness of the structures grown as a function of the substrate position along the graphite suceptor. Data for the three different growth runs is plotted. b) Estimated equivalent growth rate as a function of the substrate position. Note the logarithmic scale of the growth rate axis.

Generally non-uniform growth is considered to be caused by either thermal and/or gaseous effects. Berrigan *et al.* for example, reported the growth rate for MOCVD-grown CdTe as a function of temperature [9]. For low growth temperature, the growth rate is kinetically limited and the deposition process is governed by surface reactions. The velocity of surface reactions increases exponentionally with temperature. Then, when the growth temperature reaches ~360°C the deposition process becomes mass transport limited and consequently the growth rate depends on the substrate position for a given growth temperature, because it depends on the arrival of the precursors at the growing surface, yielding therefore a higher growth rate when a substrate is placed closer to the gas inlet of the reactor. Measurements using tin globules indicated that the temperature variation along the reactor are small, and in any case, growth profiles caused by temperature profiles generally show a peak at the centre of the susceptor (its hottest position); this is not the case in Figure 6-2. In the present case therefore, the thickness profile represents depletion of the precursor stream as it flows down the reactor, as is discussed further in section 6-6. For the purposes of what follows it can therefore be assumed that the properties of the films measured are as a function of thickness and not the growth temperature.

Figure 6-3 shows the x-ray diffraction patterns of CdTe/CdS/ITO/glass samples for different absorber thickness. The peaks observed belong to the CdTe zinc-blende structure. Some extra peaks corresponding to cadmium based oxides are also observed, probably arising from non-optimum storage conditions. It can be seen that the importance of the (331) and (422) reflections increases for thicker material while the intensities of the (111) and (511)/(333) reflections is reduced. It should be remembered that x-rays have a finite penetration depth which is a function of the incident angle and dependent on the material under investigation. Calculations of x-ray absorption as function of sample depth revealed that, for CdTe, 99% of the x-rays are absorbed within 2.3 μm at an incident angle of 2θ = 20° and within 7.6 μm at 2θ = 70°. This indicates strong absorption of the x-ray radiations in CdTe and therefore in this work only the top part of the structure was probed.

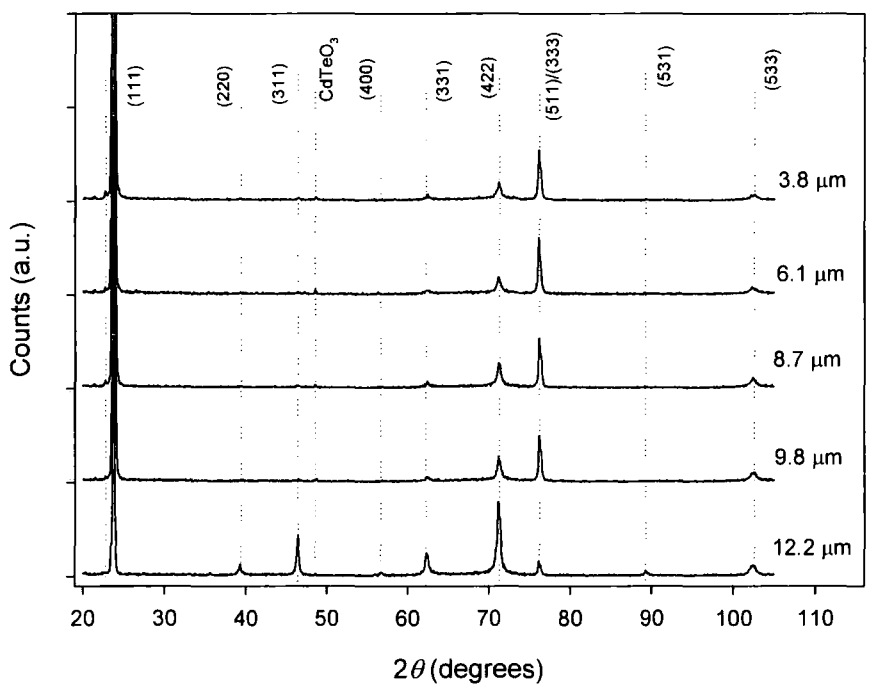


Figure 6-3 X-ray diffraction patterns for six samples with different absorber thickness. Reflections corresponding to the cubic structure of CdTe are observed. The 6 samples originate from the same growth run (RUN 3).

In order to quantify the effects of the absorber thickness and therefore the growth conditions on the texture of the samples, the evolution of preferred orientation σ and texture coefficients C_{hkl} were analysed (section 4.7.3). The preferred orientation σ is used to compare the degree of orientation between different samples so that lower σ values indicate more randomly oriented samples, while C_{hkl} gives a measure of the enhancement of the *hkl* reflection in comparison to a completely randomly oriented sample [5]. In the analysis nine planes were considered, namely (111), (220), (311), (400), (331), (422), (531), (620) and (533), excluding the (333) and (511) reflections due to their overlapping in the diffraction patterns. For a completely oriented sample, this gives a maximum value of $\sigma = 2.8$ and $C_{hkl} = 9$. Table 6-1 shows the C_{hkl} and σ values corresponding to the as-grown samples for the three growth runs.

	Absorber Thickness (μm)	C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{531}	C_{620}	C_{533}	σ
RUN 1	13	4.0	0.1	0.5	0.2	0.7	1.8	0.3	0.1	1.3	1.2
	12.7	4.8	0.0	0.1	0.1	0.5	1.5	0.1	0.0	1.5	1.5
	9.3	7.4	0.0	0.0	0.0	0.1	0.5	0.0	0.0	0.9	2.3
	8.5	6.3	0.0	0.1	0.0	0.2	1.0	0.1	0.0	1.3	1.9
	4.7	8.3	0.0	0.0	0.0	0.1	0.2	0.0	0.0	0.4	2.6
	4.7	8.3	0.0	0.0	0.0	0.1	0.2	0.0	0.0	0.4	2.6
RUN 2	12.5	4.2	0.1	0.4	0.1	0.7	1.9	0.2	0.0	1.4	1.3
	12.3	2.8	0.3	1.3	0.2	0.9	2	0.5	0.0	1.1	0.9
	9.1	7.4	0.0	0.0	0.0	0.1	0.5	0.0	0.0	0.9	2.3
	4.5	7.9	0.0	0.0	0.0	0.1	0.4	0.0	0.0	0.6	2.5
RUN 3	12.2	4.3	0.1	0.4	0.1	0.6	1.8	0.2	0.0	1.4	1.3
	9.8	7.9	0.0	0.0	0.0	0.1	0.3	0.0	0.0	0.7	2.4
	8.7	8.2	0.0	0.0	0.0	0.1	0.3	0.0	0.0	0.5	2.5
	6.1	8.3	0.0	0.0	0.0	0.1	0.2	0.0	0.0	0.4	2.6
	3.8	8.5	0.0	0.0	0.0	0.0	0.2	0.0	0.0	0.3	2.7

Table 6-1 Values of texture coefficients C_{hkl} and degree of preferred orientation σ for the absorber layer deposited on CdS/ITO/glass substrates. Results for the three growth runs are presented. CdS and CdTe layers were grown at 300 and 350°C, respectively and further details about the growth ambient can be found in section 6.2.

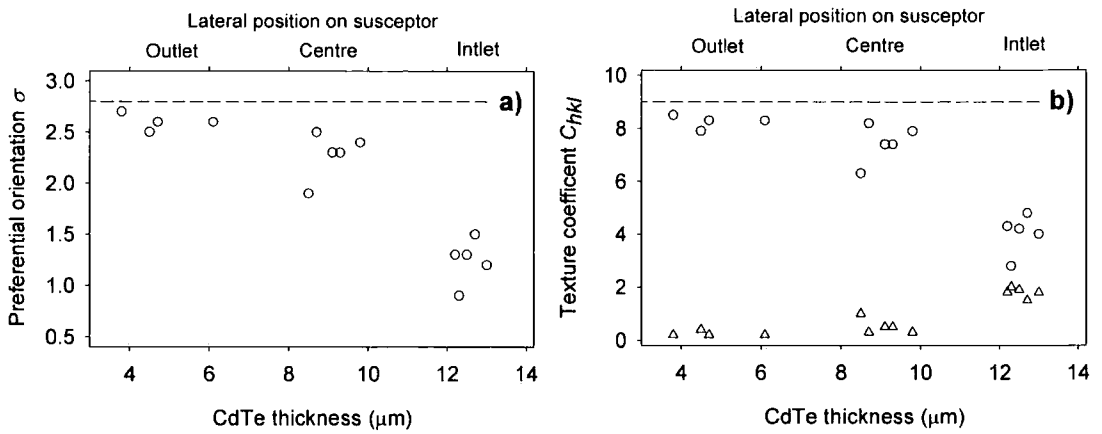


Figure 6-4 a) Degree of preferred orientation σ as a function of the absorber thickness and b) texture coefficients of the (111) (O) and (422) (△) reflections as a function of the absorber thickness. The dashed lines represent values for a completely oriented sample.

The data of Table 6-1 is plotted in Figure 6-4. Figure 6-4 a) is a scatter plot of the preferred orientation σ as a function of the absorber layer thickness and Figure 6-4 b) is a scatter plot of the C_{111} and C_{422} texture coefficients against the absorber layer thickness. The dashed lines corresponds to $\sigma = 2.8$ $C_{hkl} = 9$ for a completely oriented sample. It can be seen that there is decrease of the [111] preferred orientation as the CdTe thickness increases. Structures with 4-6 μm CdTe are nearly completely oriented in the [111] direction (σ = 2.5-2.7 and C_{111} = 7.9-8.5). While structures with 8-10 μm still have a [111] preferred orientation, there is an important loss of this preferred orientation for thicker structures (~12 μm). Although the [111] direction is the dominant one for all the samples studied, thicker samples exhibited an increased C_{422} texture coefficient indicating a change of orientation in this direction. This structural change to the [422] preferred orientation is associated with thicker films.

The crystallite sizes at the surface of the absorber layer were estimated from secondary electron micrographs for three different substrate positions. It was found that the grain size increases linearly with the thickness of CdTe material. The absorber layer grown on the *outlet* substrate (~4 μm) had a grain size of 0.2 μm, while at the *centre* it is 0.7 μm for a 9 μm thick CdTe and ~1 μm for a 12 μm thick layer grown at the *inlet*. There is a linear relationship between the grain size measured at the top surface of the absorber layer and the film thickness expressed as

$r = 0.050 \times x - 0.10$ where r is the grain radius and x the thickness expressed in microns. It must be noted that the interpolation at $x = 0$ is not expected to be valid since the near-interface material in similar structures grown by CSS has smaller grains than the linear relation (for thicknesses > 1μm) would suggest [12]. By comparison, Cousins *et al.* [13] measured the grain size of the absorber layer as a function of distance from the CdS/ITO interface for CSS-grown structures and also found a linear relationship ($r = 0.107 \times x - 1.06$) for $1 < x < 9$ μm. Although the absolute grain size increases with thickness in both deposition techniques, grains develop in size at half the rate in MOCVD at 350°C as they do in CSS growth.

6.4 Heat Treated Samples (No $CdCl_2$)

Samples grown on the *inlet* substrates were annealed in nitrogen in a tube furnace over the temperature range of 360-500°C for 5-70 min. All the samples used for this work had a CdTe absorber layer thickness of ~12 μm and have been studied by XRD and SEM. Figure 6-5 shows the XRD patterns of samples annealed at 360, 400, 440 and 500°C for 20 min. All samples showed peaks corresponding to the cubic structure of CdTe. Also peaks belonging to cadmium oxides were observed for samples treated at higher temperatures.

The texture coefficients C_{hkl} and preferred orientation σ were determined for all the CdTe peaks. Figure 6-6 shows the variations of σ, C_{111} and C_{422} as function of the annealing time for different annealing temperatures. At all temperatures there is a slight loss of [111] preferred orientation following the first 20 min of annealing due to a decrease in C_{111} texture coefficients. For longer anneal, σ remains constant indicating no change in the crystallite arrangements. Despite no significant variation of σ, there is a strong decay in the C_{111} coefficients indicating a distinct loss of the [111] preferred orientation. On the other hand the loss of [111] preferred orientation is accompanied by an increase in C_{422} texture coefficients (Figure 6-6 c)) indicating that the [422] direction becomes the preferred orientation following annealing. However, this is less pronounced for samples treated at 360°C. This temperature is close to the growth temperature and offers little energy for the driving force of recrystallisation. Annealing samples at 400°C and 440°C yielded layers presenting very similar structural changes. The 500°C annealings resulted in stronger structural

changes for the first 5-10 min, with samples randomly oriented after 5 min but for longer annealings, these became the most oriented along the [422] direction.

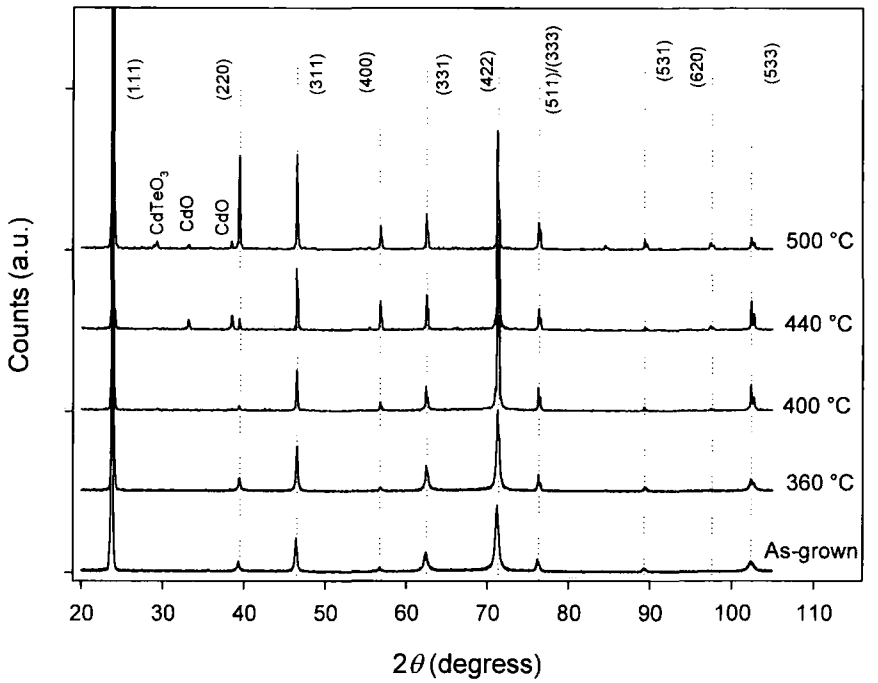


Figure 6-5 X-ray diffraction patterns for samples annealed for 20 min at different temperatures. Reflections corresponding to the cubic structure of CdTe are observed as well as cadmium based oxides for samples treated at higher temperatures.

This confirms that an increased growth temperature or post-growth anneal favours a structural rearrangement in the [422] direction. The structural changes in the CdTe are caused by the recrystallisation process and this recrystallisation process is dependent upon temperature and time of anneal. Recrystallisation process can occur during post-growth processing of materials and also during the growth itself. It uses strain energy either from planar defects such as grain boundaries or epitaxial mismatch [14]. In the case of small grained material, the strain energy per unit volume may be sufficient to cause recrystallisation on annealing. A small grain size also encourages recrystallisation by providing a higher density of nucleation sites, i.e. grain boundaries. For the samples processed at 360°C it is concluded that the recrystallisation process was in the early stages because σ and C_{hkl} vary only slightly with time. At higher processing temperatures recrystallisation takes place during the

first 20-30 min and then the films are completely recrystallised which is indicated by an invariant σ and texture coefficients C_{hkl}.

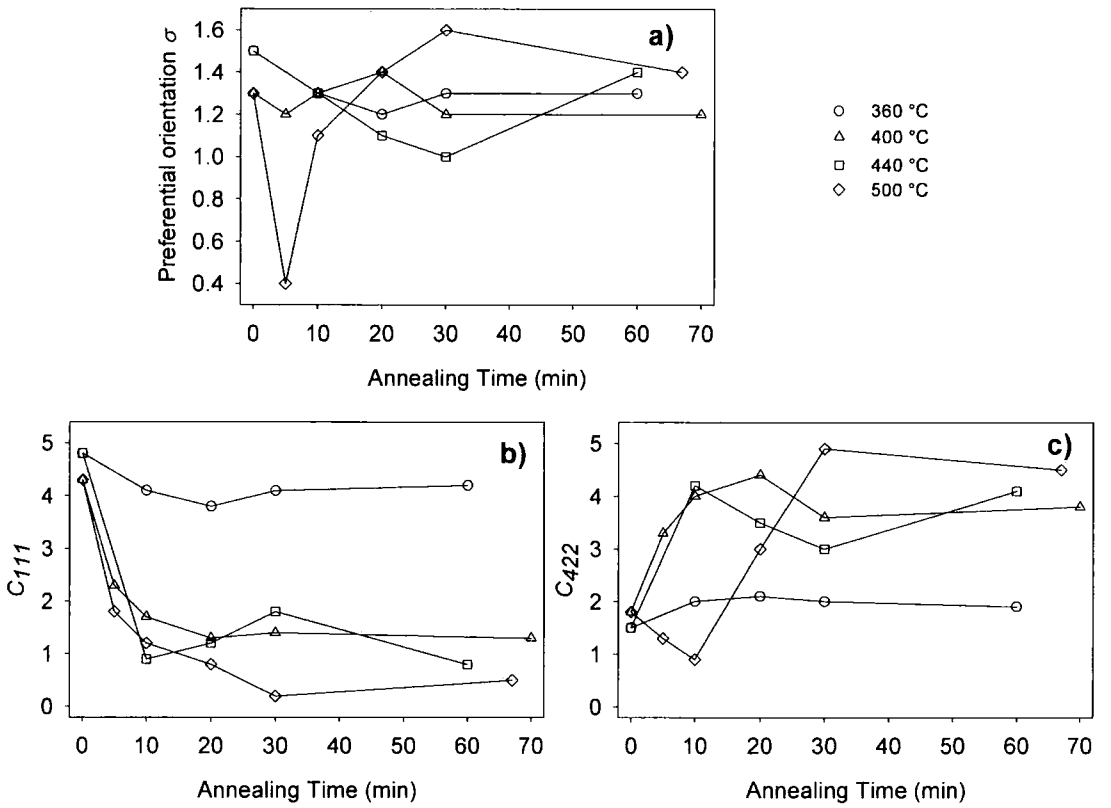


Figure 6-6 Degree of preferred orientation σ (a), texture coefficients of the (111) (b) and (422) (c) reflections as function of the annealing time for different annealing temperatures. The markers are experimental data and the lines are a guide to the eye.

Figure 6-7 shows the influence of annealing on the lattice parameter a. For all treatment conditions a was found to be larger than the lattice parameter for a powdered CdTe film (a = 6.481 Å), indicating a compressive stress in the plane of film growth. However, there is a clear reduction in a following a 10-20 min heat treatment for all temperature. When the annealing step is sustained beyond 20 min, the lattice parameter is nearly invariant for treatment temperatures below 500°C. Treatment at this temperature induced greater variations in lattice parameter with a decreasing further with longer annealing times. The reduction in the lattice parameter is due to a decrease in the material strain following the heat treatment. This was confirmed by Williamson-Hall plots (see section 4.7.2) which indicated that the internal strain for the as-grown layers, found to be between 1×10^{-3} and 5×10^{-3}, was

reduced to 1×10^{-5}-7×10^{-4} after heat treatment. Some examples of Williamson-Hall plots are shown in Figure 6-8. Figure 6-8 a) shows plots for two as-deposited samples with a 12 μm thick CdTe absorber. The internal strain is given by the slope of the linear fit to the data and is 2.1×10^{-3} and 3.3×10^{-3} for the examples shown. Following heat treatment of 12 μm thick films the internal strain reduces as shown in Figure 6-8 b). For processing at 400°C the resulting strain is 7.3×10^{-4} while it is 3.9×10^{-4} at 440°C and 5.0×10^{-4} at 500°C.

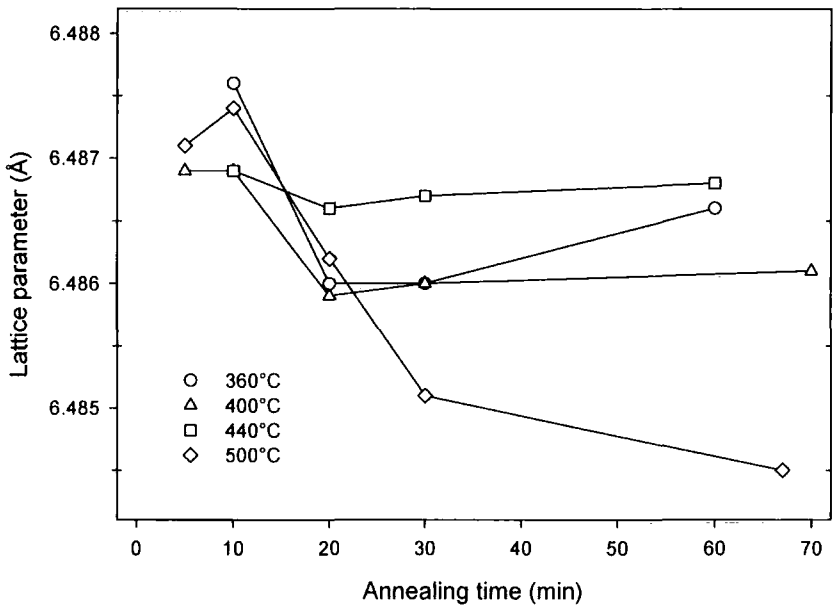


Figure 6-7 Lattice parameter as function of annealing time for different annealing temperatures. The markers are experimental data and the lines are a guide to the eye.

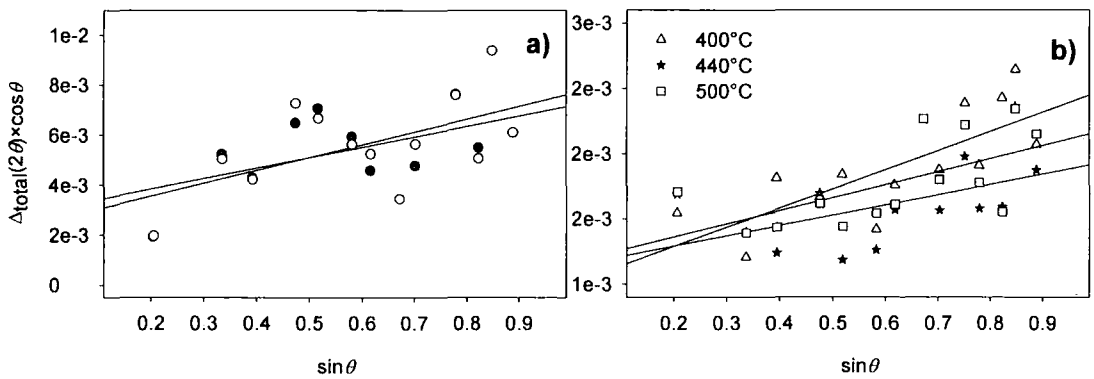
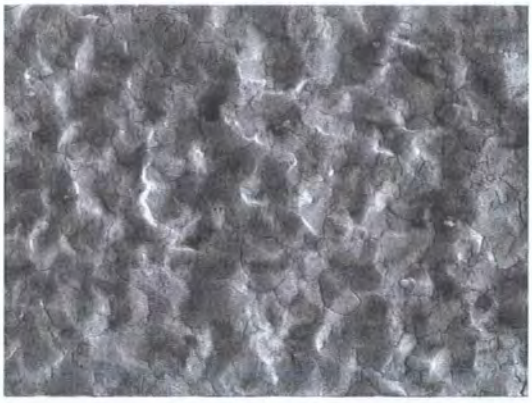


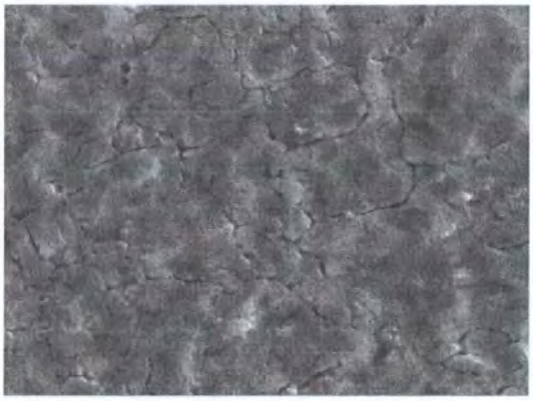
Figure 6-8 Williamson-Hall plots for a) two as-deposited 12 μm thick films and b) following a 20 min heat treatment at different temperatures. The lines represent the best fit for each group of data.

The treated layers were examined by SEM in order to reveal the morphology of the absorber layer, characteristic micrographs are shown in Figure 6-9. Prior to analysis, the sample were etched in a nitric/phosphoric mixture (see section 4.3) for 15 seconds in order to remove any oxides from the surface of the absorber layer.



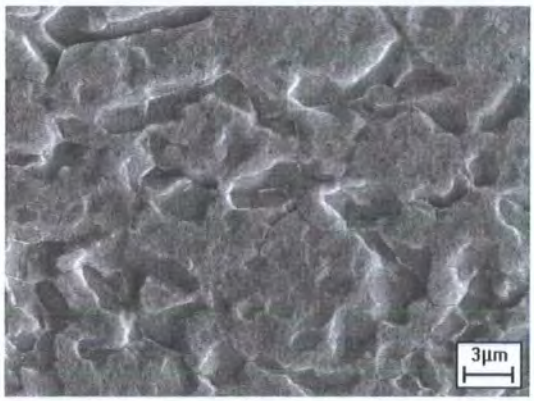
a) As-deposited film (12 μm thick)

b) 400°C - 20 min



c) 440°C - 20 min

d) 440°C - 60 min



e) 500°C - 20 min

Figure 6-9 SEM micrographs of the absorber layer surfaces for CdTe/CdS structures treated in nitrogen at different annealing temperature. The images were recorded at 20 keV. The scale marker is identical for all images.

When treated at 360°C the surface features of the CdTe layer were found to be identical to those of the as-grown layer (Figure 6-9 a)), and this was the case for all annealing times. Annealing at higher temperatures and for longer times encouraged thermal etching and evaporation from the films. There was also some indication of grain coalescence. For example Figure 6-9 c) (440°C, 20 min) shows more deeply (thermally) etched grain boundaries than does Figure 6-9 b) (400°C, 20 min). Annealing for 60 min at 440°C causes the film to begin to break up (Figure 6-9 d)), while a 20 minute anneal at 500°C (Figure 6-9 e)) causes inhomogeneous evaporation of the complete film thickness. The extent to which grain growth occurs is difficult to determine since the grain boundaries are not always made more distinct by the annealing in nitrogen. Figure 6-9 does show some evidence of grain coalescence but such effects are much clearer for $CdCl_2$ treated samples which are discussed in detail in the next section.

6.5 $CdCl_2$ Treated Samples

Samples grown on substrates positioned at the centre of the susceptor were annealed in nitrogen in a tube furnace at temperatures of 400 and 440°C for 5 to 60 min. Prior to annealing, samples were coated with a ~90 nm layer of $CdCl_2$. For this study, the samples had an initial CdTe thickness of 8-10 μm and were characterised by XRD and SEM.

6.5.1 Effect on Crystal Structure

Figure 6-10 shows XRD patterns of samples treated at 440°C for annealing times of 5-60 min. The peaks belong to the zinc-blende structure of CdTe. Peaks corresponding to cadmium based oxides are also observed, their intensity being more pronounced for longer annealing times. It can be seen that the intensity of some peaks increases with annealing time, e.g. (311), (422) and (531) while it is reduced for others, e.g. (111) and (511)/(333).

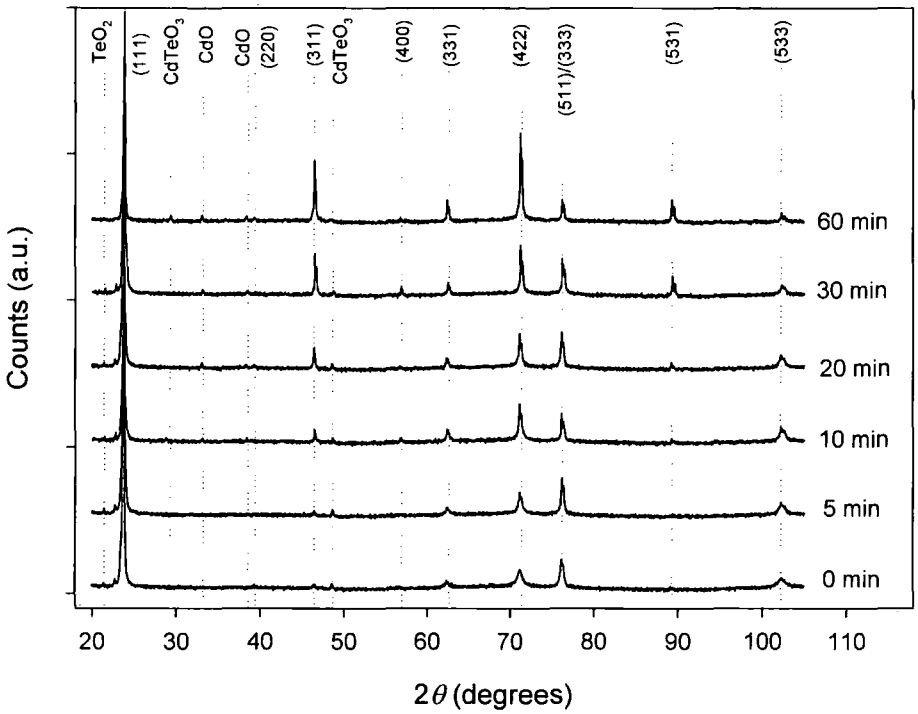


Figure 6-10 X-ray diffraction patterns for samples heat treated with $CdCl_2$ at 440°C for different annealing times. Reflections corresponding to the cubic structure of CdTe are observed as well as some oxides.

Table 6-2 summarises the values of texture coefficients and preferred orientation for the samples considered in this section. The loss of [111] preferred orientation can be seen and the randomisation of the crystallite arrangements is confirmed – evidenced by a decrease of the C_{111} coefficient and increase of the C_{311}, C_{422}, C_{331}, C_{531} coefficients with annealing time. The loss of [111] preferred orientation and randomisation of the layers becomes especially significant for 60 min annealings. However, the [422] preferred orientation is still favoured at higher temperatures and this is marked by a higher C_{422} coefficient. The samples treated at 400°C had, in general, a more random structure than layers treated at 440°C. This is consistent with the higher temperature processing favouring the [422] direction as discussed in the previous section.

	Annealing Time (min)	C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{531}	C_{620}	C_{533}	σ
	Untreated	8.2	0.0	0.0	0.0	0.1	0.3	0.0	0.0	0.5	2.5
440°C	5	7.9	0.0	0.0	0.0	0.1	0.3	0.0	0.0	0.6	2.5
	10	6.3	0.0	0.1	0.0	0.2	1.1	0.1	0.0	1.2	1.9
	20	7.1	0.0	0.2	0.0	0.0	0.8	0.1	0.0	0.8	2.2
	30	6.4	0.0	0.4	0.1	0.1	1.2	0.4	0.0	0.4	1.9
	60	1.6	0.0	1.1	0.0	0.0	4.6	0.8	0.0	0.5	1.4
	Untreated	7.4	0.0	0.0	0.0	0.1	0.5	0.0	0.0	0.9	2.3
400°C	5	6.8	0.0	0.0	0.0	0.2	0.7	0.0	0.0	1.2	2.1
	10	5.6	0.0	0.1	0.1	0.3	1.3	0.0	0.0	1.5	1.7
	20	5.9	0.0	0.0	0.0	0.2	1.2	0.0	0.0	1.6	1.8
	30	8.0	0.0	0.0	0.0	0.1	0.3	0.0	0.0	0.6	2.5
	60	2.2	0.3	0.9	0.3	1.0	2.3	0.3	0.2	1.4	0.8

Table 6-2 Values of texture coefficients C_{hkl} and degree of preferred orientation σ for the absorber layer heat treated with $CdCl_2$. Results for annealings at 400 and 440°C for 5-60 min are presented.

The variations of lattice parameter with annealing time are shown in Figure 6-11 a). The lattice parameter initially increases for shorter annealings and then reduces for longer ones. For all treatment conditions the lattice spacing was found to be greater than for a powder sample (6.481 Å). The variations in lattice parameter indicate an increased compressive stress following the first 10-20 min of annealing and then for longer annealing times this stress is released. In order to assess the variations of stress in the films, the in-plane stress (σ_s) magnitude was estimated using the formula suggested by Clemens and Bain [15]:

$$\varepsilon = \frac{a_{film} - a_{powder}}{a_{powder}} = \sigma_s \left(\frac{2S_{11} + 4S_{12} - S_{44}}{3} \right) \tag{6-1}$$

where ε is the strain of the film, a_{film} and a_{powder} are the inter-planar distances for the CdTe films studied and powder sample, respectively, S_{11}, S_{12} and S_{44} are the components of compliance. For CdTe, S_{11} = 4.27×10^{-12} dyn.cm^{-2}, S_{12} = -1.73×10^{-12}

dyn.cm^{-2} and S_{44} = 5×10^{-12} dyn.cm^{-2}* [16]. Positive and negative signs of stress correspond to tensile and compressive stress, respectively. The variation of stress in the treated films with annealing temperature and time are shown in Figure 6-11 b). It can be seen from the figure that the as-grown film is under compressive stress and the stress increases with annealing time reaching a maximum after 10 min at 440°C and 20 min at 400°C. The in-plane stress then decreases for longer annealing times. However, throughout the experiment, the films are only submitted to a compressive stress.

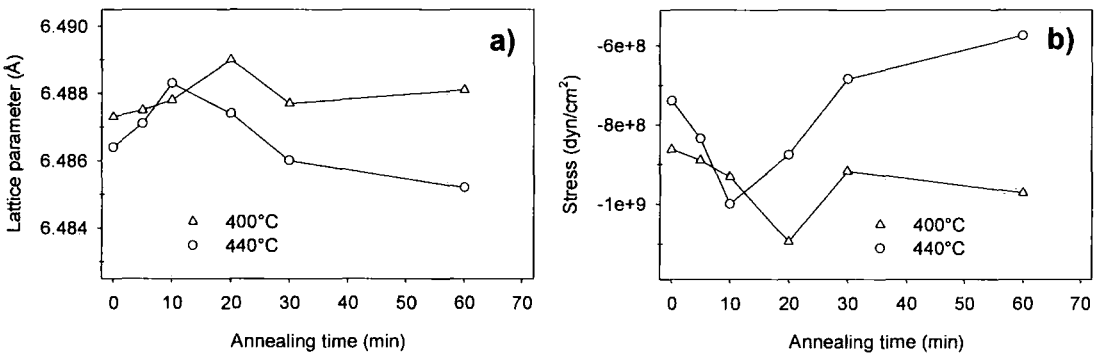


Figure 6-11 a) Lattice parameter as function of annealing time for $CdCl_2$ treated samples at 400 and 440°C. b) Magnitude of the in-plane stress in the CdTe films as a function of annealing time. The markers are experimental data and the lines are a guide to the eye.

During the post-deposition thermal treatment, the stress falls from ~-1.1×10^{9} to -5.8×10^{8} dyn.cm^{-2}. These values are larger than the critical value of formation of structural defects for CdTe (~10^{8} dyn.cm^{-2} [17]) and therefore the formation of crystalline defects in the layers such as twinning and dislocations is anticipated [12, 18, 19].

* The dyne (dyn) is the centimetre-gram-second unit of force. Although this unit is rarely used nowadays it was the unit used in the original reference [15]. The International System of Units would require to use the Newton so as 1 dyn = 1×10^{-5} N

6.5.2 Effect on Crystallite Size

The size of crystallites in the samples was determined from SEM imaging. Prior to analysis, the samples were etched in a nitric/phosphoric mixture (see section 4.3) for 15 sec in order to remove any oxides and/or cadmium chloride residuals from the surface of the absorber layer. From the secondary electrons micrographs the shape of the grains were marked on a transparency film, scanned and analysed using PC-Image 2.0 software from Foster Findlay Associates Ltd. PC-Image allows the determination of the area of every single object and then the radius of the grain is calculated assuming a circular grain shape.

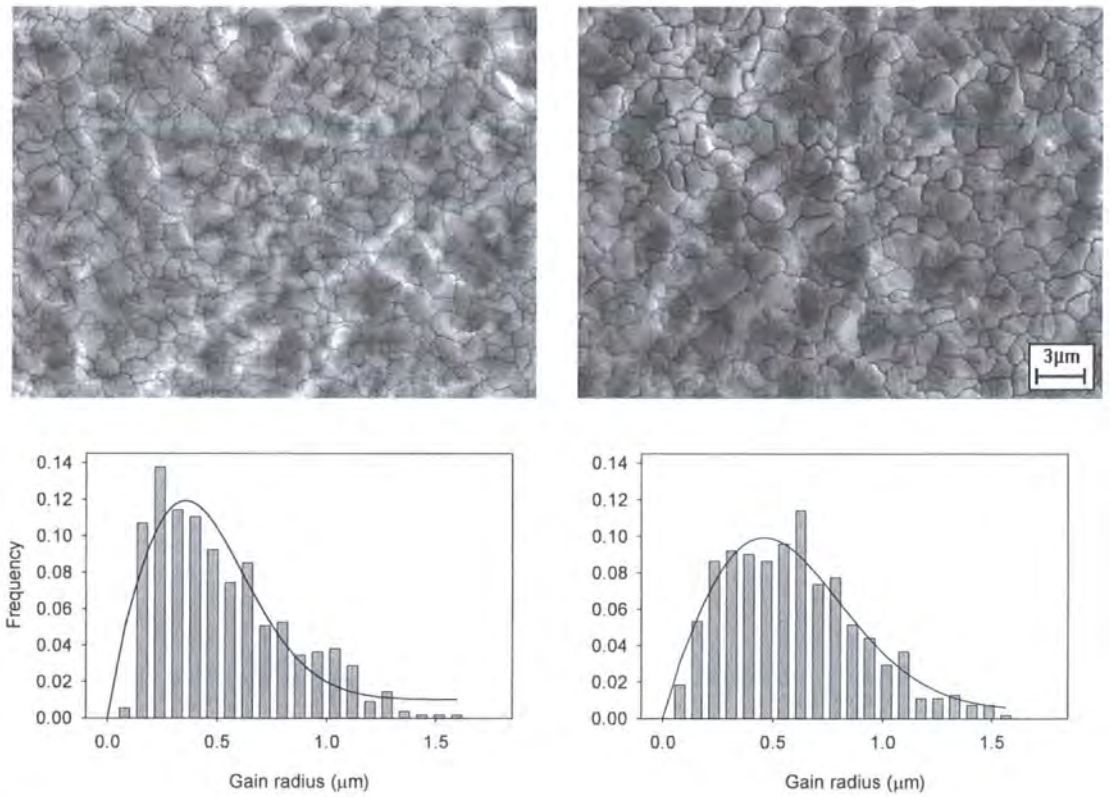


Figure 6-12 SEM micrographs (top row) and grain size distributions (bottom row) of $CdCl_2$ treated samples annealed at 400°C (left column) and 440°C (right column) for 30 min.

Figure 6-12 shows the SEM images and grain size distributions for $CdCl_2$ treated samples at 400 and 440°C for 30 min. The $CdCl_2$ treated layers showed an uniform and smooth surface. However, for long annealing (> 60 min) at 440°C, coalescence of CdTe grains and evaporation of the film start to occur similarly to that

shown for $CdCl_2$ free annealing (Figure 6-9). The grain size distributions were fitted using a Rayleigh distribution model [20]:

$$f(r) = ar\exp\left(-\frac{r}{r_0}\right)^2 \tag{6-2}$$

where r is the grain radius and a and r_0 are constants. The use of this distribution function has previously been demonstrated by Cousins *et al.* [13] to describe the grain size distribution of CSS-grown CdTe/CdS solar cells. It gave closer fits than other grain size distribution functions.

Figure 6-13 a) shows the evolution of grain size as function of annealing time for the treated samples. For all annealing times it was observed that the mean grain size was greater for the higher temperature processing. A 35-55% increase in grain size was measured between 400 and 440°C. It was also noted that the distribution of grain sizes becomes wider as the annealing temperature increases (Figure 6-12). Figure 6-13 a) shows that grain growth occurs during the first 30 min of annealing then the grain size is reduced for a 60 min annealing compare to a 30 min annealing. This observation may well be an artefact in the apparent grain sizes caused by significant inhomogeneous evaporation from the films. Available data for sample treated at 500°C (see chapter 7) was also included in Figure 6-13 a). Note that for this particular sample the thickness of the absorber layer was only 4 μm compared to 8-10 μm for all the other samples considered. The time and temperature dependent grain growth observed in the initial stages of annealing can be studied using the parabolic grain growth law described by Burke and Turnbull [14]:

$$\left(D^2 - D_0^2\right)^{1/2} = Kt^{1/n} \tag{6-3}$$

where D and D_0 are the average grain sizes before and after annealing, t the annealing time, K a constant and n the grain growth exponent. Values of n are usually much greater than 2 and only approach 2 for very pure metals – this is the "parabolic grain growth" law.

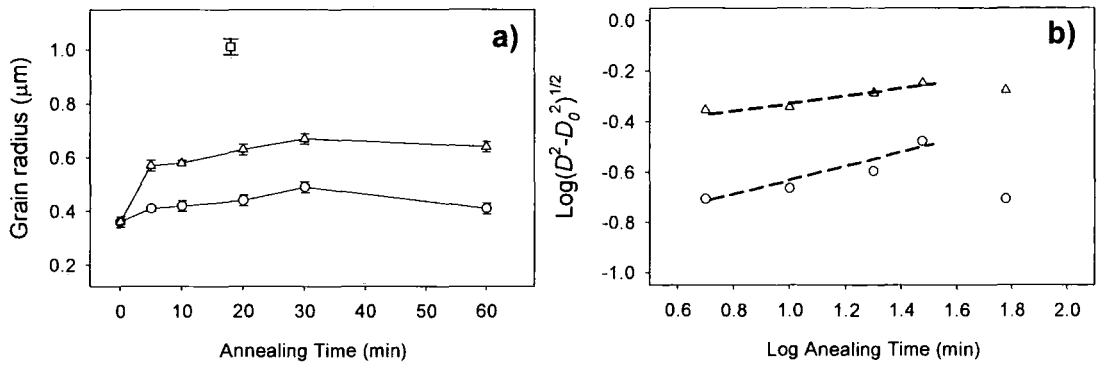


Figure 6-13 a) Evolution of the grain radii with annealing time for samples treated in $CdCl_2$ at 400°C (○) and 440°C (△) and 500°C (□). The markers are experimental data and the lines are a guide to the eye.
b) Grain growth isotherms for sample treated with $CdCl_2$ at 400 and 440°C. The lines are the best fits for each temperature. Note that data for the 60 min annealings were not taken into account for the fittings as reduced grain growth was observed for these samples compared to those annealed for 30 min.

The logarithmic plot of $\left(D^2 - D_0^2\right)^{1/2}$ as function of log t is shown in Figure 6-13 b). The slope of the best fit line was used to determine the grain growth exponent for the two annealing temperatures. As the data showed reduced grain size for 60 min annealings, only annealing time up to 30 min were considered in the determination of n. It was found that $n = 7$ for treatment at 440°C and $n \sim 4$ at 400°C. The value of the grain growth exponent is smaller at higher annealing temperature because at this temperature the grain size is already much larger after shorter time.

6.6 Discussion

The growth rate in a MOCVD reactor is dependent on the position of substrate along the susceptor. The growth rate was found to decrease when the substrate was moved away from the inlet side of the reactor. The variation of the growth rate on the susceptor with position (Figure 6-2) was consistent with the effects of gas phase precursor depletion during the growth of the CdTe layers. Since the growth was under a VI/II precursor ratio of 1, depletion is expected to affect both precursors equally and so no chemical imbalance is expected. It has also been inferred that the effects of temperature are minimal. It is on this basis that the

variations of structural effects with thickness are considered to be due to thickness rather than to some confounding variable.

MOCVD-CdTe films grown on CdS/ITO/Glass are mainly [111] oriented. This is expected because of the low energy of formation associated with the [111] surface and the underlying CdS layer which is mainly [002] oriented [21]. However, there is a relationship between preferred orientation and the layer thickness, with thin layers being [111] oriented, this giving way to more randomised texture as the layers thicken. The most dominant emerging orientation was [422], as shown in Figure 6-4. Further to this for the as-grown films, the crystallite size of the CdTe absorber layer was found to increase with the layer thickness. Similar results have also been reported in the case of columnar structures by several other authors for PVD-grown films [22], CSS-grown films [13] and electrodeposited (ED) films [23]. For the MOCVD films grown at 350°C, the grains increase in size with thickness at half the rate that they do in CSS material, and moreover they are smaller overall: for films of 1 μm thickness the average grain size for CSS material is ~1.2 μm while that for MOCVD material is ~0.15 μm. There are many examples of the increase in grain size of grains in polycrystalline films with the thickness of the film grown, but for any given growth method, the temperature has a strong influence on the overall grain size. Hence the low temperature of MOCVD growth (~350°C compared to ~500°C for CSS) could account for the large difference in grain size with the two methods. Whatever the exact cause, the small grain size of MOCVD material makes it inferior to CSS material for solar cell applications in which grain boundaries interfere with carrier collection.

Given that the thicker films have increasing [422] orientation and larger grains while the thinner films have [111] orientation and smaller grains it is interesting to speculate whether there is a crystallographic component to grain size development during growth. [422] is parallel to the [211] direction, the former being recognised in diffraction patterns since the {211} reflections are structure factor disallowed. Planes of the <211> zone contain {111} close packed planes, the Te terminated variant being the fastest growing CdTe plane of all in vapour growth experiments of orientation versus growth rate. Grain size development is considered to occur by means of competition between grains with the fastest growing faces of

grains competing favourably against the slower growing faces of their neighbours. If this is the case, then grains with a [211] surface orientation will be at an advantage since the <211> directions are perpendicular to {111} planes, these being the fastest growing in CdTe.

The behaviour of these MOCVD-grown CdTe films with annealing in both N_2 and in the presence of $CdCl_2$ was broadly consistent with the response of films deposited by other methods to annealing. For instance, measurable changes in the preferred orientation and grain size were only observed for temperatures greater than 400°C, this being significantly higher than the growth temperature of 350°C. Generally the [111] preferred orientation of the as-grown films gave way to an increasing proportion of the [422] with annealing and this was accompanied by grain growth. Both effects were enhanced by higher temperatures, longer annealing times and by the presence of $CdCl_2$ which is considered to act as a flux.

The structural changes in the CdTe layer are caused by the recrystallisation process that occurs during annealing. The recrystallisation is dependent upon the temperature and the time of the annealing but also upon the original grain size, orientation and lattice strain of the layer [14]. This is also indicated by a change in lattice parameter which is reduced following heat treatment, with or without $CdCl_2$. The primary effect of annealing is the reduction of the defect concentration and hence the availability of diffusion paths. The reduction of lattice parameter suggests that there is relief in tensile strain perpendicular to the substrate by reduction in compressive forces at the film surface. This is consistent with the observation that the lattice parameter also reduces with increasing film thickness for as-grown films. The recrystallisation is more pronounced in the presence of $CdCl_2$, indicated by the more randomly oriented layers and the significant increase in grain sizes. This indicates that intragrain (randomisation) and intergrain (grain growth) recrystallisation occurs in MOCVD-CdTe films. The heat treatment coupled with the presence of $CdCl_2$ promotes expansion of grains, the driving force for this grain growth being the minimisation of the grain-grain boundary energy.

In the as-grown state the CdTe layers are under compressive stress, indicated by a lattice parameter higher than that of a powder sample. The primary effect of annealing is to release this stress, measured by analysing the variation of lattice parameter. It is common, in the case of CdTe/CdS solar cell structures, to attribute the reduction in lattice parameter for annealed material to an intermixing between the two semiconductors creating an intermediate CdS_xTe_{1-x} alloy [5, 24, 25] – and also Te diffusion into the CdS layer creating a $CdTe_yS_{1-y}$ alloy. This can usually be observed on the XRD pattern by either a displacement of all the CdTe peaks towards higher angle if the CdTe film is completely replaced by the CdS_xTe_{1-x} alloy, or by the appearance of adjacent peaks to the CdTe peaks. This has been observed to happen at 400-450°C for $CdCl_2$ or air treated 1-3 μm thick CdTe/CdS structures, and sulphur has been found to diffuse as far as 500 nm away from the CdTe/CdS interface [23]. The lattice parameter values reported in the literature indicate a change in stress in the absorber layer following treatment, from compressive to tensile [3-5, 23, 24]. However, in the case of the samples analysed in this section, no extra peak was observed and therefore the change in lattice parameter is attributed only to the reduction of the in-plane stress of the CdTe films. However, it is anticipated that interdiffusion does occur, but because the films studied are ~8-12 μm thick and x-ray absorption calculations (see section 6.3), the intermixing cannot be detected using wide angle x-ray diffraction in the present case.

The grain growth exponent n was measured for the samples treated with $CdCl_2$ and was found to be higher for the higher annealing temperature. The higher values of n may be attributed to (i) the preferred orientation of the films and (ii) the residual stress in the layers. In general, reduced grain growth occurs when the films are more oriented. This was the case for the $CdCl_2$ treated layers; the structures treated at 400°C were more random compared to those annealed at 440°C and the grain growth exponent was lower. Normal grain growth occurs as a result of the surface energy stored in the grain boundaries but it is also possible for crystals to grow as a result of strain energy [26]. However, strain-induced grain growth should not be expected in a polycrystalline material after complete recrystallisation. It was shown that the CdTe thin films characterised here had residual stress, stress which is

reduced for higher annealing temperatures and therefore the time required for complete recrystallisation decreases with increasing annealing temperature.

This study partly confirms the results reviewed earlier in Table 3-2 indicating that grain growth occurs following $CdCl_2$ treatment on MOCVD-grown CdTe thin films. However, some differences are noticed in the structural changes following this treatment, which showed a reorientation of the film in the [422] direction rather than a randomisation.

6.7 Conclusion

The thickness and therefore the growth rate, of CdTe films grown by MOCVD on CdS/ITO/glass substrate were found to be dependent upon the position of the substrate on the susceptor block, this being consistent with the effects of precursor consumption during growth. The preferred orientation and morphology of the CdTe layers were found to be dependent upon the thickness of the films. *Outlet*/thinner films are mainly [111] oriented while *inlet*/thicker films are more textured in the [422] direction. The grain size, estimated at the surface, was five times greater for the thicker films i.e. 1 μm for a 12 μm thick film compared to 0.2 μm for a 4 μm thick film.

The effects of the post-deposition heat treatment on thick CdTe films (8-12 μm) grown were investigated in this chapter using x-ray diffraction and electron microscopy. In the case of $CdCl_2$ free treatment, little grain growth was observed. However, strong structural changes were measured. For treatment temperatures greater than 400°C the [111] preferred orientation is lost for the profit of the [422] orientation. In the case of heat treatment with $CdCl_2$ grain growth occurs and was measured as function of time and temperature. It was measured that growth occurs for the first 30 min of annealing and is accentuated for higher treatment temperature. The grain size distributions were described by a Rayleigh distribution function and the increase in grain size was found to obey the non-ideal Burke and Turnbull kinetics (n = 7 at 440°C). In all cases, the absorbed layer was submitted to a compressive stress, stress which was released upon annealing, but not totally.

In the next chapter, the use of appropriate post-deposition heat treatment conditions will be employed to process solar cell devices in order to study their performances.

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Chapter 7

Characterisation of $CdCl_2$-Treated Solar Cell Devices

7.1 Introduction

The possibility of *in situ* doping of the absorber layer of a CdTe/CdS cell with a perspective of supplanting the post-growth $CdCl_2$ heat treatment step was discussed in Chapter 5. However, this proved to be unsuccessful in that while growth conditions could be optimised to increase the dopant incorporation, this incorporation yielded more resistive CdTe films making them inadequate for solar cell applications.

Hence as an alternative to the doping route, several large CdTe/CdS/ITO/glass solar cell structures grown by MOCVD were activated via the usual route using a cadmium chloride heat treatment. Cells made from these structures are the subject of this chapter. A wide range of post-growth processing parameters were investigated in order to improve the performance of the devices and to determine the optimum post-growth treatment conditions for this system. This chapter summarises the results obtained using current-voltage measurements and microscopy characterisation techniques such as SEM and EBIC.

7.2 Description of the Samples Used in this Study

7.2.1 The Samples

The substrates used for this study were of two kinds. The first one was used to grow two sets of structures (SETS 1 and 3) and was supplied by Merck Display Technology (MDT). The MDT substrate consists of a 0.7 mm soda lime glass coated with a bilayer of silicon dioxide (SiO_2 ~20 nm) and indium doped tin oxide (ITO ~100 nm). The ITO has the high conductivity required to reduce the sheet resistance of the front contact whereas the silicon dioxide layer acts as a barrier against the diffusion of impurities from the glass. The second substrate was provided by ANTEC GmbH and was used to deposit the structures of SET 2. This substrate is somewhat different from the first one as it comprises a ~4 mm soda lime glass coated with a bilayer of ITO (~250 nm) and tin oxide (SnO_2 ~30 nm). In this case the SnO_2 layer is used to reduce the diffusion of the indium atoms from the ITO layer into the rest of the cell. It also acts to reduce the electrical losses due to any pinholes that may be present in the ITO coating. This substrate was commercially used by ANTEC GmbH to produce CdTe based photovoltaic modules.

As these transparent conductive oxide (TCO) layers are conductive, the classic four-point probe and the Van der Pauw techniques (see section 4.5.2) were used to determine the sheet resistance of the TCO provided by the two companies. Both techniques gave similar results and it was measured that the ANTEC films were nearly twice as conductive as the ones provided by MDT, 7.2±0.7 Ω/□ compared to 13.7±0.4 Ω/□, respectively. As the TCO resistance significantly influences the overall series resistance of the device, this difference in sheet resistance could be shown to be an important limiting factor in achieving highly efficient devices.

The three sets of samples (SETS 1, 2 and 3) grown by MOCVD have been used in this study for processing via the standard $CdCl_2$ route. The main difference between the three sets of samples was the change in thickness of the CdTe absorber layer. The sample growth parameters are detailed in Table 7-1. Samples from SET 1 were grown on MDT ITO/glass substrate. The CdS window layer was grown at

300°C with a VI/II precursor ratio of 1.48 and the thickness of the layer was estimated from the *in situ* interferometry measurements to be 120 nm. Other details concerning the CdTe absorber layer are shown in Table 7-1. The thickness of the CdTe layer (2-3 μm) was confirmed by the Alpha Step profilometer. The second set of samples (SET 2) was grown on the ANTEC substrate. Six samples were grown in 6 runs with a 120 nm window layer deposited at 300°C and a VI/II ratio of 1.3. Details of the CdTe layer (4 μm) are specified in the Table. The third batch of samples (SET 3) grown on MDT substrate consisted of three runs of three samples each as explained in section 6.2. The CdS was varied in thickness between 120 and 500 nm while the CdTe layers had thicknesses of 3-12 μm (see Table 7-1).

		CdS			CdTe		
		Temperature (°C)	Thickness (nm)	VI/II ratio	Temperature (°C)	Thickness (μm)	VI/II ratio
SET 1	RUN 1	300	120	1.5	400	2	1.0
	RUN 2-3	300	120	1.5	350	3	1.0
SET 2	RUN 1	300	120	1.3	370	4	0.7
	RUN 2-6	300	120	1.3	350	4	0.9-1.0
SET 3	RUN 1	300	120	1.2	350	3-12	1.0
	RUN 2	300	240	1.4	350	3-12	1.0
	RUN 3	300	500	1.2	350	3-12	1.0

Table 7-1 Sample growth details for structures used in this chapter.

7.2.2 Post-Growth Treatment and Parameters

Samples were activated using the $CdCl_2$ post-growth treatment, details of which were described in sections 3.4 and 4.3. Table 7-2 summarises the different parameters used for the deposition of the $CdCl_2$ layer, the annealing of the structures and the chemical etching prior to the back contact deposition.

	SET 1	SET 2	SET 3
$CdCl_2$ thickness (nm)	0-90	0-140	0-100
Annealing temperature (°C)	340-420	380-500	420-500
Annealing time (min)	10-20	18	10-45
Etching	Br_2/MeOH	Nitric/Phosphoric acid	

Table 7-2 Post-growth treatment parameters for all processed samples.

In addition, different etching procedures were performed for the preparation of the back contact deposition. For SET 1 a solution of bromine methanol (Br_2/MeOH) in concentration of 0.03-0.5% was used while samples from SET 2 & 3 were dipped into a solution of acid nitric/acid phosphoric (1% HNO_3, 70% H_3PO_4, 29% H_2O) [1]. After rinsing the samples with the appropriate solution (boiled deionised water for the NP etch and methanol for the Br_2/MeOH etch), the cells were dried under nitrogen. Finally, gold contacts (~2.5 mm diameter dots) were evaporated onto the CdTe layer as back contacts, and In-Ga amalgam was applied to the ITO (after removing the CdTe and CdS layers) to make use of the front contact. The devices measured comprised 4 gold dots on a ~1 cm^2 area. The contacts dots were not scribed to define their area.

7.3 Performance of Cells with ~2 and ~8 μm Thick CdTe Absorber

This section presents the results of cells from SET 1 (2-3 μm thick CdTe, i.e. relatively thin) and cells from SET 3 with a CdTe thickness greater than 8 μm (both of these sets gave poor photoresponse relative to those of SET 2, the results of which

are deferred to section 7.4). MOCVD solar cells with thin CdTe absorbers (SET 1) were coated with a thin $CdCl_2$ film and heat treated. They were then etched by bromine methanol before applying the back contact. In this series 16 devices were produced. Typical current-voltage (*J-V*) curves recorded in the dark and under 100 $mW.cm^{-2}$ AM1.5 standard illumination conditions are shown in Figure 7-1 a). This device was coated with 20 nm of $CdCl_2$ and annealed at 360°C for 18 min. Poor photoresponse of the device is apparent: for the example described here, the short circuit current density was 0.2 $mA.cm^{-2}$, the open circuit voltage was 0.3 V and the power conversion was below 0.1%. Although the device gives good diode shape responses both in the dark and under illumination, the dark *J-V* curve exhibits lower current in high forward bias, nearly two orders of magnitude lower than under AM1.5 illumination.

All thin CdTe cells from SET 1 treated with the bromine methanol etch exhibited this poor photoresponse behaviour ($\eta < 0.1\%$), this being weaker than in the as-grown state ($\eta \sim 0.4\%$). However, for this thickness of material the best cell was obtained using the NP etch ($\eta \sim 1\%$). Furthermore all treated cells examined under the SEM showed small-grained structures with a maximum grain size around 200 nm. SEM also showed that the combination of $CdCl_2$ and etch treatments caused perforation of the layers. For all processing conditions investigated it was concluded that the layers did not survive the treatment conditions used and thicker devices should be investigated in order to sustain the post-growth treatment conditions used.

While results for devices with intermediate thickness (~4 μm) are presented in the next section, it should be stated here that structures with thick CdTe absorber (8 μm and above) showed similar device response to the cells with thin absorbers. An extensive survey of processing parameters was made. However, even using a wider range of post-growth treatment conditions (by changing the $CdCl_2$ thickness, the etchant composition and concentration and using a longer heat treatment at higher temperature) did not appear to make any significant impact on the cell performances.

This can be observed in Figure 7-1 b) where the dark and light *J-V* characteristics are presented for a 12 μm thick device. The absorber layer was coated with 50 nm of $CdCl_2$ then annealed at 480°C for 20 min followed by the NP etch. It

can be seen that this cell as well as all the other treated cells from SET 3, showed a very weak photoresponse similar to the one of the cells processed from SET 1. For the example exposed in Figure 7-1 b) the short circuit current density was $J_{sc} \sim 0.4$ mA/cm^2 and the open circuit voltage was $V_{oc} = 0.17$ V, resulting in very low power conversion ($\eta << 0.1\%$).

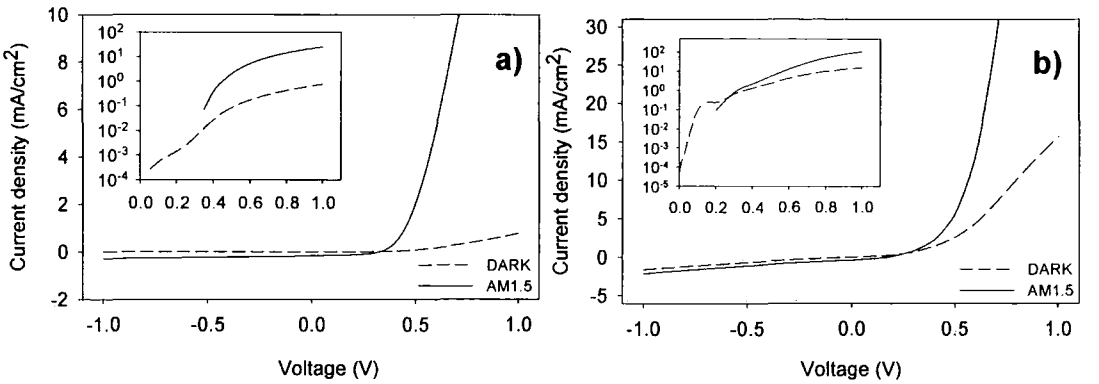


Figure 7-1 Current-voltage curves in the dark (dashed line) and under AM1.5 illumination (solid line) for a) a cell with 2 μm CdTe absorber treated at 360°C for 18 min and b) a cell with 12 μm CdTe absorber treated at 480°C for 20 min. The insets show the *J-V* characteristics plotted on a log scale at forward bias.

In order to investigate the materials contribution to performance, the grain sizes were studied as a function of processing. The strongest microscopic changes of the CdTe layer were observed in cells from SET 3 and this is shown in Figure 7-2. The as-grown material (Figure 7-2 a) has a pyramidal hillock structure and grains cannot easily be defined. However, the grain size of these layers was estimated in Chapter 6 to be 0.7 μm. Processing the cells flattens the absorber layer surface and reveals the grain boundaries. Processing at 420°C yielded grains with an average diameter of 1.09 μm, while devices processed at 500°C have a mean grain diameter of 2.03 μm. This represents an increase by a factor of 2: the influence of annealing temperature is clearly seen here. The higher annealing temperature yielded not only larger grains but also wider grain boundaries or more precisely wider trenches between grains introduced by the back surface etching.

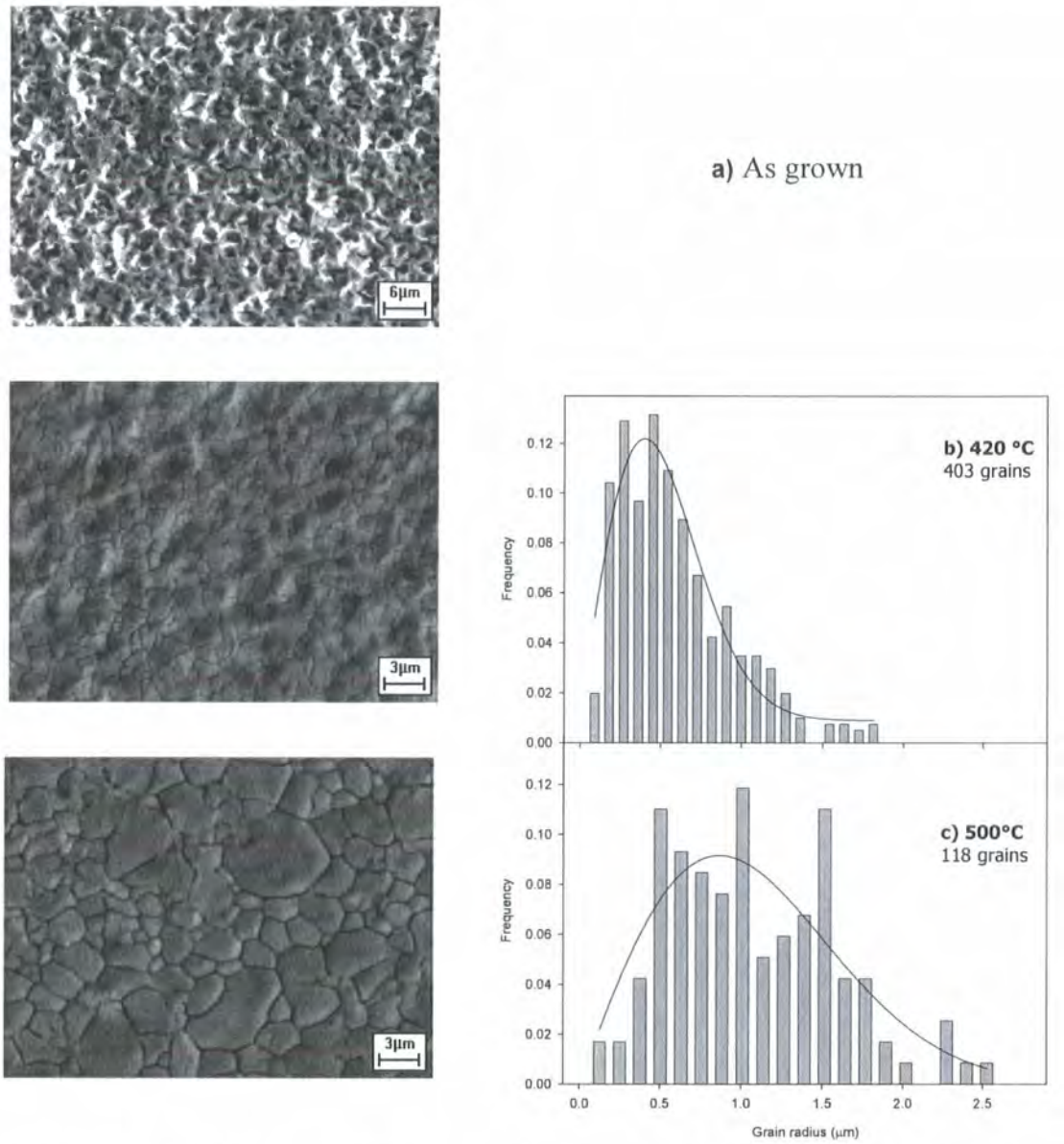


Figure 7-2 SEM images of the absorber layer surface of cells with thick CdTe (> 8 µm) in the as-grown state (a) and processed at 420°C (b) and 500°C (c). Also shown is the grain radius distribution for the processed samples. The solid lines are a fit to the data using a Rayleigh distribution function.

Figure 7-2 also shows the grain size distributions from the SEM images. The data were fitted using a Rayleigh distribution function (see Chapter 6). The best fit was obtained for the sample processed at 420°C than at 500°C because the number of grains taken into account is about three times higher for the former and it has therefore a better statistical representation. It must be noted that the three devices of Figure 7-2 showed similar conversion efficiencies and that in the case of structures with thick CdTe the morphology of the absorber layer is not the performance

determining factor, rather it is likely to be the junction properties of the devices that reduces performance to such low levels. The devices parameters are now discussed.

In general, processed cells exhibited much lower shunt resistance than in the as-grown state as can be observed in Figure 7-3 where the current-voltage curves for a thick device (SET 3) under illumination are plotted for both cases. The low shunt resistance was noticeable by the decrease in current with increasing applied voltage in reverse bias. Processed cells also showed smaller open circuit voltage and fill factors yielding lower efficiencies than the as-grown cells, even though the short circuit currents were increased by an order of magnitude following processing, possibly owing to grain growth. But overall poor performance could be explained by the fact that the as-grown structure was already inefficient with a V_{oc} of 0.32 V, FF of 48% and a J_{sc} of 0.15 mA.cm^{-2} under illumination ($\eta \sim 0.01\%$). Processing the cells increased the current at zero bias but reduced both V_{oc} and FF due to high series resistance, low shunt resistance and poor diode factor.

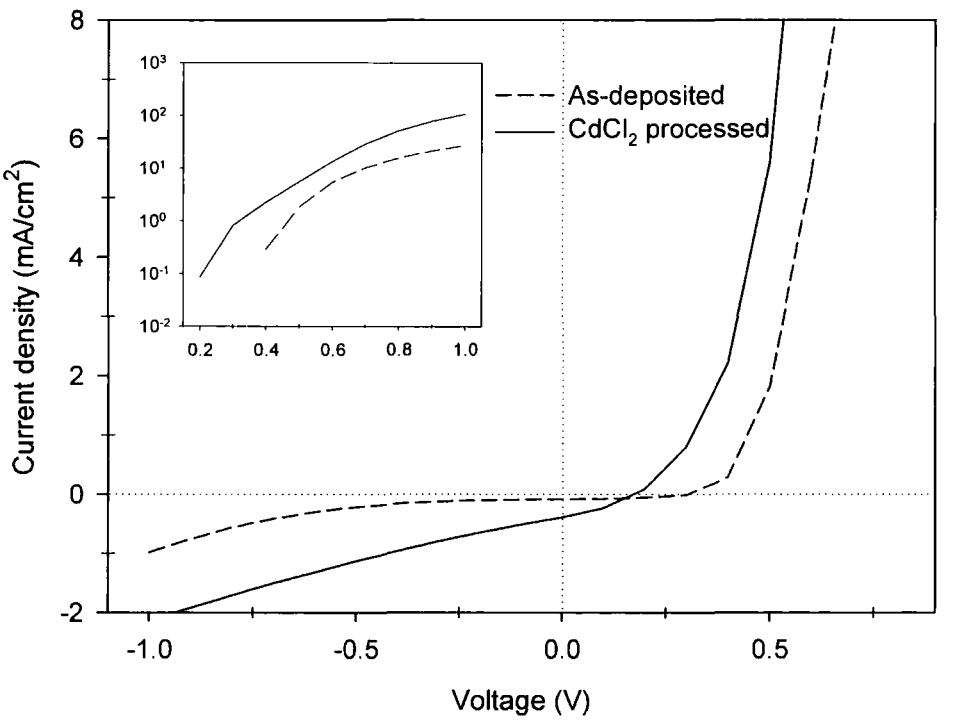


Figure 7-3 Current-voltage curves under AM1.5 illumination for an 8 μm (SET 3) as-deposited cell (dashed line) and a $CdCl_2$ processed cell (solid line). The inset shows the J-V characteristics plotted on a log scale at forward bias.

If the results for the thin CdTe cells (2 μm) can be understood by the use of damaging post-growth treatment conditions, results for cells with thick CdTe (> 8 μm) are less explicable. While processing caused perforation of the thinnest CdTe films this was not observed for the thickest. Moreover, while the range of $CdCl_2$ treatment conditions used for the thick CdTe films was great, no effective devices resulted. Elsewhere several groups have made cells with 8-10 μm thick CdTe which reach efficiencies greater than 10% [2-4], but these have been for CSS-grown CdTe rather than by MOCVD growth used here.

7.4 Results for Cells with ~4 μm Thick CdTe Absorber

This section exposes the performances of cells with ~4 μm CdTe absorber layer from SETS 2 & 3 processed using variable thicknesses of $CdCl_2$, annealing temperature and time. They were all finished with the nitric-phosphoric etch. First, the influence of the post-growth treatment parameters is described followed by the analysis of the overall performance and its variations using information extracted from the *J-V* curves and using SEM and EBIC techniques.

7.4.1 Influence of $CdCl_2$ Thickness

Firstly, the results of varying $CdCl_2$ thickness while annealing at 420°C for 18 min are described. Figure 7-4 shows the working parameters of all the cells processed as a function of $CdCl_2$ thickness. Each point represents data taken from a single 2.5 mm gold dot on a ~1 cm^2 plate. The lines on the plots indicate the upper and lower extremes of response and are purely manual fittings, i.e. drawings. Variability of the performance arises most strongly from the scatter in the values of J_{sc} obtained. There is considerably less variation in the V_{oc} values (~0.5 V) and the fill factor values (~25-35%). However, for the cells with highest J_{sc}, the efficiency was limited by the low fill factor. As the area of the cells were not scribed around the gold contact, errors on the short circuit current values might arise but considering the number of points plotted this is not likely to be the parameter with the most important effect as dots from the same plate gave similar results in most cases. Hence

while absolute values shall be subject to a consistent systematic error, the trend in processing-performance relationships shall nevertheless be revealed.

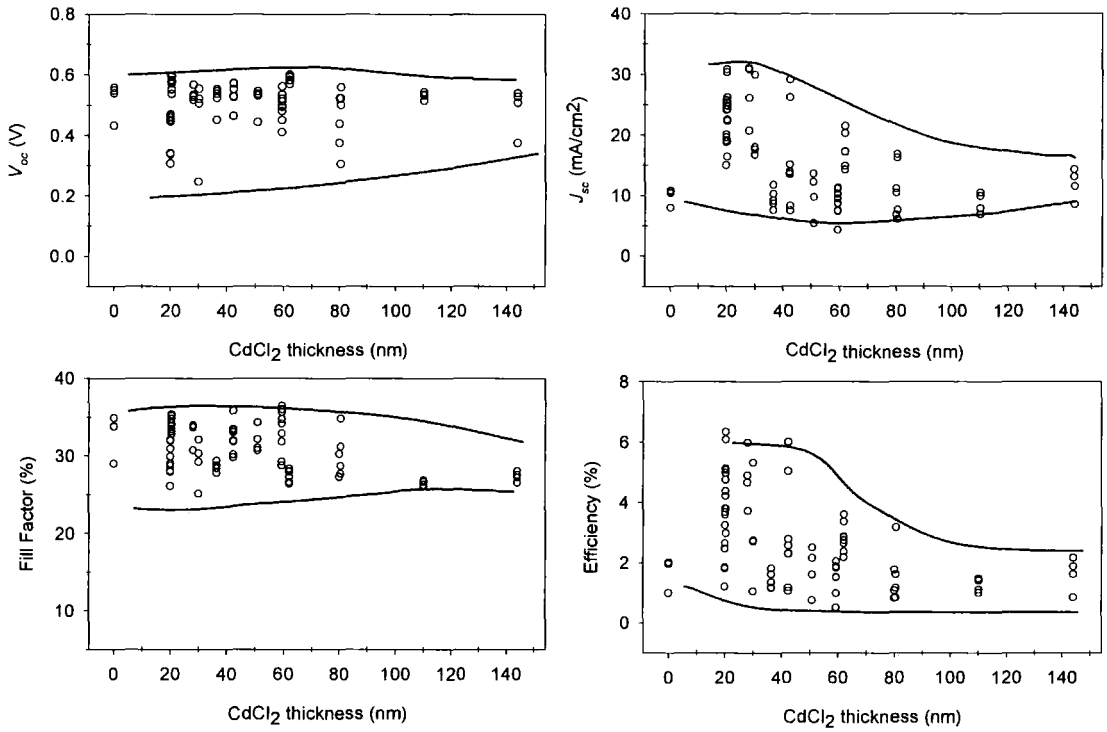


Figure 7-4 Variation of cell parameters for cells with ~4 μm thick CdTe processed at 420°C as a function of $CdCl_2$ layer thickness (SET 2). The lines indicate the extent of the scatter of the data. There is great scatter in the Jsc values, but the best cells are limited by the fill factor.

The best cells were obtained for a $CdCl_2$ thickness of 20-40 nm which results in a power conversion efficiency of ~6%. In all cases the fill factor was affected by low shunt resistance and high series resistance and this is explained in section 7.4.4. It can be noticed that in some cases the short circuit current densities reach values of 30 mA/cm^2 which is very close to the theoretical maximum calculated for a CdTe/CdS solar cell [5]. However, this is unlikely to be true and the high J_{sc} values are due to errors in estimating the active area of the dot contacted cells.

7.4.2 Influence of Annealing Temperature

In a second series, the $CdCl_2$ thickness was fixed at 30 nm while the annealing temperature was adjusted from 380 to 500°C for 18 min. The working parameters of the cells processed in this series are plotted in Figure 7-5. Trends

emerge even though the number of devices is lower than in Figure 7-4. In general, higher temperature processing yielded higher fill factors and efficiencies. Despite this, the best single devices were made at 420°C. For this series also, it was the variation in J_{sc} that caused the strongest scatter in the data. SEM imaging showed that processing devices at higher temperature yielded some shunts in the materials (see section 7.4.4). The tendency for shunting was greater at high temperature (75% at 500°C) compared to lower temperature (25% at 440°C) for samples used from SET 2. Shunts were indicated by the absence of short circuit current (J_{sc} = 0 mA.cm^{-2}) and ohmic behaviour of the response.

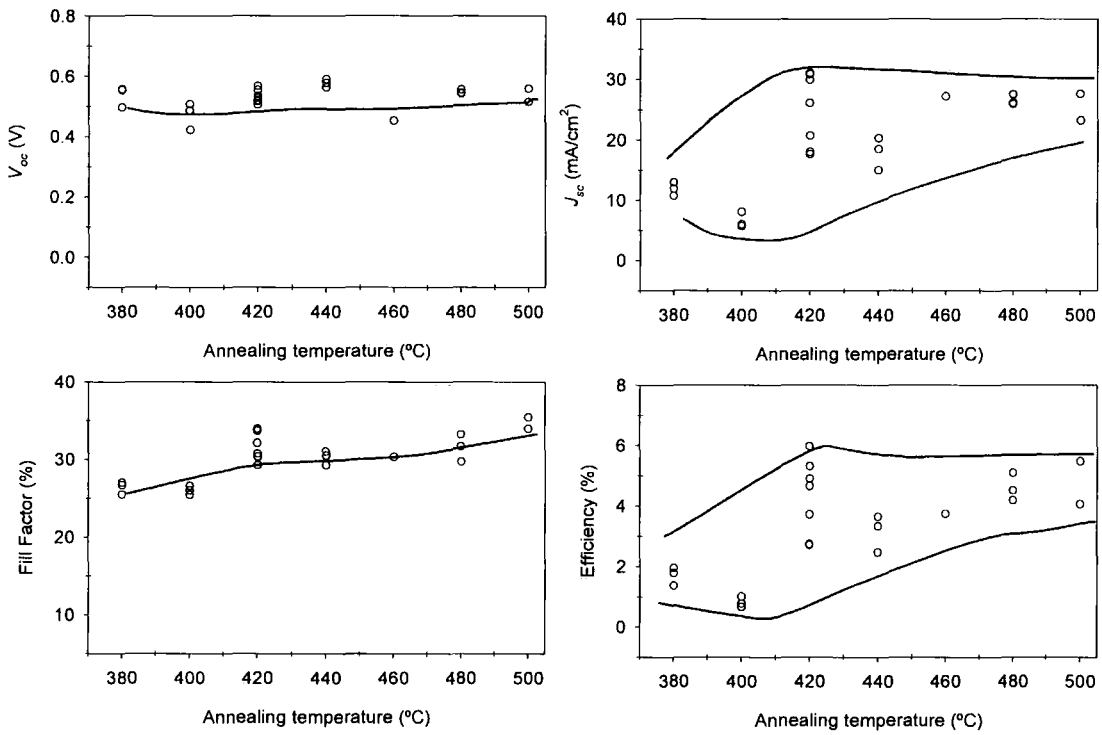


Figure 7-5 Variation of cell parameters for cells with ~4 μm thick CdTe processed using 30 nm of $CdCl_2$ as a function of temperature (SET 2). There is indication of trend to higher efficiency and fill factor with increasing processing temperature. Nevertheless the performance reproducibility is still dominated by the variation in J_{sc} while the best performance is limited by low *FF*.

7.4.3 Influence of Annealing Time

In a third series of measurements, the $CdCl_2$ thickness and annealing temperature were kept constant at 60 nm and 500°C, respectively while the annealing time was varied between 9 and 25 min. Although the previous section showed that best results were obtained using a treatment temperature of 420°C, best consistency with samples from SET 3 was obtained when processed at 500°C. Working parameters of the cells produced are plotted in Figure 7-6. This series of measurements used 4 μm CdTe thick samples from SET 3 and did not present any shunts in the material although SEM revealed degradation of the surface of the CdTe with the formation of craters that might become shunt paths if the annealing was to be sustained.

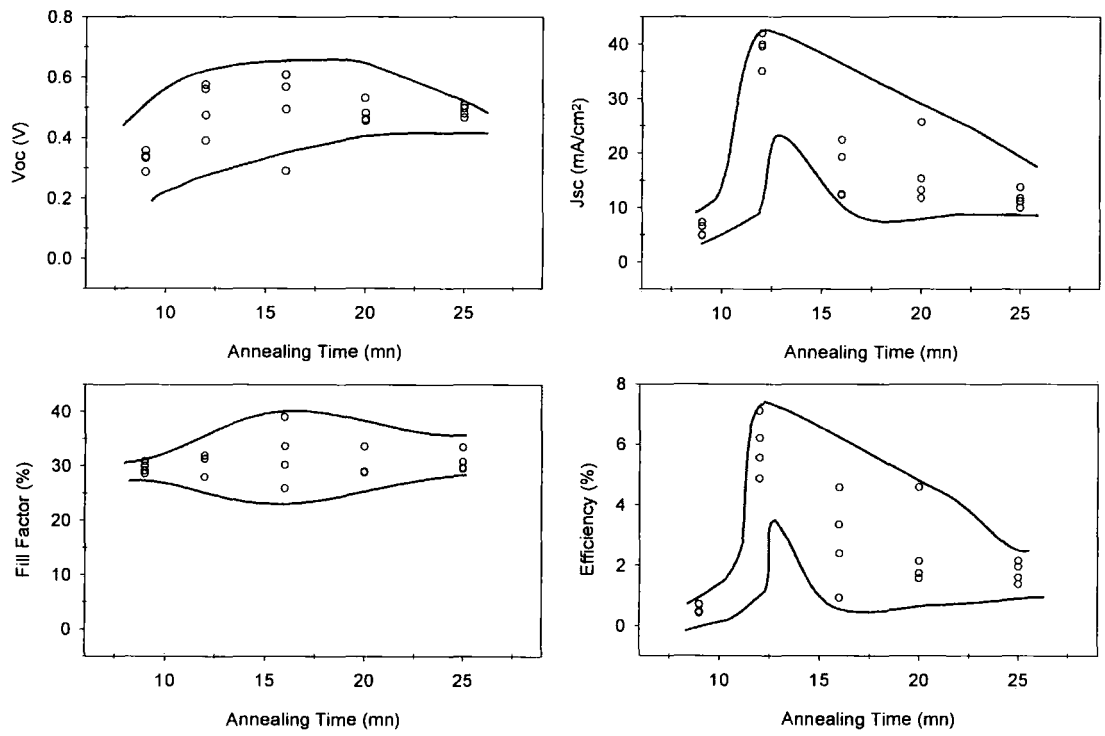


Figure 7-6 Variation of cell parameters for cells with ~4 μm thick CdTe processed at 500°C using 60 nm of $CdCl_2$ as a function of annealing time (SET 3). The lines indicate the extent of the scatter of the data. There is great scatter in the J_{sc} values, but the best cells are limited by the fill factor.

The variation of the fill factor does not seem to be influenced by the annealing time as its value is stationary around 30%. This time, greater variation is observed in open circuit voltage values (~0.3-0.6 V). The best values are obtained for

a 16-20 min anneal but a better consistency is seen with anneal of 20-25 min. Short baking time of only 9 min clearly limits the performance of the devices. Again the scatter in short circuit current density values influences strongly the overall efficiency of the cell. There seems to be a maximum in performance for a 12 min annealing. However, the short circuit current density values measured for this particular plate (4 dots) were high, higher than the maximum theoretical J_{sc} value ($J_{sc\ max}$ = 30.5 mA.cm^{-2} [5]). This again shows the impact of using contact dot devices with small area: the active area can easily be underestimated, probably by a factor of 2 or greater which results in higher short circuit current density and efficiency values.

From the three series of measurements we can try to assess the optimum parameters for processing MOCVD CdTe/CdS solar cells via the $CdCl_2$ route. It was found that an evaporation of ~30 nm of $CdCl_2$ followed by an annealing at 420°C for 12-18 min give the best results when followed by the nitric-phosphoric acid etch. These findings are similar to those reported by other research groups [6-8] who optimised post-growth processing parameters for PVD and CSS-grown materials.

7.4.4 Limiting Factors for Higher Efficiencies

It was suggested earlier that the efficiency of the devices is limited by the low fill factor. Figure 7-7 shows a scatter plot of the ratio of the efficiency over the open circuit voltage as a function of the short circuit current. The entirety of the processed samples is plotted regardless of the processing conditions. This confirms that J_{sc} is the greatest cause of cell to cell variability. The slope of this graph multiply by the incident light intensity (P_{in} = 100 mW.cm^{-2}) gives the average fill factor for the set of samples analysed and is FF = 33%. This value is less than the usually reported values for CdTe based solar cells [4, 9], and is the cause for underperforming devices.

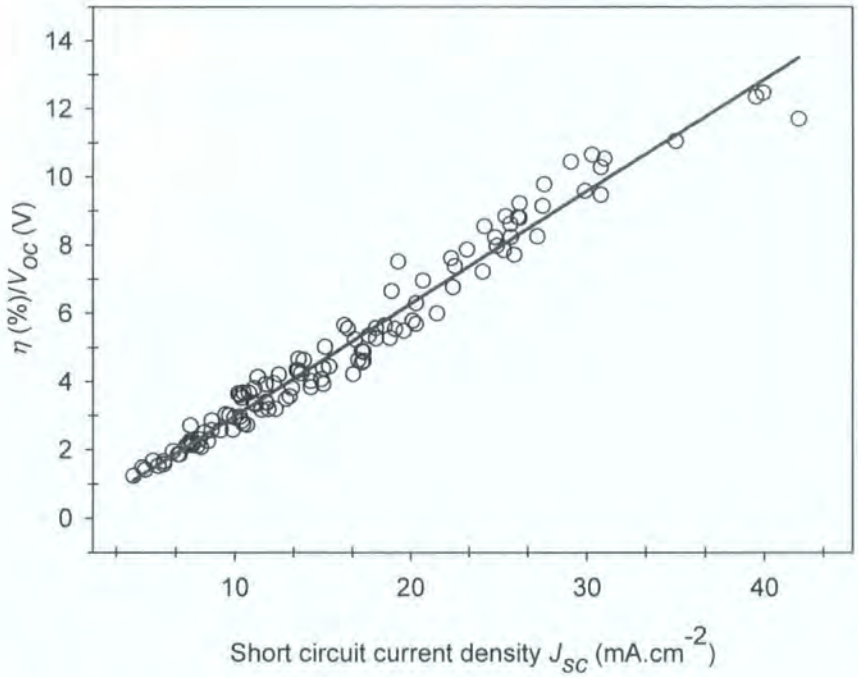


Figure 7-7 Scatter plot showing efficiency over open circuit voltage as a function of the short circuit current density for all processed devices. It shows the strong influence of J_{sc} on performance.

Evidence is now exposed about the factors inducing the low fill factor observed in the devices prepared. Figure 7-8 a) shows a typical current-voltage curve in the dark and under AM1.5 illumination. The cell presented was coated with an 80 nm layer of $CdCl_2$ then annealed at 420°C for 18 min and followed by a NP etch prior to gold contact deposition. The conversion efficiency of this device was η = 3.7% for a short circuit current density J_{sc} = 19.1 mA/cm^2, an open circuit voltage V_{oc} = 0.52 V and a fill factor FF = 38%.

The quantum efficiency (QE) of this particular device is shown in Figure 7-9 b). The spectral response exhibits the typical top-hat shape characteristics of a heterojunction cell. A small drop is observed at a wavelength of ~750 nm and is due to the change of order sorting filter in the spectral response measurement setup. At photon energies greater than the CdS bandgap (λ < 520 nm), optical absorption in the window layer reduces the number of photons penetrating through to the depletion region. A similar cut-off is seen at 830 nm corresponding to the energy bandgap of the CdTe absorber layer. It can be seen that the highest current collection occurs near

the CdTe band edge at ~830 nm which would indicate the presence of a buried junction. Consequently a poor quantum efficiency is seen at the CdS absorption edge, about half of the maximum QE.

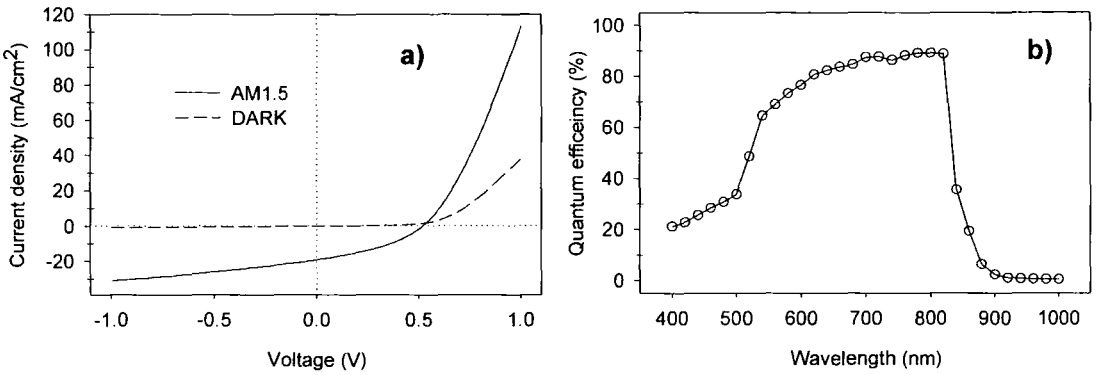


Figure 7-8 a) *J-V* curves in the dark (dashed line) and under illumination (solid line) for a sample coated with 80 nm of $CdCl_2$ and annealed at 420°C for 18 min. b) Spectral response characteristic of the device.

Detailed analysis of the room temperature *J-V* behaviour was carried out to characterise the diode behaviour and identify the possible cause of the reduced performance of the device. The data are described by a standard diode model with the forward diode current limited by Shockley Read Hall recombination states within the space-charge region [10]. This gives a modified single diode equation:

$$J = J_0\left[\exp\left(\frac{q(V - JR_s)}{AkT}\right) - 1\right] - J_L + \frac{V}{R_{sh}} \qquad (7\text{-}1)$$

where J_0 is the reverse saturated current, A the diode quality factor, J_L the light generated current, R_s the series resistance and R_{sh} the shunt resistance.

The accurate determination of the diode parameters is known to be difficult for thin film solar cells especially under illumination conditions. This is particularly true for the determination of A and R_s because (i) both of them have qualitatively similar effects on the shape of the *J-V* curve; (ii) both A and R_s vary with the illumination intensity; (iii) there are possible shunting effects, current limiting effects and changes in collection efficiency which affect the analysis but are not easily quantified. For this analysis it was assumed that R_s and R_{sh} are constant, i.e. the series and shunt terms are ohmic. In addition J_L can be voltage dependent, but it is required that the light generated current is constant and is approximate to the short circuit current ($J_L = J_{sc}$).

To analyse the *J-V* data R_{sh} is first determined from the minimum value of the slope *dJ/dV* in reverse bias. Series resistance and diode quality factor are determined by differentiation of the diode equation resulting in the relation [11]:

$$\frac{dV}{dJ} = R_s + \frac{AkT}{q}\left(\frac{1 - \frac{1}{R_{sh}}\frac{dV}{dJ}}{J + J_{sc} - \frac{V}{R_{sh}}}\right) \tag{7-2}$$

A linear fit to the plot *dV/dJ* versus the term in brackets in equation (7-2) yields R_s and A from the intercept and the slope, respectively. Finally, when the assumptions of constant R_s, R_{sh} and J_L apply, a logarithmic plot of $J+J_{sc}$ versus $V-JR_s$ will give an intercept of J_0 and a slope of q/AkT.

Figure 7-9 a) shows the *dJ/dV* versus applied voltage plots for the device presented in Figure 7-8 both in the dark and under AM1.5 illumination. For the cell operating in the dark, *dJ/dV* is constant in reverse bias voltage up to $V = 0.3$ V. This gives a dark shunt resistance of 1060 $\Omega.cm^2$. When operating under AM1.5 light, the plot is more scattered, indicating the voltage dependence of the light generated current. The average plot of this graph is linear at reverse bias but voltage dependent at forward bias. The equivalent light shunt resistance is 140 $\Omega.cm^2$. Strong differences between light and dark behaviour are also observed in Figure 7-9 b), where *dV/dJ* is plotted against the function of equation 7-2. The intercepts give a series resistance R_s of 2.1 and 6.8 $\Omega.cm^2$ under illumination and in the dark, respectively, and the slopes yield a diode quality factor A of 4.4 and 2.4, respectively for light and dark conditions.

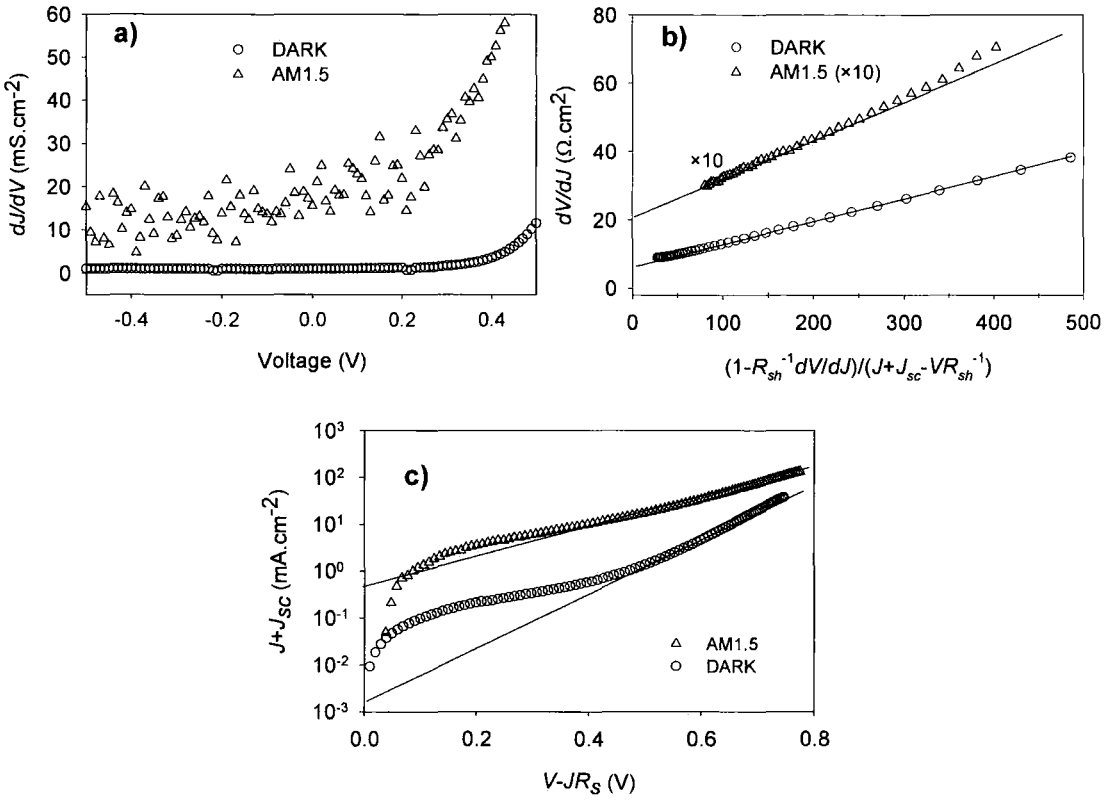


Figure 7-9 AM1.5 illuminated and dark plots of a) dJ/dV versus applied voltage, b) dV/dJ versus $(1-R_{sh}^{-1}dV/dJ)/(J+J_{sc}-VR_{sh}^{-1})$ and c) logarithmic plots of $J+J_{sc}$ versus $V-R_sJ$. Solid lines show the fit to determine R_s and A from b), and J_0 and A from c)

Using the above values of R_s the logarithmic plot of $J+J_{sc}$ versus $V-JR_s$ is shown in Figure 7-9 c). Extracted values for J_0 were 1.6×10^{-3} and 3.2×10^{-1} mA.cm^{-2} in the dark and under AM1.5 conditions, respectively. The measured values are several orders of magnitude higher than the usually reported values for CdTe solar cells [12]. The diode quality factor values obtained from this plot also confirms the ones previously derived. The results are summarized in Table 7-3.

	R_{sh} (Ω.cm^2)	R_s (Ω.cm^2)	A	J_0 (mA.cm^{-2})
DARK	1060	6.8	2.4	1.6×10^{-3}
AM1.5	140	2.1	4.4	3.2×10^{-1}

Table 7-3 Diode quality factor A, reverse saturated current J_0, series R_s and shunt R_{sh} resistances in the dark and under AM1.5 conditions for the cell presented in Figure 7-8.

Overall the devices are characterised by low shunt resistance and large series resistance and diode quality factor. The reverse saturation current is also high. By using the parameters from Table 7-3 and the single diode equation for a real solar cell (equation 2-17) R_s, R_{sh}, A and J_0 can be refined to fit the data. This is shown in Figure 7-10. A good fit is obtained from this model but not at high forward bias. The assumption of a constant light generated current equal to the short circuit current clearly does not stand at high forward bias. Also the presence of a voltage dependent current collection function could explain this behaviour and the strong differences between the dark and light plots of Figure 7-9 and 7-10. The performances of the devices were found to be limited by the open circuit voltage and the fill factor. Those limitations arise from the poor junction parameters (R_{sh}, R_s, A, J_0).

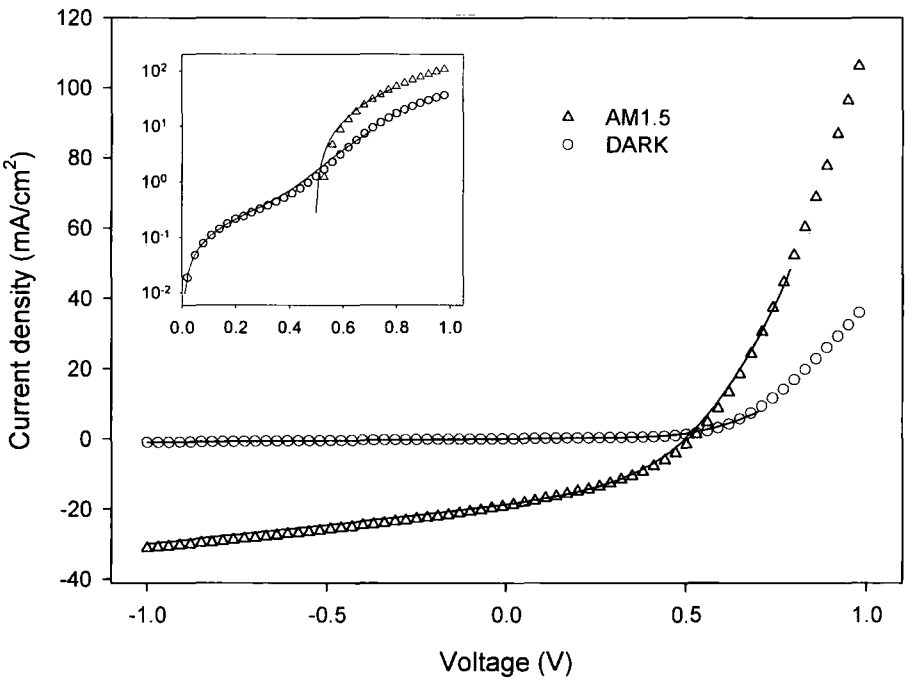


Figure 7-10 *J-V* curves in the dark and under AM1.5 illumination. The solid lines represent the fit to the data using the single diode model for a real solar cell. Refined parameters from Table 7-3 are: Dark: R_s = 10 Ω.cm^2, A = 2.9, and AM1.5: R_{sh} = 90 Ω.cm^2 and A = 5.1.

Investigation of the influence of the illumination intensity on cell parameters is now described. Varying light intensity was possible by the use of neutral density filters. An expression for the open circuit voltage for an ideal solar cell was derived in section 2.3.3.2. If we assumed the light generated current to be independent of the bias voltage then equation 2-18 becomes:

$$V_{oc} = \frac{AkT}{q} \ln\left(\frac{J_{sc}}{J_0}\right) \tag{7-3}$$

For ideal *p-n* junctions it can be assumed that A and J_0 are constant with irradiance, i.e. illumination intensity. Since J_{sc} is assumed to be linear with illumination intensity it follows that the open circuit voltage is proportional to the light intensity. The linear dependence of the short circuit current density on the light intensity is shown in Figure 7-11 a). The relative V_{oc} of the investigated cell normalised to V_{oc} under 100 mW.cm^{-2} AM1.5 conditions is shown in Figure 7-11 b). At an illumination of 1 mW.cm^{-2}, V_{oc} is 0.332 V still more than 60% of the value under standard test conditions. However, the variation of the relative open circuit voltage is not strictly linear which indicates that either the diode quality factor or the reverse saturation current or both depend on the irradiance.

The change in diode quality factor with irradiance is shown in Figure 7-11 c). Under lower light levels A decreases. According to equation 7-3 this causes a decrease in V_{oc} for lower light intensity levels, in the order of 2. This leads to the conclusion that $A(G)$ is not the sole determining factor for the irradiance dependence of V_{oc}. The value of A is determined by the type of current transport mechanism in the solar cell. Typically a value of $A = 1$ is assigned to an ideal transport across the junction according to the Shockley theory, which is diffusion and direct recombination. A value of $A = 2$ is assigned to predominating defect recombination via mid-gap states in the space charge region, i.e. Shockley-Read-Hall recombination. Values higher than 2 are possible by multiple recombination steps or multi-step tunnelling [13]. Hence it seems that a tunnelling transport is the dominant transport mechanism for the cell investigated.

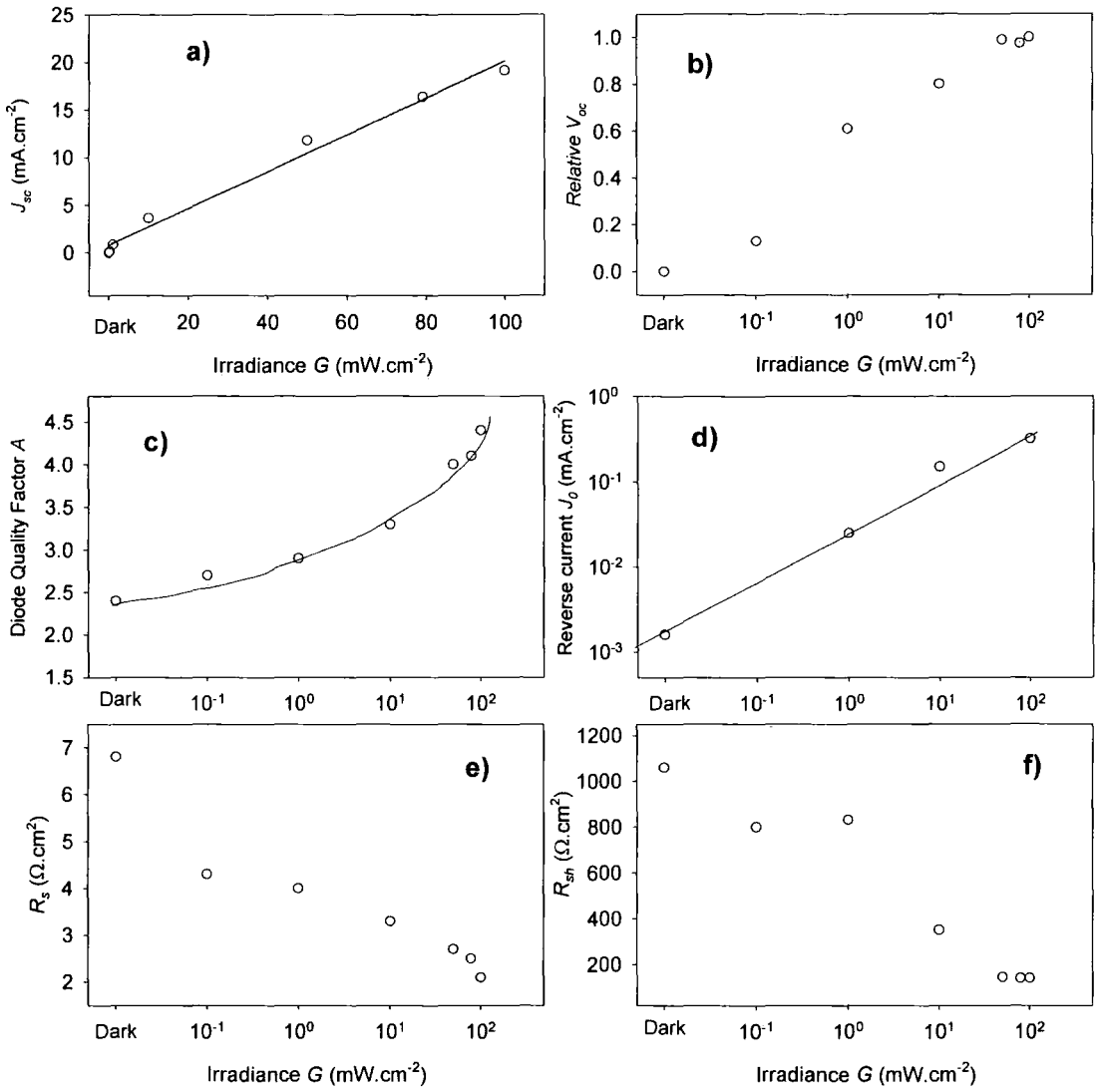


Figure 7-11 Variation of cell parameters with light intensity. a) short circuit current density J_{sc}, b) relative open circuit voltage V_{oc}, c) diode quality factor A, d) reverse saturation current J_0, e) series resistance R_s and f) shunt resistance R_{sh}.

Since the variations of A do not fully explain the behaviour of $V_{oc}(G)$, it is necessary to further investigate the dependency of the dark current J_0 on the irradiance. This is shown in Figure 7-11 d). J_0 increases by 2 orders of magnitude over the range of illumination levels used. This is the main cause for a retained higher V_{oc} at low light levels. It also indicates that the diode quality of the *p-n* junction suffers from a rising J_0, which is possibly due to parasitic currents that become more important for higher injection. The approximation in equation 7-3 excludes the influence of shunt resistance, which will become important if R_{sh}

becomes too low. In this case a low R_{sh} acts like a high J_0 and reduces V_{oc}. The variation of R_s and R_{sh} at different light levels are plotted in Figure 7-11 e) and f).

The series resistance increases smoothly at lower light intensities. The shunt resistance of the device also increases more or less linearly with decreasing light intensity. The lower value at higher irradiance causes a limitation of the voltage at maximum power (V_{mp}) available in standard test conditions. The increase in R_{sh} and R_s at lower intensities probably results from the high photoconductivity in the CdS window layer.

Evidence for the origin of the cell-to-cell and in-cell variability is now presented. The CdTe surfaces of the series of cells processed from SET 2 and 3 in the range 380-500°C were examined by SEM, with representative images being shown in Figure 7-12. The samples presented were coated with 30 nm $CdCl_2$ and annealed for 18 min followed by NP etch. Also shown in Figure 7-12 is the grain radius distribution of the continuous films displayed. At every condition processing at 380-420°C yielded a continuous film with grains in the range 1-3 μm. The structure displayed processed at 380°C has a mean grain diameter of 1.08 μm, which is the same value as for the thicker structures processed at the same temperature range. Processing at 440-500°C yielded larger grains (1-8 μm) with the sample shown having a mean grain diameter of 2.74 μm.

However processing at this temperature also interrupted the continuity of the films. Some areas of some plates had holes ~1 μm wide at grain boundaries as shown in Figure 7-12 c), while others had large grains but fewer or no holes. Generally the tendency for film breakdown was greater for the higher temperatures used. Such holes might be expected to give shunts, especially for the high temperature films. Shunting of cells from SET 2 was noticed and in proportions such as 75% shunted cells at 500°C and 25% at 440 °C. It must be noted that shunting was not observed for the thicker structure, 8 μm and above even when annealed for one hour.

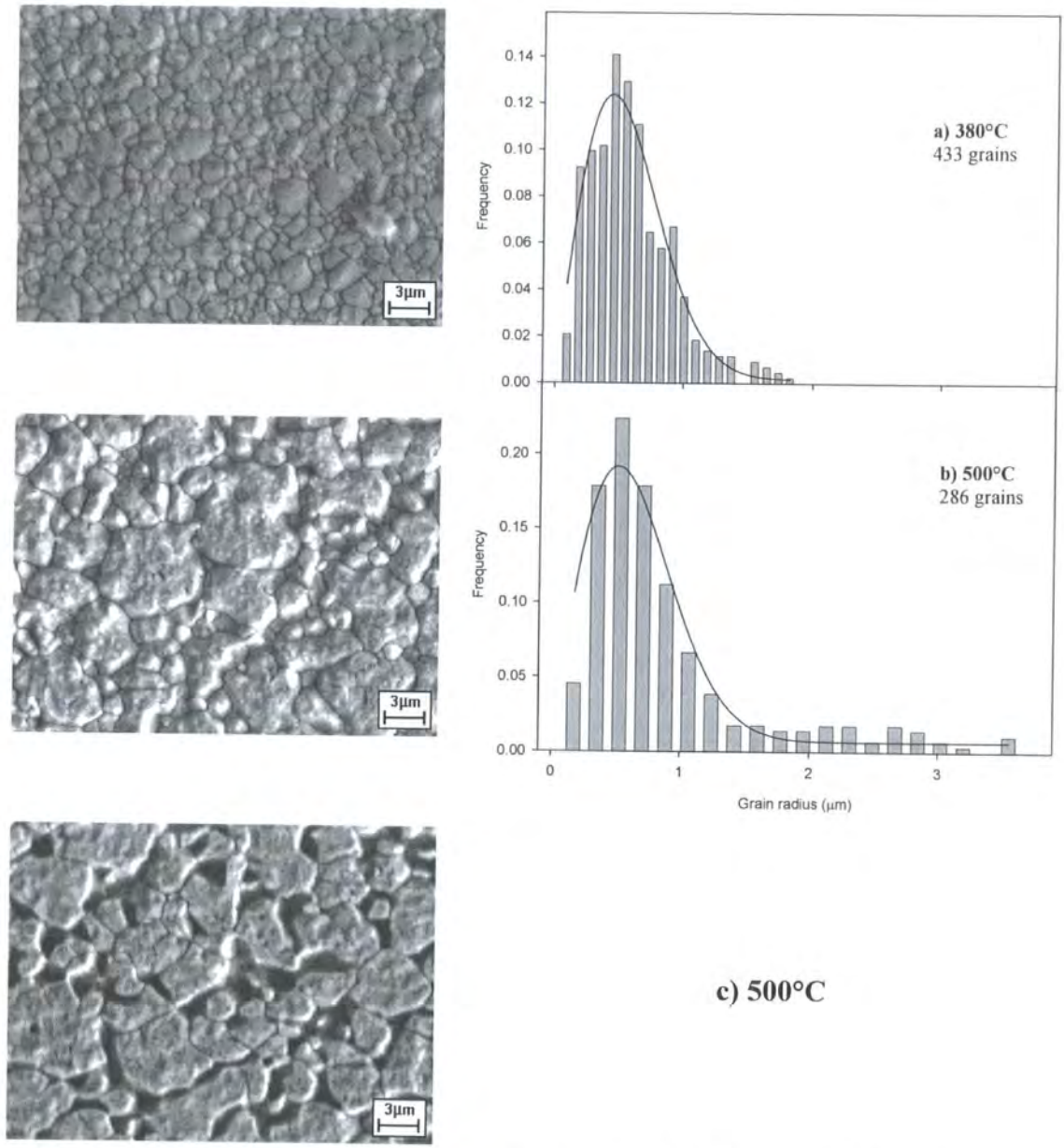


Figure 7-12 SEM images of CdTe surfaces processed at high and low temperatures a) 380°C - showing small grains in a continuous film, b) 500°C – the film has larger grains and c) 500°C - showing discontinuities in the film. Also shown is the grain radius distribution for the processed samples. The solid lines are a fit to the data using a Rayleigh distribution function.

7.5 EBIC Measurements (Cells with ~4 μm CdTe)

Cells from SET 2 performing relatively well were characterised using electron beam induced current (EBIC) technique. The technique was presented earlier in section 4.6 and can be performed in three different configurations: front-wall EBIC when the electron beam irradiates the front part of the solar cell, back-wall EBIC when irradiating the back surface and cross-sectional EBIC. The latter geometry was not used in this work but has previously been applied to CdTe/CdS solar cells, see for example [14]. Here EBIC was used to examine the uniformity of the cell response and the junction position.

7.5.1 Front-Wall EBIC

Front-wall EBIC was used to probe the non uniformity in a given device, using the illumination side geometry or front-wall EBIC. The glass substrate was removed as described in section 4.6 and the experimental setup is illustrated in Figure 7-13.

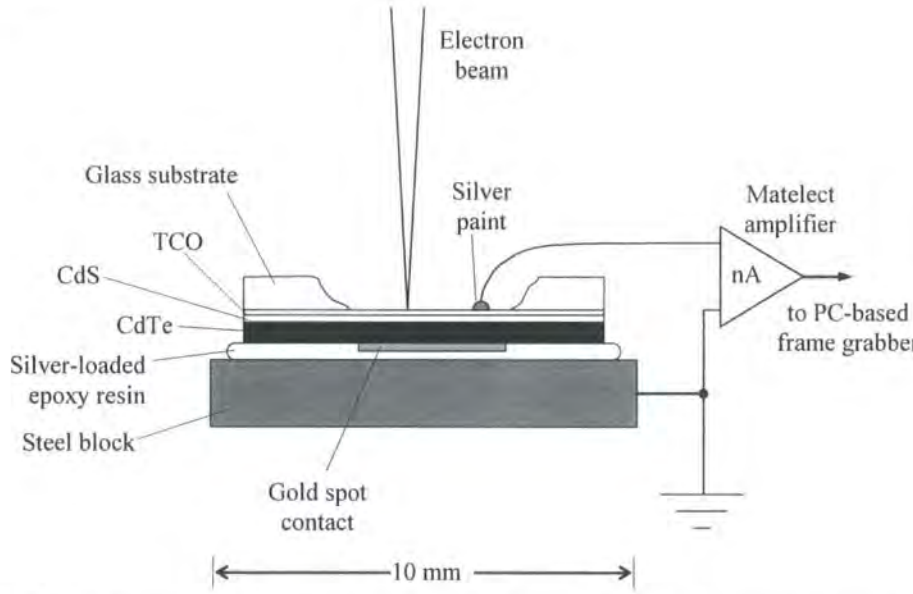


Figure 7-13 Experimental arrangement used for front-wall EBIC measurements [15].

Figure 7-14 shows a front-wall EBIC micrograph recorded at a beam voltage of 20 kV. Bright signal levels indicate high collection current while dark levels mark lower or no collection current due to recombination or poor junction properties for example. The cell presented was processed at 420°C with 20 nm $CdCl_2$ coating and

had a power conversion of ~5%. Considerable contrast can be seen at all length scales, especially 20-50 μm and ~5 μm. The origin of the former is unknown, while the latter is attributed to grains.

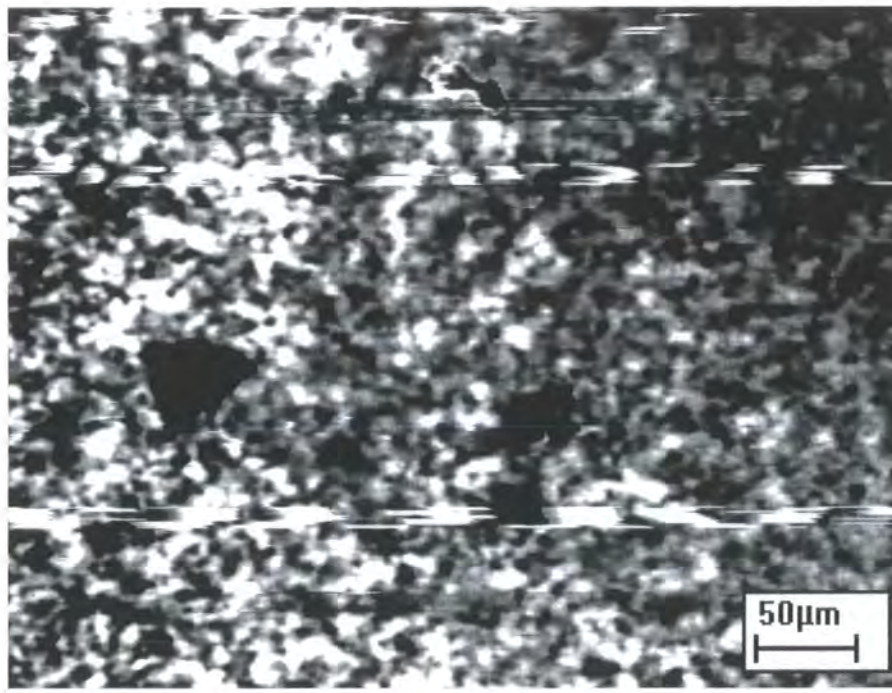


Figure 7-14 Front wall EBIC micrograph of a cell with 5% efficiency. Bright contrast represents high current collection. Performance variation is on the scale of ~20-50 μm and also on the scale of grains (5 μm). Note that the horizontal banding is due to electrical noise.

It can also be stated that the presence of pin-holes might be the origin of some of the different contrast levels. Pin-holes may originate from the growth of the thin CdS layer but it was also found that pin-hole formation was due to particles located at the surface of the substrate prior to growth as will be explained later in section 7.6.

7.5.2 Variation of Back-Wall EBIC Signal with Beam Voltage

Back-wall EBIC was used as a tool for investigating the junction position in the solar cell. This experiment is known to be difficult to interpret due to the surface roughness of the material and the strong absorption that occurs when bombarding with electrons (or illuminating with photons) the top layer of the cell [16] but it has been successfully used by Scheer *et al.* with chalcopyrite solar cells [17, 18]. For this

study the cells were used as-processed without any polishing or preliminary etching apart from the one used for the back contact formation.

7.5.2.1 Theory and Experimental Procedure

In an EBIC experiment, electron-hole pairs are generated by electron impact ionisation and collected at a rectifying contact. The method is used to determine the depth dependent collection function of the structure by measuring the collection efficiency of the cell as a function of the beam energy. The charge collection efficiency $\Sigma(E_b)$ is given by [17]:

$$\Sigma(E_b) = \int_0^\infty F(z)g(E_b,z)dz \tag{7-4}$$

where $g(E_b,z)$ is the generation function for minority carriers at a depth z and for a beam energy E_b. $F(z)$ is the collection probability as a function of sample depth z. The EBIC $I_c(E_b)$ is measured experimentally for different accelerating voltages and is correlated to the collection function $F(z)$ by the relation:

$$\Sigma(E_b) = \frac{E_i I_c(E_b)}{(1-f)E_b I_b} \tag{7-5}$$

where E_b is the energy beam, I_b the beam current, E_i the energy of ionisation of the semiconductor and f is the fraction of the backscattered electron.

$F(z)$ is specific to the material characterised and if $g(E_b,z)$ is known, $F(z)$ can be found using the experimental $\Sigma(E_b)$ and known assumptions about $F(z)$. The carrier rate generation function $g(E_b,z)$ also called depth-dose function is modelled using Monte Carlo simulation software developed by Napchan and Holt [19].

7.5.2.2 Monte Carlo Simulation of Carrier Generation

The Monte Carlo method is a general technique of statistical sampling employed to approximate solutions to quantitative problems. The trajectory of one electron or particle through the specimen is calculated using random numbers and this is repeated for a large number of electrons in order to give an accurate result of the process. The software uses known empirical expressions to calculate the electron range and trajectory. Repeating the calculation for thousands of electrons yields quantitative information about the rate of secondary electron emission. An example of this is shown in Figure 7-15, which shows a 40 keV electron beam bombarding

the back surface of a CdTe/CdS solar cell comprising of 70 nm Au, 3.5 μm CdTe, 120 nm CdS, 100 nm ITO and a thick substrate glass.

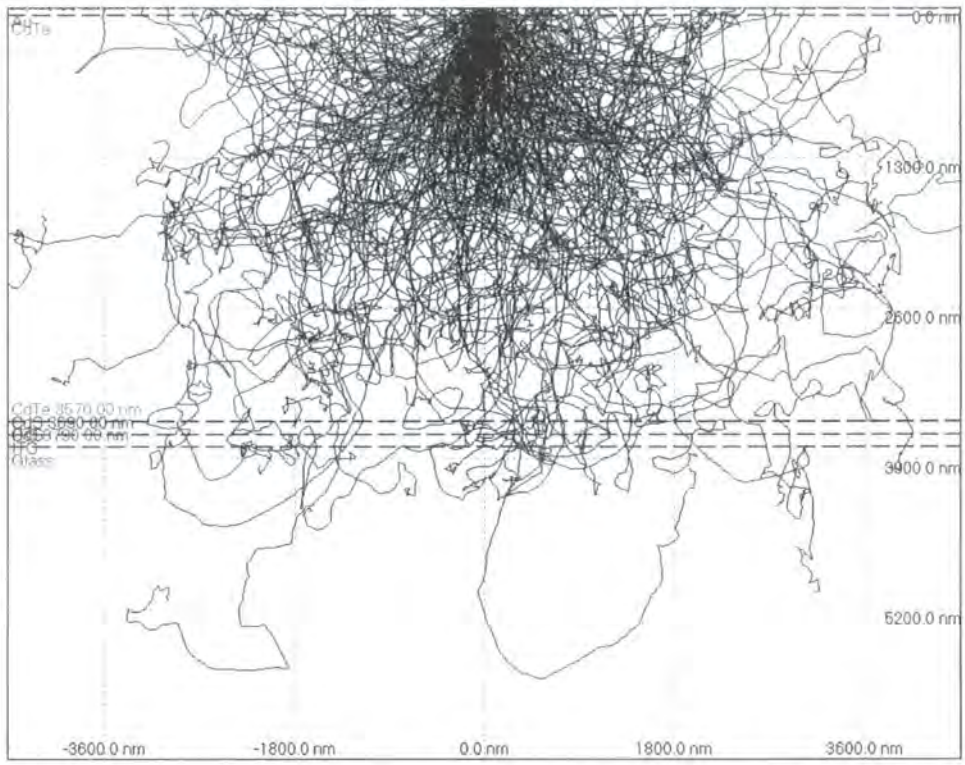


Figure 7-15 Electron trajectories of 500 electrons simulated with CASINO [20] showing the interaction of a 40 keV electron beam with a Au/CdTe/CdS/ITO/glass solar cell via the back-wall.

In order to fit the experimental EBIC data, simulations using 5×10^4 electrons were used to produce the depth-dose functions at the relevant beam accelerating voltage. Figure 7-16 shows a selection of depth-dose functions generated for a 20, 30 and 40 keV beam energy and in back-wall EBIC configuration. It can be seen that the rate of carrier generation rapidly decreases due to the absorption in the back contact and CdTe layer.

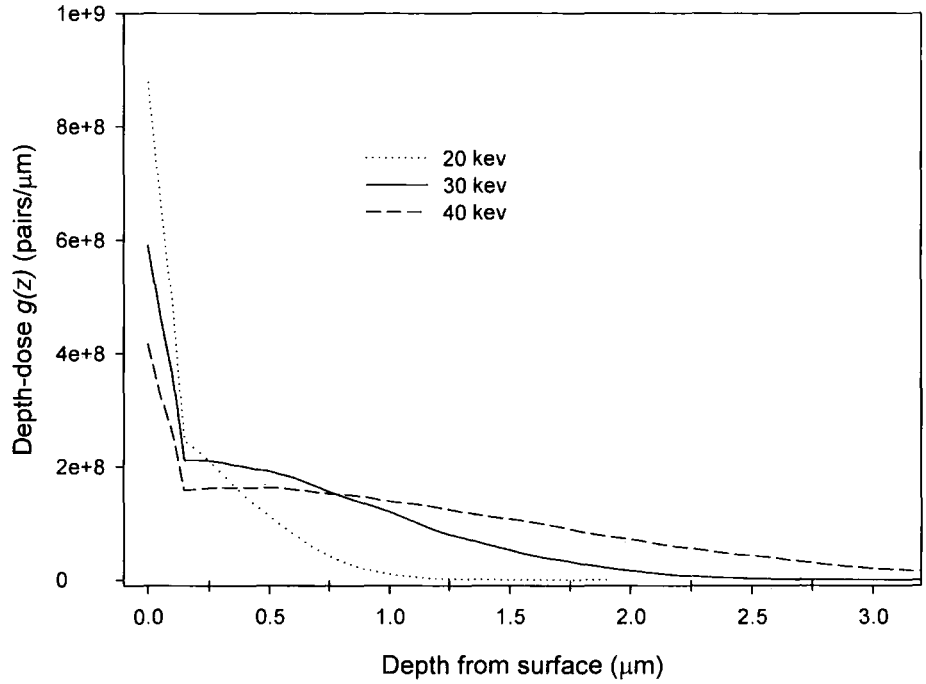
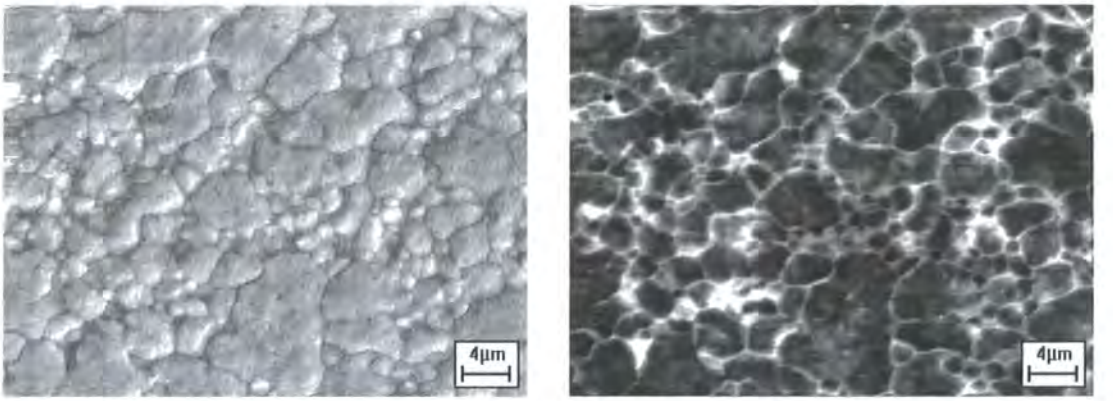


Figure 7-16 Depth dependent generation functions for back-wall Au/CdTe/CdS/ITO solar cell under electron beams of three different accelerating voltages. Functions simulated using Monte Carlo software with 5×10^4 electron trajectories for each curve.

7.5.2.3 Experimental Results

An SEM image and the equivalent back-wall EBIC image are shown in Figure 7-17 for a sample processed with 30 nm $CdCl_2$ at 500°C for 18 min. This sample has a power conversion of 5% (V_{oc} = 0.56 V, J_{sc} = 27 mA.cm^{-2}, FF = 35%). The SEM image reveals the polycrystalline morphology of the CdTe absorber. The region presented includes large grains (4-5 μm) with relatively flat surfaces and smaller grained regions forming a roughened surface. The polycrystalline nature of the film is also reflected on the EBIC image. Contrast difference between grains and grain boundaries is clearly seen and most collection current occurs when the beam is at the grain boundaries. This is purely a geometric effect: the grain boundaries are thin points in the layer and when the beam is incident at them it excites the junction more effectively than when it is at a grain centre. This was demonstrated for CSS-grown material by Galloway *et al.* [21].



a) SEM image **b)** Back-wall EBIC

Figure 7-17 a) Secondary electron micrograph of the surface morphology of a 5% efficient CdTe cell and b) corresponding back-wall EBIC image. Brightness of the EBIC image is proportional to the collection efficiency. Images were recorded at a beam voltage of 30 kV and a beam current of 72 nA.

Beam energy dependent EBIC results for the whole area of the images displayed above are presented in Figure 7-18. It must be noted that the measurements were carried out using a widely defocused beam in order to reduce the carrier injection density and hence eliminate the possibility of high-injection plasma effects occurring. It must be also noted that for the range of beam current used, the EBIC gain was independent of the beam current.

Figure 7-18 a) shows the charge collection efficiency $\Sigma(E_b)$ calculated from equation 7-4 as a function of the beam energy. For beam energies smaller than 20 keV the electron beam does not penetrate deep enough into the sample for carriers to be collected by the junction of the device and no induced current is measured. On increasing energy (20-40 keV) the carrier generation function begins to extend into the depletion region of the device, whence the carriers are collected by the junction with a higher efficiency. This results in an increase in the induced current detected. It is expected that for beam energy greater than 40 keV the collection efficiency will reach a maximum followed by a small decrease or a plateau, but higher beam energy could be achieved with the equipment used. However, the charge collection efficiency remains low, < 10%, even at high energy electron beams. The reasons for this will be explained later on.

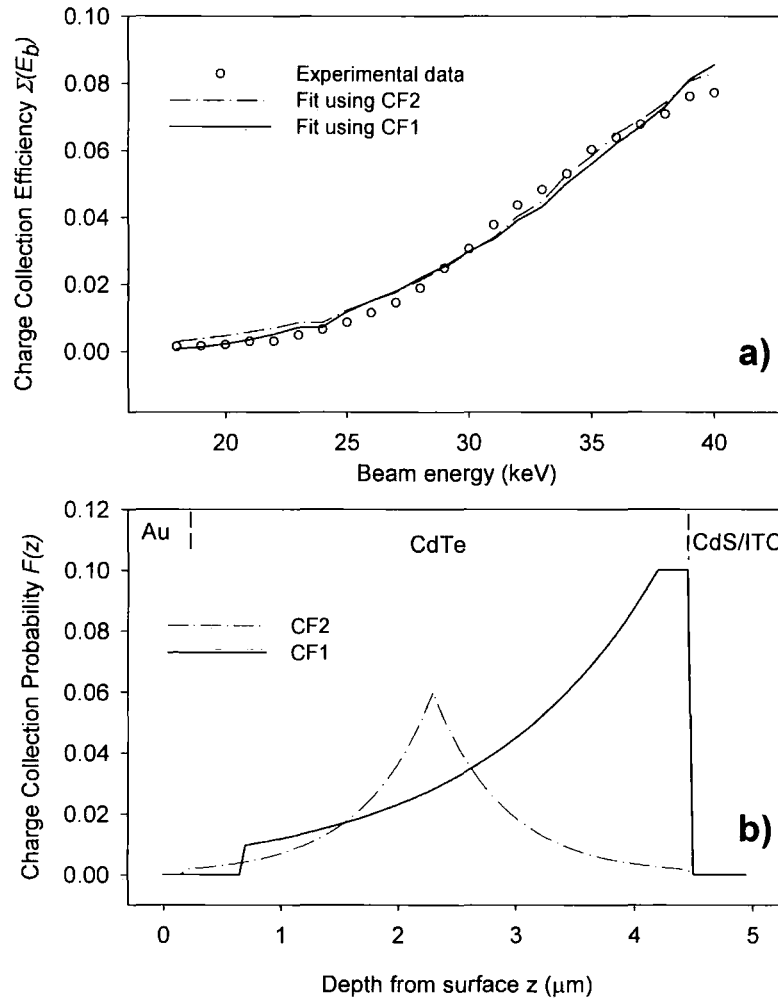


Figure 7-18 a) Collection efficiency of the CdTe solar cell as a function of the primary beam energy. b) Collection functions (CF) which were used for the fit as a function of depth.

Figure 7-18 b) describes the extracted collection function *F(z)* derived from equation 7-5. The data could be fitted with numerous collection functions but only two are presented here, CF1 and CF2. CF1 describes the collection function expected for a heterojunction solar cell. It assumes that (i) no collection occurs within the CdS and ITO layers due to the small minority carrier lifetime in theses layers; (ii) maximum collection occurs within the depletion region located in the CdTe absorber layer; (iii) the collection efficiency decreases exponentionally with distance from the edge of the depletion region in the neutral region of the absorber layer; (iv) no collection occurs in the back contact. This function could well describe the experimental behaviour of the EBIC as a function of the beam voltage but only when

the no-collection in the back region assumption was extended further into the absorber layer (z = 0.7 μm). However this is unlikely and other functions were investigated.

CF2 describes the function that can be ascribed to a buried junction. The assumptions for this function are as follows: (i) no collection occurs within the CdS and ITO layers; (ii) the collection increases exponentially from the CdTe/CdS interface; (iii) maximum collection in the depletion region occurs deep into the CdTe absorber layer; (iv) the collection function decreases exponentially away from the buried junction. The simulation indicated a very narrow depletion width (50 nm) located half way through the absorber layer. This collection function is in agreement with the spectral response measurements (Figure 7-8) which showed the presence of a buried heterojunction.

Four other collection functions were found to be appropriate to describe the collection efficiency of the solar cells investigated and therefore no conclusion regarding the properties of the junction could be made. However, more information is now known about the EBIC technique. Firstly, it can be seen that few electrons can reach the CdTe/CdS interface due to the strong absorption of CdTe and for beam voltage less than 25 kV no electron can reach the depletion region. This means that a small induced current is measured resulting in a small EBIC gain and charge collection efficiency. In this particular experiment less than 10% efficiency is achieved for an EBIC gain of ~400 at a beam voltage of 35 kV. By comparison, for a chloride treated CSS cell an EBIC gain of ~4000 for a charge collection efficiency of 90% was measured by Edwards *et al.* [22] in front-wall configuration at the same beam voltage. Although good contrast is observed in back-wall images, it is suspected that the absorber layer of the devices is too thick to allow quantification of the induced current $I_c(E_b)$ because electron penetration through the CdTe only just approaches the metallurgical interface for a 4 μm thick film and at a beam energy of 25 keV (see Figure 7-16). Therefore to increase the induced current it is necessary to prepare specimens with thinner CdTe absorber layer in order to allow maximum collection at the junction supposedly located at CdTe/CdS interface.

Figure 7-17 showed that brightness levels were higher at grain boundaries than at grain levels suggesting that current collection occurs mainly at grain

boundaries. This would be in direct opposition with the fact that one of the effects of the $CdCl_2$ post-deposition treatment is thought to passivate grain boundaries (see section 3.4). However, grains boundaries with deeper valleys measured from the top surface had even higher brightness levels. This suggests that back-wall image contrast is characteristic of the surface morphology of the absorber layer rather than the electronic properties of the material. By using a defocused beam in the energy dependent EBIC, both the grain boundary and grain centre responses were averaged. This made the possibility of a unique fit to a collection function less likely.

An attempt to quantify the front-wall induced current was done but this was unsuccessful due to the geometry of the device processed. The active area consisted of one ~2.5 mm diameter gold dot turned out to be too small for the preparation of good front-wall EBIC specimens.

7.6 Influence of CdS Thickness and the ITO Substrate Type

Each growth run of the SET 3 sample series had a specific window layer thickness, i.e. 120, 240 and 500 nm. Devices with 4 μm CdTe and with a CdS thickness of 120 nm were produced and analysed for various post-deposition treatment as detailed in the previous sections. On the other hand, devices with 240 nm thick CdS layer had limited efficiency (~0.5%) and no photoresponse was observed from devices made from structures with 500 nm thick CdS. Figure 7-19 shows the transmittance spectra of 120, 240 and 500 nm thick CdS layers grown on ITO/glass at 300°C. Reduced transmission was observed for wavelengths below 500 nm for the 120 nm thick layer while the other two layers absorb all the photons. At higher photon energies the transmittance decreases with increasing CdS thickness. This is due to the low hole lifetime and high recombination that occurs within the CdS layer and therefore it is necessary to minimise the CdS thickness.

The absorption coefficient, α, is given by the relation:

$$T = (1 - R)^2 \exp(-\alpha d) \tag{7-6}$$

where T is the transmittance, R is the reflectance and d is the thickness of the film. Assuming negligible reflections yield:

$$\alpha = -\frac{1}{d}\ln T \tag{7-7}$$

The absorption coefficient is closely related to the energy bandgap of the material studied and is for a direct bandgap material [23]:

$$\alpha = \frac{C}{h\nu}\left(h\nu - E_g\right)^{1/2} \tag{7-8}$$

where E_g is the material energy bandgap, $h\nu$ the photon energy and C a constant. Therefore a plot of $(\alpha h\nu)^2$ versus $h\nu$ yields the energy bandgap of the film investigated at the intercept of the linear portion of the curve with the photon energy axis. This is shown in the inset of Figure 7-19 for the three films studied here. In all cases, the measured energy bandgap was 2.41 eV which is close to the usual reported value for CdS (2.42 eV at 300 K). Figure 7-19 is sufficient in itself to explain the influence of thick CdS films on the performance of solar cells.

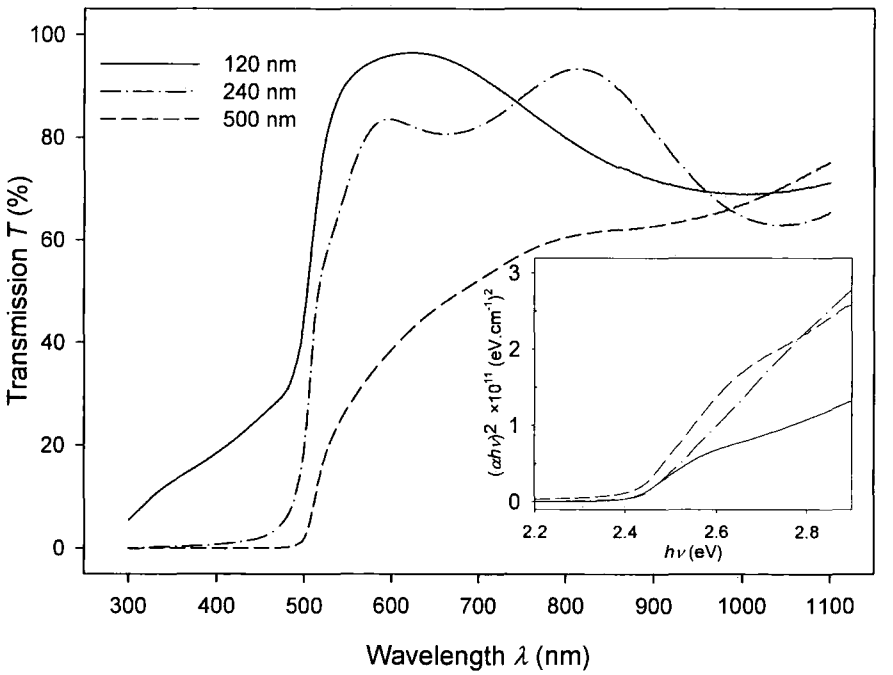


Figure 7-19 Transmittance of 120 nm (solid dark line), 240 nm (dashed-dotted line) and 500 nm (dashed line) thick MOCVD-grown CdS layers.

Two different substrates, detailed in section 7.2.1, were used through the course of this work and both gave similar results. Although no experiment was done to identify any possible influence of the TCO/glass substrates, they are not the

limiting factor in this study as ~4 μm devices grown on the two different substrates (SET 2 and 3) had similar efficiencies. However, the pre-growth cleaning process of the substrate revealed to be of particular concern. Devices from SET 2 used a standard cleaning process and when devices were processed at high temperature (480-500°C) shunts formed at the CdTe surface, killing the devices. This was not observed with devices made from SET 3 and it is thought to be due to the thorough cleaning of the substrate. The process involved cleaning in an ultrasonic bath filled with deionised water for 10 min followed by refluxing in toluene for one hour [24]. This procedure produced much cleaner surfaces and was adopted for growing the structures of SET 3.

Shunts are believed to be created by the removal of the particles (~10 μm) present at the substrate surface following cell processing, e.g. device transport between the different processing steps are likely to be the main causes. These particles are bigger than the layer thickness and their removal before the application of the back contact allows direct connection between front and back surface yielding short-circuiting paths. These particles also created pin-holes in the window layer and pin-holes can be an important factor of reduced performance of the devices. Indeed, it was demonstrated by McCandless *et al.* [25] that 1% of fractional area of holes in the CdS film would reduce the open circuit voltage by 300 mV and would therefore increase the diode current (J_0) by several orders of magnitude resulting in a reduced fill factor.

7.7 Discussion

CdTe/CdS solar cell structures grown by MOCVD were $CdCl_2$-treated and characterised by means of current-voltage and microscopy measurements. It was demonstrated that the power conversion of the solar devices is dependent on the thickness of the two semiconductors. Only structures with a 4-6 μm thick CdTe absorber could be processed into efficient solar cells. Processing cells with absorber layer thickness of 2-3 μm and 8-12 μm resulted in inefficient devices. Among the devices with 4-6 μm thick CdTe, only structures with 120 nm thin window layer were efficient. It is concluded that the 2 μm thin structures did not survive the post-deposition treatment conditions. On the other hand, the reasons of failure of the 8-

12 μm devices remain unclear. It is suggested that the poor conductivity of the absorber layer may be the cause of these results. Low conductivity arises from the fact that the CdTe layer presented non-columnar grains, and therefore the conduction is limited by the high density of grain boundaries.

However, solar cell devices were produced and the influence of the post-growth treatment conditions was demonstrated. Best devices were made with cells processed at 420°C for 18 min with 30 nm of $CdCl_2$. This is in good agreement with other work published [26-28]. During the $CdCl_2$ heat treatment of MOCVD-grown CdTe/CdS solar cells, significant recrystallisation of the absorber layer occurred. This grain growth is temperature dependent and also slightly dependent on the material thickness. While no significant recrystallisation was observed for the thin structure treated at relatively low temperature (360-400°C), thicker devices had grain growth occurring from 380°C. Increasing the temperature to 500°C yielded an increase in the average crystallite size by a factor of 2.5 compared to 380°C. However, for the thickest devices (8-12 μm) recrystallisation was more limited, with grain sizes increasing by a factor of ~1.8 between 420°C and 500°C. The absence of recrystallisation for the thinner structures is due to the fact that the cells examined were grown at 400°C and the treatment performed at temperatures below the growth temperature cannot provide significant energy for the driving forces of recrystallisation of the absorber layer.

The $CdCl_2$ treatment was shown to improve the cell performance. Significant improvements were observed for treatment temperatures of 420°C and above with the best results obtained at 420°C. As the largest crystallite size was obtained for the highest processing temperature this indicated that grain growth of the small-grained absorber layer is necessary but only to a certain extent for producing efficient devices and that other phenomena induced by the $CdCl_2$ treatment are to be considered. The apparition of holes at the grain boundaries observed on samples treated at higher temperatures (Figure 7-12) may be one of them: at high annealing temperature, the CdTe starts to disintegrate and the etching step accentuates this, yielding intergrain gaps. Best devices were achieved for limited $CdCl_2$ thickness (~30 nm) and increasing this reduced the device performance. This may be due to (i) the doping limit of chlorine in CdTe being reached. Because the solubility of $CdCl_2$ in CdTe is

low [29], the grain boundaries are rich in $CdCl_2$ and hence there is a gradient of electrically active species near the grain boundaries [30]; (ii) it is also well known that the addition of chlorine in CdTe can produced highly restive CdTe crystals [31, 32]. This is also true for the layers used in this work as reported in Chapter 5. This would seriously affect the conduction in the absorber layer.

The study of dark and light current-voltage characteristics showed that devices had poor junction parameters affecting mainly the open circuit voltage and fill factor. Low shunt resistance, high series resistance, diode quality factor and reverse current were measured. The high series resistance values arise firstly from the resistivity of the TCO and active layers but also possibly from potential barriers located at grain boundaries in the absorber layer and at the back contact junction. The high reverse current indicates a low carrier lifetime and the high diode factor suggests that the tunnelling transport mechanism is dominant in the devices. A tunnelling transport mechanism would be promoted by the presence of a barrier located either near the front or back contact [33]. Under low light intensities the diode factor decreased to $A \sim 2$ indicating a change in transport mechanism corresponding to a junction dominated by defect recombination via mid-gap states in the space charge region. This excess forward recombination current is responsible for the high diode factor and is mainly due to the polycrystallinity of the layers [34]. The presence of a buried junction was supported by quantum efficiency measurements which revealed the presence of such an interface. Although this could not be confirmed by EBIC measurements, it was not disputed, as a collection function corresponding to a buried junction could fit the data recorded in back-wall measurements (Figure 7-18).

Front-wall EBIC imaging showed the important variations of collection efficiency at the junction especially at a grain level. This was illustrated by strong variation of the image contrast on a grain scale (Figure 7-14). The grain to grain contrast variations are caused by changes in recombination and/or collection efficiency. The recombination rate at the interface may be position dependent in the substrate plane due to variations in the density of point or structural defects from grain to grain. The depth position of the electrical junction may vary and also be position dependent. This would also cause different levels of contrast on an EBIC

image. The position of the junction depends on the abruptness of the metallurgical interface and the doping concentration on the two sides with variations in concentration impurity influencing this. Grains with a shallower junction will therefore collect more beam-generated carriers, yielding an increased induced current.

7.8 Conclusion

The activation of solar cells grown by MOCVD using a $CdCl_2$ post-growth treatment was studied extensively using 200 trial dot-contacted devices. The process was successfully applied to MOCVD-grown CdTe/CdS structures and results showed an increase in performance from the as-grown state to the treated state by a factor of ~10, from ~0.3 to ~6%. The devices are limited by their junction parameters and the type of transport mechanism characterising these structures. Also there are definite concerns about the as-grown performance which are very low ($\eta \sim 0.5\%$).

One of the main findings of this study is that the performances are dependent on the thickness of both CdS and CdTe layers. Efficient devices could only be produced using ~4 μm thick CdTe coupled with a 120 nm CdS window layer. Other structures were inefficient. A set of optimum post-deposition heat treatment parameters were derived for the samples investigated and the most efficient devices were produced using a 30 nm $CdCl_2$ layer followed by an 18 min annealing at 420°C. The cell parameters were $\eta = 6\%$, $J_{sc} = 30$ mA.cm^{-2}, $V_{oc} = 0.595$ V and $FF = 35\%$. The short circuit current density was the cell parameter that was most affected by the changes in the post-deposition heat treatment.

The performances of the devices were limited by the low fill factor arising from low shunt resistance and high series resistance and diode quality factor: shunt resistances of 1060 and 140 Ω.cm^2, series resistances of 6.8 and 2.1 Ω.cm^2 and diode factor of 2.4 and 4.4 were derived from *J-V* measurements for a 5% efficient device in the dark and under illumination, respectively. The junctions of efficient devices were investigated using spectral response and EBIC measurements. Maximum quantum efficiency was recorded near the CdTe band edge indicating a buried junction. Analysis of the variations of the back-wall EBIC confirmed that maximum collection efficiency occurred in the absorber layer and not at the metallurgical

junction. This indicates that the devices are characterised by high recombination losses and high reverse saturation current densities (J_0 = 1.6×10^{-3} mA.cm^{-2} in the dark).

In order to assess the reason why thick devices (8-12 μm) were not performing, structures with different thicknesses were examined using impedance spectroscopy in order to gain in-depth information about the device junction and this is outlined in the next chapter.

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Chapter 8

AC Impedance Measurements

8.1 Introduction

It was demonstrated in Chapter 7 that the low performance of CdTe/CdS solar cells grown by MOCVD is linked to the thicknesses of the two semiconductors. Influence of the window layer thickness is generally understood in terms of low minority carrier lifetime and high recombination rate occurring in the CdS layer. However, the reason that efficient devices ($\eta \geq 5\%$) produced only from structures with ~4 μm thick absorber layers remains unclear. It is understood that thin absorbers (2 μm) cannot sustain the post-deposition conditions employed in this work but on the other hand the reasons for the failure of structures with thick absorber (12 μm) are still unproven. The polycrystalline nature of the CdTe layers used (they have small non-columnar grains) and their very low conductivity seem to be the main reason. However, junction phenomena cannot be ruled out and this is the subject of the investigation in this chapter where they are studied by means of small AC signal spectroscopy.

Impedance analysis is a powerful tool for investigating the electrical properties of specimen of almost any kind. Impedance measurements enables a

qualitative analysis of the electric behaviour leading to an equivalent circuit model for the sample under investigation and quantitative contributions of the respective circuit elements to the overall impedance can be determined. Impedance analysis can also be used as a tool for investigating deep impurity levels, i.e. impedance spectroscopy [1], and ideally can allows the determination of the energy, carrier capture cross section, concentration, and spatial profile of each electrically active defect. Alternating current impedance spectroscopy has been widely used to analyse electrolytic solutions in order to gain separate information about cathode and anode reactions [2]. The technique has also been developed for the analysis of solid electrolytes and solid materials in general. It is capable of distinguishing between bulk, grain boundary and sample-electrode interface effects. Particular interest for solar cells is the extraction of complex, real and imaginary capacitances characteristic of the *p-n* junction. Parallel analysis and correlation can also be made with capacitance-voltage measurements.

It is necessary, at this point, to stress to the reader that this chapter is not an extensive or complete impedance spectroscopy study but comes as complement to support the investigations presented earlier and should be viewed as a way of further understanding the CdTe/CdS thin film solar cell.

8.2 Theoretical Approach

Impedance spectroscopy enables the determination of the frequency dependence of the real and imaginary parts of the impedance. This technique is equivalent to admittance spectroscopy as both quantities are closely related as will be shown next. Using a suitable electrical circuit model, real and imaginary parts can then be translated into physical properties such as capacitance and conductance. The technique was first developed by Losee [3] and has several times been applied to CIS-based devices [4-6]. The technique has also recently been applied to CdTe/CdS solar cells by Gilmore *et al.* [7].

The impedance Z^* is defined by:

$$Z^* = \frac{V^*}{I^*} = \frac{V_m \sin(\omega t)}{I_m \sin(\omega t + \varphi)} = Z' + jZ'' \tag{8-1}$$

where * denotes the complex nature of the measurement, ω is the angular frequency of the applied voltage, V^* is the time (t) dependent voltage, V_m is the amplitude of the applied signal. I^* is the resulting current through the sample with I_m its amplitude and φ the phase shift with respect to the input voltage. Z' denotes the real part of the impedance and Z'' the imaginary part. Similarly the admittance is defined as:

$$Y^* = \frac{1}{Z^*} = Y' + jY'' \tag{8-2}$$

From Z^* and Y^* "series" and "parallel" terms are identified:

$$\text{Series resistance: } R_s = Z' \tag{8-3}$$

$$\text{Parallel resistance: } R_p = \frac{1}{Y'} = \frac{1}{G} \tag{8-4}$$

$$\text{Series capacitor: } C_s = \frac{1}{\omega Z''} \tag{8-5}$$

$$\text{Parallel capacitor: } C_p = \frac{Y''}{\omega} = C \tag{8-6}$$

where G and C will be referred as the conductance and the capacitance of the device from this point.

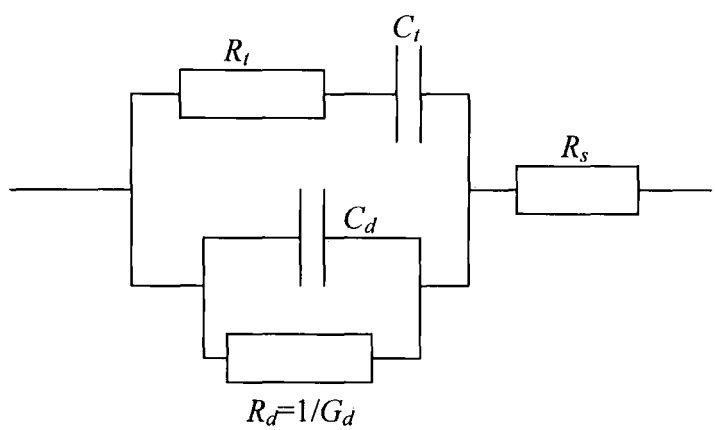

Figure 8-1 Schematic of the standard model used for admittance spectroscopy of CdTe based solar cells [8, 9].

The basic standard electrical model of a solar cell used for impedance spectroscopy analysis is shown in Figure 8-1 [8, 9]. This model consists of a single diode (and assumes an ohmic back contact), of capacitive and conductive elements C_d and G_d in parallel. The diode is coupled in parallel with series connected capacitance and resistance elements, C_t and R_t. These account for the deep level

(trap) response to the applied oscillating voltage. A series connected resistor R_s accounts for the resistance of the layers.

Using thermal impedance spectroscopy it is possible to determine the activation energy, density of states and capture cross section of deep trap levels due to their contribution to the total capacitance of the system. As the frequency modulation of the input AC signal changes, the trap capacitance C_t will also change, decreasing for frequency ω greater than the trap characteristic frequency ω_t and increasing for $\omega_t < \omega_t$ [4, 5]:

$$C_t \propto \frac{1}{1+\left(\omega/\omega_t\right)^2} \tag{8-7}$$

where ω is oscillation frequency of the input signal, ω_t is the characteristic frequency for the defect and C_t is the trap contribution to the total capacitance.

The trapping and detrapping of deep levels generated by small AC signals occurs at the characteristic frequency ω_t and is given by the relation [9]:

$$\omega_t = 2\upsilon_0 \exp\left(-\frac{E_t}{kT}\right) \tag{8-8}$$

with $\upsilon_0 = \sigma_p \upsilon_{th} N_V$ (8-9)

where k is the Boltzman constant, T is the temperature, υ_0 is the "attempt-to-escape frequency", N_V is the effective density of states in the valence band, σ_p is the capture cross section for holes, υ_{th} is the carrier thermal velocity and E_t is the defect energy level above the valence band. The capture cross section is assumed to be temperature independent whereas N_V and υ_{th} vary as function of $T^{3/2}$ and $T^{1/2}$, respectively. Rearrangement of Equation 8-8 yields:

$$\ln \omega_t = \ln(2\upsilon_0) - \frac{E_t}{kT} \tag{8-10}$$

Therefore an Arrhenius plot of the natural logarithm of the characteristic frequency ω_t divided by T^2 (to account for the temperature dependence of N_V and υ_0) versus the inverse temperature yields the determination of E_t and υ_0 from the slope and intercept of the graph, respectively.

It is then easy to extract the capture cross section for the deep level investigated using Equation 8-9 and calculated values of N_V and υ_{th} [10]: N_V = 1.8×10^{19} cm^{-3} and υ_{th} = 1.3×10^{7} cm.s^{-1}. Finally, the determination of the defect density of states $N_t(E_\omega)$ from thermal admittance spectroscopy is possible and has been performed by Walter *et al.* [6] for a *n-i-p* and n^+-*p* junctions. It was shown that for an n^+-*p* junction which corresponds closely to the band diagram of a CdTe/CdS solar cell:

$$N_t(E_\omega) = -\frac{2V_{bi}^{3/2}}{x_d\sqrt{q}\sqrt{qV_{bi}-(E_g-E_\omega)}}\frac{\omega}{kT}\frac{dC}{d\omega} \tag{8-11}$$

where V_{bi} is the built-in voltage, x_d is the width of the depletion region, E_g the energy bandgap. Similarly, an expression can be derived from the conductance G using the relation between conductance and capacitance [11]:

$$G(E,\omega) = \frac{\omega^2}{\omega_t}C(E,\omega) \tag{8-12}$$

and therefore:

$$N_t(E_\omega) = -\frac{2V_{bi}^{3/2}}{x_d\sqrt{q}\sqrt{qV_{bi}-(E_g-E_\omega)}}\frac{\omega^2}{kT}\frac{d}{d\omega}\left(\frac{G}{\omega^2}\right) \tag{8-13}$$

8.3 Experimental Details

Two CdTe/CdS structures processed and presented in the previous chapter were selected for impedance spectroscopy studies. Sample A was a 4 μm CdTe/120 nm CdS structure grown on an ANTEC substrate and sample B was a 12 μm CdTe/120 nm CdS structure grown on a MDT substrate. Both structures received similar post-deposition heat treatment comprising the deposition of a 40 nm $CdCl_2$ layer followed by annealing for 18 min at 420°C and both were finished with the nitric/phosphoric acid etch. Sample A had a power conversion of 5% while sample B exhibited no significant photoresponse. The *J-V* curves of these samples recorded under AM1 .5 illumination are shown in Figure 8-2.

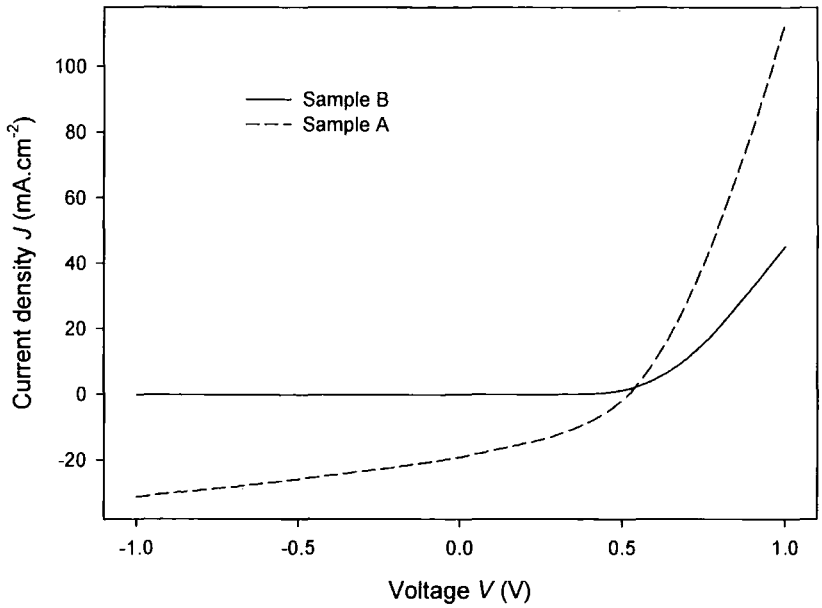

Figure 8-2 Current-voltage curves recorded under AM1.5 illumination for the two samples used in this chapter.

Impedance measurements were performed using a Solartron 1260 Frequency Response Analyser (FRA) and a 1296 dielectric interface. The 1260 FRA supports frequencies varying from 10 μHz to 32 MHz for sample impedances between 100 mΩ and 100 MΩ. The use of the dielectric interface reduces the frequency range (10 mHz–10 MHz) but allows ultra low current to be driven through the sample making it possible to analyse specimens with impedance over 100 TΩ. The amplitude of the AC signal was 20 mV for frequencies from 1 Hz to 1 MHz at ten values per decade. For thermal admittance measurements, the samples were mounted in a low vacuum cryostat with a closed cycle cooling/heating system by Janis Inc. The sample temperature was varied in 5K steps between 30 and 350 K using a Lakeshore temperature controller.

8.4 Thermal Admittance Results

The frequency dependence of the device capacitance $C(f)$ and the contribution of traps to the device conductance $G(f)$ for different temperatures are displayed in Figure 8-3 for samples A. To separate the contribution of traps to the conductance, the DC conductance determined at low frequencies was subtracted to

the measured values. This accounted for leakage currents that would increase the conductance.

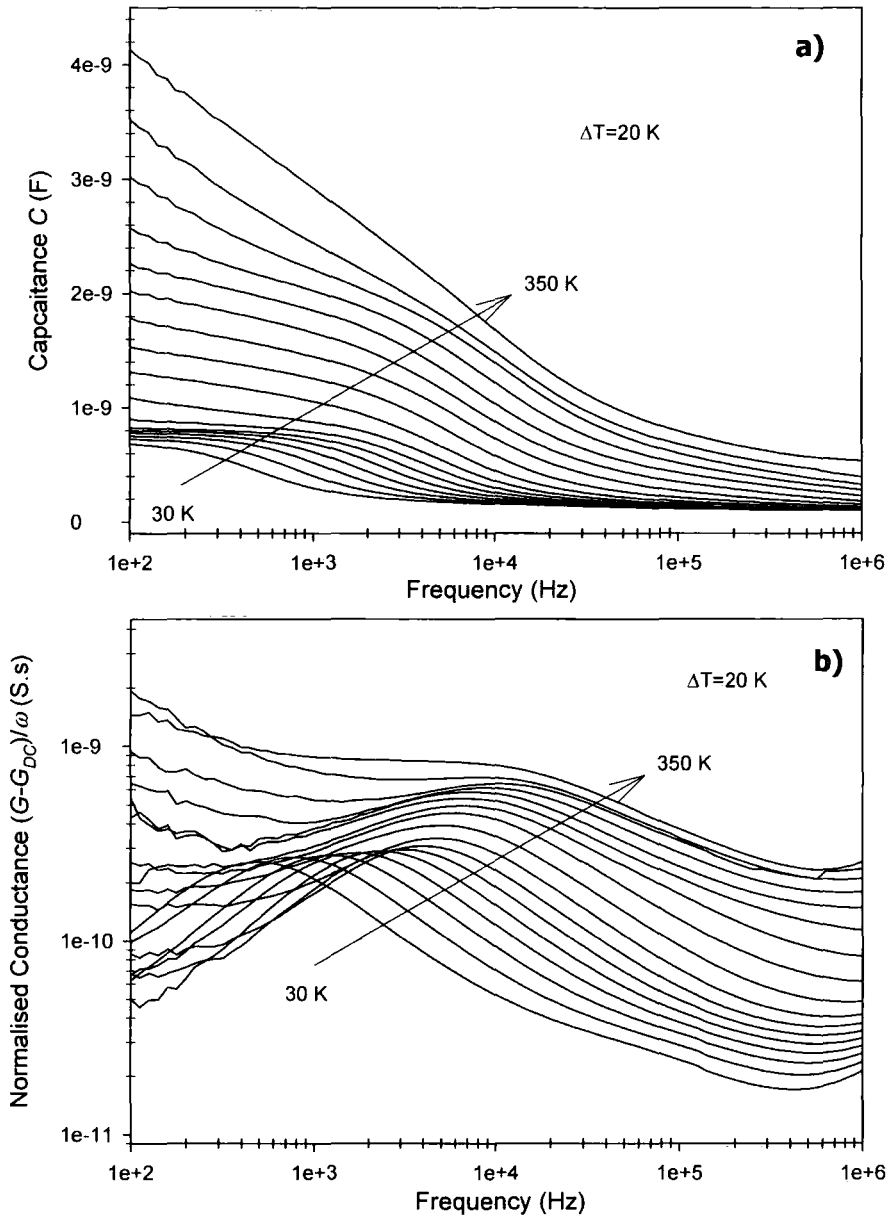

Figure 8-3 Temperature dependent admittance measurements (20 K steps) on sample A. a) frequency dependence of the capacitance, b) frequency dependence of the trap contribution to the device conductance.

It can be seen that the shape of the capacitance curves depends strongly on temperature and frequency (Figure 8-3 a). At low temperatures (30-130 K), the capacitance falls off from a low frequency value of 0.8 nF after the first decade of frequency. The cut-off frequency lies initially at 500 Hz and increases with

temperature. For this range of temperatures, the capacitance curves are converging at high frequency to a value of ~0.15 nF. For higher temperature (T > 130 K) a strong decay in capacitance occurs already at low frequency and is more pronounced as the temperature increases. The curves also seem to be converging at high frequencies. The capacitance on the low frequency side of the plots is fairly constant at low temperature (30-130 K). This is interpreted as the depletion capacitance of the *p-n* junction. At higher temperatures, deep levels make the main contribution to the capacitance. This is indicated by the strong dependence of C on both temperatures and frequencies.

The conductance is also frequency and temperature dependent (Figure 8-3 b). A peak is observed for each curve corresponding to the presence of a defect. However, it can be seen from the figure that inaccuracies in the determination of the DC conductance have a large impact at low frequencies of the spectra indicated by the curves bending upward. This is because at low frequencies the conductance is oscillating around a minimum value and the exact determination of this minimum is difficult and yields errors which are embedded at low frequencies.

The low temperature (T < 130 K) capacitance step (Figure 8-3 a) is attributed to the freeze out of the free carriers [5]. Because the main contribution to the capacitance is the depletion capacitance caused by the swing of the free carriers at the edges of the space charge region, at low temperature, the free carriers are moving too slowly to compensate the electric field of the applied AC voltage.

Due to the Kramers-Kronig relations [12], the same information is comprised in the real and imaginary part of the admittance and is independent of the way the spectra are displayed. The Arrhenius data was derived from the capacitance and the normalised conductance spectra. In the first case, the cut-off frequency is yielded by the minimum of the derivative $\omega dC/d\omega$ and in the second case by the maximum of the $(G(\omega)-G_{DC})/\omega$ curve itself. Due to the broad defect distribution in CdTe-based cells, the extremes are not very pronounced, but relevant information was extracted and is plotted in Figure 8-4. It can be seen that both extraction technique gave similar results.

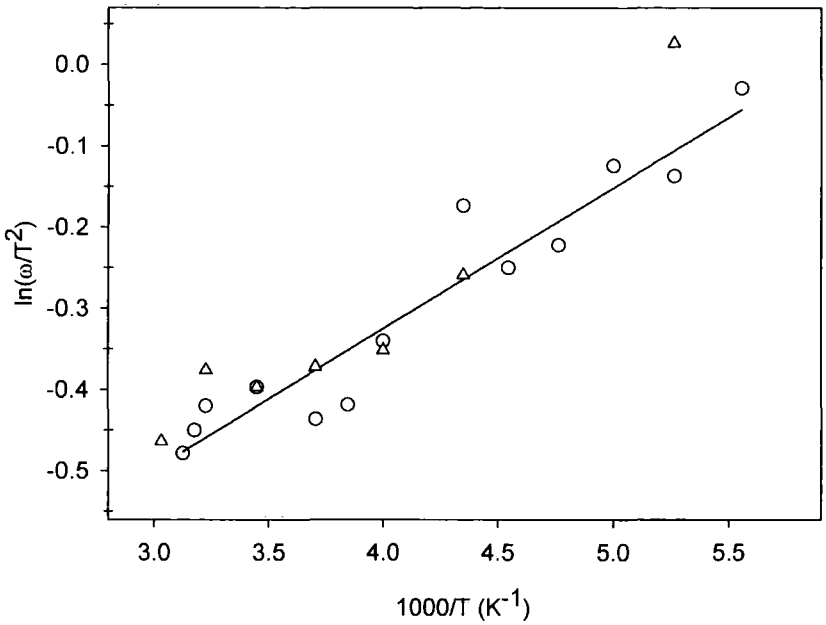

Figure 8-4 Arrhenius diagram using data extracted from $C(\omega)$ (△) and $(G\text{-}G_{DC})/\omega$ (○) spectra of sample A.

However, from this data an attempt-to-escape frequency and activation energy of the defect cannot be extracted as the slope of the graph is positive and Equation 8-11 require a negative slope. This can be anticipated by looking closely at the conductance plots of Figure 8-3 b): the peak position changes only slightly with temperature. Therefore the subsequent defect density of states could not be estimated. This anomalous behaviour has also been observed on CdTe/CdS solar cell provided by ANTEC by Proskuryakov [13] who studied the influence of the nitric/phosphoric etching time on the admittance plots. The cells studied had about the same efficiency as sample A ($\eta \sim 6\%$). But the anomalous Arrhenius plot behaviour was found to be a function of the CdTe etching time: it occurred following etchings of 20 s or longer. However, to date, this behaviour is not fully understood. Other authors [6, 14] have suggested that the temperature dependencies of υ_{th} and N_V can be neglected. Using this assumption, the plot of ω versus $1/T$ is a straight line and the slope is negative yielding a value of 6.4×10^4 s^{-1} for υ_0 and 21 meV for E_t. This would give a hole capture cross section of $\sigma_p = 3.7\times10^{21}$ cm^2. It is evident that those values are not characteristics of deep levels and that the above assumption cannot stand in the present case.

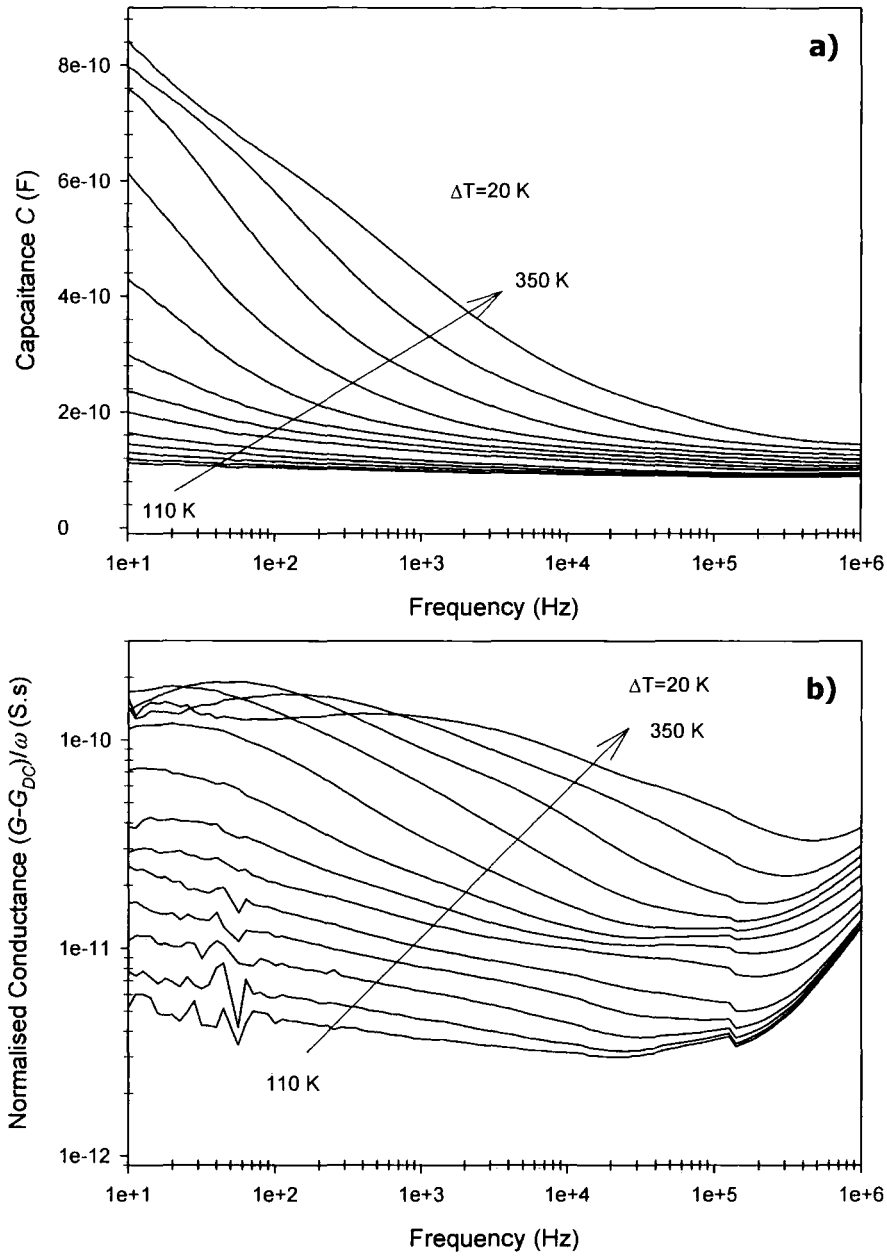

Figure 8-5 Temperature dependent admittance measurements (20 K steps) on sample B. a) frequency dependence of the capacitance, b) frequency dependence of the trap contribution to the device conductance.

Capacitance and conductance spectra for sample B are presented in Figure 8-5. The shape of the curves is noticeably different for those of sample A (Figure 8-3). The conductance curves decrease monotonously when the frequency is varied, with no inflection point apart from the ones at the extremities of the spectra, these being due to uncertainties on the estimation of the DC conductance. No drop-off can

be seen on the capacitance spectra and no peak was found when calculating the derivative of the curves. For temperature range 110-210 K the capacitance varied little with frequency, while it decreases continuously at higher temperatures. The derivative plot of the capacitance did not reveal the presence of any inflection points. Compared to sample A, the capacitance and conductance curves of sample B are more converging at high frequencies. According to Kneisel *et al.* [4], this would indicate higher series resistance of the solar cell. Effectively, the dark and light resistances measured across the structure were 100 times higher for sample B and this can be seen on the Z'-Z'' plots shown in Figure 8-6. The amplitude of both the real part and imaginary part of the impedance is two orders of magnitude greater for sample B.

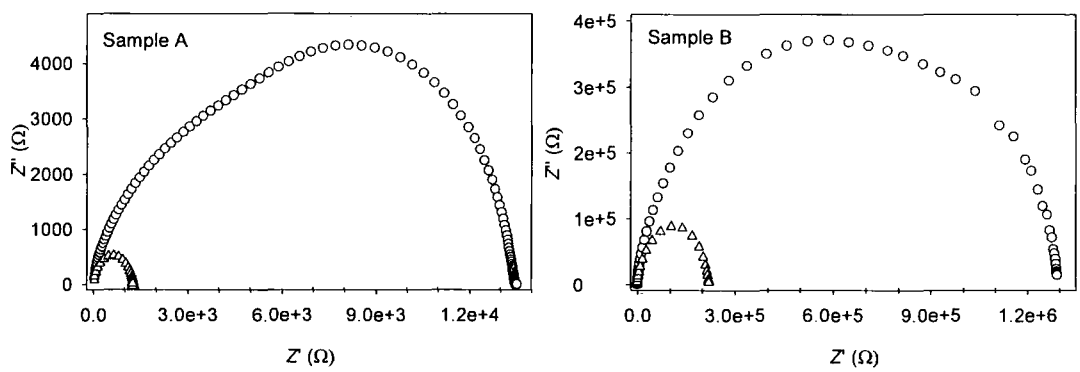

Figure 8-6 Nyquist plots (Z'' versus Z') of sample A and B measured at room temperature in the dark (O) and under AM1.5 illumination (△).

One of the uses of AC measurements is to find a suitable equivalent circuit model to describe the behaviour of the impedance. Modelling the data of Figure 8-6 using the electrical circuit of Figure 8-1 proved unable to describe the variations of the impedance with frequency either in the dark or under illumination. Although the data recorded under illumination could be fitted with a semi-circle representing a parallel *RC* sub-circuit in series with a resistor, this model could not be applied to the data recorded in the dark. In this case, the shape of the Nyquist plot depends on the sample as can be seen in Figure 8-6. For sample A, the shape of the Z''-Z' plot is similar to that representing a double semi-circular diagram. This would be characteristic of double *RC* sub-circuits in series with a resistor, a model that is usually applied to describe the current-voltage and capacitance-voltage

characteristics of CdTe/CdS solar cells [15]. This model was, however, not applicable to sample B. It is therefore necessary to find a suitable electrical model capable of describing simultaneously the behaviour of the devices under different light and bias conditions, and the use of a more advanced model is required. It has been shown in the case of dye-sensitized solar cells that the electrochemical behaviour of the device can be described using a transmission line-based model [16, 17] and it is thought that such a model could also be suitable to describe the performance of CdTe/CdS thin film solar cell. This would require further investigations and this is beyond the scope of this work.

8.5 Conclusion

In this chapter, the use of impedance (or admittance) spectroscopy for the characterisation of CdTe/CdS solar cell has been documented. From thermal admittance measurements, the usual behaviour of solar cell (with conventional thermally activated behaviour described by an Arrhenius plot with a negative slope) as observed in references [4-6] has not been detected in this study. The efficient device (sample A) investigated here showed anomalous Arrhenius behaviour that has been attributed to a contribution from the etching step required in processing devices. It is possible that the etching produced semi-metallic leakage paths that act to change the junction response under AC stimulation. It was therefore not possible to extract trap energies from the data. In the case of sample B, a thick and inefficient solar cell structure, the classic capacitance and conductance plots were not observed, and this is thought to be due to the high resistivity of the absorber layer. Modelling of Z''-Z' response using simple equivalent circuits was unsuccessful. This indicates that the materials have a complex response, and that its description by the transmission line models used for dye sensitised solar cells may meet with more success.

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Chapter 9

Conclusions

9.1 Summary of Conclusions

This thesis has documented the use of MOCVD for the growth of thin film materials for use in solar cells. In particular, this work was concerned with the characterisation of CdTe thin films doped with arsenic, and of CdTe/CdS solar cells following the post-deposition heat treatment with cadmium chloride. For characterisation purposes, some new experimental techniques were set up and some specific designs were implemented in order to facilitate their use. Also control programs were written in some cases for data acquisition.

At first, in Chapter 5, this work focussed on the electrical and structural characterisation of *in situ* arsenic doped MOCVD-grown CdTe thin films on sapphire. The initial objective was to provide a high conductivity *p*-type CdTe films for solar cell applications. The organometallic precursors used for the growth of CdTe:As layers were dimethylcadmium (DMCd), di-isopropyltelluride (DIPTe) and dimethylamino arsine (DMAAs). It was demonstrated that for a growth temperature of 400°C the arsenic concentration in the films is dependent on the tellurium to cadmium precursor partial pressures ratio (VI/II ratio) in the growth ambient. Hence it can be controlled by varying the VI/II ratio. Arsenic concentrations as high as 2×10^{19} at.cm^{-3} were measured by SIMS for a cadmium rich growth (VI/II ratio of 0.73). However, it was observed that the lateral resistivity of the films increased

accordingly with increasing arsenic incorporation. Minimum resistivity of 200 Ω.cm was obtained for an arsenic concentration of 2×10^{18} at.cm^{-3} at a VI/II ratio of 0.95. The low conductivity is thought to be due to the formation of [V_{Cd}-As_{Te}] complexes and [As_{Cd}]$^{+}$ donors due to the low solubility of As in epitaxial CdTe films (~2×10^{17} at.cm^{-3} when using arsine as the dopant species) but also due to the polycrystallinity aspect of the CdTe films. The high density of grain boundaries and the very likely incorporation of As at them would yield very resistive layers. The growth of CdTe films onto sapphire substrates is characterised by a lattice under compressive stress and a small grained structure (grains are ~100 nm) with dopant incorporation having almost no effect on the structural properties of the specimens. Structural analysis of the layers showed that the higher growth temperatures (350-400°C) favour the [111] preferred orientation compared to growth at 320°C, which favoured a random orientation of the crystallites. The achieved resistivity of the CdTe films (200 Ω.cm) shows that *in situ* arsenic doped CdTe films grown by MOCVD can provide suitable absorber layers for solar cells if the carrier concentration can be increased beyond 10^{15} cm^{-3}. However, since the *in situ* doping could not provide the required films properties - high conductivity ($\sigma_i < 10^{-2}$ S.cm^{-1}) and high carrier concentrations ($p > 10^{18}$ cm^{-3}) - suitable for solar cells with tunnel junction, undoped CdTe/CdS structures were activated using the more widely used $CdCl_2$ post-growth heat treatment.

Chapter 6 discussed the microstructure of the absorber layers with regard to the growth parameters and post-deposition heat treatment conditions. Growth rate, grain size and crystallographic orientation were found to be dependent on the position of the substrate along the susceptor block, this being due to the gas phase precursors' consumption. When the substrate was positioned closer to the gas inlet side of the reactor, the growth rate and the degree of [111] preferred orientation increased with respect to the usual centre position on the heater block. When the substrate was sited away from this inlet position, the growth rate decreased significantly and the films became more [422] oriented. It was also found that the grain sizes develop significantly slower compared with films grown by other high temperature techniques. Indeed for the MOCVD films studied grown at 350°C, the grains increase at half the rate as they do in CSS-grown materials.

The influence of the post-deposition heat treatment with and without $CdCl_2$ was studied for structures with 8-12 μm thick absorber layers. When heated without $CdCl_2$ (12 μm thick layers, film nearly completely [111] oriented, original grain size of ~1 μm) little grain growth, defined as the general uniform expansion of grains, was observed for treatment temperature ranging between 360 and 500°C. However, for high annealing temperatures and/or times, strong morphological changes were observed as CdTe grains coalesced together leading to a non-uniform surface and eventually the films started to evaporate. When treated with $CdCl_2$ (8 μm thick layers, film slightly less [111] oriented, original grain size of 0.7 μm), the film surfaces appeared to be smoother with rounded grain surfaces and grain growth was measured. There was a significant increase in grain size following the first 5 min of annealing (1.1 μm at 440°C) and then the grains were still growing for annealing times up to 30 min (1 μm at 400°C and 1.3 μm at 440°C). The grain growth was enhanced for higher treatment temperatures and followed the parabolic grain growth law described by Burke and Turnbull's (section 6.5.2). Grain growth exponents of 4 and 7 were derived for samples treated at 400°C and 440°C, respectively. Devices with 12 μm thick CdTe also showed grain growth when processed with $CdCl_2$ and therefore it is concluded that the $CdCl_2$ flux is necessary to promote grain growth. Following treatment, with or without cadmium chloride, the films lost their [111] preferred orientation and became more [422] oriented. The annealing step also reduced the in-plane stress in the films.

The performances of $CdCl_2$-treated MOCVD-grown CdTe/CdS were investigated using light and dark current-voltage and SEM/EBIC measurements (Chapter 7). The successful activation of the structures was dependent on the thickness of both semiconductors. When window layers thicker than 120 nm were used, it was not possible to produce efficient devices. It was necessary to reduce the thickness of the CdS window layer to minimum probably due to the low hole lifetime and high recombination rate occurring in CdS thin films. As for the absorber layers, it was only possible to process efficient devices using ~4 μm thick structures. Thinner cells (~2 μm) were inefficient because the layers did not survive the post-deposition heat treatment conditions employed for processing devices. On the other hand, thicker devices (8-12 μm) also produced solar cells exhibiting no

photoresponse. The junctions of efficient devices were investigated using spectral response and EBIC measurements. Maximum quantum efficiency was recorded near the CdTe band edge indicating a buried junction. Analysis of the variations of the back-wall EBIC confirmed that maximum collection efficiency occurred in the absorber layer and not at the metallurgical junction.

However, solar cell devices were produced and the influence of the post-deposition $CdCl_2$ heat treatment was demonstrated. The influence of the $CdCl_2$ layer thickness, annealing temperature and time on the cell parameters was studied on some 200 solar cells. The short circuit current density was the cell parameter that was most affected by changes in the post-deposition treatment conditions. The performances following this treatment were increased by an order of magnitude compare to the untreated structures. Best devices, with efficiency up to ~6% (J_{sc} = 30 mA.cm^{-2}, V_{oc} = 0.595 V, FF = 35%), were made with cells processed at 420°C for 18 min with 30 nm of $CdCl_2$. It is again reminded that the collecting area of every devices might have been underestimated by a factor of two or greater yielding therefore an overestimated short circuit current. Generally, the solar cells had low efficiency and were limited by the low fill factor (35 %) arising from low shunt resistance and high series resistance and diode quality factor: shunt resistances of 1060 and 140 Ω.cm^2, series resistances of 6.8 and 2.1 Ω.cm^2 and diode factor of 2.4 and 4.4 were derived from J-V measurements for a 5% efficient device in the dark and under illumination, respectively. Therefore devices were characterised by high recombination losses and high reverse saturation current densities (J_0 = 1.6×10^{-3} mA.cm^{-2} in the dark). The limited performance of the solar cells processed could originate from the post-deposition treatment itself, as from the strong changes that accompany the processing: stress relief and grain growth can promote perforation of the films leading an increase in leakage current.

The reasons of failure of 12 μm thick devices were explored using alternative current impedance measurements and compared with a 4 μm thick 5% efficient device (Chapter 8). Impedance spectroscopy applied to the 4 μm structure revealed an anomalous Arrhenius behaviour thought to be a consequence of the processing etching step. No defect information could be deduced from the measurement applied to the 12 μm thick cell. This is thought to be originating from the poor conductivity

of the absorber layer characterised by an overall small grain size and non columnar grains. Indeed, the resistances measured across the structures were 100 times higher for the thicker cell compared to the thinner one. Analysis using simple equivalent circuits proved unsuccessful indicating the complex response of the materials.

This thesis has documented on the possible opportunities offered by the MOCVD technique for the growth of CdTe/CdS thin film solar cells. It has been shown that a moderate doping level of CdTe with As could be achieved. This could provide a new route for doping the active region of CdTe-based solar cells if the carrier concentration could be increased to 10^{15} cm^{-3} and beyond. However, the fabrication of a tunnel junction requires an extremely high carrier concentration and this has not yet been achieved. The $CdCl_2$ post-growth processing applied to MOCVD-grown CdTe/CdS structures has been extensively explored. However, if MOCVD is to play an important role in the development of CdTe/CdS solar cells, improvements and further understanding must be achieved if it is to compete with other well established techniques such as CSS.

9.2 Suggestions for Future Work

Further to the work describe in this thesis, a number of questions remain and more studies are needed in order to further develop the investigated work.

- The effectiveness of the post-deposition treatment of CdTe/CdS bi-layers could be questioned. The process used in this work should be tested with structures that have proved to be suitable for high efficiency devices. Due to the many steps involved in the procedure, improvements can be expected.
- It seems that the conductivity of the absorber layer remains one of the main issues limiting the progress of MOCVD-grown CdTe/CdS thin film solar cells. For this, more investigations of the film conductivity in the thickness direction are required with and without dopant incorporation. This would help in understanding the effect of non columnar grains that seem to characterise the layers investigated.
- Finally, the use of impedance spectroscopy introduced in this work should be further researched. Finding a suitable model and correlating the results with current-voltage but also quantum efficiency measurements is essential.