The simulation, fabrication and testing of widely tunable micromachined capacitors

Andrew Gallant

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Andrew Gallant B.Sc. (Hons)
School of Engineering
University of Durham

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Abstract

This thesis is concerned with the development of widely tunable micromachined capacitors. These devices form part of the emerging field of radio frequency microelectromechanical systems (RF MEMS). Micromachined switches, resonators, capacitors and inductors are reviewed from both a technological and commercial perspective.

Micromachined devices can exploit low loss air dielectrics in conjunction with thick structural metallisations to realise high performance RF components. The demand for high performance tunable capacitors in the RF industry is strong because modern communications requires signal agility in crowded frequency bands. This is best achieved using low loss capacitors which allow for sharp tuning and filter peaks. However, in order to achieve the required signal agility the tuning range needs to be large.

The tuning range of single-gap electrostatically actuated micromachined capacitors is limited by an electromechanical instability known as pull-in. A two-gap approach is modelled using Coventorware. The simulations show that this approach can eliminate the pull-in limitations, leading a very wide tuning range. These results are used to identify key parameters for the fabricated devices.

Fabrication of the capacitors is demonstrated using both nickel and gold electroplating based processes. This surface micromachined approach uses a titanium sacrificial layer and has led to devices with tuning ratios of up to 7.3:1.

A dual sacrificial layer technique is developed which enables thick interconnect metallisations on a range of substrates to be implemented. A quality factor 243 at 0.9GHz for a 0.26pF capacitor on a glass substrate is reported. This process flow is also directly compatible with air suspended inductors which are fabricated and RF tested.

Acknowledgements

First, I acknowledge the unwavering support and contribution from my supervisor, Dr. David Wood, for the previous four years. I would also like to thank EPSRC and Filtronic for sponsoring this research. In particular, I wish to thank my industrial supervisor, Richard Jackson, and all of the staff at Filtronic who have contributed to the direction of this work.

I need to draw attention to the practical wizardry of John Gibson and the other members of technical staff in the School of Engineering. I must also acknowledge the input received from the members of the rapidly expanding Microsystems Technology Group.

Finally, I would like to thank my family and friends.

Declaration

I declare that no material in this thesis has previously been submitted for a degree at this or any other university.

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Chapter 1

Background

At the end of the 20^{th} century, the wireless telecommunications industry entered a period of significant growth. In response to the increased demand for mobile telephones and base stations, RF component manufacturers ramped up production.

GaAs power devices such as amplifiers show good linearity and efficiency making them preferred components for many mobile applications. In September 1999, Filtronic Compound Semiconductors Ltd (FCSL) acquired the former Fujitsu DRAM facility at Newton Aycliffe, County Durham. Filtronic wanted to create a GaAs pHEMT foundry for discretes and microwave monolithic integrated circuits (MMICs).

To meet the high demand for RF devices and to drive costs down, Filtronic decided to utilise the high volume production techniques more commonly found in the silicon industry. Tooling was introduced at FCSL to handle 150mm GaAs substrates with a production capacity of over 40000 wafers per annum [1]. Both of these figures are large by compound semiconductor standards.

The transfer of discrete circuit board components to the MMIC provides clear cost and space benefits. However, GaAs does not offer a complete high performance single-chip solution. The aim of the research in this thesis was to develop a micromachined tunable capacitor which would demonstrate advantages in terms of both tunability and RF performance over solid-state equivalents.

The variable capacitor can be used in voltage controlled oscillators (VCOs) and tunable filters. These are essential building blocks for wireless communications systems. A benefit of surface based micromachining techniques is that they can be made substrate independent. Therefore, in many cases the technology can be complementary to the MMIC. Ultimately micromachined and MMIC devices could be integrated onto the same die to maximise performance. This process flow compatibility appealed to Filtronic and consequently the company funded a CASE award in conjunction with EPSRC to support the capacitor development.

The emerging technologies, presented in this thesis, are now commonly described as radio frequency microelectromechanical systems (RF MEMS) [2-7]. The aim is to replace solid-state solutions with micromachined RF devices which include switches, tunable capacitors, inductors and resonators.

Traditionally though, micromachining has been led by the sensor market through, for example, miniaturised accelerometers, gyroscopes and pressure sensors. Relative to these applications, RF MEMS is in its infancy.

Micromachining developed into a successful industry because it achieved cost minimisation through batch processing and volume production. Many micromachining techniques are derived from standard integrated circuit processes. This makes micromachined devices suitable for mass market production.

When the project details were finalised in early 2000, research into micromachined tunable capacitors was relatively immature. In general, electrostatic tuning was identified as a preferred route due to its negligible power consumption and rapid response when compared to alternative actuation mechanisms.

Two main routes existed in the literature for electrostatically tunable micromachined capacitors. Area tuning capacitors were reported with arrays of interdigitated fingers, often formed by deep reactive ion etching (DRIE) of silicon [2]. Alternatively, a gap tuning approach had been demonstrated which essentially miniaturised the parallel plate capacitor [8]. The parallel plates could be formed using substrate independent surface micromachining with thick metallisations to minimise resistive losses [9]. The gap tuning approach was chosen for the thesis because it was better suited to the process flows encountered at Filtronic.

1.1 The widely tunable capacitor approach

A full review of the various tunable capacitors is presented in the next chapter. Brief details relevant to the project background are given here.

An electromechanical instability, known as pull-in, limits the controllable deflection of an ideal parallel plate single-gap capacitor to one third of the unbiased gap. This, in turn, limits the tuning ratio to 1.5:1. Dec and Suyama [10] used a three plate approach to increase this to 1.87:1 with a quality factor, Q, of 7.1 at 2 GHz. This represented state-of-the-art for the continuous gap tuning approach in the literature up to the year 2000.

In order to remove this electromechanical instability a two-gap tuning approach has been used. This is shown in fig. 1.1. A DC bias is applied between the upper electrode A and the lower electrodes, B. The upper electrode electrostatically deforms to reduce the gap between it and electrodes B. Electrodes A and C form the capacitive structure. As the upper electrode deforms, so the gap and hence the capacitance varies. If near contact can be achieved between the capacitive electrodes before pull-in occurs then very small gaps, and hence high capacitances, can be realised.

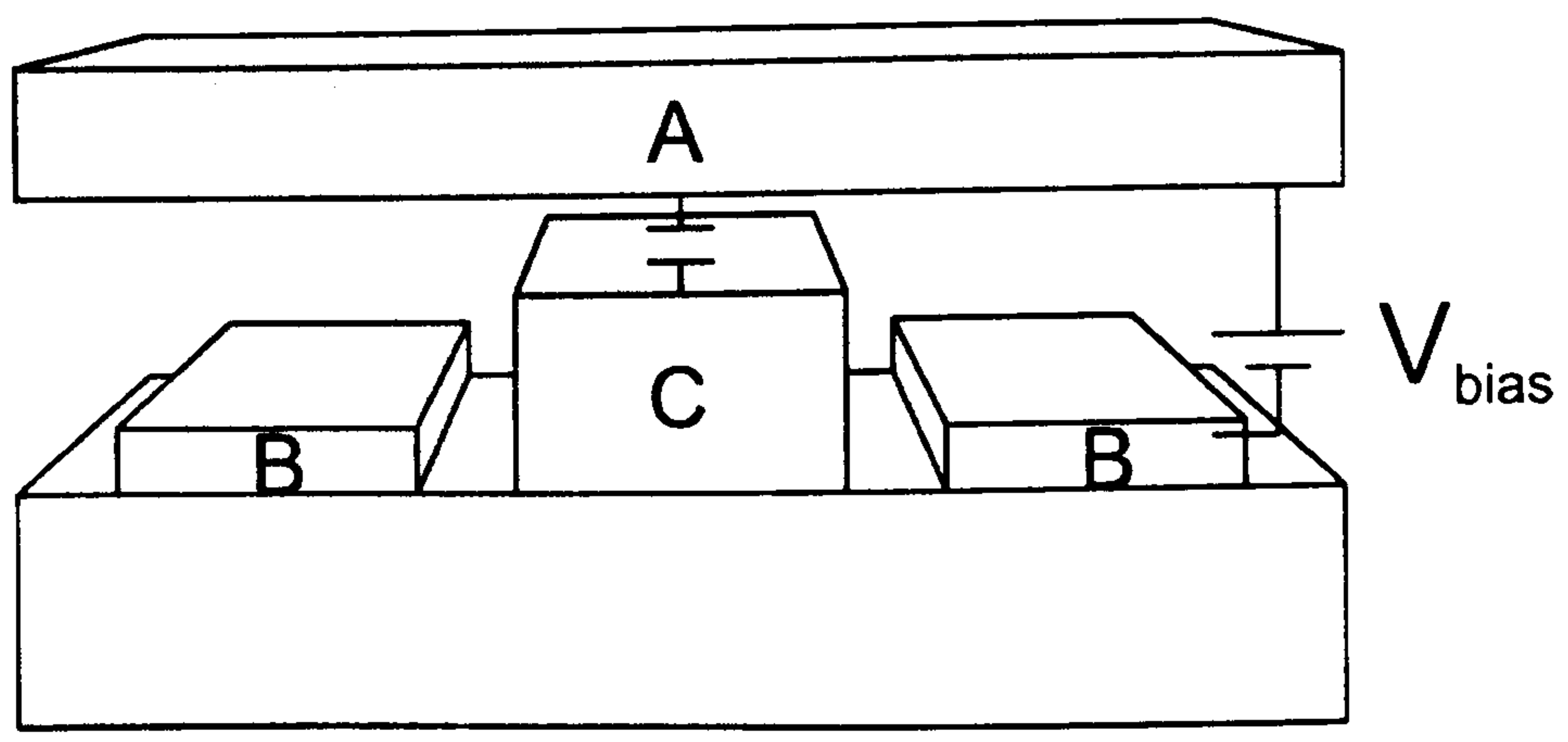


Fig. 1.1 The two-gap electrostatically tuned micromachined capacitor.

Air is an excellent dielectric for low GHz operation. Many high performance RF devices exploit it because of its negligible losses. The use of micromachining enables micron scale air gaps to be fabricated. It is therefore feasible to miniaturise devices such as air gap parallel plate capacitors or inductors. When losses are minimised, sharper tuning peaks can be achieved. This enables the RF spectrum to be used more effectively which is particularly important where there is high demand. Furthermore, battery consumption is also reduced enabling portable devices to be operated for longer.

1.2 Thesis overview

Chapter 2 introduces the state-of-the-art for the main RF MEMS devices, i.e. switches, capacitors, inductors and resonators. These will be able to implement many of the key RF circuit functions, which are currently circuit board based. Due to the commercial potential, all of these devices have been subject to intensive research in recent years. In particular, the RF switch has reached the open market through Teravicta [11].

Chapter 3 presents the results from using Coventorware [12], a commercial microsystems simulation package, to study methods of increasing the tuning range of electrostatically actuated capacitors through changes in design and electrode layout. This has been used to identify key parameters and produce a starting point for fabrication.

Chapter 4 provides an introduction to the key fabrication techniques used for micromachined devices. Many of these are comparable to those used in IC production. Photoresist based contact photolithography is used to pattern individual layers. Thin film metal deposition is achieved through evaporation, sputtering and electroplating. Wet and dry etching is performed on metals and organics.

The three dimensional nature of micromachined devices introduces additional considerations which are not found in the IC industry. One of the most important concepts is the use of a sacrificial layer. This is used as a mechanical support during fabrication and is selectively etched to release the device. Thin film stress minimisation is also very important because it can lead to considerable deformation in air suspended structures.

The effective commercialisation of microsystems devices relies upon the availability of reliable simulation software. In general, the initial development of micromachined devices can prove costly due to the requirement of cleanroom fabrication tools. Virtual development and testing can prove much more cost effective and minimise the cleanroom prototyping cycle.

Chapter 5 examines the choice of sacrificial layer for the fabrication of the two-gap structure. Photoresist has been reported as a suitable sacrificial layer in the literature[13]. However, the additional requirement of the two-gap structure identified in chapter 3 which needs very small gaps to achieve the high tuning ratio, make this less attractive. It was found to consistently leave residual organic scum in the critical gaps.

Removal of the organic scum is achieved through aggressive wet etches but these are found to influence mechanical stresses and are incompatible with many metallisations. An alternative approach is developed which uses titanium as a sacrificial layer. This is thickness limited to thin film stresses but suits the two-gap structure well because it etches cleanly in HF based solutions. Due to the non-planarising nature of titanium, a self-planarising process flow is used.

Chapter 6 details the fabrication route available for widely tunable capacitors. Gold and nickel electroplated devices are developed which exhibit a tuning ratio of up to 7.3:1. A scanning electron microscope (SEM) has been used to relate device performance and failure to topological structure. The sub-micron gaps achievable through the use of titanium as a sacrificial layer make considerations of the surface topology of the capacitive plates particularly important. An atomic force microscope (AFM) is used to examine the electrode surfaces and propose a model for their topological meshing.

The primary application for the micromachined capacitor is as part of voltage controlled oscillators or tunable filters in the GHz regime. Chapter 7 uses a vector network analyser to extract the quality factors, Q, for the structures in chapter 6. The quality factor is a key figure of merit for RF MEMS components because it is indicative of devices losses at a particular frequency. A high Q corresponds to low losses.

A modified process flow is reported which uses a dual sacrificial layer to enable a very thick interconnect feed to the capacitor structure. This enables fabrication on a range of substrates including silicon, glass and gallium arsenide. Glass in combination with thick interconnect is shown to achieve very high quality factors. The dual sacrificial layer approach is also compatible with the fabrication of on-chip micromachined suspended inductors.

Chapter 8 discusses key results from previous chapters. In particular, attention is paid to key future developments required for effective commercialisation. One conclusion is that novel micropackaging solutions need to be developed to provide integration with existing ICs.

Chapter 2

Radio Frequency Microelectromechanical Systems

In recent years, microelectromechanical systems have received considerable attention in the literature. A comprehensive review of the entire field is now beyond the scope of a single chapter. Instead, this chapter starts by introducing a few examples of commercially advanced MEMS devices and the market prospects for RF MEMS. Subsequent sections detail a selection of the main RF MEMS devices. Micromachined RF switches, resonators, capacitors and inductors are described in terms of technical operation, performance and commercial readiness.

2.1 Introduction

In order to succeed, a new product must present clear benefits in its intended market. Micromachining technology has attempted to break into consumer arenas citing cost reduction and miniaturisation whilst maintaining, and often improving, performance.

The primary issue for the uptake of micromachined devices in the marketplace is a realisation that initial investment costs can be immense without a guarantee of success. Although many of the fabrication techniques are compatible with existing microelectronic processing, this 'compatibility' is a very loose term. It tends to refer to the use of standard cleanroom equipment.

Even for an existing microengineering company, the introduction of MEMS devices to the product line requires new processes and an initial disruption to manufacturing. This has associated costs. For a MEMS start-up company, the cost of owning the fabrication process will be of the order of $5 - $50 million or even more, depending on the size of the facility.

During the 1990s MEMS based sensing and optical applications were primary investment areas. The automotive industry is a ready, and large, market for low cost small sensors. Consequently micromachined accelerometers such as those developed by Analog Devices [14] have achieved good market penetration in car airbag sensing.

In recent years, the traditional overhead projector has been superseded by the digital projector which now has a market valued at $4 billion [15]. Texas Instruments (TI) developed the Digital Micromirror Device (DMD) in 1987 [16]. It uses micromachined tilting mirrors to direct light towards the projection surface. Competing against liquid crystal display (LCD) technology, the DMD projectors have demonstrated lifetime and image quality improvements. TI predicts a 30% market share by 2006. It should be noted though that this will be nearly two decades since device conception.

Seiko Epson [17] have pushed microfluidics technology into the marketplace with piezoelectric print heads in their colour printers. As with TI, Epson became interested in MEMS technology in the late 1980s. Now they are the largest user of silicon wafers in the printer industry [18]. The precision of the MEMS based print heads has led to low cost colour printers with the resolution required to fulfil the demand for photo printing.

In the late 1990s a new application arena evolved, now referred to as radio frequency microelectromechanical systems (RF MEMS) [2]. The primary attraction of using micromachining to produce RF devices is that performance can be retained or improved whilst enabling integration with existing ICs. In 2003, a total of 500 million mobile phones were sold globally [19]. In developing countries mobile telephone base stations are being installed in preference to costly landlines.

The mobile telephone is now a disposable item. Some basic GSM handsets can be purchased outright for £30. For the consumer, the cost of replacing a failed rechargeable battery pack often exceeds the initial cost of the handset. The advantage of this market place is that a high turnover of mobile telephones is maintained.

For the mobile telephone manufacturers this is a very dangerous economy to trade in. In order to retain profits in a competitive market, manufacturing costs have to be driven down. However, in parallel the additional RF requirements of 3G [20] have to be implemented in new handsets whilst minimising price increases.

The volume market for handsets now exists but a technology such as RF MEMS needs to provide clear cost reductions for the manufacturers. Fig. 2.1 shows a market forecast for RF MEMS devices. In 2007, the predicted market exceeds $1 billion dollars.

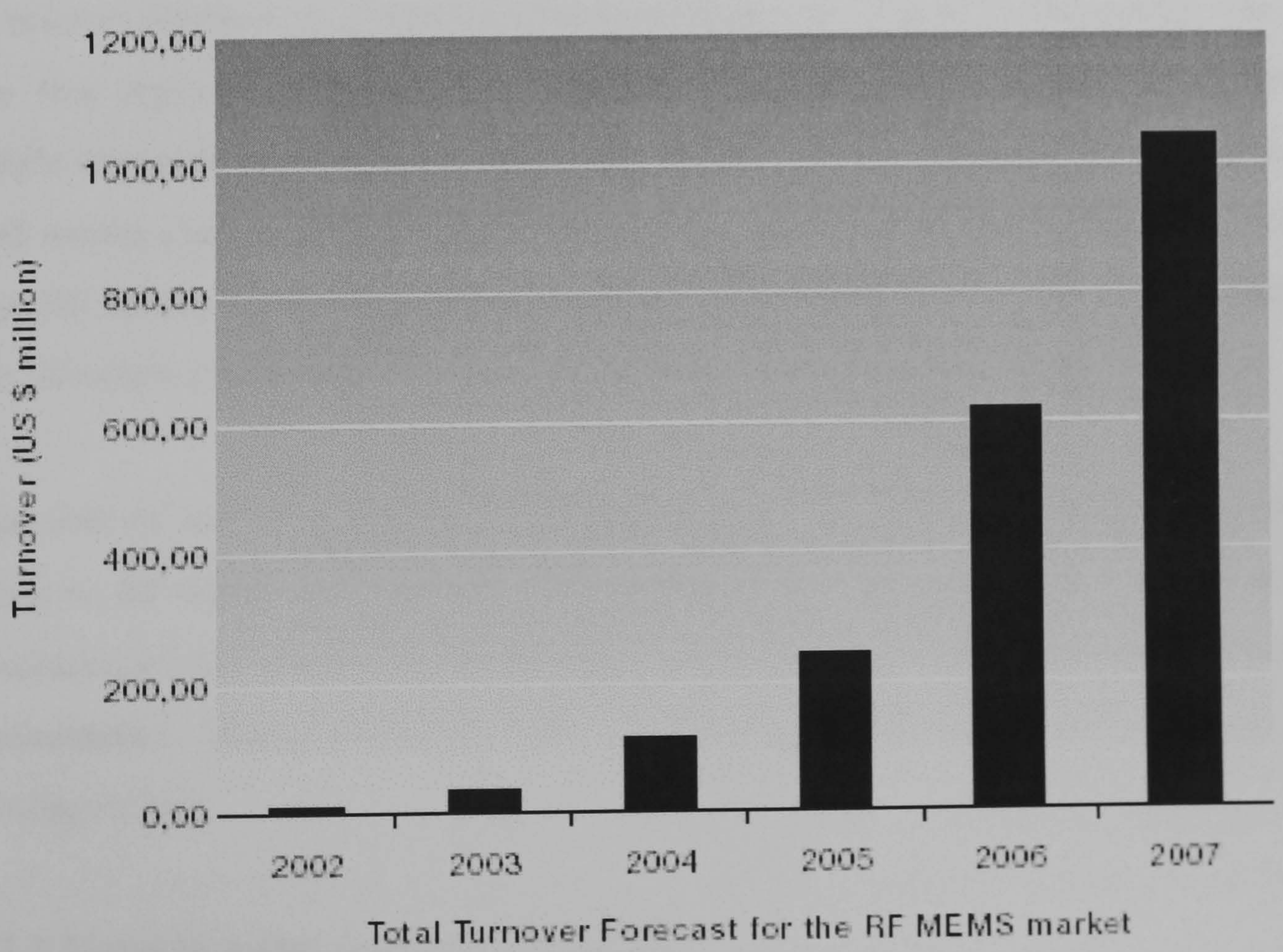


Fig. 2.1 Market forecast for RF MEMS. Reproduced from WTC [21].

2.2 RF MEMS switches

Switches are used to route RF signals when multiple circuits need to be implemented on a circuit board or IC. In mobile telecommunications they are used to switch multiband phones, providing global compatibility. Electromechanical switches have existed on the macroscale for many years and are available as plug-in modules. Actuated by electromagnetic relays, these are bulky and have a limited switching speed (typically ms). However, their RF performance up to several hundred MHz and power handling capabilities are good.

Solid-state RF switches exist in the form of PIN diodes and GaAs FETs. These semiconductor based switches do not provide the RF isolation of electromechanical switches but provide high switching speeds (typically ns) and on-chip compatibility. To date, these have market saturation for modern wireless applications.

Micromachining provides the mechanism to miniaturise the electromechanical switch to micron dimensions. Demonstrated by Peterson in 1978 [22], the switch was one of the first reported micromachined devices. Peterson produced bulk micromachined single crystal silicon switches. However, these were not designed for RF applications and would yield a poor RF performance due to the lossy silicon structural material. The RF switch is currently the most mature RF MEMS device with many examples in the literature [3, 23-36].

The role of the micromachined RF switch is to provide a mechanism to open and close an RF signal line. This has been implemented through a wide range of actuation mechanisms and circuit configurations. However, two configurations are commonly encountered. These are series metal to metal contact and capacitive shunt switch configurations.

2.2.1 Metal to metal contact RF switches

The first device to be discussed is the metal to metal contact switch. Fig. 2.2 shows the principle of operation for an electrostatically actuated switch. A DC voltage applied across electrodes A and B causes the movable electrode, A, to be electrostatically attracted towards the fixed electrodes B and C. When A and C make contact an electrical short is achieved. This biasing voltage, comparable to the threshold voltage in a FET, enables the switched to be closed.

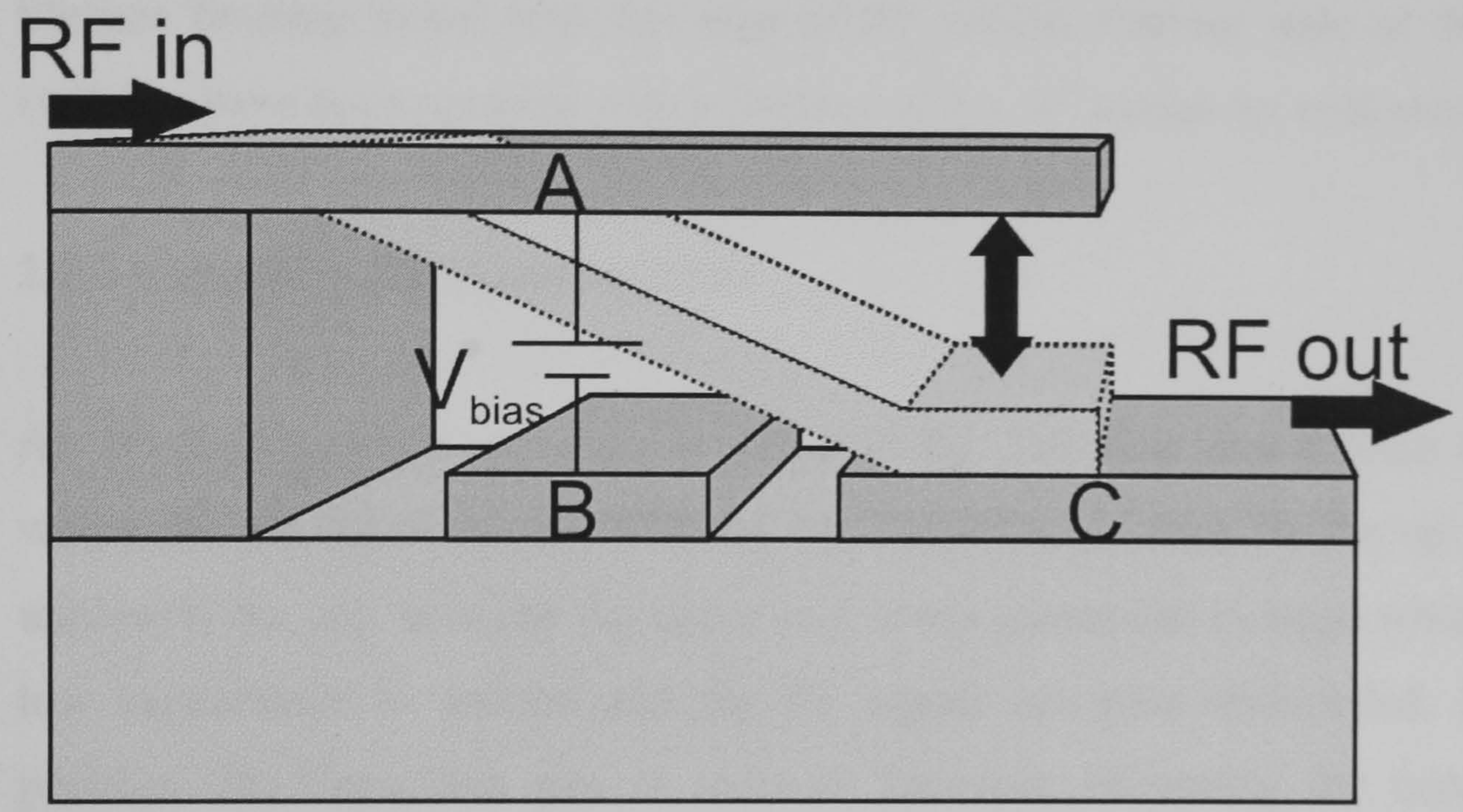


Fig. 2.2 The electrostatically actuated metal to metal contact switch.

The switch in fig. 2.2 is in a series configuration. This is best suited to frequencies below 10 GHz [37]. The isolation of a series RF switch degrades with increasing frequency [32]. Metal contact switches are suitable for switching DC signals as well as RF.

The primary issue with this type of RF MEMS switch is reducing the insertion losses by ensuring a low contact resistance. In order to achieve this, the upper electrode needs to be in good physical and electrical contact with the lower electrode.

Electrostatic pull-in is usually exploited to increase the contact force. If a DC voltage is applied, which causes a displacement in excess of approximately one third of the unbiased gap, the movable electrode uncontrollably snaps down to contact the fixed lower electrode. This is an electromechanical instability caused by the restoring spring forcing being unable to counter the electrostatic force of attraction (see chapter 3). Over a large number of switching cycles the topology of the electrode can alter due to physical wear - especially for relatively soft metals such as gold [38].

As will be discussed in chapters 4, 5 and 6, micromachined electrodes are susceptible to stiction failure. This is where the electrodes irreversible adhere together. Ideally planar surfaces are used for the contacts because they provide the minimum on state resistance for the least contact force. However, these planar electrodes have a larger contact area and are more likely to encounter stiction failure [39]. This is the main lifetime limiting factor with this type of RF switch. Current state of the art contact switches have been reported with a lifetime of 7 x 10^9 cycles for cold switching [40].

2.2.2 Capacitive RF shunt switches

An alternative switch approach is shown in fig. 2.3. This uses a shunt configuration where the RF signal is controlled by two capacitance states. In the up position (i.e. unbiased) the gap between the upper and lower electrodes is large which provides a low capacitance to ground and the RF signal can pass unimpeded. In the down position, the capacitive gap is reduced therefore increasing the capacitance and shorting the RF signal to ground. As with the series contact switches electrostatic actuation is predominantly used for the capacitive shunt switches.

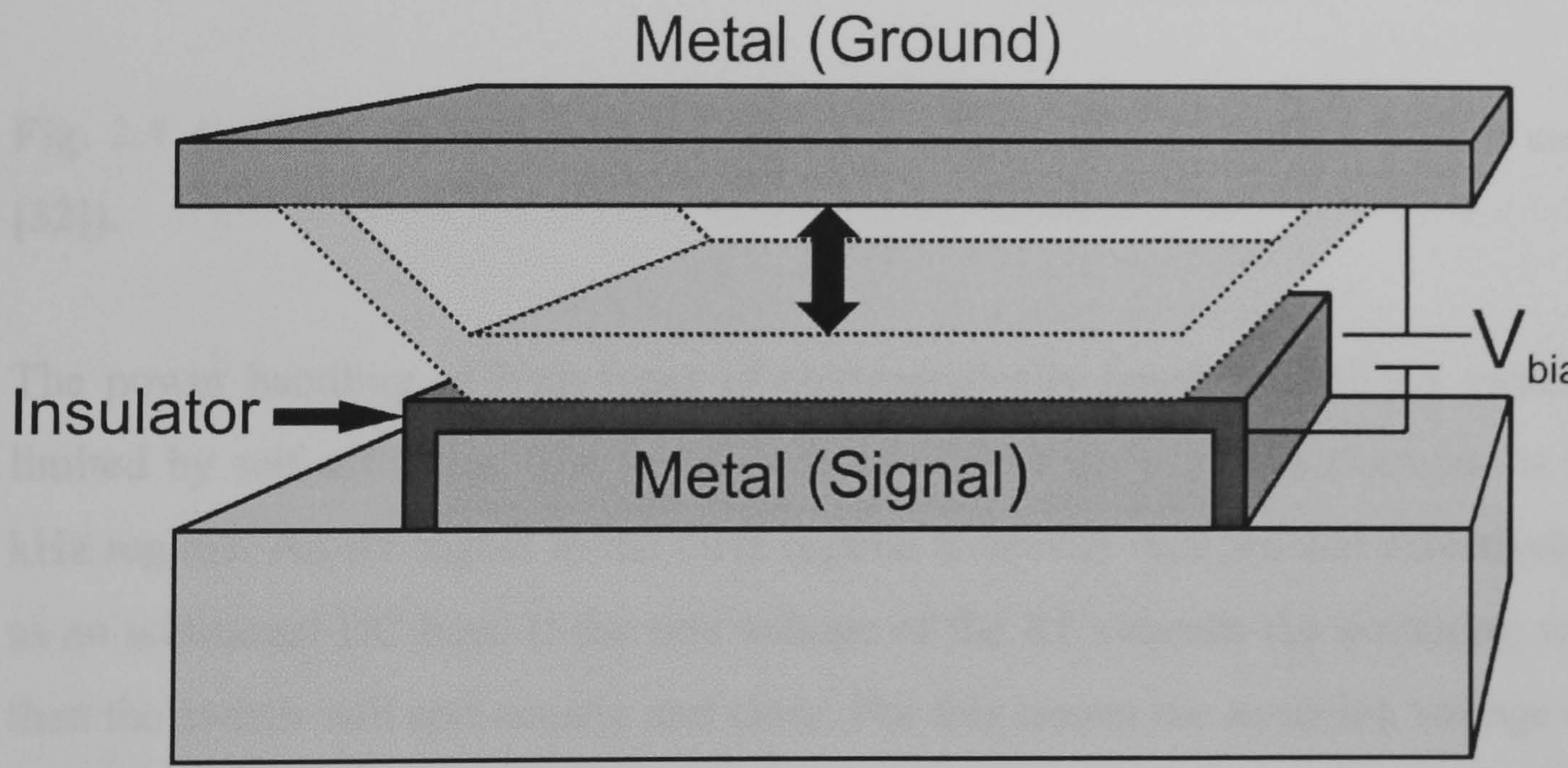


Fig. 2.3 A capacitive shunt switch configuration.

The advantage of this capacitive approach is that the need for low resistance metal contacts is eliminated. This enable anti-stiction measures to be utilised such as dielectric materials in conjunction with anti-stiction coatings [41].

Unfortunately, this has not solved the lifetime issues of RF MEMS switches. Dielectric charging has been reported after repeated operations [42]. As with stiction, this leads to the upper electrode sticking to the dielectric. In this state the switch remains closed.

The shunt configuration is readily compatible with coplanar waveguide (CPW) implementation. The switch is essentially a movable airbridge. Fig. 2.4 shows a schematic of a CPW switch implementation.

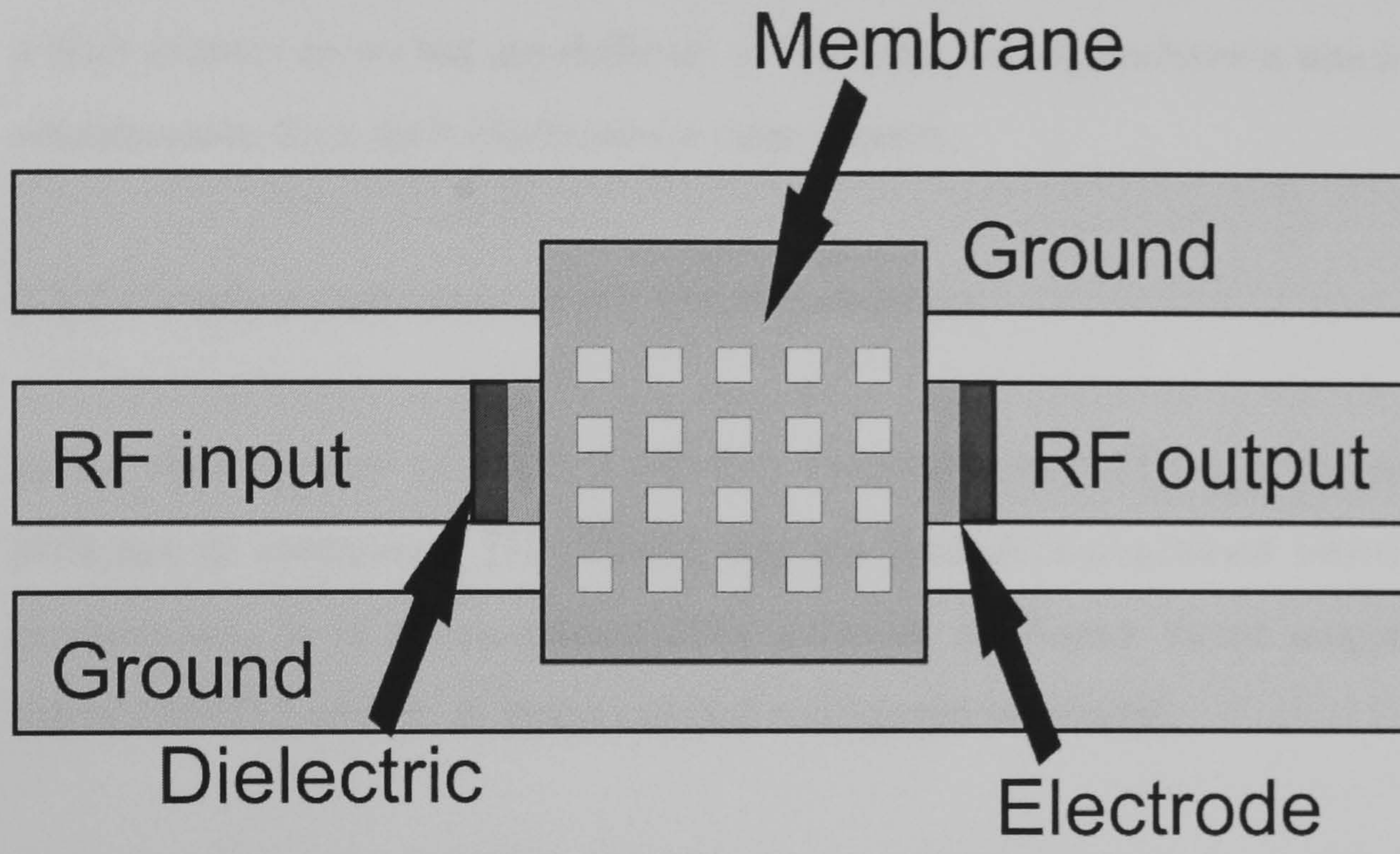


Fig. 2.4 A CPW capacitive shunt switch configuration (Adapted from Yao et al [32]).

The power handling of both types of electrostatically tuned RF MEMS switches is limited by self-actuation. The resonant frequency of the movable electrode is in the kHz regime. An RF signal in the GHz regime is heavily damped and effectively acts as an additional DC bias. If the rms voltage of the RF exceeds the switching voltage then the switch will self-actuate and close. For this reason the actuation voltage of RF MEMS switches must exceed the rms RF voltage.

This forces the biasing voltages high. The gap cannot be reduced to decrease the biasing voltage because this reduces the switch isolation. Instead, either larger actuation electrodes or improved upper electrode suspensions have to be used.

Switching speed is an important figure of merit for RF MEMS switches. It is challenging for a mechanical system to compete directly with an electrical based switch. However, figures are typically in the μs regime [2].

The actuation mechanism for the switches tends to be exclusively electrostatic. Although electrothermal actuation can be used, it is too slow and has a high power consumption but can allow a low operating voltage. Electromagnetic systems provide a high contact force but are difficult to fabricate and again have a much higher power consumption than their electrostatic counterparts.

2.2.3 Commercialisation of RF MEMS switches

In the final quarter of 2003, Teravicta Technologies [11] began to ship RF MEMS switches to customers. The TT612 was the first micromachined switch to reach the marketplace. It is an electrostatically actuated cantilever based single-pole double-throw (SPDT) switch. A metal contact configuration is used.

These micromachined RF switches are in direct competition with the solid-state equivalents. However, currently they are only being sold as discrete devices for circuit board mounting. Table 2.1 shows a comparison of the key performance parameters of the TT612 against a solid-state GaAs equivalent.

	TT612	**FMS2001QFN**
Freq. (GHz)	DC – 6	DC – 2.5
Insertion loss (dB)	0.15@ 1 GHz, 0.3@ 6GHz	0.6@ 2.5 GHz
Isolation (dB)	30@1 GHz, 24@ 6 GHz	30 @ 2.5 GHz
Bias voltage (V)	2.7-5.5	2.7

Table 2.1. This table compares key performance parameters of the RF MEMS switch from Teravicta Technologies (TT612) against a Filtronic pHEMT MMIC SPDT switch (FMS2001QFN) [43].

The first commercially available RF MEMS switch shows insertion loss and frequency operation advantages over a GaAs equivalent. However, there is no gain in isolation. The main advantage of using a lower insertion loss switch for wireless devices is an improvement in battery lifetime.

For the RF MEMS switches to succeed in the market place they ideally need to be integrated into existing RFICs. As discretes they eliminate the key attractions of MEMS to the wireless industry of cost and space reduction.

2.3 Micromachined Resonators

Mechanical resonators provide the capability for stable frequency generation, filtering and mixing in a single device. Ideally the resonant frequency is independent of external conditions and mechanical losses are negligible.

Mechanical resonators are commercially available as quartz, surface acoustic wave (SAW) and cavity resonators. The quartz crystal oscillators cannot be readily integrated on-chip. SAW based resonators can be fabricated on GaAs substrates [44]. However, the SAW devices typically require large substrate areas of up to $1cm^2$ which limits their attraction for integration. Waveguide based cavity resonators are suitable for operation above 2 GHz. Generally, these are costly large scale devices. However, attempts to miniaturise them to dimensions comparable to SAW devices have been successful [45].

Research into micromechanical resonators is well advanced due to sensor applications. Many MEMS accelerometers and gyroscopes are excited into resonance during operation [46]. This has the effect of increasing their sensitivity.

2.3.1 Microelectromechanical beam resonators

Fig. 2.5 shows a simple beam resonator configuration fabricated by Wang et al [47]. The upper movable beam is clamped at both ends. The lower electrode is used to provide an ac signal to excite the beam into resonance.

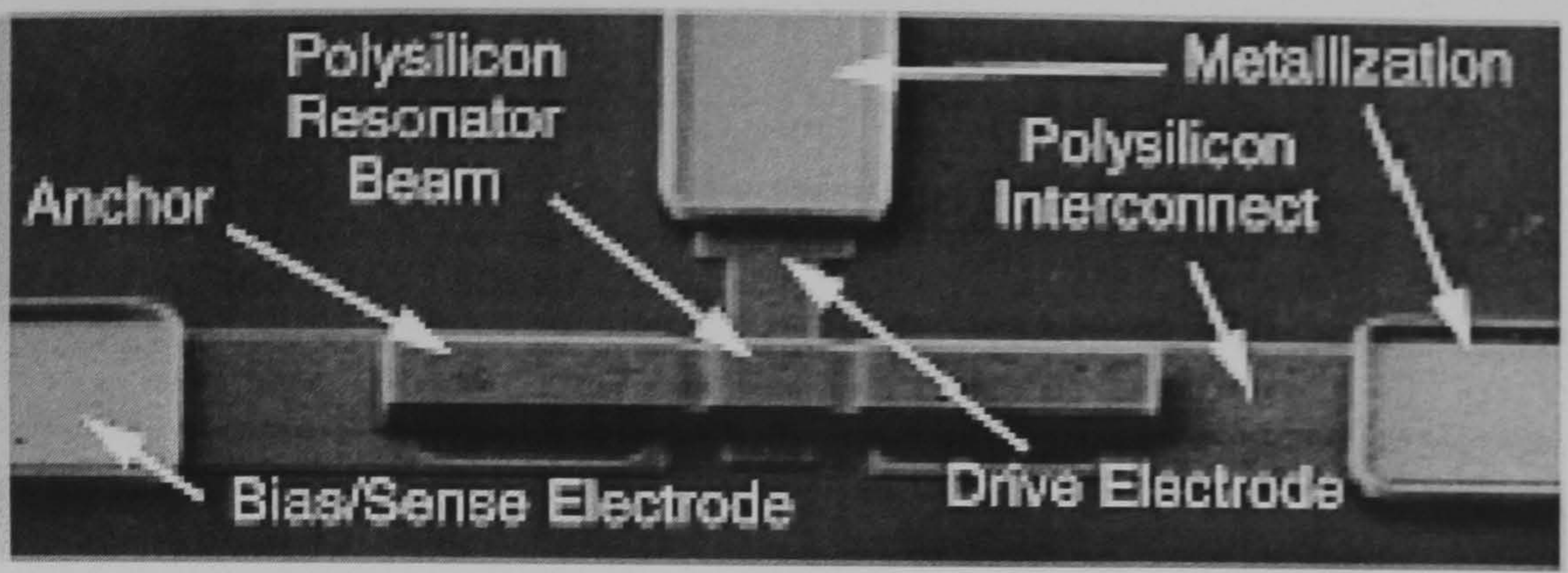


Fig. 2.5 A simple micromechanical resonator arrangement from Wang et al [47].

The MEMS resonator shown in fig. 2.5 has the opposite requirements to the RF switches outlined in the previous subsection. In this case the movable beam must be designed with as high a resonant frequency as possible.

A DC biasing voltage is usually applied to the lower electrode. This is to stop the double actuation of the free beam during ac biasing (for a sinusoidal ac voltage, both the positive and negative swings cause electrostatic attraction). This leads to device actuation at twice the true applied frequency. By applying a DC bias to the resonator electrodes with a magnitude greater than that of the ac voltage, the input signal can be shifted either to fully positive or negative, thus solving the frequency problem.

The beam resonator can be tuned during resonance by applying DC biasing voltage between the beam and the lower electrode. The resonator in fig. 2.5 has a resonant frequency of 54.2 MHz and a mechanical quality factor, Q, of 850. These types of resonators are aimed at VHF applications.

MEMS beam resonators must operate in a vacuum environment, as air damping increases mechanical losses and impairs the mechanical quality factor, Q. Hermetic sealing of devices is expensive.

Various materials have been reported for the beam. In MEMS resonators, polysilicon is commonly used because it has excellent mechanical properties [48]. Metals suffer from fatigue and creep during prolonged operation at resonance [49].

2.3.2 Thin film bulk acoustic resonators

The beam approach is physically limited in frequency to the VHF regime. Therefore alternative designs have been developed which can achieve resonant frequencies nearing 1 GHz.

The general thin film bulk acoustic resonator (FBAR) structure is shown in fig. 2.6. The FBAR works using a metal - piezo - metal sandwich. An RF signal across the metal electrodes excites the piezoelectric material. Therefore electrical energy is converted into mechanical. The FBAR is fabricated on a thin membrane which isolates the device acoustically from the substrate. This significantly reduces mechanical losses and increases the Q [50].

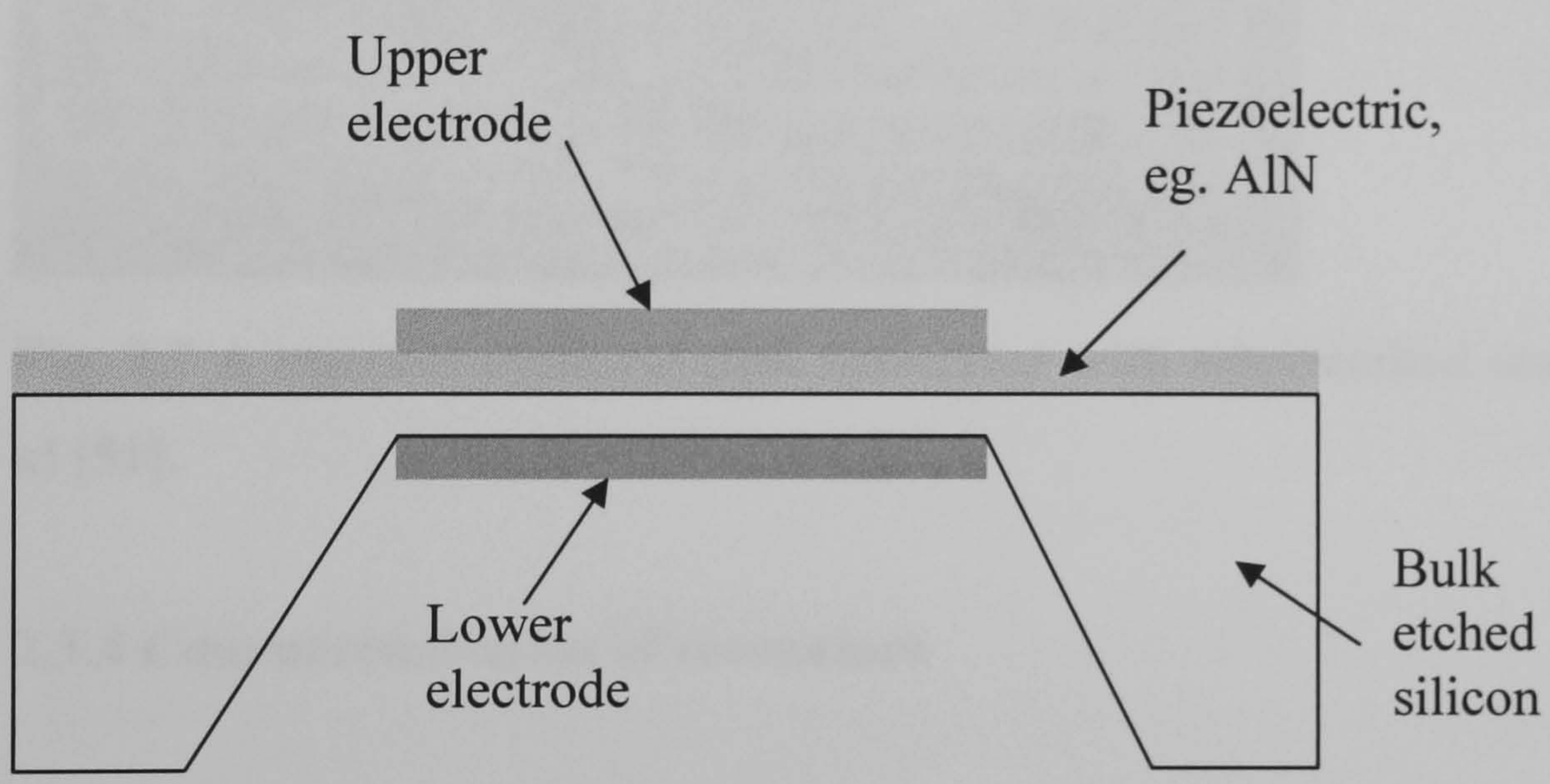


Fig. 2.6 A typical FBAR resonator arrangement

2.3.3 Micromechanical disk resonators

In recent literature Wang et al have reported a micromechanical disk resonator with a resonant frequency of 1.51 GHz and a Q of 11,555 [51]. This represents state-of-the-art at the time of writing for this type of resonator. This frequency regime is suitable for mobile phone applications such as frequency reject filters on the front end.

Fig. 2.7 shows an image of the disk resonator fabricated by Wang et al. An applied high frequency signal causes the disk to be attracted to the biasing electrodes. These electrodes are spaced 100nm from the edge of the disk.

The diamond disk was deposited using chemical vapour deposition (CVD). Diamond has a high acoustic velocity of up to 18000ms^{-1} [52]. The acoustic velocity is proportional to the resonant frequency. The supporting stem is formed using polysilicon. The authors state that the use of mismatched materials reduces losses from the disk to the stem. This, in combination with the small gap, leads to high Q and high frequency operation even in air.

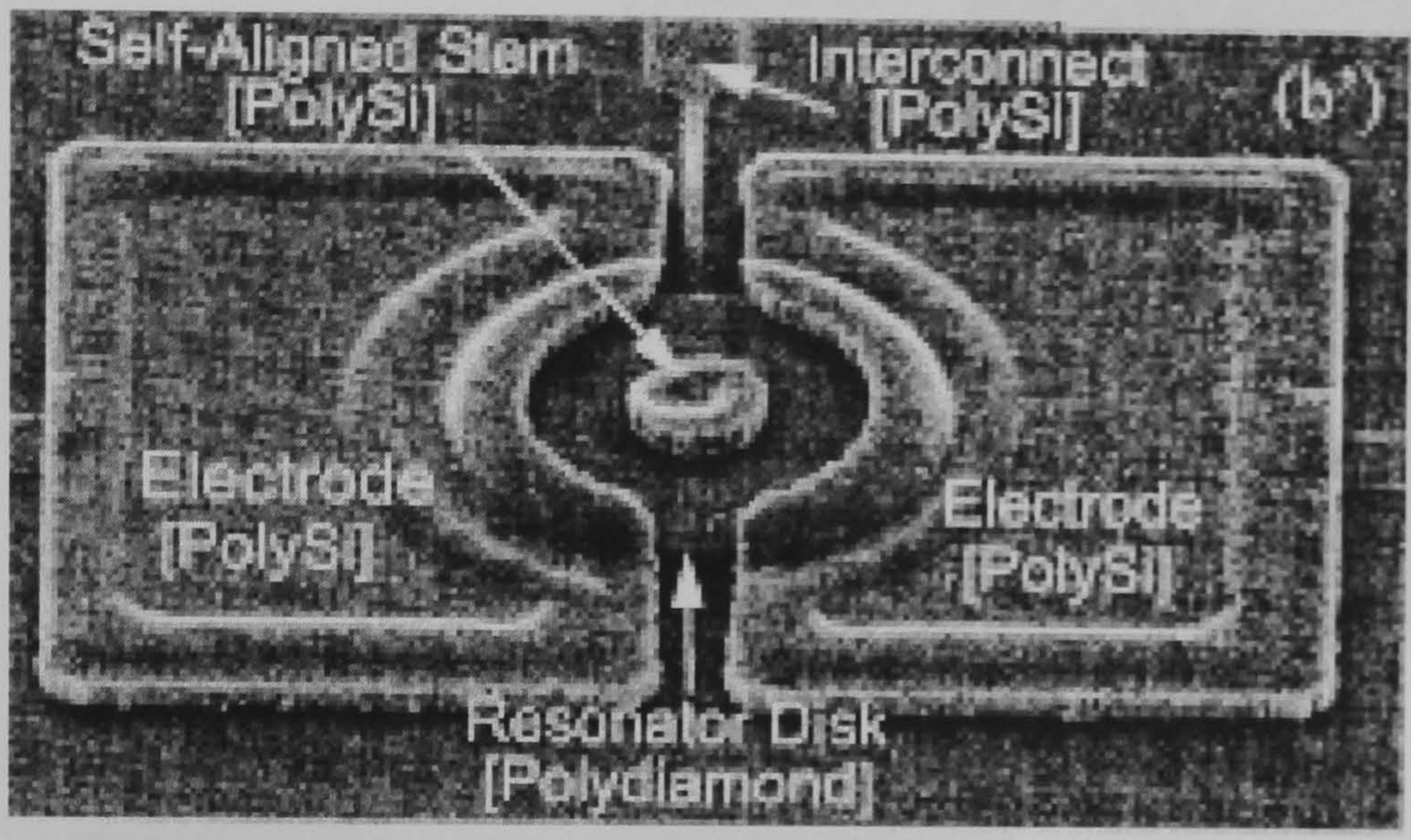


Fig. 2.7 A micromechanical disk resonator with mismatched stub from Wang et al [51].

2.3.4 Commercialisation of resonators

In summary, the beam type resonators are limited to VHF type applications up to 100MHz. Recent advances in surface micromachined disk resonators have led to devices with resonant frequencies up to 1.51 GHz. These examples, however, are still being actively researched and are not nearing the market.

FBAR devices have been released to the market by Agilent. Ruby et al [53] have developed FBAR filters for the US mobile telephony market, which uses the CDMA (code division multiple access) standard. The CDMA standard operates in the 1900MHz PCS band. This uses the mobile phone in fully-duplexed mode which requires simultaneous transmit and receive.

SAW based CDMA solutions are off chip and require two filters in a 3.8mm x 3.8mm package which is typically 2mm thick [53]. In order to switch between the SAW filters a separately packaged RF switch is required. This is in addition to the power amplifier module.

The Agilent solution only requires one FBAR filter which is small enough (1.2mm x 1.7mm) to be integrated (using wire bonding) in the same packaged module as the power amplifier. Fig 2.8 shows a packaged FBAR filter before and after bonding.

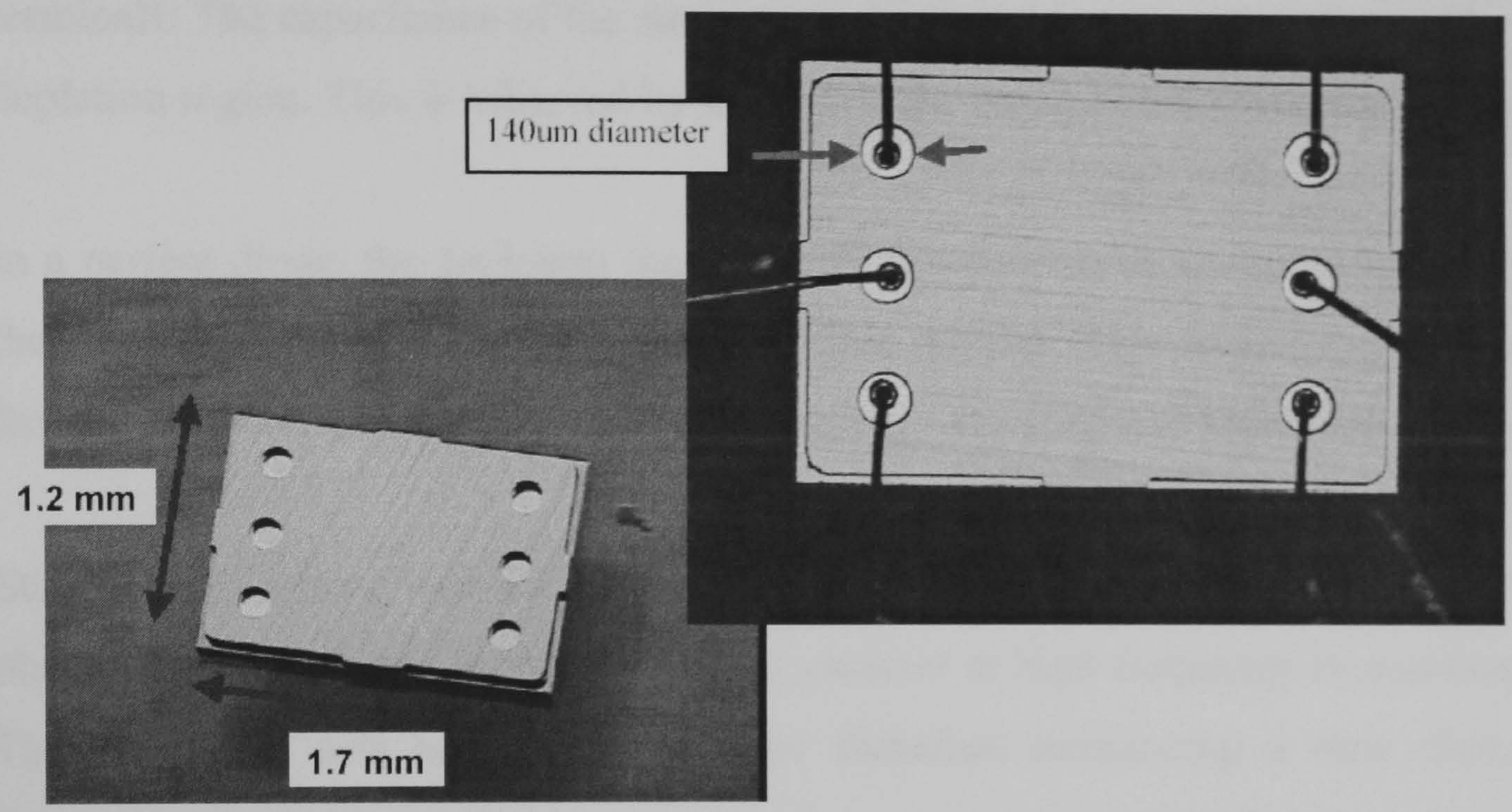


Fig. 2.8 A packaged FBAR filter. Reproduced from Ruby et al [53].

Unlike the RF MEMS switches of Teravicta, Agilent integrated the FBAR devices to provide a single module solution. This has immediate benefits to the wireless market by providing smaller, lighter and lower cost handsets.

2.4 Micromachined tunable capacitors

A variable capacitor is a device which can have its capacitance varied in response to a stimulus. For circuit applications this stimulus is usually electrical. However, in MEMS, the variable capacitor structure forms the basis of many sensing elements. These include accelerometers and pressure sensors.

In RF systems the variable capacitor is used in conjunction with an inductor to form an *LC* tank. This forms the basis of a tunable filter or voltage controlled oscillator (VCO).

Traditional electronic variable capacitor implementations are solid-state. Solid-state varactors are formed using p-n diodes in silicon [54] or Schottky diodes in GaAs [55]. In both cases a depletion region bounded by static charge is formed at the junctions.

The depletion region acts as a dielectric thus providing a capacitance between the terminals. The capacitance of the structure is decreased by increasing the width of the depletion region. This is achieved by increasing the reverse bias across the junction.

In a perfect diode, the depletion region would not conduct at all. However, in reality there exists a small conduction current in these devices. This contributes to losses in the structure and these losses become increasingly significant at higher frequencies.

Standard solid-state varactors show tuning ratios of approximate 4:1, for sub 5V biasing [56]. The main problem with the varactor at high frequency is non-linearity. The RF signal acts to bias the varactor therefore introducing a time dependent capacitance and signal noise.

2.4.1 Electrical quality factor for capacitors

The demand for high performance tunable capacitors in the RF industry is strong because modern communications requires signal agility in crowded frequency bands. This is best achieved using low loss capacitors which allow for sharp tuning and filter peaks. But in order to achieve the required signal agility the tuning range needs to be large.

The quality, Q, factor is an important concept in the field of RF MEMS, as it is indicative of the losses in a system. Formally, it is defined as the ratio of energy stored in a system to the energy dissipated per cycle of resonance [2]. It is common for a MEMS device to have two quality factors, electrical and mechanical.

In variable capacitor applications, the electrical Q is of importance to RF designers. These devices are typically used in inductance-capacitance (LC) voltage controlled oscillators (VCOs). The electrical Q of the LC tank must be as high as possible to achieve low phase noise in the output. The square of the quality factor for the LC tank configuration is inversely proportional to the product of the phase noise and the current consumption [57].

The losses in a variable capacitor arise from the dielectric medium and the finite resistance of the conductors. If dielectric losses have been eliminated, and the resistive losses dominate, then electrical Q can be calculated using eqn. (2.1).

$$Q = \frac{1}{wCR} \qquad \textbf{- (2.1)}$$

where C is the capacitance of the device, Q is the electrical quality factor, w is the oscillation angular frequency and R is the equivalent series resistance [2]. The equivalent series resistance has to be kept low to achieve a high Q.

In direct current (DC) applications, the thickness of metal interconnect determines the resistive losses with an increase in the resistance as interconnect becomes thinner. RF signals tend to propagate only on the surface of conductors due to skin depth effects. Hence, in RF design, the resistivity of the metal determines the RF losses. Low resistivity metals such as gold are then desirable for RF MEMS.

MEMS tunable capacitors use air as the dielectric medium. This is advantageous, because the dielectric losses of air are negligible, even at RF. The combination of low dielectric losses and the ability of MEMS devices to be fabricated using low resistivity metals such as gold leads to high Q operation.

2.4.2 Area tuning capacitors

There are two types of MEMS variable capacitors, gap tuning and area tuning. Eqn. (2.2) shows the capacitance, C, for a parallel plate capacitor with air as the dielectric, neglecting fringing effects.

$$C = {}^{\varepsilon_0 A}\!/_{g} \qquad \textbf{- (2.2)}$$

where ε_0, is the permittivity of free space (8.85×10^{-12} Fm^{-1}), A is the electrode overlap area and g is the electrode spacing.

Mechanical area tuning capacitors have been used in RF systems for many years. Air gap variable capacitor modules are used for VHF radio tuning. This type of unit, although exceptionally bulky compared to an on-chip varactor, provides excellent RF performance.

In order to tune the capacitance the overlap on a series of metal electrode plates is varied. An air gap is used to ensure a high Q. However, this module alone can weigh more than the modern mobile telephone and is poorly suited to the high speed electronic tuning systems.

The aim of area tuned MEMS capacitors is to miniaturise this type of variable capacitor whilst retaining good RF performance. The approach commonly reported the literature is illustrated in fig. 2.9.

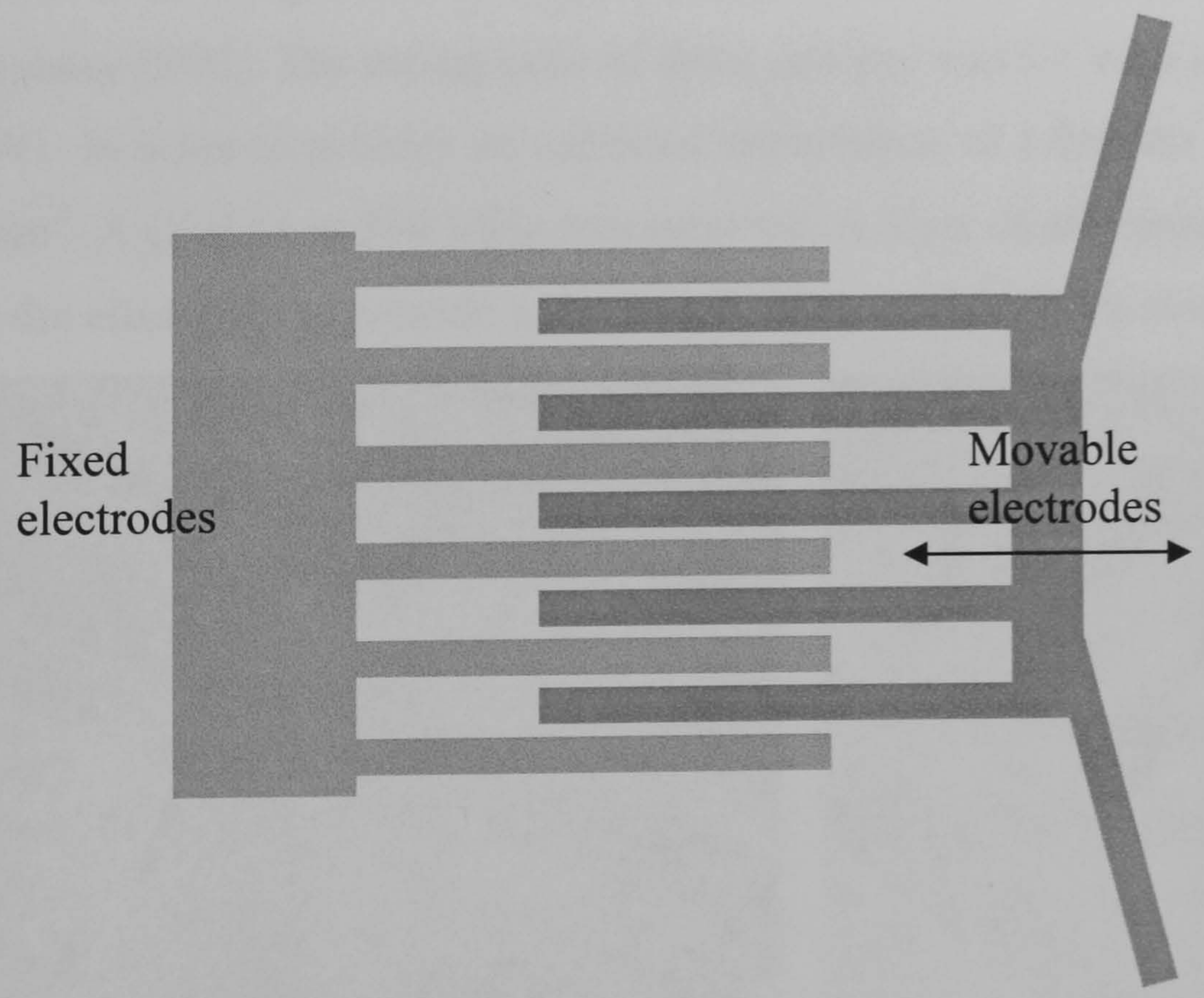


Fig. 2.9 A typical comb drive arrangement for an area tuned micromachined capacitor.

A series of interdigitated fingers are fabricated. One set of the fingers is suspended above the substrate. This comb arrangement of electrodes is then subjected to an applied biasing voltage. As the voltage is increased the electrostatic force between the fingers causes the suspended fingers to move thereby increasing the overlap, and hence the capacitance.

In principle the tuning range is only limited by the difference between the capacitance at unbiased overlap and the capacitance at maximum overlap. However, the system relies upon the interdigitated fingers being equally spaced. With equal spacing the electrostatic forces between the fingers cancel therefore eliminating any lateral movement. During motion the electrodes can drift from their lateral centre points. This imbalance can lead to a pull-in type instability and cause the sets of fingers to stick.

Larson et al [58] demonstrated an area tuning capacitor in 1991. They reported a tuning ratio of 2.85:1 with a tuning voltage between 80-100V. The unbiased capacitance of the device was 35fF.

Yao et al [2] have fabricated an area tuning capacitor which is shown in fig. 2.10. This is fabricated using DRIE of single crystal silicon. The starting substrate was silicon on insulator (SOI). The tuning ratio of these devices was 3:1 with a biasing voltage up to 14V. In order to achieve an unbiased capacitance of 1.8pF the overall device area is $2mm^2$. A Q of 34 at 500 MHz was reported. A layer of aluminium has been deposited on the electrodes to provide a low loss RF line on the silicon structures.

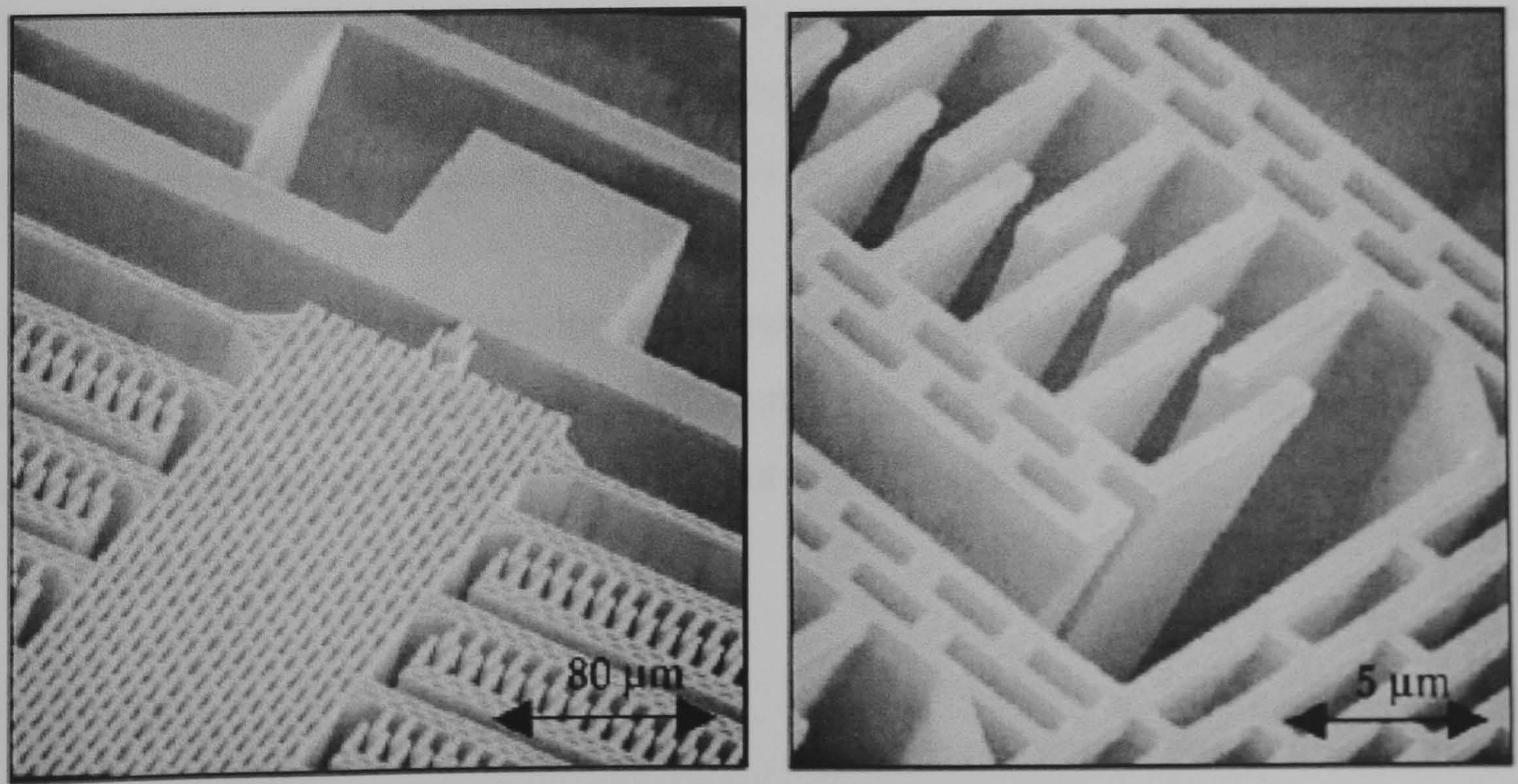


Fig. 2.10 An area tuning capacitor developed by Yao et al [2].

More recently this type of structure was reported by Borwick et al [59] with a tuning ratio of 8.4:1 using a biasing voltage of 8V from an initial capacitance of 1.4pF. The device has a Q in excess of 100 at 700 MHz and a self resonant frequency (SRF) of 3GHz. The SRF is the frequency at which the complex impedance of the capacitor becomes inductive. Above the SRF, the capacitor is unusable. As with Yao et al [2] the device is formed from deep reactive ion etched (DRIE) metallised silicon. The authors cite that suspension improvements have led to greater electrode movement and consequently an improved tuning ratio.

The main difficulty with an area tuning capacitor is effectively ensuring a compatible process flow with existing integrated circuits. The DRIE approach is not directly IC compatible. This restriction has limited the interest in the area tuning approach for MEMS to date and more focus has been placed on the alternative gap tuning approach.

2.4.3 Gap tuning capacitors

Gap tuning capacitors use the variation of the distance between two electrodes to alter the capacitance. An important advantage of the gap tuning capacitor is that they can be fabricated using relatively planar thin film technologies which are better suited to integration with existing ICs.

Fig. 2.11 shows a typical electrostatically biased device configuration. As a voltage is applied between the movable driving electrode and the fixed ground electrode, electrostatic attraction reduces the gap. This increases the capacitance.

Although comparable in operation to the switches presented in section 2.2, the aim of the capacitor structure is to achieve continuous tuning over a large range. The switches achieve very high tuning ratios but only in a bistable state.

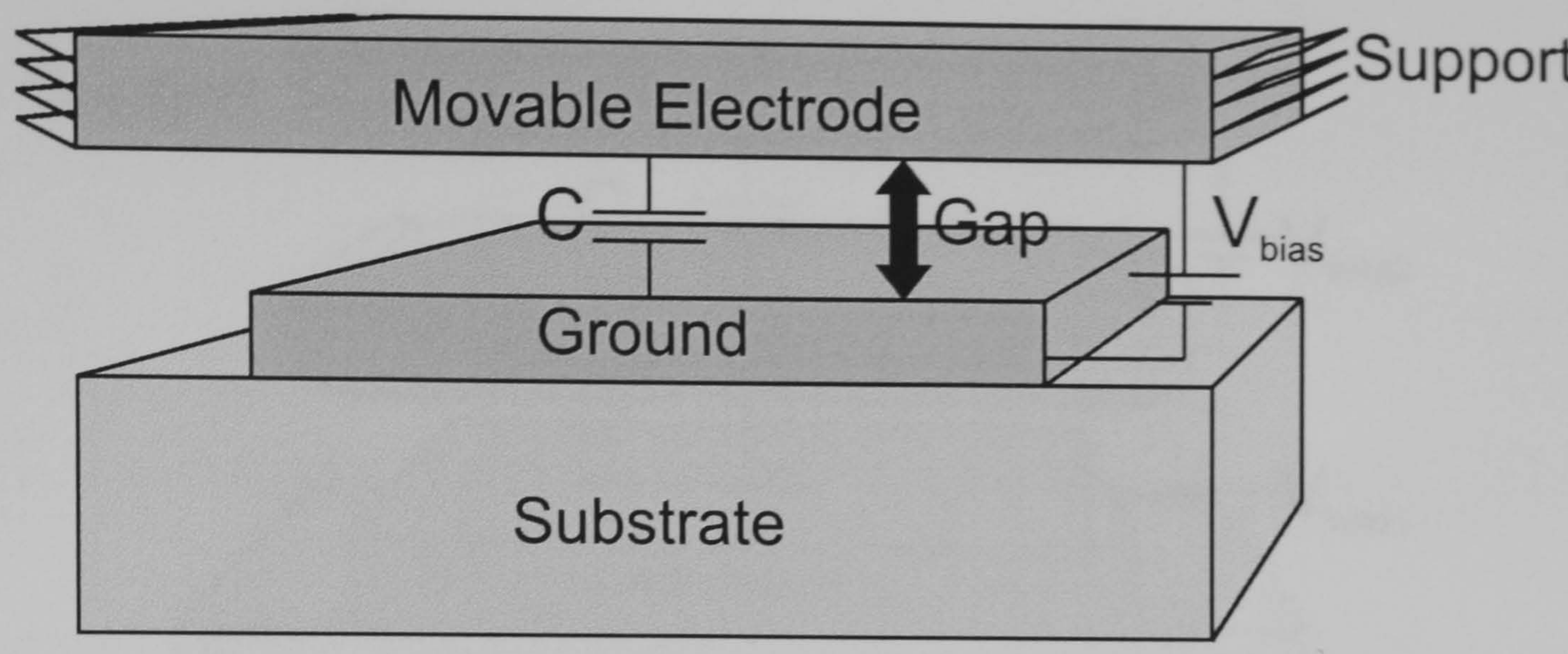


Fig. 2.11 A simple parallel plate micromachined capacitor arrangement.

Dec and Suyama [8] fabricated this type of capacitor with a Q-factor of 9.3 at 1.9GHz and a tuning ratio of 1.38:1 from an initial capacitance of 2.1pF. A tuning voltage up to 4V was used. This was fabricated using the multi user MEMS process (MUMPS) which uses polysilicon as a structural material. In 1997, Young and Boser [9] reported devices with aluminium as a structural material. Their reported tuning ratio was lower at 1.16:1 but the Q was higher at 60 for 1 GHz.

When a potential difference is applied between the plates of a gap tuning capacitor, the electrostatic force attracts the movable electrode towards the ground electrode. The spring force of the movable electrode opposes this attractive force.

For the gap to remain stable the spring force must be able to balance the electrostatic force. For a parallel plate capacitor, this only occurs for displacements up to one third of the unbiased gap. This puts a limit on the tuning ratio of the single-gap devices to 1.5:1. The mathematics of this are covered in more detail in chapter 3.

Dec and Suyama [10], proposed the three plate capacitor arrangement shown in fig. 2.12. With appropriate biasing the movable electrode can be displaced either towards the top or the bottom ground electrodes. In each direction a displacement of one third of the initial gap is permissible before the onset of pull – in. This arrangement can theoretically achieve a 2:1 ratio. The devices, again fabricated using the MUMPS process, achieved a 1.87:1 ratio with a Q of 7.1 at 2 GHz.

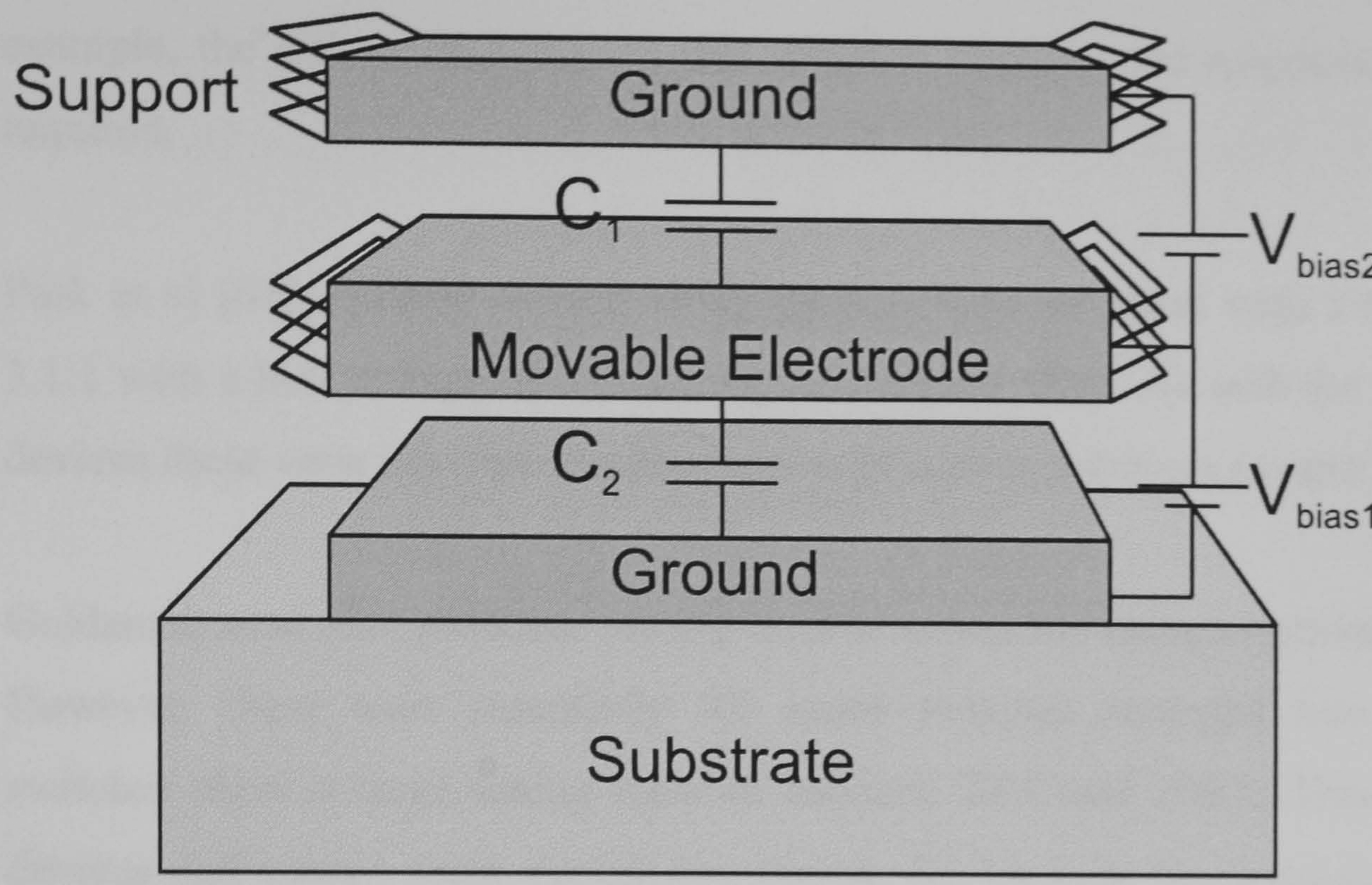


Fig. 2.12 A three plate tunable capacitor arrangement. [10]

Typical tuning ranges in the literature for actual devices have proved to be significantly less than 1.5:1 due to the effect of parasitic capacitances at bond pads and substrate interfaces.

A solution to the electrostatic pull-in limitations has been developed by Harsh et al [60]. They achieved a 7:1 tuning ratio by using electrothermal actuation which relies on current flow through a metal conductor to cause an increase in temperature which in turn causes an expansion of the metal.

The structure presented by Harsh et al was fabricated using the MUMPS process. However, the silicon based devices were flip-chip bonded onto a ceramic substrate with much better RF performance than lossy silicon. The silicon which remained after flip chip bonding was etched away during device release. The quality factor of these devices was reported to be 1050 at 1 GHz for a series mounted device.

As with the switches, the downsides of electrothermal actuation are higher power consumption and slower response time compared to the electrostatic regime. However, unlike the RF switches the response time is less important. With wide tuning range devices, frequency switching can be performed across RF bands. For mobile phone applications this may only occur when the user moves from, for example, the UK to the USA. In this situation microsecond response times are not required.

Park et al [61] reported devices using piezoelectric actuation with a tuning ratio of 3.1:1 with a bias voltage of 6V and a Q of 210 at 1 GHz. As with the electrothermal devices these were flip-chip bonded onto an insulating substrate (quartz).

Goldsmith et al [62] produced widely tunable capacitors using electrostatic actuation. However, these were essentially RF shunt switches arranged into a bank. The switches show a large tuning ratio of between 70:1 and 100:1. These are bistable devices and cannot show continuous tuning. By banking the capacitors a range of capacitance values can be tuned. Goldsmith et al reported a tuning ratio of 22:1 from an unbiased value of 1.5pF.

Rizk and Rebeiz [63] used metal contact series switches in a capacitor bank. The maximum capacitance of RF shunt switches is dependent on the degree of contact with the lower electrode dielectric. Rizk and Rebeiz identified this as a source of device to device variation. Their approach used a metal-insulator-metal lower electrode structure as illustrated in fig. 2.13.

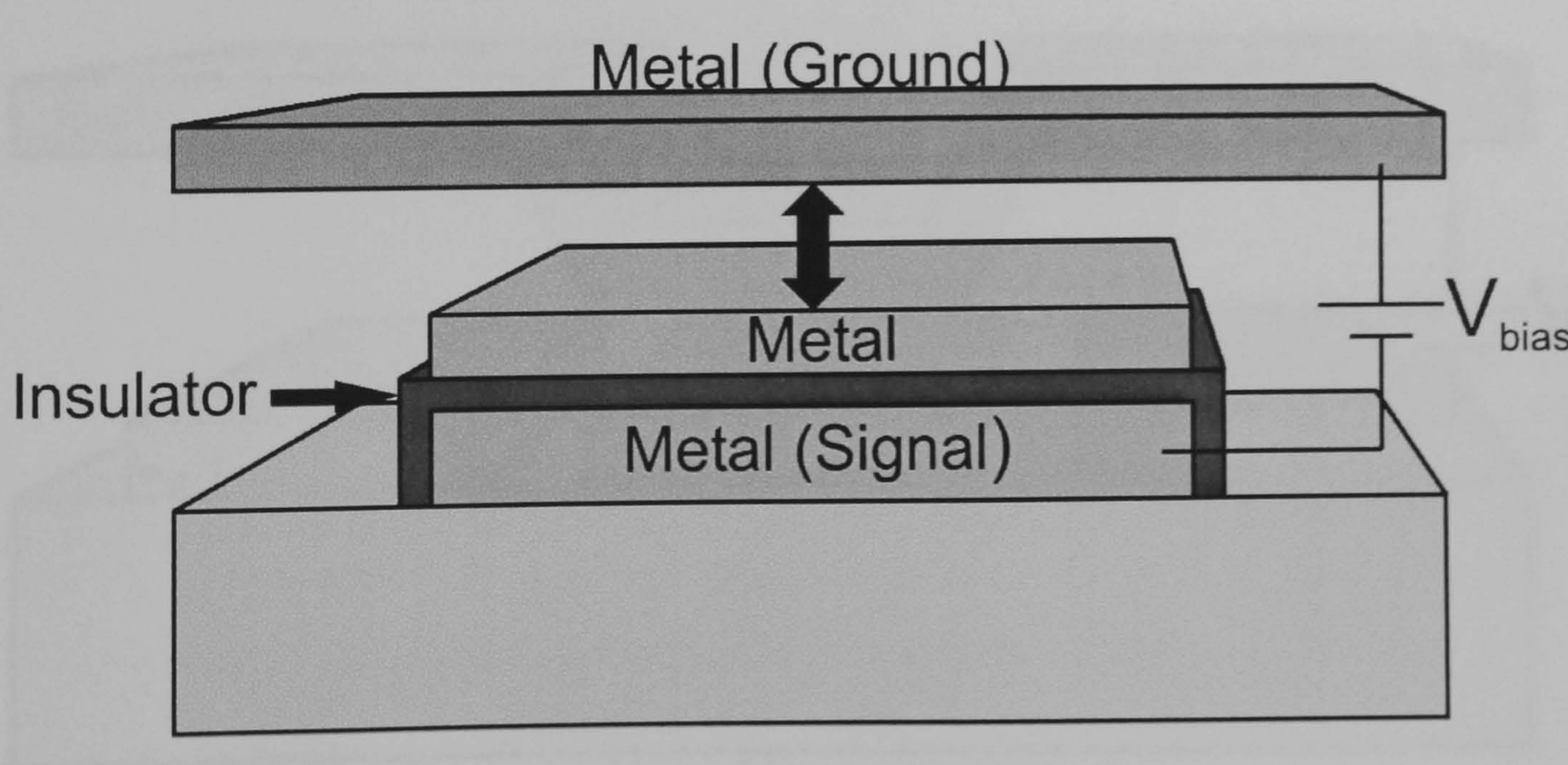


Fig. 2.13 The metal-insulator-metal switch for capacitor bank tuning.

When a biasing voltage is applied to this structure, the upper electrode deforms to contact the top metal of the lower electrode. This capacitively connects the lower metal signal line to ground. The on state capacitance is predetermined by the MIM structure and minimises contact related variation. Two capacitors were used in the bank which allows for four discrete capacitances to be tuned. In this implementation a peak tuning ratio of 20:1 was achieved.

However, for nearly continuous tuning large banks of capacitors are required. They consume significant substrate areas and the additional interconnect impairs overall RF performance. The discretely tunable capacitor can provide a wide tuning range but fails to address the crowded frequency band issue. The demand exists for a capacitor with a wide tuning ratio and a continuous tuning range. This serves the co-requisites for frequency agile communications and wideband tuning.

2.4.4 Widely tunable micromachined capacitors

The first approach to avoid pull-in was published by Zou et al [64] in 2000. Their device is illustrated in fig. 2.14. It uses the principle discussed in the RF switch section of separating the biasing electrodes from the RF signal line. This alone can produce benefits in terms of avoiding pull-in and will be discussed much further in chapter 3. However, the second feature of the device is the use of different gaps for the biasing and capacitive electrodes.

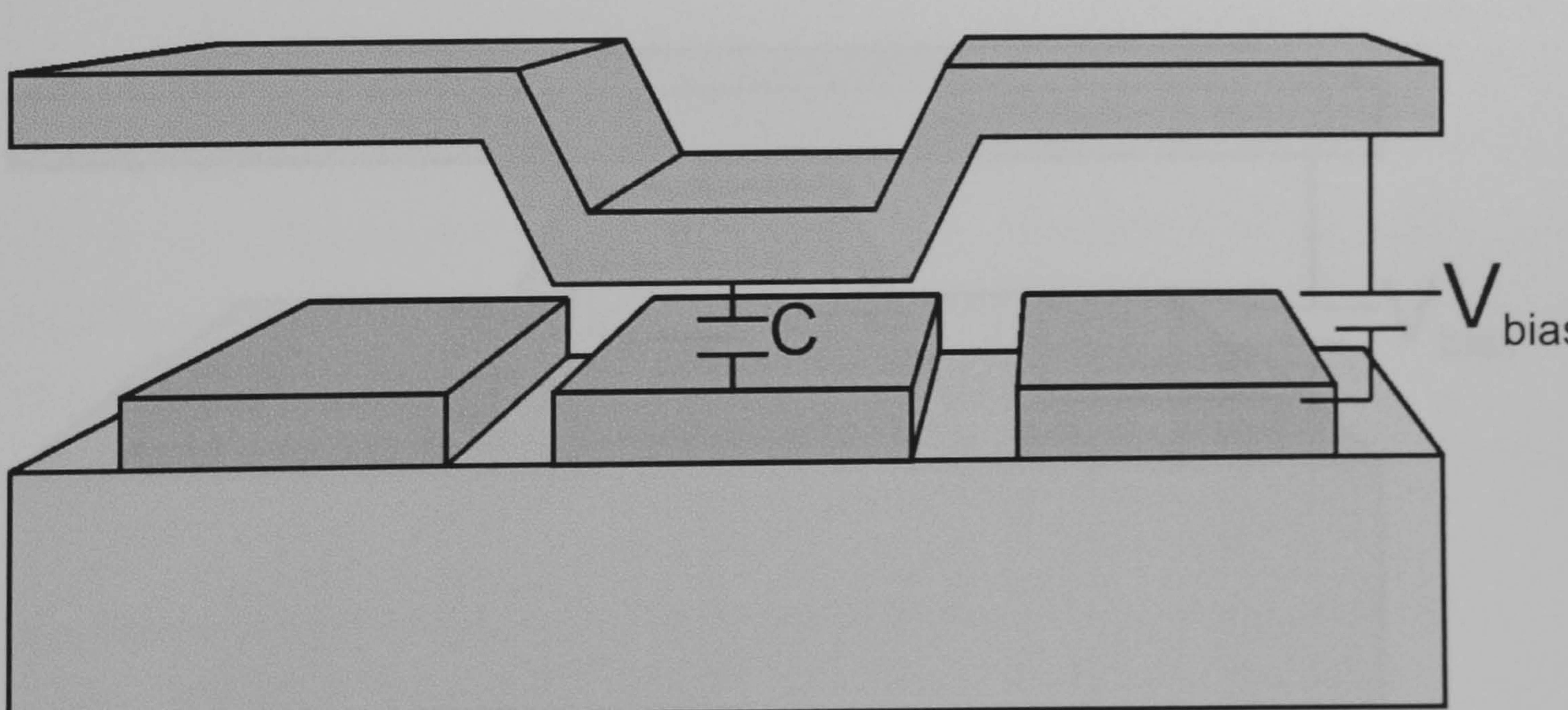


Fig. 2.14 The two-gap tunable capacitor with a stepped upper electrode as implemented by Zou et al [64].

If the gap of the biasing electrodes is more than three times greater than the capacitive gap then electrostatic pull-in is eliminated. A tuning ratio of 1.4:1 was reported. In this design evaporated gold was used for the lower electrodes and permalloy (NiFe) for the upper electrode. A copper sacrificial layer was used. The authors set the biasing and capacitive gaps to 3 μm and 2 μm respectively.

The use of permalloy for the upper electrode is a non-standard choice for micromachined tunable capacitors. The application was revealed in a subsequent publication by Chen et al [65]. The authors used the permalloy to provide a magnetic part for the self-assembly of inductors. This will be discussed further in the next section.

Nieminen et al [66, 67] in 2002 extended the approach taken by Zou et al [64] with the device structure shown in fig 2.15. In this design the upper electrode is planar but the lower electrode topology is varied to set the gaps. This has led to devices with a tuning ratio of 2.25:1 from an initial capacitance of 1.58pF and a *Q* of 66 at 1 GHz.

Their fabrication route for the two-gap tunable capacitor used gold as the structural material with a polymer sacrificial layer providing gaps of 0.5 μm and 1.5 μm. These devices were developed in parallel with the structures presented in this thesis.

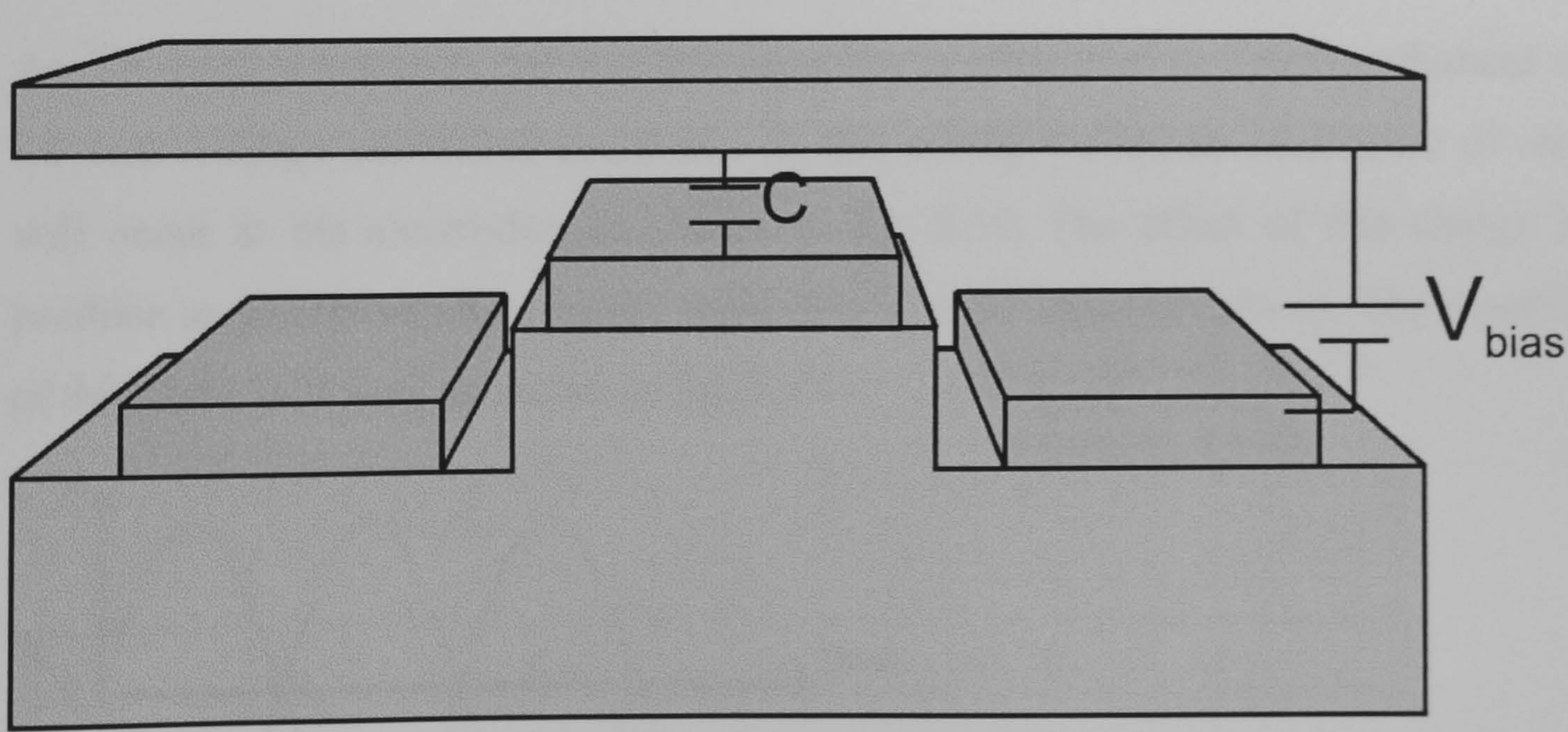


Fig. 2.15 The two-gap tunable capacitor approach used by Nieminen et al [66,67].

In 2003, Tsang et al [68] utilised the MUMPS process to develop a two-gap tunable capacitor and reported a tuning ratio of 5.3:1 with a *Q* up to 50 at 2.5 GHz. As with previous MUMPS implementations, RF improvements are limited due to the use of polysilicon and relatively thin metallisations.

Interest in the widely tunable gap based capacitor continued in recent literature with Rijks et al [69] reporting a tuning ratio of 17:1 with a Q of 150 at 1 GHz. They have used the PASSI™ surface micromachining process developed by Philips. This uses 5μm aluminium as a structural material on high resistivity silicon.

The high tuning ratio has been achieved partially through the two-gap structure but also by exploiting the native oxide on the Al to allow complete contact of the electrodes whilst retaining a capacitor. These devices are combining the high tuning ratio of the capacitive shunt RF switches and the continuous tuning ratio available from the two-gap structure.

2.4.5 Harmonic distortion in gap tuning MEMS capacitors

The gap tuning capacitor uses a DC bias to alter its capacitance. This bias causes charge to accumulate on the electrode plates. As described previously, these form the basis of electrostatic tuning. In reality, the variable capacitor will be used as a circuit element. This introduces additional charge effects associated with the circuit.

As discussed previously, the variable capacitor is often used as a tuning element in an LC tank voltage controlled oscillator. In this configuration, an oscillation of charge will occur at the electrodes, as shown in fig. 2.16. The effect of this charge is to produce an attractive electrostatic force between the capacitor plates. The magnitude of this force will vary as shown in fig. 2.17.

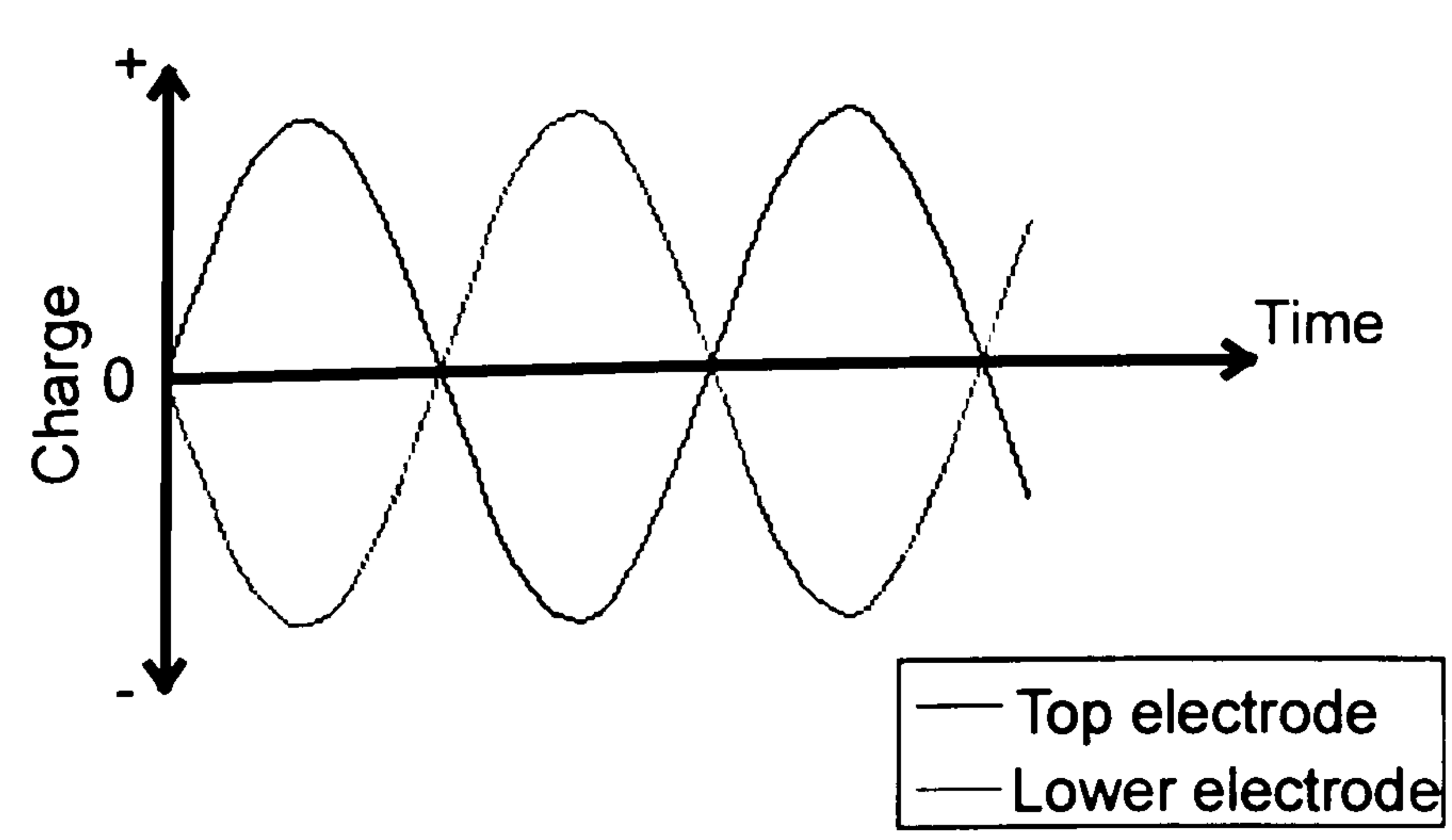


Fig. 2.16 Charge on the electrodes of a capacitor with respect to time.

The mechanical resonant frequency of the movable electrode is important when determining the effect of the oscillating electrostatic force. If the mechanical resonant frequency is comparable to the electrical frequency of the VCO then the movable electrode will move directly in response to the electrostatic force waveform shown in fig. 2.17. It follows that the capacitance of the device will also oscillate. This harmonic distortion is superimposed onto any DC biasing and limits the tuning resolution of the VCO.

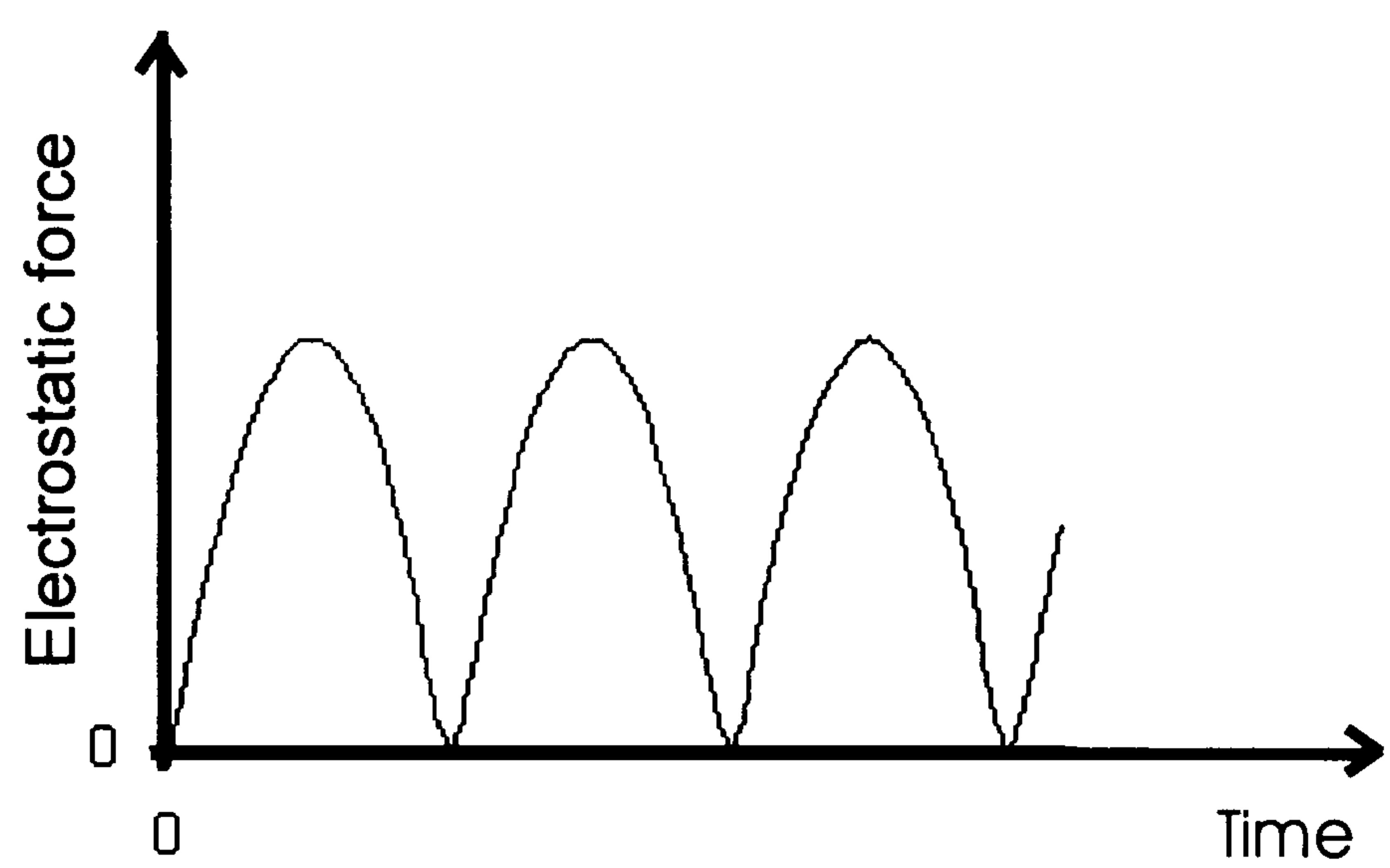


Fig. 2.17 Electrostatic force on the movable electrode of a tunable capacitor with respect to time.

MEMS tunable capacitors typically have mechanical resonant frequencies in the order of kHz. However, they are used at electrical frequencies of MHz or higher. This frequency disparity means that the movable electrode does not respond directly to the electrostatic oscillation. Instead, an average force of attraction, and hence displacement, is experienced by the movable electrode. The magnitude of this displacement is determined by the root mean squared (rms) voltage across the capacitor in the VCO [26].

The advantage of the MEMS tunable capacitor is that it introduces negligible harmonic distortion to the VCO. However, in addition to the DC biasing voltage, the RF rms voltage must be considered in the electromechanical modelling of these devices.

2.4.6 The commercialisation of the micromachined tunable capacitor

The tunable capacitor has received considerable interest in recent literature owing to its promise to significantly improve on both the tuning ratio and RF performance of solid-state varactors. However, much of the work is still at the research stage and currently devices have not yet entered large scale production.

A key feature of these capacitors and many of the other RF MEMS devices is that there is no defined process flow. Almost all of the devices presented in this section are using different process flows and until one ideal route emerges industry take up is limited. The best fabrication route depends on compatibility with existing ICs.

Another important factor is that the primary application of the capacitor is integrated in an *LC* tank with an on-chip inductor. Capacitor process flows need to be shared with good inductors to achieve the best performing tank.

2.5 Micromachined inductors

Demand exists for on-chip, low loss, inductors with high Q factors. As described previously, they have applications in VCO and filter applications. On-chip spiral inductors have been available for many years [70]. However, their RF performance is limited due to a high capacitance to ground which reduces the self resonant frequency and eddy current losses to the substrate which limit the Q.

These performance limitations arise from the fact that the inductors are in physical contact with the substrate. A quality factor of 3 at 1 GHz is typical [70]. Micromachining techniques allow the third dimension to be fully exploited during fabrication which enables inductors to be isolated from the substrate by air.

Initial MEMS based inductors were used to provide electromagnetic actuation. However, recent interest in RF applications has led to research focusing on the improvement of high frequency performance.

Fig. 2.18 shows a miniaturised coil inductor fabricated by Malba et al [71]. This is a solenoid type inductor fabricated using thick electroplated metals. An alumina core has been included in the structure which was attached to the substrate using adhesive during processing. For this four turn coil with an inductance of 18nH the authors reported a Q of 18 at 0.7 GHz. However, the process flow for these devices is incompatible with existing IC techniques.

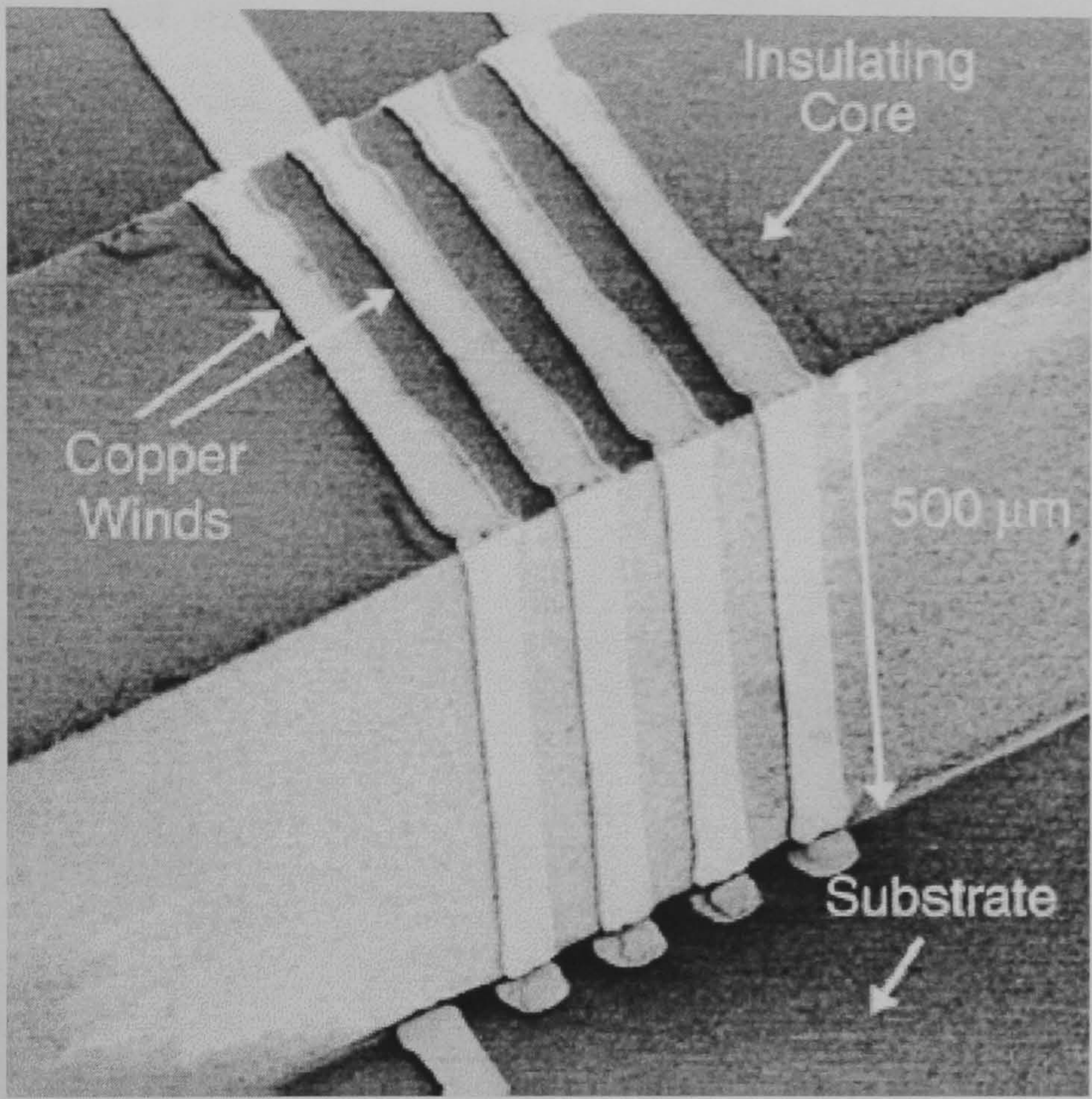


Fig. 2.18 Alumina coil inductor fabricated by Malba et al [71].

Malba et al used an approach which focused on the miniaturisation of a copper coil inductor for RF applications. The majority of inductor research [72-82] for RF applications focuses on improving the performance of air based spiral or meander inductors. The general aim of this research is to remove the substrate from the inductor. There are various routes to achieve this isolation which will be discussed in the following sections.

2.5.1 Surface micromachined suspended spiral inductors

By suspending the inductor above the substrate the capacitance to ground can be reduced thereby increasing the self resonant frequency. The coil is surrounded by air which minimises dielectric losses at RF and increases the Q.

The use of surface micromachining enables thick metallisations to be used which minimises the coil resistance and reduces skin depth related losses. Again, this acts to elevate the Q.

Fig. 2.19 shows a suspended spiral inductor arrangement from Yoon et al [83]. It was fabricated using electroplated Cu with an electroplated Ni sacrificial layer above a glass substrate. The inductor has an inductance of 1.75nH with a Q of 57 at 10 GHz.

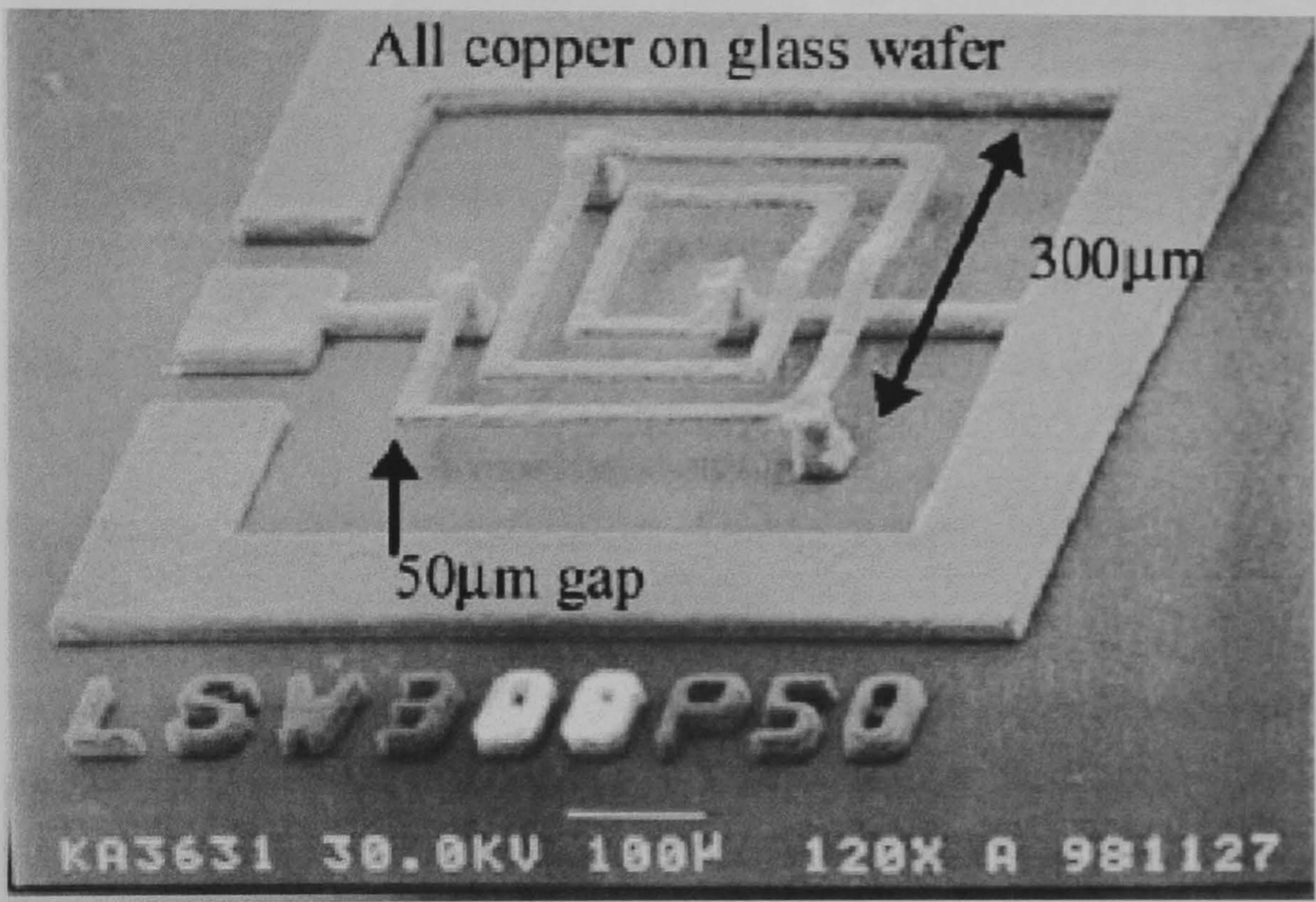


Fig. 2.19 Suspended copper inductor from Yoon et al [83].

2.5.2 Self-assembled spiral inductors

Self-assembly techniques have been used by some research groups to further reduce the capacitance to ground of the suspended inductors. By rotating the inductor through 90° it is possible to virtually eliminate its footprint on the substrate.

Chen et al [65] used a magnetic assembly technique to fabricate their inductors. They developed a shared capacitor and inductor process flow. Permalloy (NiFe) was used as the primary structural material for the upper electrode of the capacitors and the spiral inductors (see fig. 2.20).

After release, the inductors are magnetically attracted into the vertical position. Compared to equivalent 4.5 nH planar inductors, the authors reported a quality factor increase from 3 to 12 and a self resonant frequency improvement from 1 GHz to above 4 GHz.

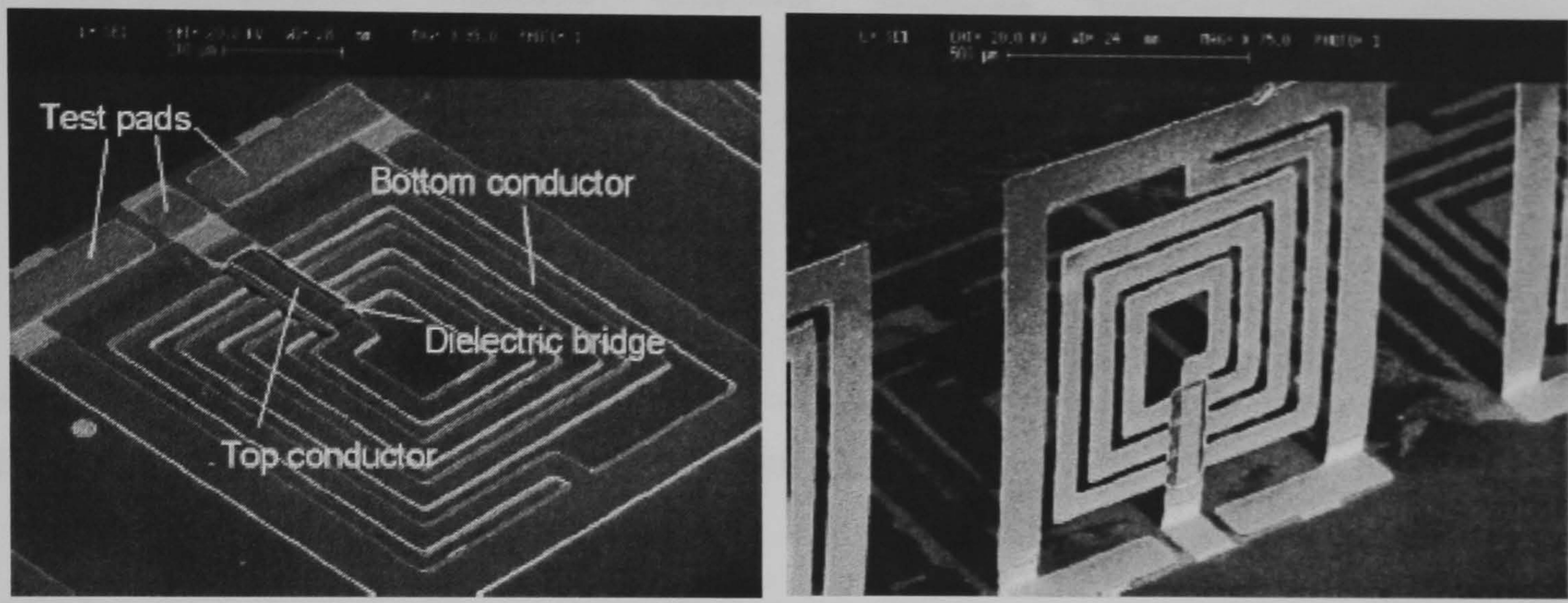


Fig. 2.20 A self assembled inductor from Chen et al [65].

Dahlmann et al [73] used surface tension to assemble RF inductors. The inductor is initially fabricated using standard planar based surface micromachining. Solder is applied and reflowed to act as a hinge which rotates the inductor and fixes it when set. Standard micromachining techniques could not achieve these extremely high aspect ratios in metals therefore self-assembly techniques are employed. For a 2nH inductance Dahlmann et al have a reported Q of 30 at 2 GHz.

Effectively packaging these vertical inductors alongside surface micromachined tunable capacitors will require the development of new techniques.

2.5.3 Bulk micromachined inductor techniques

Bulk etching approaches are available to improve the RF performance of existing planar inductors. These involve either etching the substrate from under the inductor (fig. 2.21) or thinning the substrate from the back to leave the inductor suspended on a thin membrane (fig. 2.22).

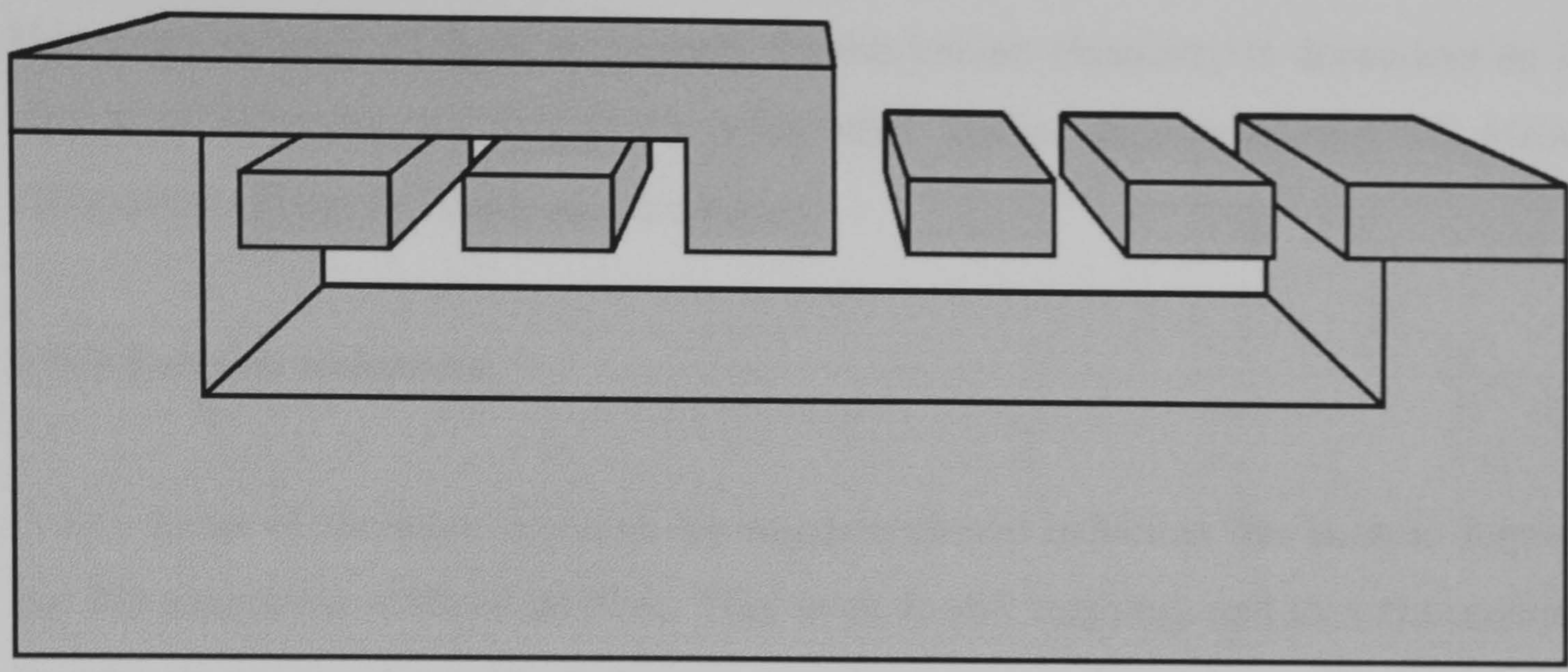


Fig. 2.21 Top side wafer etch leaving a suspended inductor

Etching the substrate from under the inductor is advantageous because the process flow can be made fairly simple using isotropic gas etches for silicon such as XeF_2. Long et al [76] reported that for a 12 nH inductor, before etching the silicon substrate, the peak *Q* factor was 5 at 3 GHz with a self resonant frequency of 5 GHz. After partially etching the substrate by 42 μm, these figures were increased to a peak *Q* of 13.3 at 7.7 GHz with a SRF of 13.4 GHz.

Muller et al [84] demonstrated the membrane technique for polyimide on a GaAs substrate. They reported a 1.84 times improvement in the self resonant frequency of a 1.51 nH meander inductor when compared to equivalent inductors on bulk silicon.

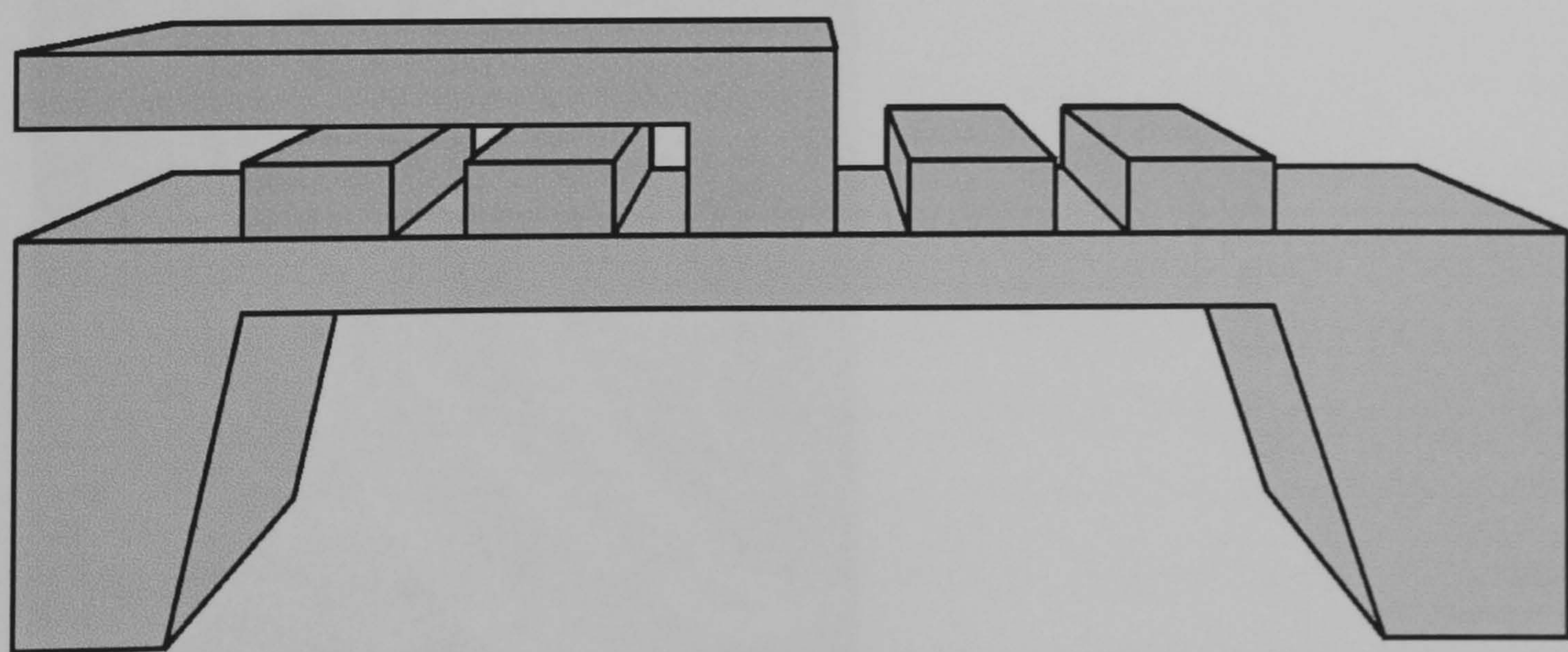


Fig. 2.22 Back side wafer etching to leave a membrane suspended inductor.

However, for each of these techniques the fabrication chemistry is dependent on the choice of substrate and integration with other surface micromachined RF MEMS components presents additional challenges.

2.5.4 Tunable inductors

A key focus of literature research for micromachined inductors has been to improve the RF properties of fixed devices. This work is still ongoing, and as a consequence the development of tunable inductors lags behind that found in tunable capacitors. Although, as with the capacitors, switched digital tuning has been reported [85].

Fig. 2.23 shows a hairpin type inductor from Lubecke et al [77]. The devices have been fabricated using a bimorph structure of metal and polysilicon. The residual stress in the inductor causes initial bending which acts to lift it from the susbtrate. As the temperature of the inductor is varied either through ambient variation or localised electrical joule heating the degree of warping varies. This has been shown to give an 18% inductance variation (from approximately 0.7 nH at 5 GHz) for a 175°C temperature variation. The Q varied by less than 10% for this temperature variation.

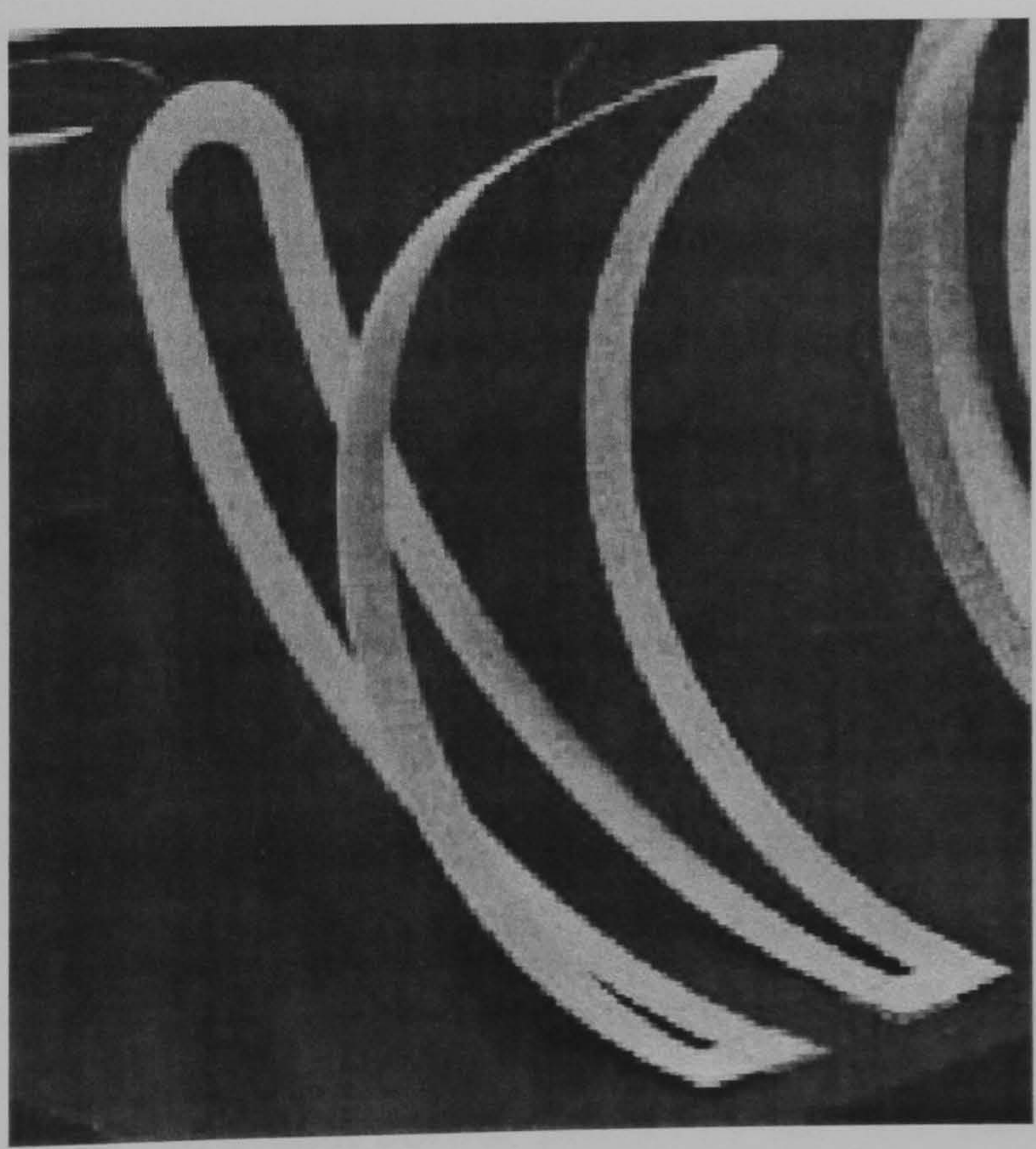


Fig. 2.23 Temperature variable inductor from Lubecke et al [77].

Zine-El-Abidine et al [86] used a modified approach by fabricating two inductors. One had a stress curvature and the second inductor was attached to electrothermal actuators. When actuated, the second inductor buckled towards the curved inductor therefore changing the angle between the inductors. This was shown to provide a total inductance variation of 13%.

The downside of these types of tunable inductors is that, by their nature, they are susceptible to environmental tuning which may limit their application in RF MEMS. In addition, the electrothermal actuation is particularly power consuming compared to electrostatic approaches.

2.5.5 Commercialisation of micromachined inductors

Fixed micromachined inductors have been demonstrated which have shown considerable improvements over existing on-chip solutions. There are only a few examples of tunable inductors in the literature and these are far from production.

The commercialisation of the inductors for RF applications is linked with the success of the tunable capacitors since the surface micromachined fabrication regimes are comparable. In both cases though, the success of the micromachined *LC* tank relies upon integration with existing ICs. There are a number of packaging issues which need to be fully resolved before these devices can truly enter the marketplace.

2.6 Chapter summary

- During the 1990s MEMS based sensing and optical applications were primary investment areas. Analog Devices has achieved good market penetration through the development of micromachined accelerometers. Texas instruments has entered the $4 billion digital projector market through the Digital Micromirror Device (DMD). Epson use MEMS based print heads to provide low cost colour printers with high resolution.

- The primary attraction of using micromachining for the production RF devices is that performance can be retained or improved whilst enabling integration with existing ICs.

- The RF switch is currently the most mature RF MEMS device with many examples in the literature. Typically, they are either metal to metal contact switch or capacitive shunt configurations. The TT612 from Teravicta is the first micromachined switch to reach the marketplace.

- Mechanical resonators can be used for frequency generation, mixing and filtering. These are commercially available as quartz, surface acoustic wave (SAW) and cavity resonators. Generally, these are costly large scale devices. Microelectromechanical beam resonators are aimed at VHF applications. Thin film bulk acoustic resonators (FBAR) can achieve resonant frequencies nearing 1 GHz. The micromechanical disk resonator has been demonstrated with a resonant frequency 1.51 GHz.

- Traditional electronic variable capacitor implementations are solid-state. The main problem with the varactor at high frequency is non-linearity. The RF signal acts to bias the varactor therefore introducing a time dependent capacitance and signal noise.

- The quality factor, Q, is an important concept in the field of RF MEMS, as it is indicative of the losses in a system. Formally, it is defined as the ratio of energy stored in a system to energy dissipated per cycle of resonance.

- MEMS tunable capacitors use air as the dielectric medium. This is advantageous because the dielectric losses of air are negligible, even at RF.

- Widely tunable capacitors are desirable because they enable wide band frequency operation from a single device. Electrostatic gap tuning capacitors suffer from tuning limitations, due to pull-in, and parasitics. Capacitance banking of single-gap capacitors can be used to increase the tuning range. However, these are substrate area intensive and only provide discrete capacitances.

- The two-gap capacitor structure has received interest in recent literature as a route to providing a wide continuous capacitance tuning range.

- Micromachining techniques enable inductors to be physically isolated, at least in part, from the substrate. This reduces the capacitance to ground and elevates the quality factor. Self-assembly techniques have been reported which enable the inductor to be positioned perpendicular to the substrate, therefore minimising its substrate footprint.

- Tunable inductor designs exist but research is limited compared to other RF MEMS devices. They tend to be based on electrothermal actuation mechanisms and show very restricted tuning ranges when compared to capacitors.

Chapter 3

Electromechanical simulation of micromachined capacitors

The installation of a fully equipped cleanroom can prove prohibitively expensive for small start-up companies. Many MEMS companies prefer to use a 'fabless' approach for initial product development. This is where external foundries are used to fabricate prototypes.

Development costs can be minimised by reducing the number of foundry runs required to achieve a working device. Computer simulation tools allow designers to expect that fabricated device parameters are comparable to the designed specification.

Coventorware (formerly MEMCAD) is a commercial finite element analysis (FEA) package specifically developed for the simulation of micromachined devices [12]. This chapter presents electromechanical simulation results from a range of tunable capacitor designs.

In reality the ideal parallel plate arrangement may not be a good approximation. The devices simulated in this chapter start with an ideal parallel plate capacitor, and then illustrate the effect of a deviation from the parallel plate approach on the tuning ratio. Devices with electrode curvature, leverage actuation and multiple electrode gaps are all considered.

3.1 The ideal parallel plate capacitor

Fig. 3.1 shows a single-gap parallel plate arrangement for a capacitor. The lower electrode is fixed to a substrate. The upper electrode is suspended and is free to move parallel to the lower electrode.

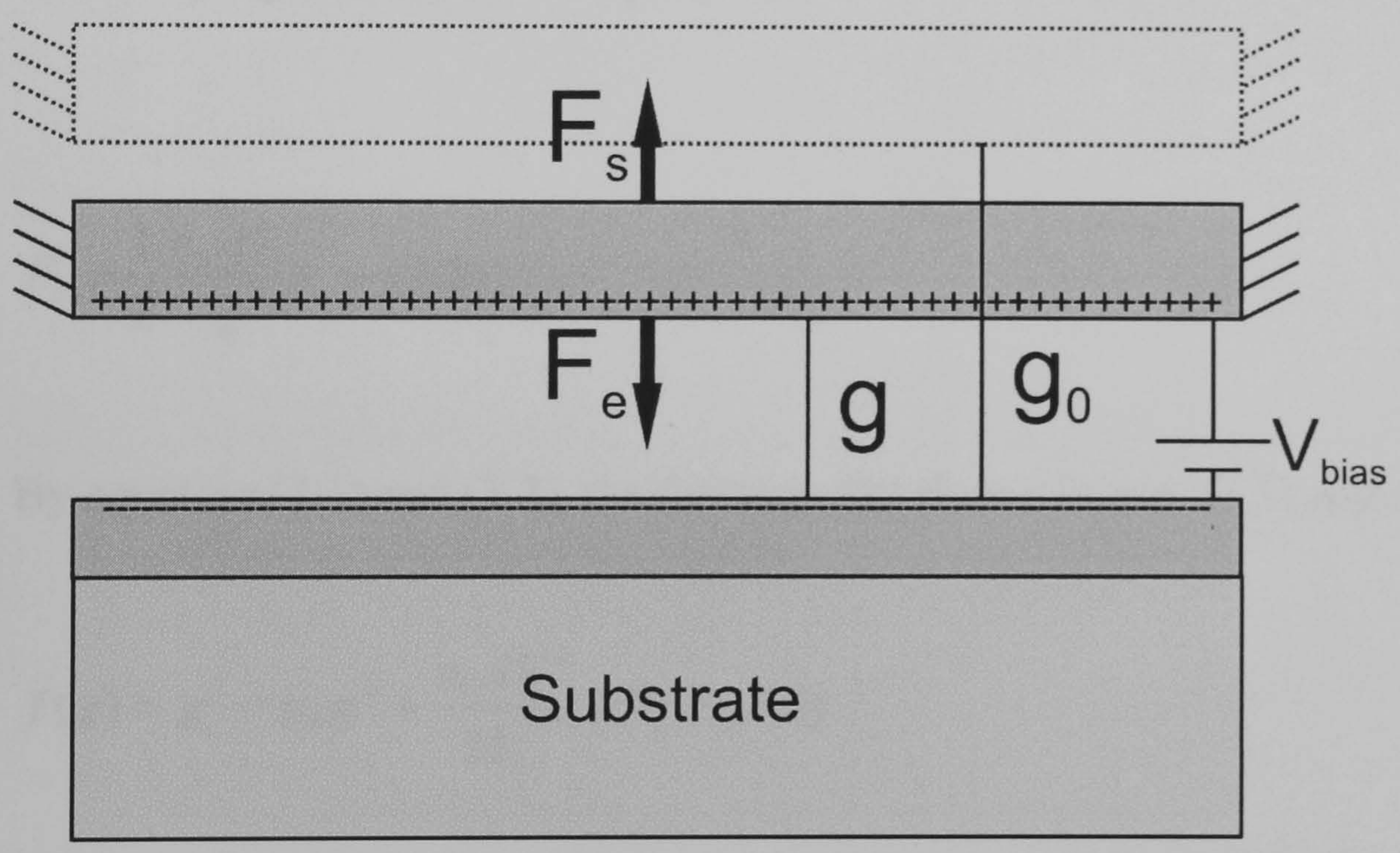


Fig. 3.1 Single-gap parallel plate capacitor arrangement. Under a biasing voltage V, the electrode gap is reduced from g_0 to g. For a stable solution the restoring spring force, F_s must counter the electrostatic force of attraction, F_e.

Pull-in can limit the tuning range of electrostatically biased micromachined capacitors. In an ideal parallel plate, single-gap capacitor the maximum tuning ratio can be shown to be 1.5:1 [87].

When a potential difference is applied between the plates of the capacitor shown in fig. 3.1, the electrostatic force attracts the upper electrode towards the lower electrode. The restoring spring force of the upper electrode opposes this attractive force. For the gap to remain stable, the spring force must be able to balance the electrostatic force.

For this parallel plate arrangement, the restoring spring force, F_s can be calculated from eqn. (3.1), where g_0 is the unbiased electrode gap, g is the actual electrode gap and k_s is the spring constant for the upper electrode.

$$F_s = -k_s (g_0 - g) \quad \textbf{- (3.1)}$$

The electrostatic force of attraction, F_e, can be calculated from eqn. (3.2) where ε_0 is the permittivity of free space, A is the overlap area of the electrodes, V is the applied voltage across the electrodes, g is the electrode gap, and the process occurs in a vacuum (otherwise the relative permittivity ε of the gap medium needs to be inserted on the top right hand side of eqn. (3.2)).

$$F_e = \frac{1}{2}\frac{\varepsilon_0 A V^2}{g^2} \quad \textbf{- (3.2)}$$

By equating (3.1) and (3.2), the function $f(g)$ shown in eqn. (3.3) is produced.

$$f(g) = g^3 - g_0 g^2 + \frac{\varepsilon_0 A V^2}{2k_s} = 0 \quad \textbf{- (3.3)}$$

Fig. 3.2 shows an arbitrary plot of eqn. (3.3). As the biasing voltage is increased then the curve is shifted upwards as indicated. In curve A there are two positive values of g where $f(g)=0$.

When a biasing voltage is applied then the upper electrode will displace until equilibrium between the electrostatic and restoring force is reached. With respect to curve A, equilibrium will be found at the value of g, which is closest to g_0. If the voltage is further increased such that curve C becomes valid then no stable solution where $f(g)=0$ exists.

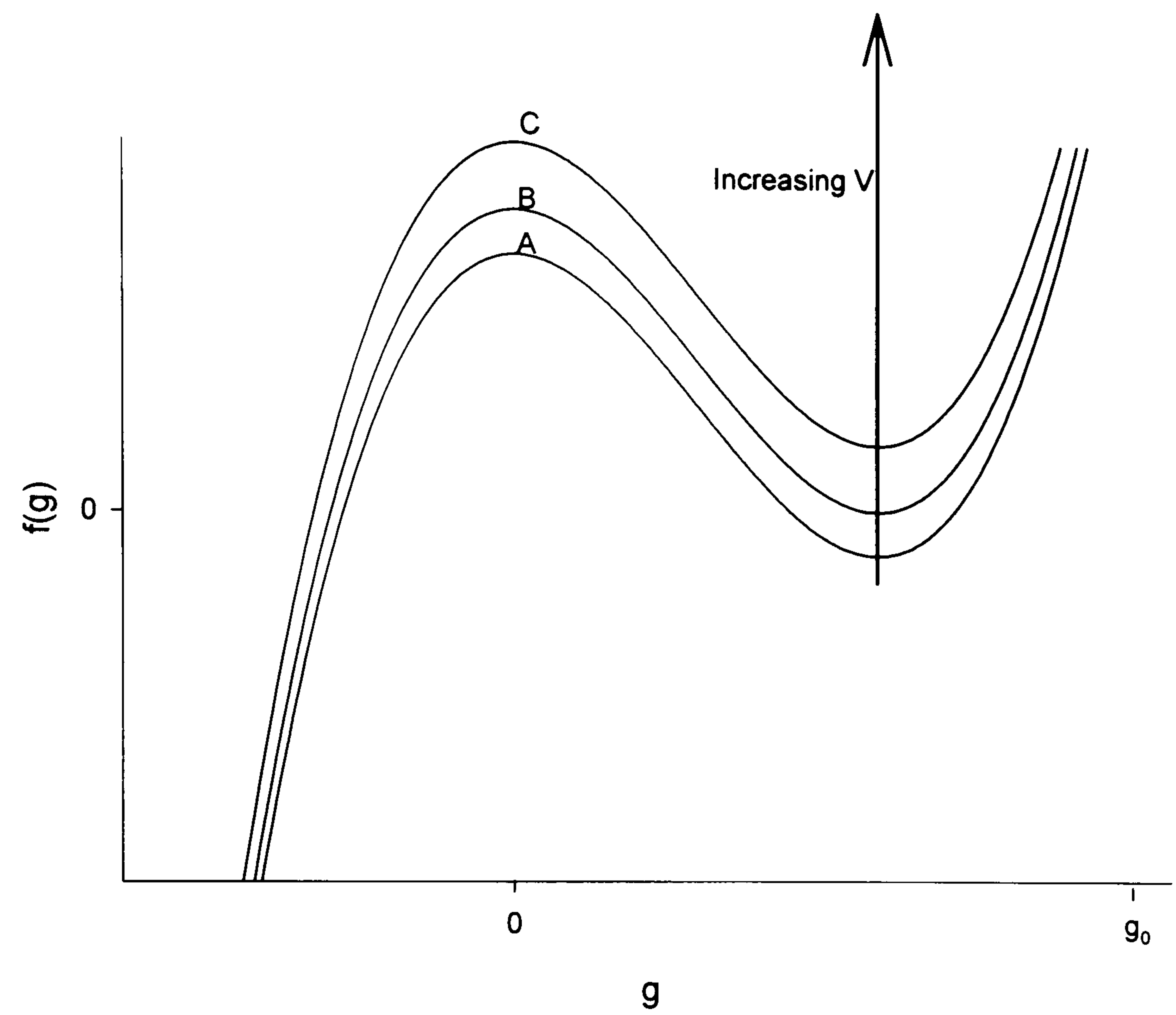


Fig. 3.2 An arbitrary plot of eqn. (3.3). Stable solutions occur when *f(g)=0* where *g* is positive.

Therefore the largest stable tuning voltage which can be accommodated is found in curve B where the turning point is in contact with f(g)=0. Only one valid solution for *g* now exists. This turning point can be found by differentiating eqn (3.3). The result is shown in eqn. (3.4).

$$\frac{df(g)}{dg} = g(3g - 2g_0) = 0 \quad \textbf{- (3.4)}$$

The valid solution for the turning point of interest in eqn. (3.4) is $g = (2/3)\, g_0$. Therefore the tuned gap cannot be less than two thirds of the unbiased gap. If the tuned gap is less than this then the restoring spring force cannot counter the electrostatic force of attraction.

In this situation the upper electrode snaps down to contact the lower electrode. This is known as pull-in and is effectively limiting the tuning range of this parallel plate arrangement to 50%, which corresponds to a ratio of 1.5:1.

In real microelectromechanical devices, the upper electrode of the capacitor may have curvature, which would reduce the validity of the parallel plate approximation [88]. This, in turn, affects the validity of the pull-in calculations. Finite element analysis software, such as Coventorware, enables these curved electrode situations to be more accurately modelled.

3.2 Electromechanical simulation using Coventorware

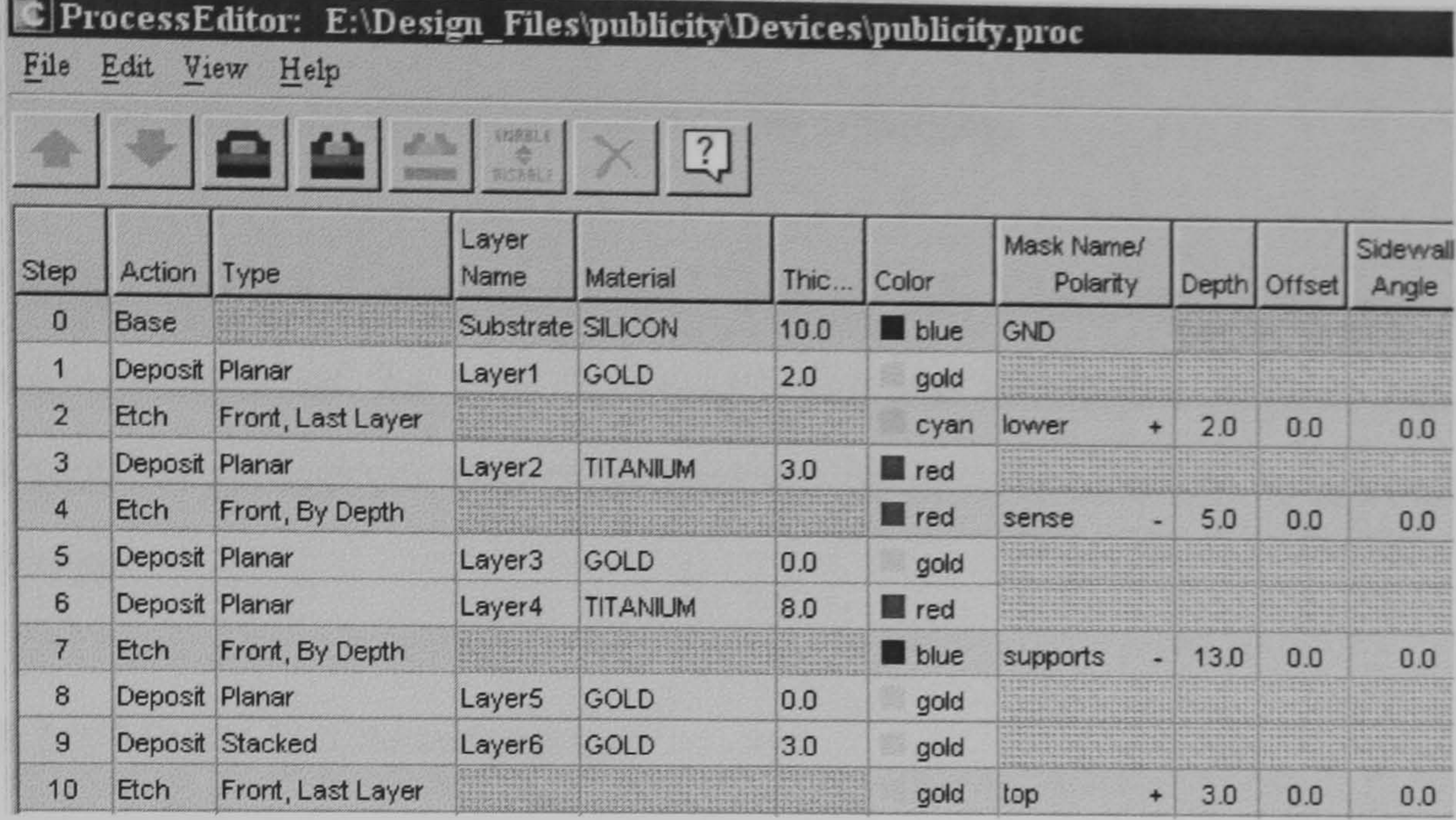
Coventorware is suitable for the simulation of curved electrodes as well as predicting the onset of pull-in. It uses a finite element approach, which can prove particularly processor intensive. However, it has the distinct advantage that it has been tailored for the simulation of microsystems. Recent software enhancements have significantly improved the robustness and efficiency of both the solvers and interfaces. The most recent version used in this thesis is 2003.1.

The focus of the software is to replicate the process flow and masks used for actual fabrication. This, in principle, enables the masks designed during simulations to be exported directly for fabrication. However, the Durham mask fabrication process uses photoreduction from a high-resolution printout onto a glass emulsion plate. Coventorware cannot export native CorelDraw files and is therefore not used for in-house mask production.

Coventorware requires four distinct stages to model a MEMS device. These are the development of a process flow, design of masks, device meshing and finally simulation using particular boundary conditions and solvers.

3.2.1 Process flows in Coventorware

Fig. 3.3 shows a sample process flow from Coventorware. It is fundamentally similar to the types of processes encountered in a fabrication environment. Layers are deposited and etched to particular mask patterns which are named in the process flow.



ProcessEditor: E:\Design_Files\publicity\Devices\publicity.proc

File Edit View Help

Step	Action	Type	Layer Name	Material	Thic...	Color	Mask Name/ Polarity		Depth	Offset	Sidewall Angle
0	Base		Substrate	SILICON	10.0	blue	GND				
1	Deposit	Planar	Layer1	GOLD	2.0	gold					
2	Etch	Front, Last Layer				cyan	lower	+	2.0	0.0	0.0
3	Deposit	Planar	Layer2	TITANIUM	3.0	red					
4	Etch	Front, By Depth				red	sense	-	5.0	0.0	0.0
5	Deposit	Planar	Layer3	GOLD	0.0	gold					
6	Deposit	Planar	Layer4	TITANIUM	8.0	red					
7	Etch	Front, By Depth				blue	supports	-	13.0	0.0	0.0
8	Deposit	Planar	Layer5	GOLD	0.0	gold					
9	Deposit	Stacked	Layer6	GOLD	3.0	gold					
10	Etch	Front, Last Layer				gold	top	+	3.0	0.0	0.0

Fig. 3.3 A typical process flow for a Coventorware simulation.

Sacrificial layers can be included to support the structure during simulated fabrication. Three types of deposition are available: planar, conformal or stacked. Fig. 3.4 illustrates these techniques, all of which are used in the devices simulated in this chapter.

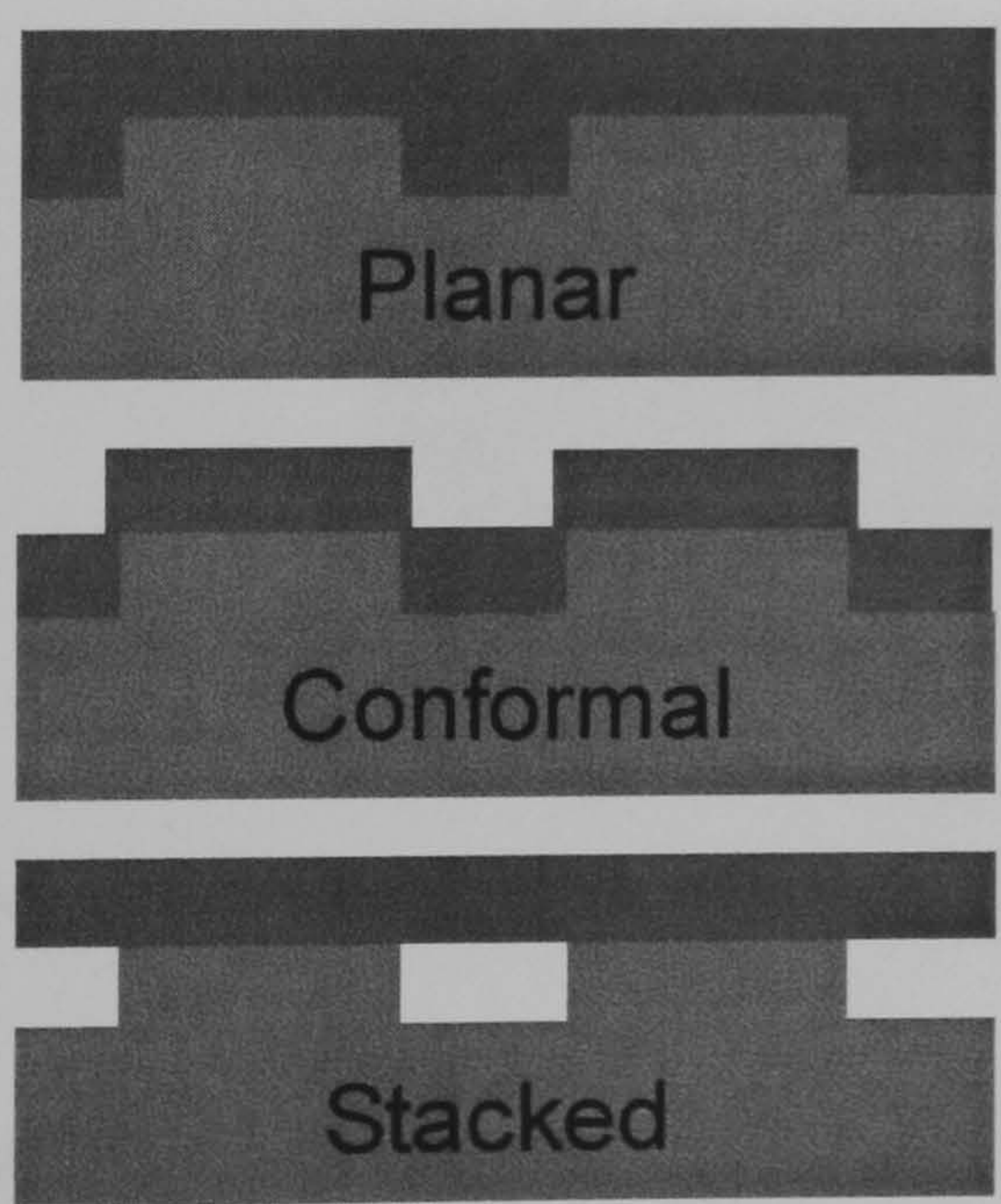


Fig. 3.4 The three deposition techniques available in Coventorware 2003.1.

The structural materials are identified in the process flow. Their mechanical properties are obtained from a central material properties database. The properties of the materials used in this chapter will be described in the relevant simulation section.

It is important to note that the Coventorware process flow only represents an approximation of a process flow found in a cleanroom environment. For example, the apparently simple planarising deposition option conceals more challenging fabrication processes such as chemical mechanical polishing.

Unlike CMOS design software, 'design rule checking' does not exist. It is the responsibility of the user to ensure that the simulated devices can be fabricated. Therefore an appreciation of fabrication limitations needs to be gained prior to device design.

3.2.2 Masks in Coventorware

Mask designs are based on the names created in the process flow. Fig. 3.5 shows a sample mask for an upper electrode including etch holes. These masks represent each patterned layer and, in conjunction with the process flow, enable Coventorware to produce a three dimensional model.

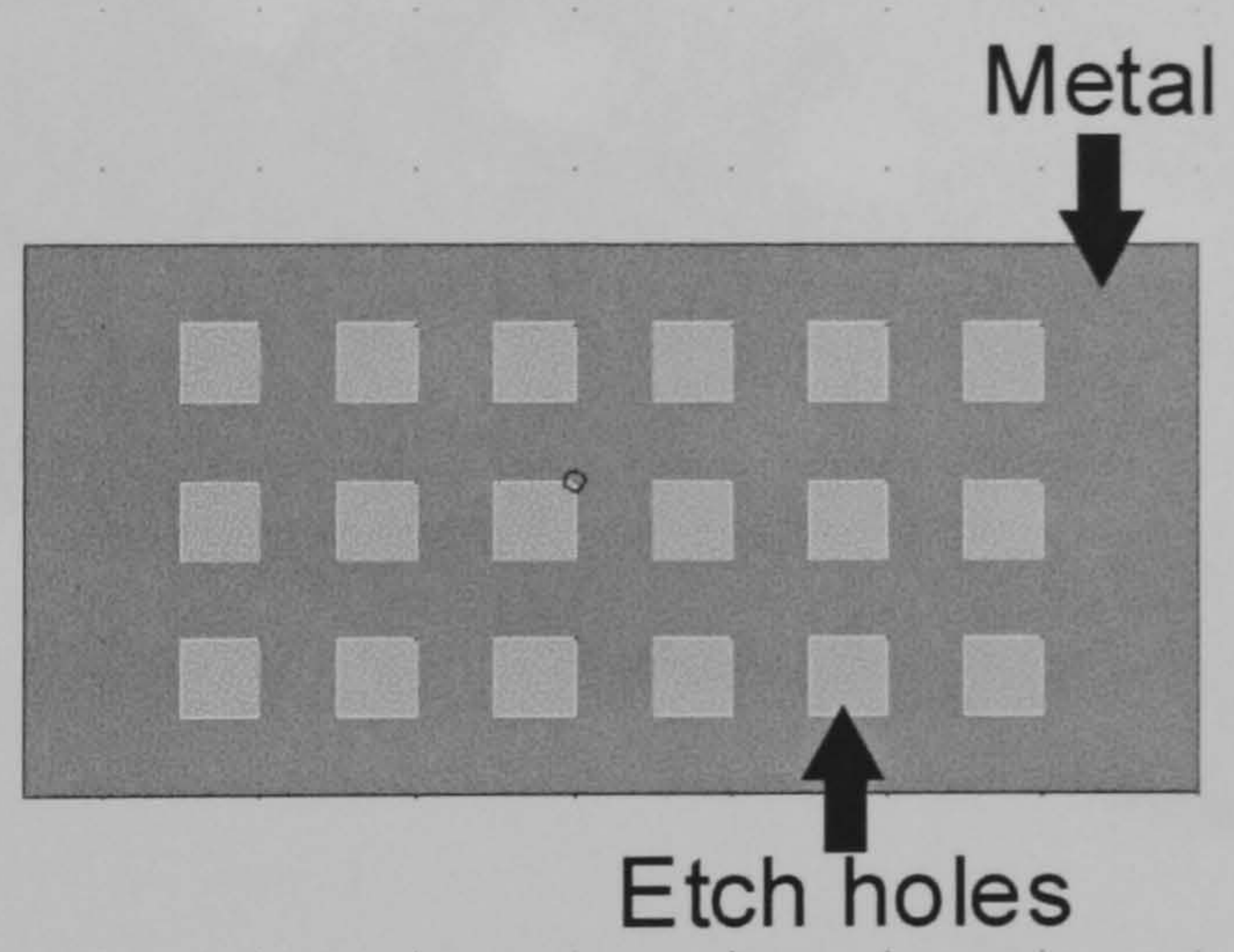


Fig. 3.5 A sample Coventorware mask design.

3.2.3 Meshing for finite and boundary element analysis

The three dimensional models produced using Coventorware need a mesh applied as shown in fig. 3.6. Coventorware uses finite element analysis for mechanical simulations and boundary element analysis (BEA) for electrostatic modelling. For FEA, the mesh needs to be applied over the entire volume of the model (i.e. not solely on the surface). This is important for mechanical analysis where the entire object volume contributes to the mechanical properties. For the BEA element in the electrostatic regime, only the exposed surface mesh is used. Unlike mechanical analysis, only the surface charge is a required consideration for electrostatic analysis [89].

The mesh size is a compromise between solution accuracy and computation time. For structures with complicated features a variable mesh size can be applied to better represent the features. Although a choice of mesh types is available, Manhattan bricks are used in this chapter because they are compatible with the electromechanical solvers and conform well to the topology found in the micromachined tunable capacitors.

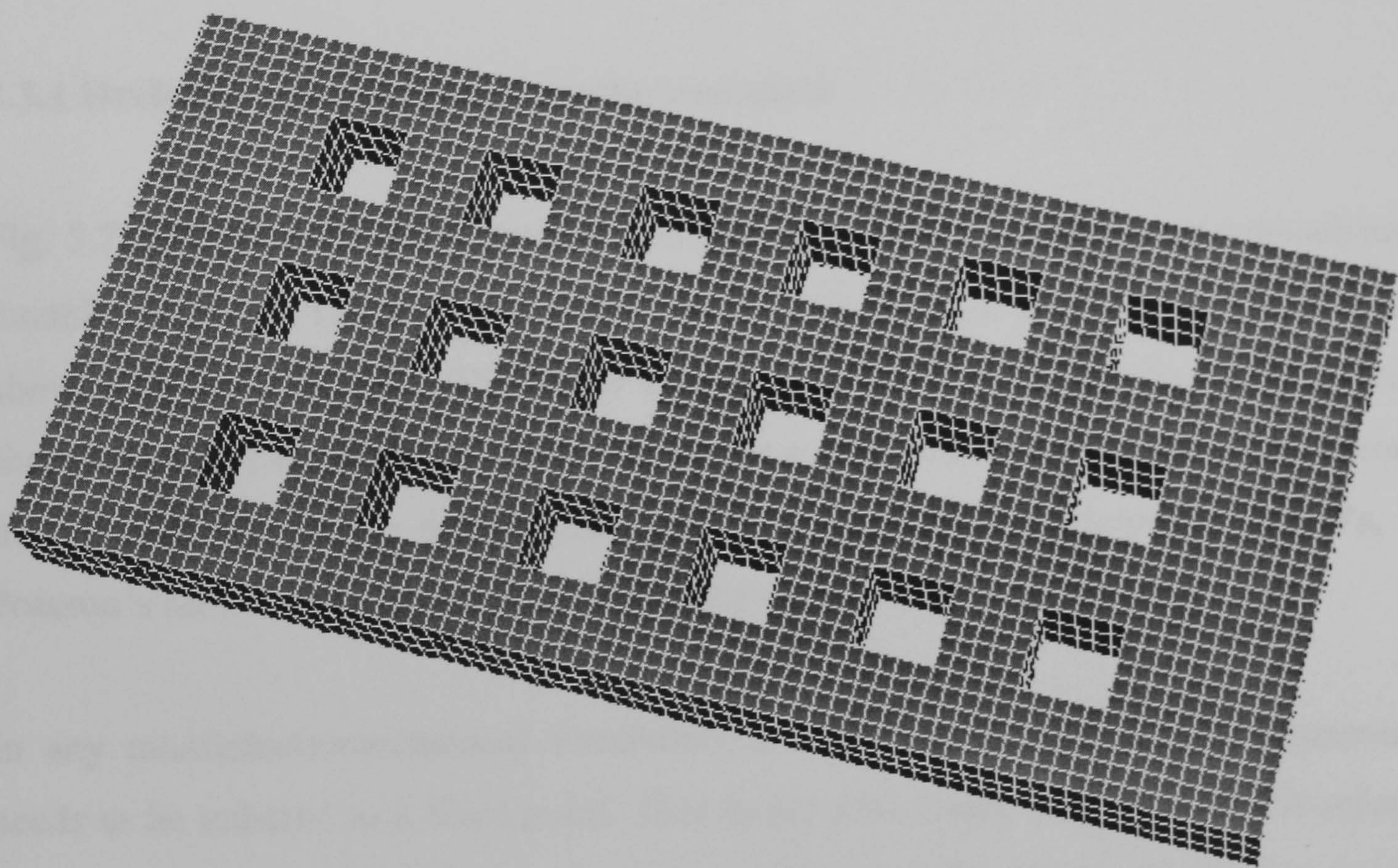


Fig. 3.6 A meshed 3D model produced in Coventorware.

3.2.4 Simulation

Using the meshed volumes created in the previous section, the structures can be solved for various boundary conditions. Boundary conditions can be mechanical such as spacially fixing particular elements, or electrical when voltages are applied to conductors.

This chapter presents results from a solver in Coventorware known as CoSolveEM. It is used to simulate electrostatically actuated devices. The solver provides displacement and capacitance data for a device subject to a particular biasing voltage.

For electrostatic actuation, Coventorware has to iterate between electrostatic and mechanical sub solvers until the electrostatic force of attraction and the mechanical restoring force are balanced for a particular displacement. The pull-in voltage is calculated when the electrostatic and mechanical forces cannot be balanced.

3.3 Simulated devices

3.3.1 Device 1: The single-gap tunable capacitor

Fig. 3.7 shows the typical dimensions of a single-gap, two electrode micromachined tunable capacitor. The movable upper electrode (1μm thick gold) is suspended 1μm above a lower electrode. The lower electrode is fixed to a substrate, which is not shown. In order to retain the generality of the results, the substrate is excluded from the simulations. In the simulations, gold has a Young's modulus of 57 GPa, a Poisson's ratio of 0.35, a density of 19300 kg m^{-3} and zero residual stress.

In any microelectromechanical simulation, at least part of the simulated structure needs to be tethered to a fixed point. This forms a boundary condition for the solver. Coventorware enables particular elements or groups of elements to be fixed in space. The upper electrode in this example has its four edges clamped as indicated in fig. 3.7.

If a voltage is applied across the two electrodes, the upper electrode will be electrostatically attracted to the lower electrode. Unlike the simple parallel plate example presented in section 3.1, the upper electrode cannot move parallel to the lower electrode. The edge clamping prohibits this and the upper electrode has to deform in response to the electrostatic force.

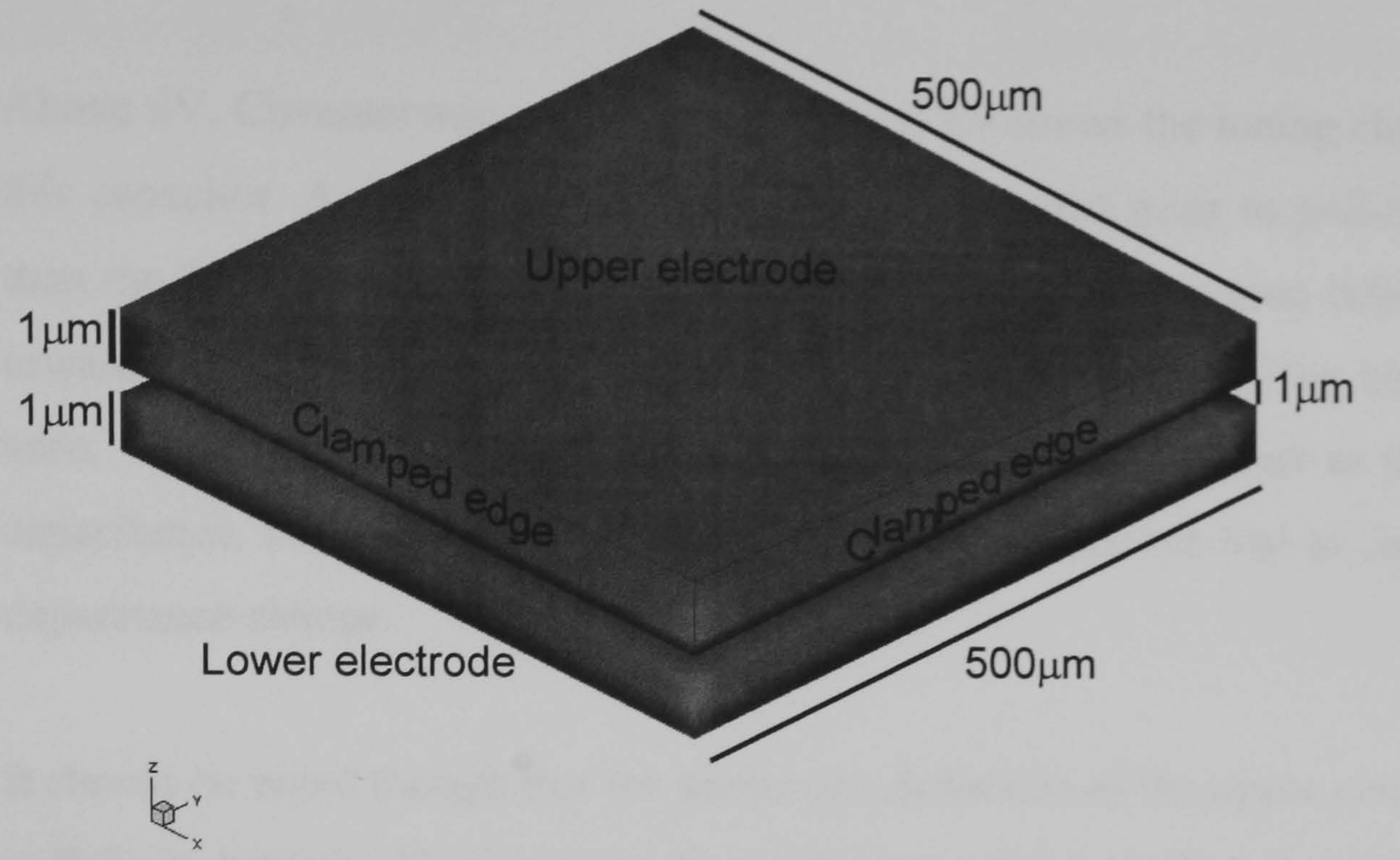


Fig. 3.7 A single-gap, two electrode tunable capacitor.

Fig. 3.8 shows the displacement of the upper electrode subjected to a range of biasing voltages. The electrode can be seen to be deforming most at the centre, the point furthest from the clamping points. The edge clamping provides the restoring force for the upper electrode.

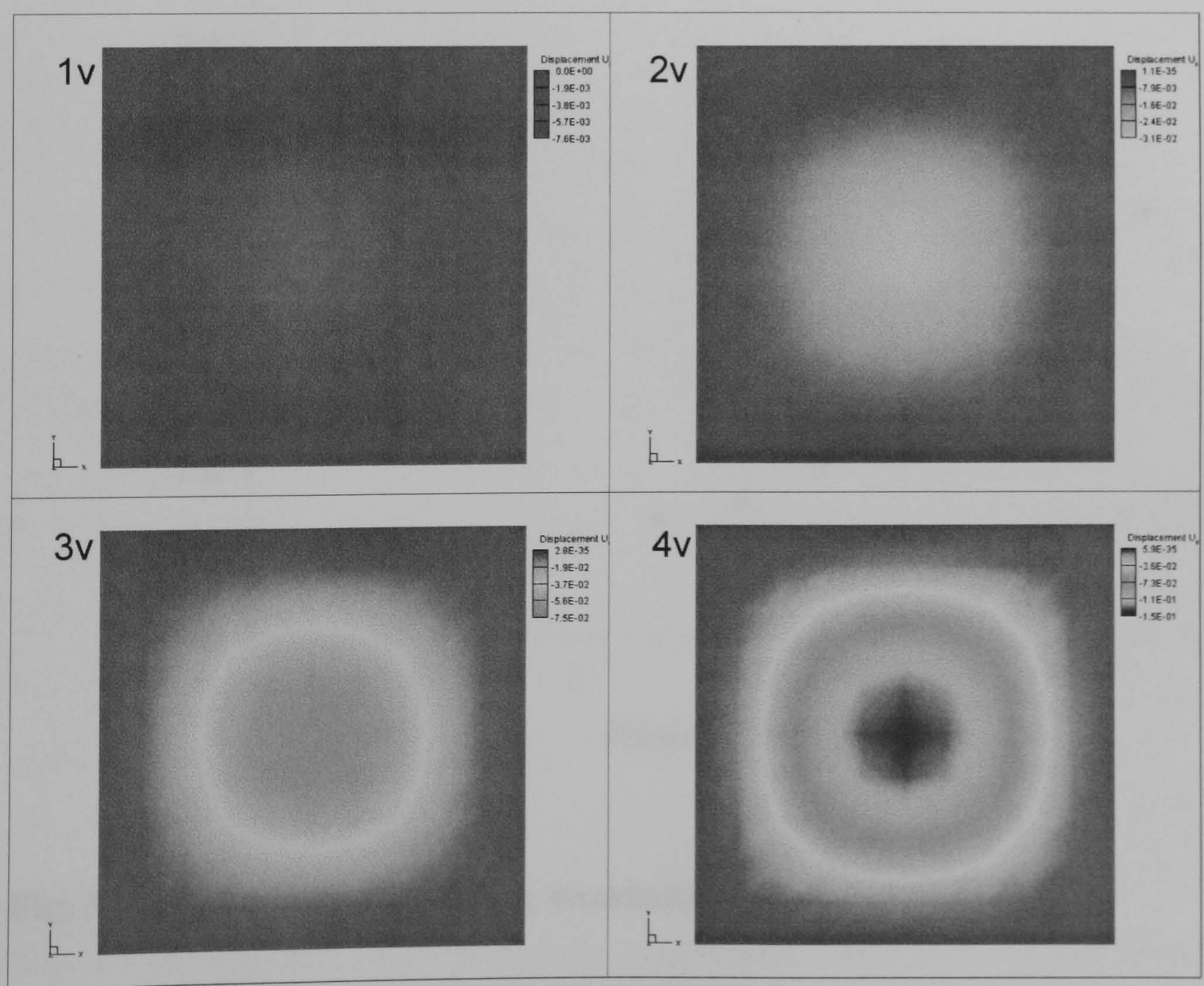


Fig 3.8. Displacement of the upper electrode in device 1 subject to a range of biasing voltages. Displacement units are μm.

Above 6V, Coventorware predicts pull-in. Fig. 3.9 shows the tuning characteristic for this capacitor. A tuning ratio of only 1.15:1 is reported prior to pull-in. This is less than the 1.5:1 predicted for the parallel plate situation. The reason behind this is that towards the edges of the upper electrode, the displacement during biasing tends to zero. The edges of the upper electrode are contributing the least to the increase in capacitance. In the pure parallel plate situation, the edges are free to contribute to the capacitance change.

It should be noted though that the maximum deflection of the upper electrode, prior to pull-in, is 0.43μm. This exceeds the predictions of the parallel plate situation, which would allow 0.33μm deflection prior to pull-in. However this is a local maximum and at the clamped edges the displacement is 0μm.

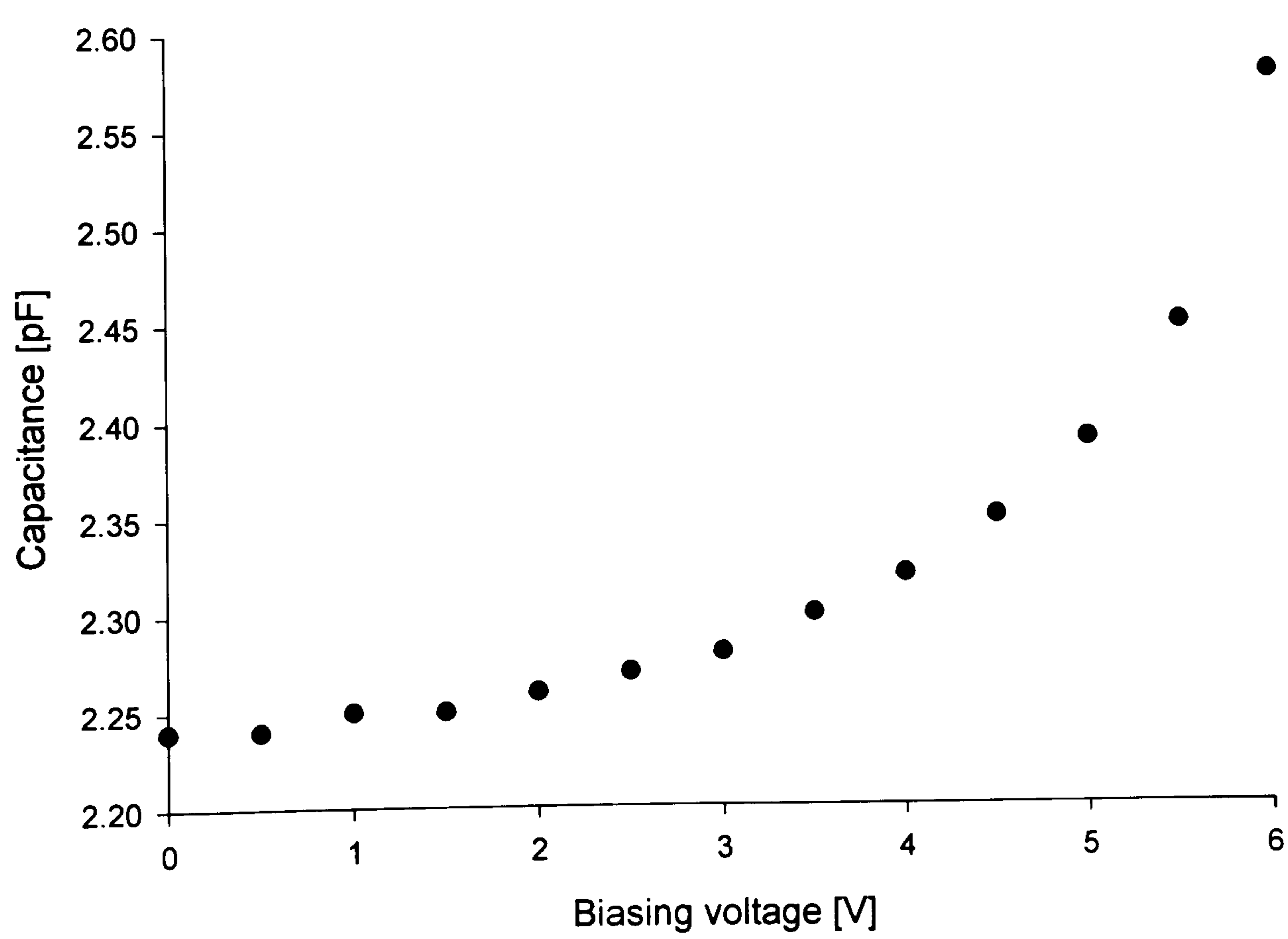


Fig. 3.9 The capacitance tuning characteristic of device 1.

3.3.2 Device 2: Enlarged upper electrode single-gap tunable capacitor

One method of lowering the tuning voltage of this capacitor is to decrease the restoring force of the clamped edges. This can be achieved by enlarging the upper electrode. The dimensions of the lower electrode remain fixed, as does the unbiased electrode spacing compared to device 1. Fig. 3.10 shows the dimensions of the modified device.

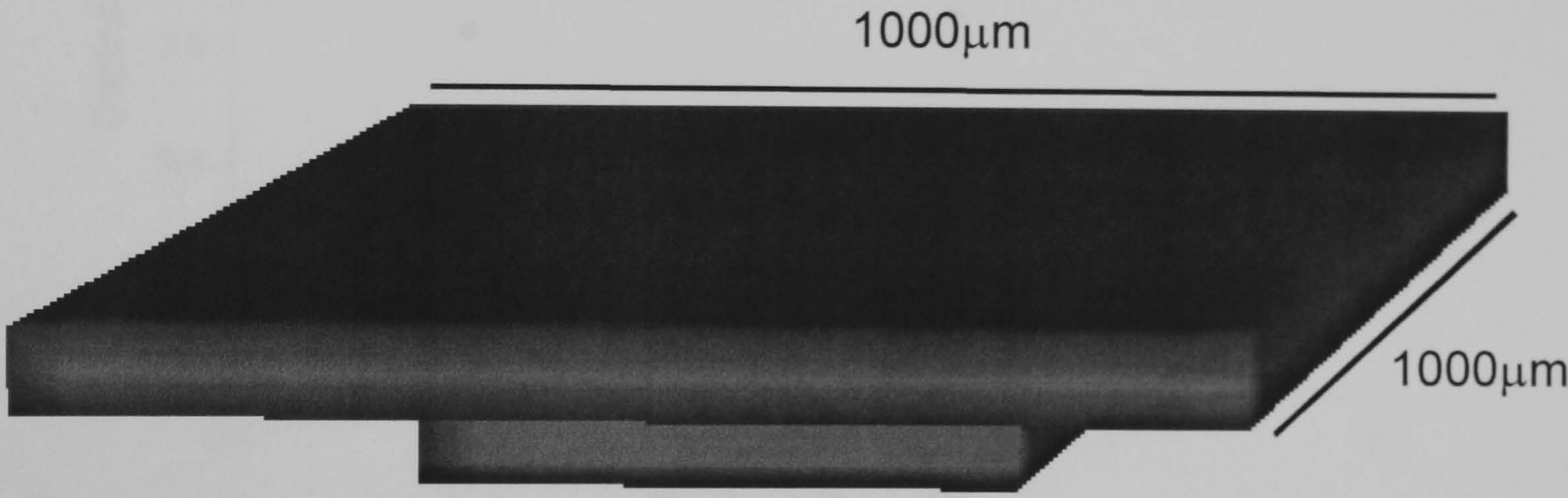


Fig. 3.10 The upper electrode dimensions of device 2. The lower electrode is centrally located.

In this device, when a DC voltage is applied across the electrodes, the electrostatic force is acting further away from the clamped edges than in device 1. The area of the lower electrode is the same as before and hence the electrostatic force is unchanged. However, the effective restoring force is reduced due to leverage. Hence, the electrostatic force and therefore voltage required for an equivalent deflection is less.

Fig. 3.11 shows the tuning characteristics of the modified device. The peak biasing voltage prior to pull-in is 1.5V. As predicted, this is less than the previous device. The maximum tuning ratio has increased to 1.25:1.

Fig. 3.12 shows displacement of the upper electrode at various biasing voltages. Prior to pull-in the maximum displacement is only 0.29μm. This is less than in the previous device. However, the tuning ratio has increased through improved planarity of the upper electrode. The upper electrode is no longer clamped directly above the edge of the lower electrode. Consequently, the edges of the lower electrode can contribute more to the capacitance change than in the previous device.

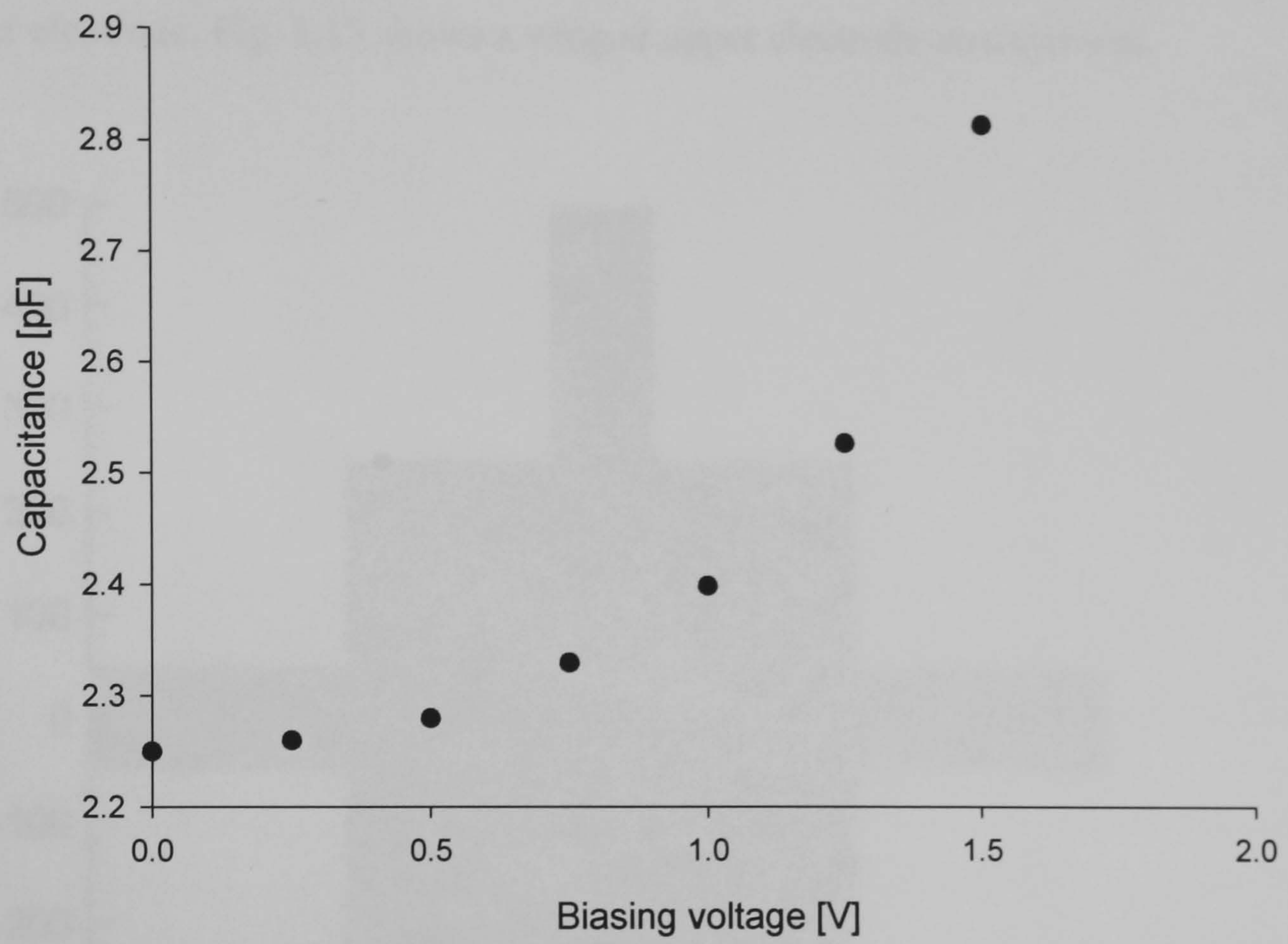


Fig. 3.11 The capacitance tuning characteristics of device 2.

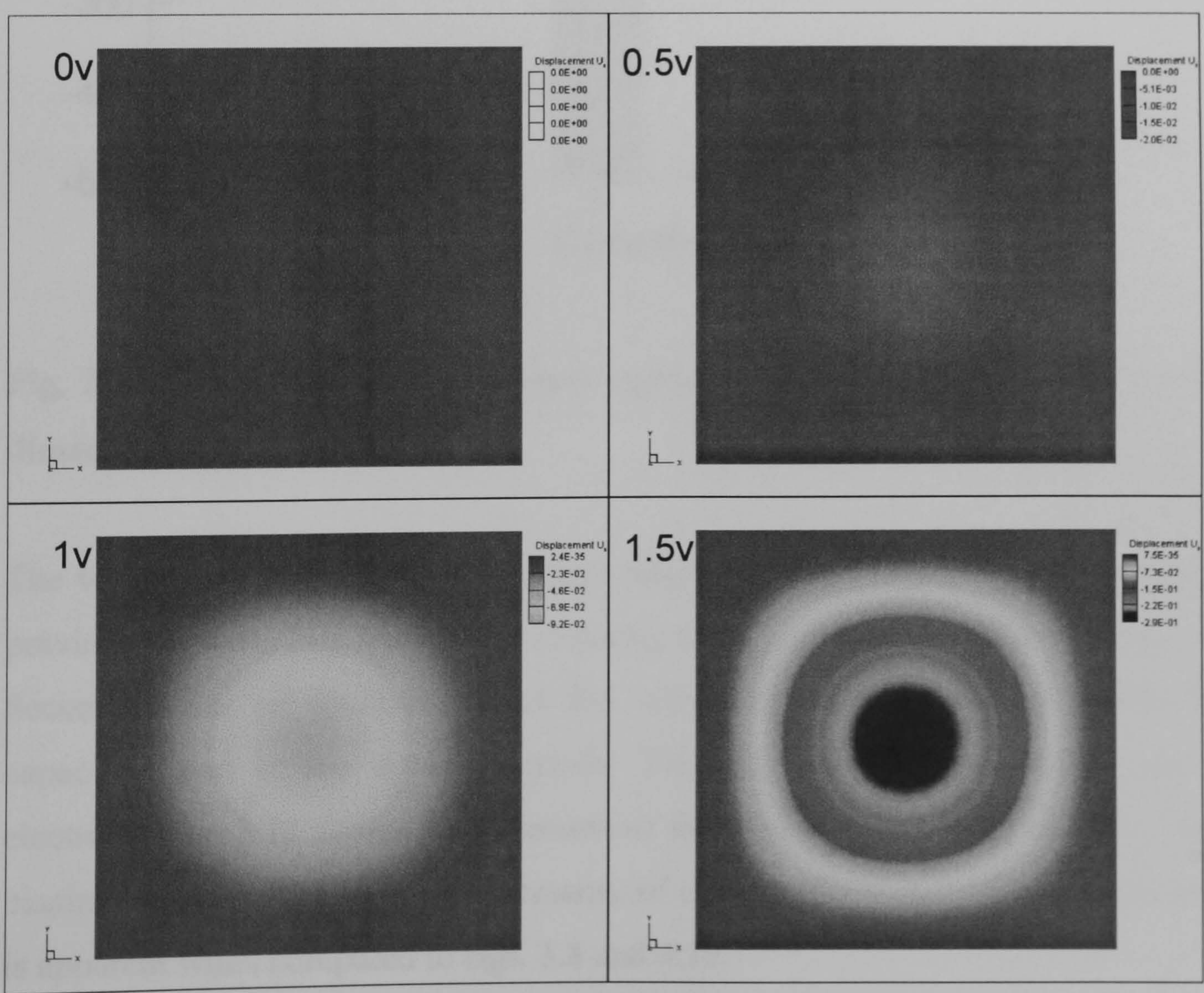


Fig. 3.12 The deformation of the upper electrode in device 2 subject to a range of biasing voltages. Displacement units are μm.

3.3.3 Device 3: Winged upper electrode single-gap tunable capacitor

A further reduction in the biasing voltage can be achieved by altering the shape of the upper electrode. Fig. 3.13 shows a winged upper electrode arrangement.

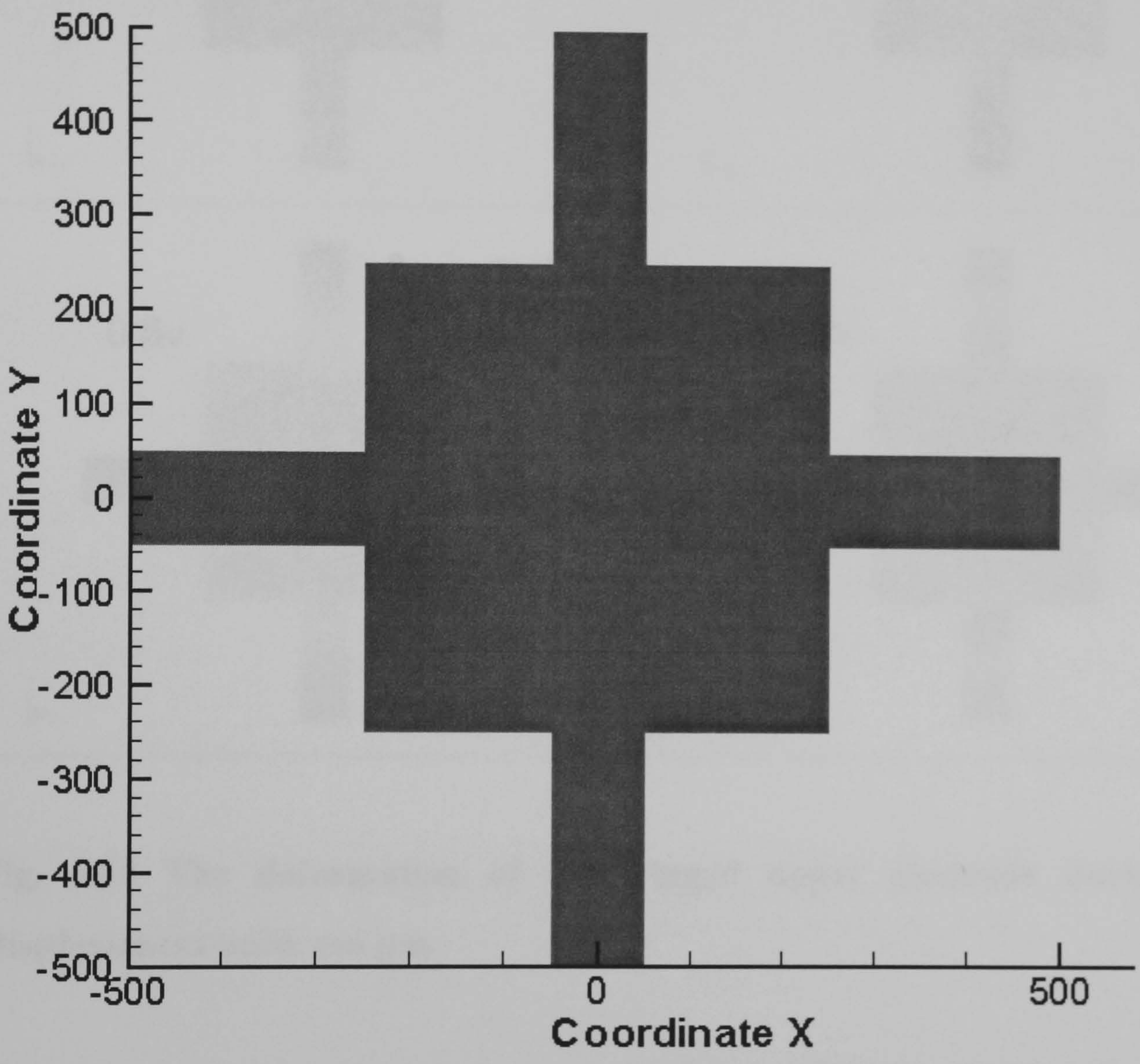


Fig. 3.13 A top view of the winged capacitor upper electrode. The coordinate dimensions are in μm.

The wings have two effects. First, they reduce the clamping area when compared to previous devices. This reduces the restoring force and enables a lower tuning voltage. Second, under an attractive force the wings can deflect without deforming the capacitive part of the upper electrode. This improves the planarity of the upper electrode. Fig. 3.14 shows displacement of the winged upper electrode for a range of biasing voltages. The improved planarity of the capacitive part of the upper electrode is apparent when compared to figs. 3.8 and 3.12.

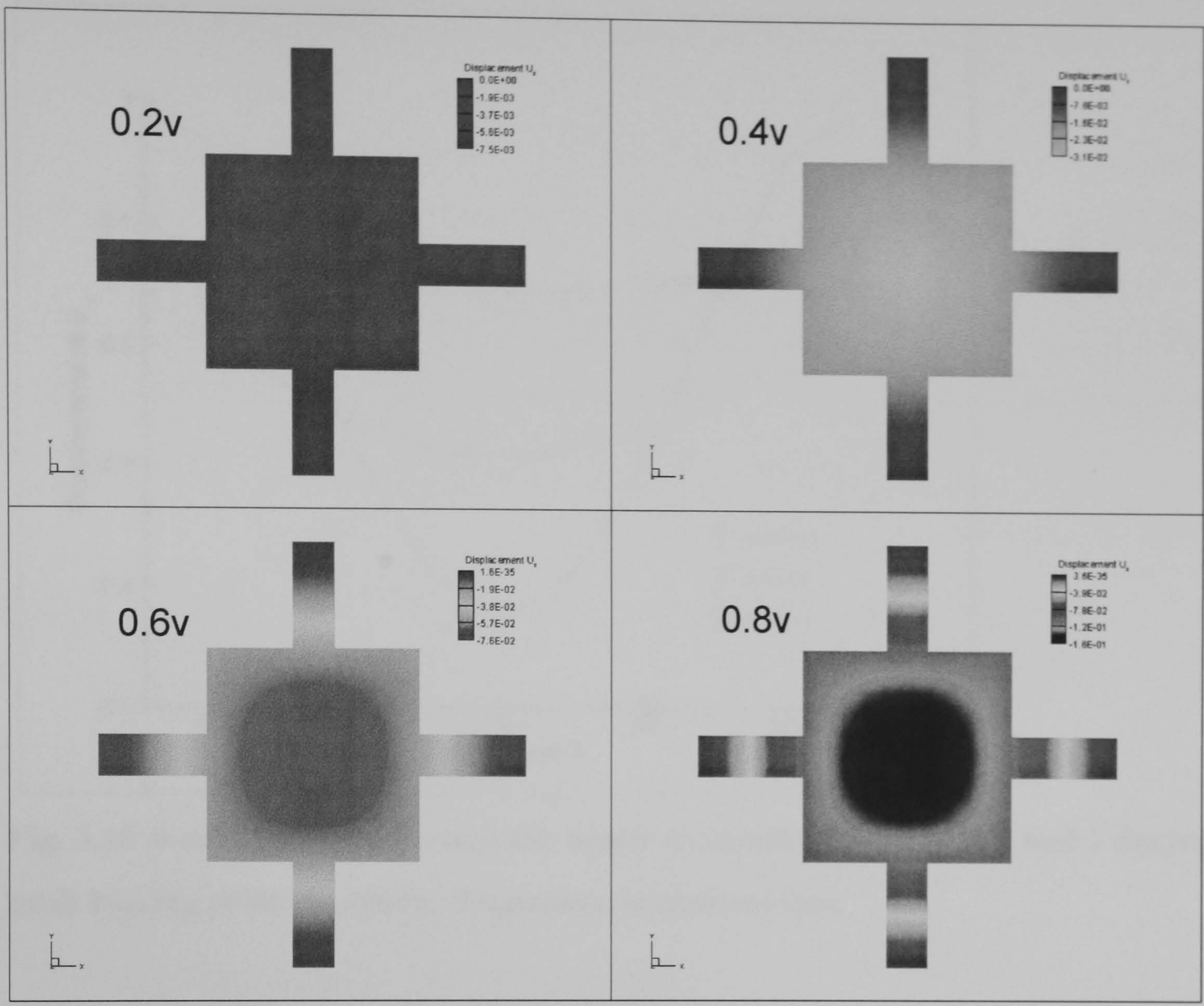


Fig. 3.14 The deformation of the winged upper electrode during biasing. Displacement units are μm.

The planarity comparisons have to be made at different control voltages because devices 1, 2 and 3 exhibit different biasing characteristics. Fig. 3.15 shows a profile of the upper electrode in each of the three devices presented in this section. In order to provide a valid comparison, each profile is taken through the centre of the upper electrode in the capacitive region at peak displacement prior to pull-in. The improved planarity in the winged design can be clearly seen.

For device 3, Pull-in is predicted to occur at 1V. This is lower than the voltage required for device 2. Fig. 3.16 shows the capacitance tuning characteristics of the winged device.

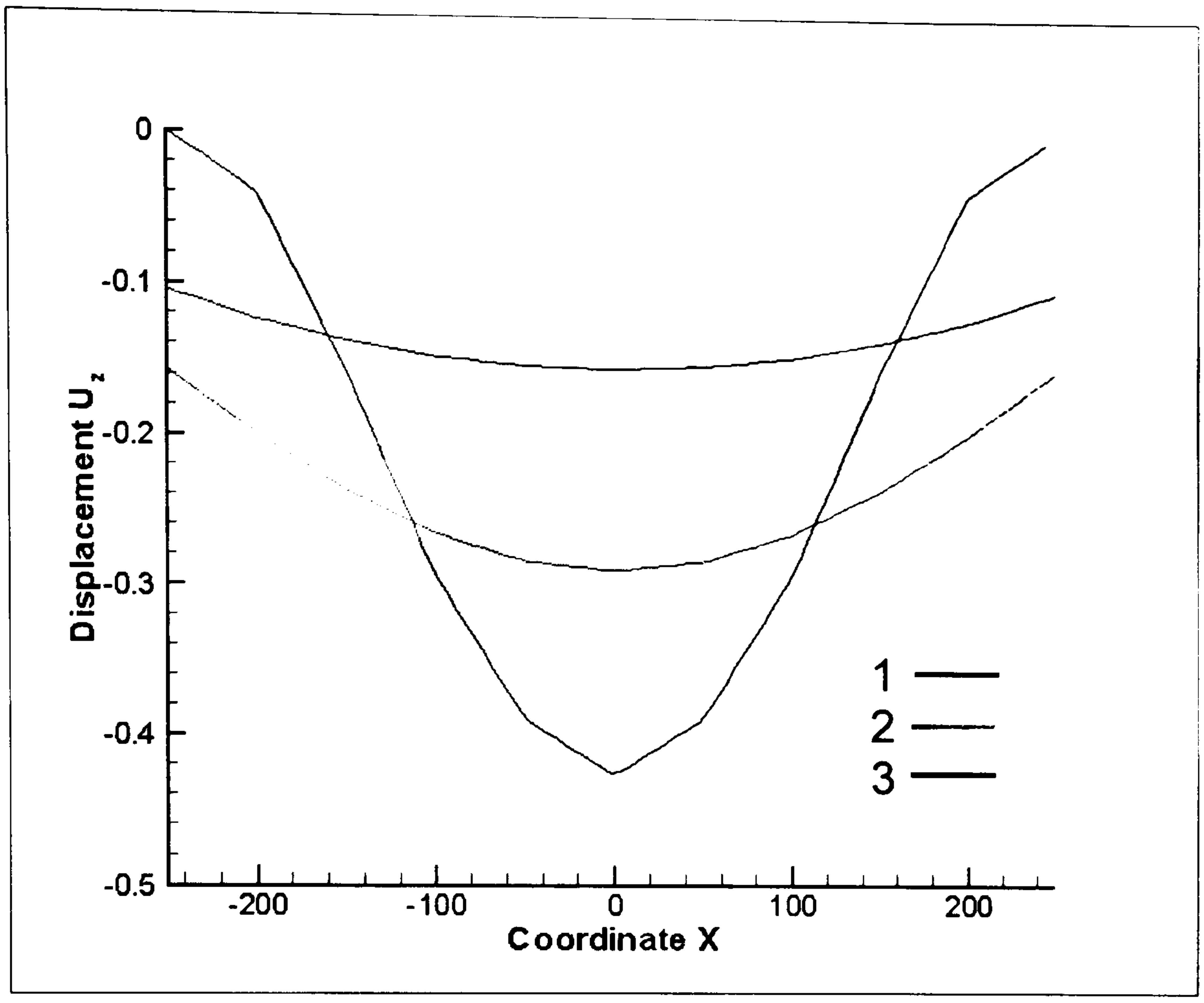


Fig. 3.15 A cross section through the upper electrode of devices 1, 2 and 3 during peak biasing prior to pull-in. Displacement units are μm

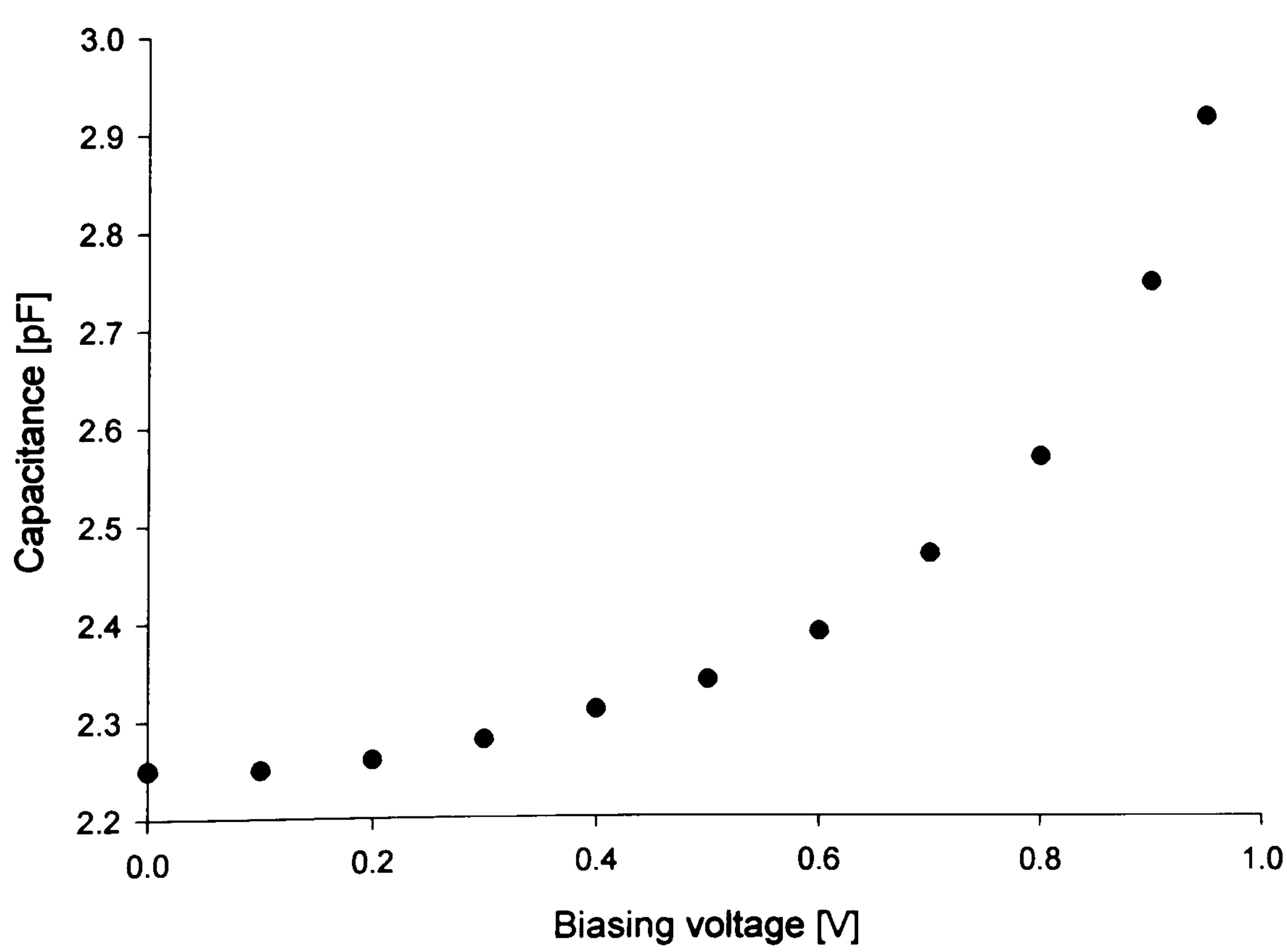


Fig. 3.16 The capacitance tuning characteristic of device 3.

The maximum tuning ratio prior to pull-in for this device is 1.29:1. This improved planarity is a better approximation to the parallel plate situation and hence the tuning ratio is nearer the theoretical maximum of 1.5:1 than in previous devices.

3.3.4 Device 4: Doubly clamped upper electrode

The previous designs have used four clamped edges for the upper electrode. Device 4 is identical to device 1 with dimensions of 500μm in both the x and y directions. However, it is clamped at only two edges as indicated in fig. 3.17. This figure shows the displacement of the upper electrode whilst subject to various biasing voltages. The deformation is now comparable to a beam rather than a membrane. When compared to device 1, the maximum voltage prior to pull-in is lower at 3.75V.

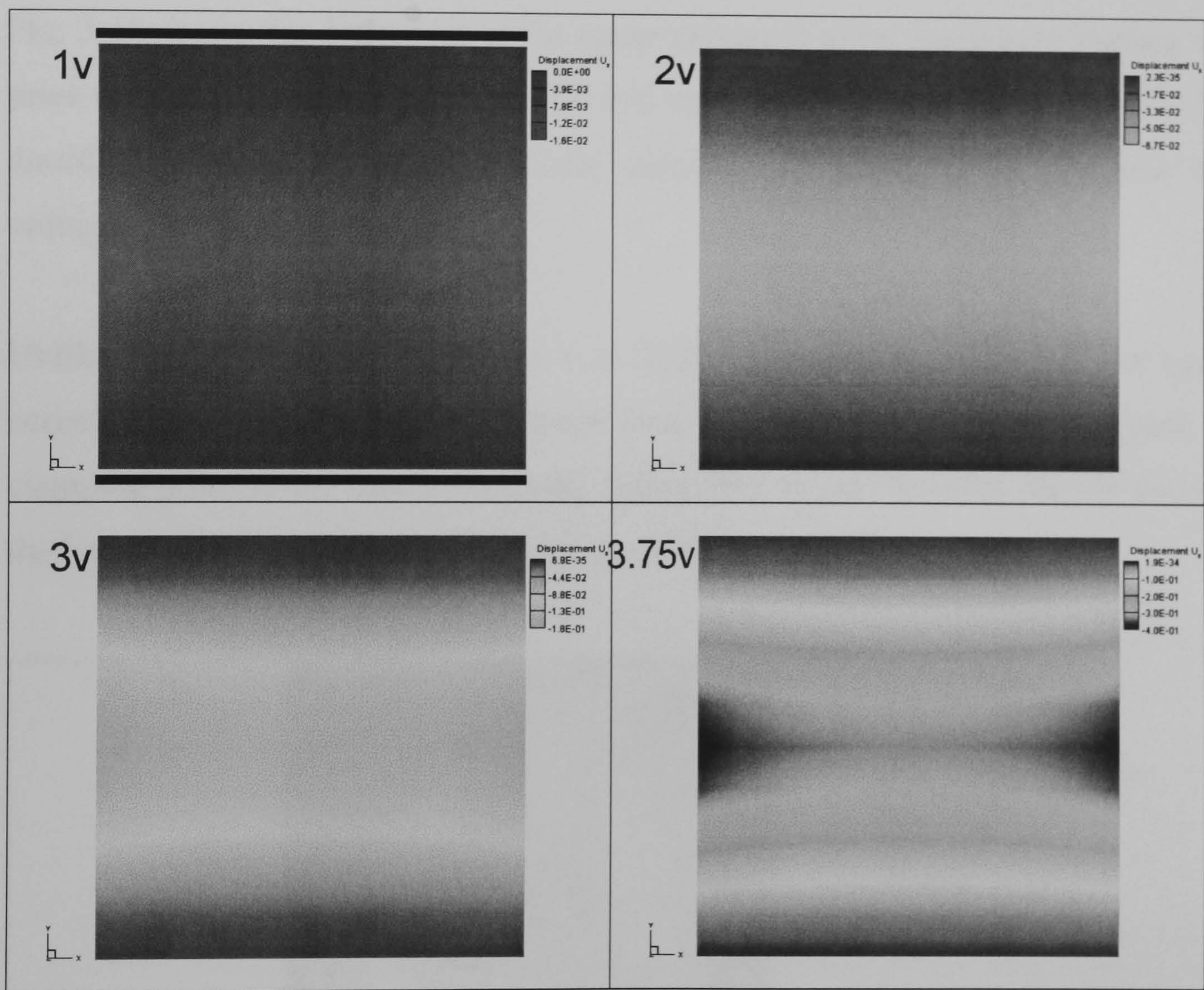


Fig. 3.17 The deformation of device 4, subject to a range of biasing voltages. Displacement units are μm. Clamped edges indicated by the black rectangles in the top left image.

The advantage of using a beam is primarily from a fabrication perspective. The removal of the two clamped edges enables interconnect to reach the lower electrode without affecting the support structure.

In order to supply interconnect to the lower electrode in device 1 the metallisation would need to pass under the support structure. This requires an insulating support that in turn would introduce dielectric losses into the capacitor therefore increasing its high frequency losses and lowering the electrical quality factor.

3.3.5 Device 5: Wide doubly clamped upper electrode

In this device the width in the y direction (distance between unclamped edges) is 1000μm. The length in the x direction (distance between clamped edges) is 500μm. The z-axis dimensions remain consistent with device 4.

Fig. 3.18 shows the deflection of the upper electrode at the maximum biasing voltage prior to pull-in. This voltage is 4.25V and corresponds to a tuning ratio of 1.21:1. A doubling of the beam width has only caused a 13% increase in the peak biasing voltage.

Unlike the transition from device 1 to 2, the increase in width has not caused a corresponding increase in the distance from the edge of the lower electrode to the clamping point in the upper electrode. Instead the larger clamping area at the ends of the beam has marginally increased the restoring force.

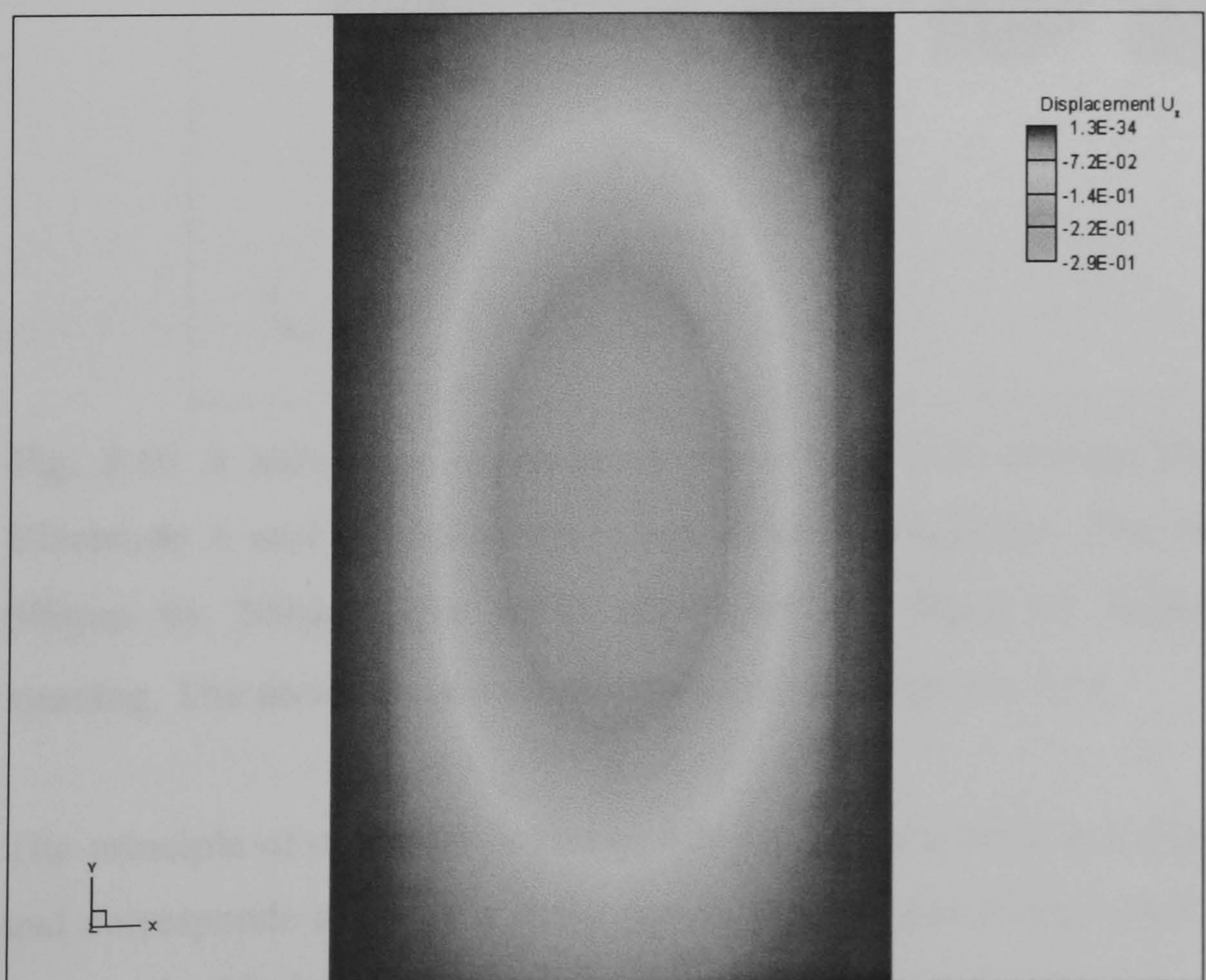


Fig. 3.18 The deformation of device 5 prior to pull-in. The long edges (1000μm) are clamped at each end. Displacement units are μm.

In devices 1 to 5, pull-in is significantly limiting the tuning ratio. Even the peak tuning ratio of 1.29:1 is less than predicted for the parallel plate approximation. The next device looks at a method of eliminating pull-in using leverage.

3.3.6 Device 6: Leverage based pull-in avoidance

Fig. 3.19 shows a view of device 6. It is a beam with only one end clamped, therefore forming a cantilever. There are five lower electrodes, labelled A to E. Electrode A and the cantilever form the capacitor electrodes whereas electrodes B to E are used for DC biasing.

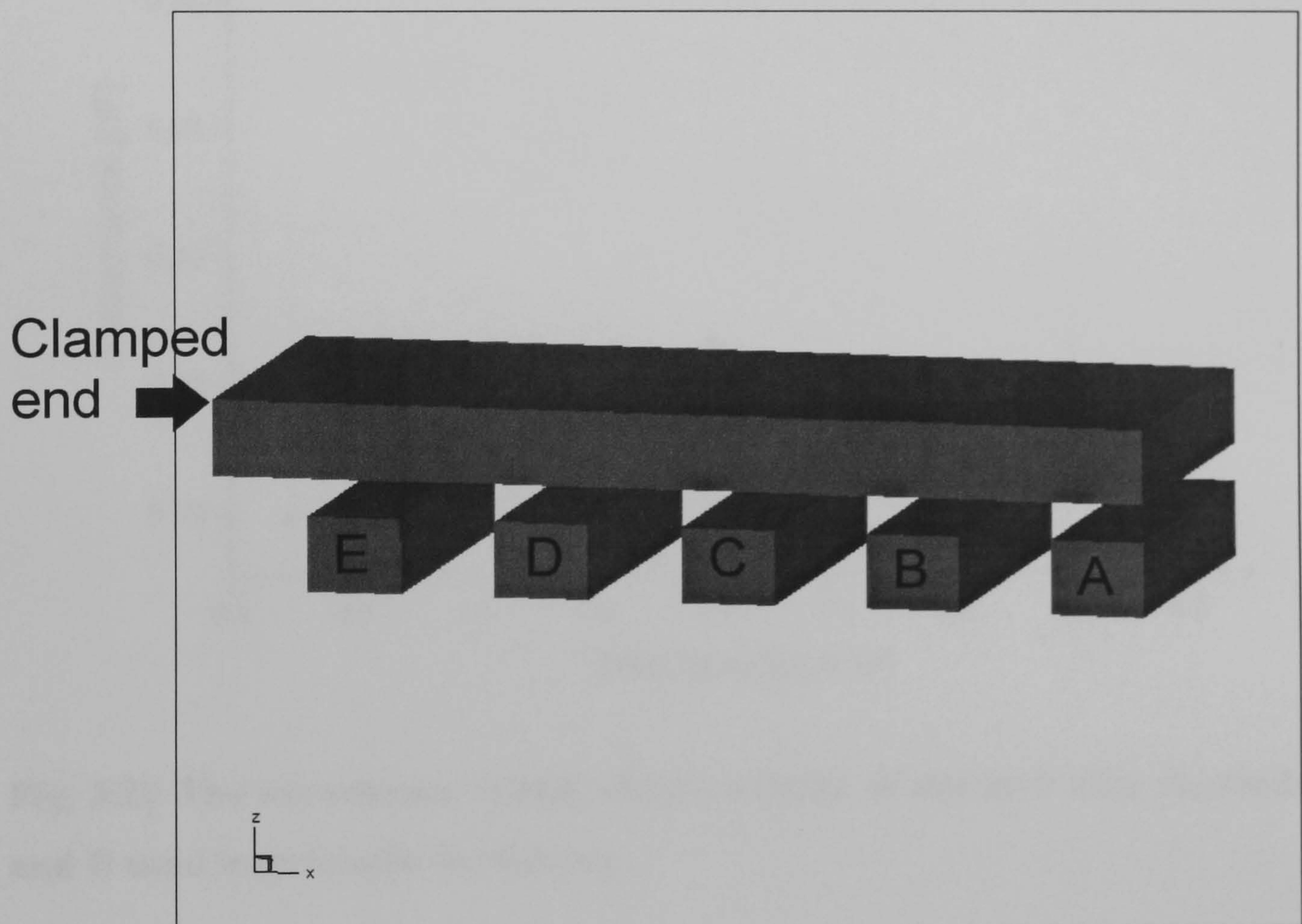


Fig. 3.19 A side view of device 6. Electrodes B-E are the biasing electrodes. Electrode A and the upper electrode form the capacitor. The upper electrode is 500μm by 200μm. The lower electrodes are 50μm by 200μm with a 50μm spacing. The metallisation thicknesses and air gaps are 1μm.

The principle of operation is that of a lever, where a deflection near to the clamping end corresponds to a larger deflection at the free end of the upper electrode. In this design, the biasing and capacitive electrodes have been separated. This enables the capacitive electrode to be positioned at the free end of the upper electrode. The biasing electrode can then be placed nearer to the clamped end. There will reach a point when the biasing electrode will be able to displace the upper electrode to contact the lower capacitive electrode whilst avoiding pull-in.

Fig. 3.20 shows the tuning characteristic of the device. When only electrode B is biased, the tuning ratio is 1.39:1 prior to pull-in. This shows an improvement over the previous devices.

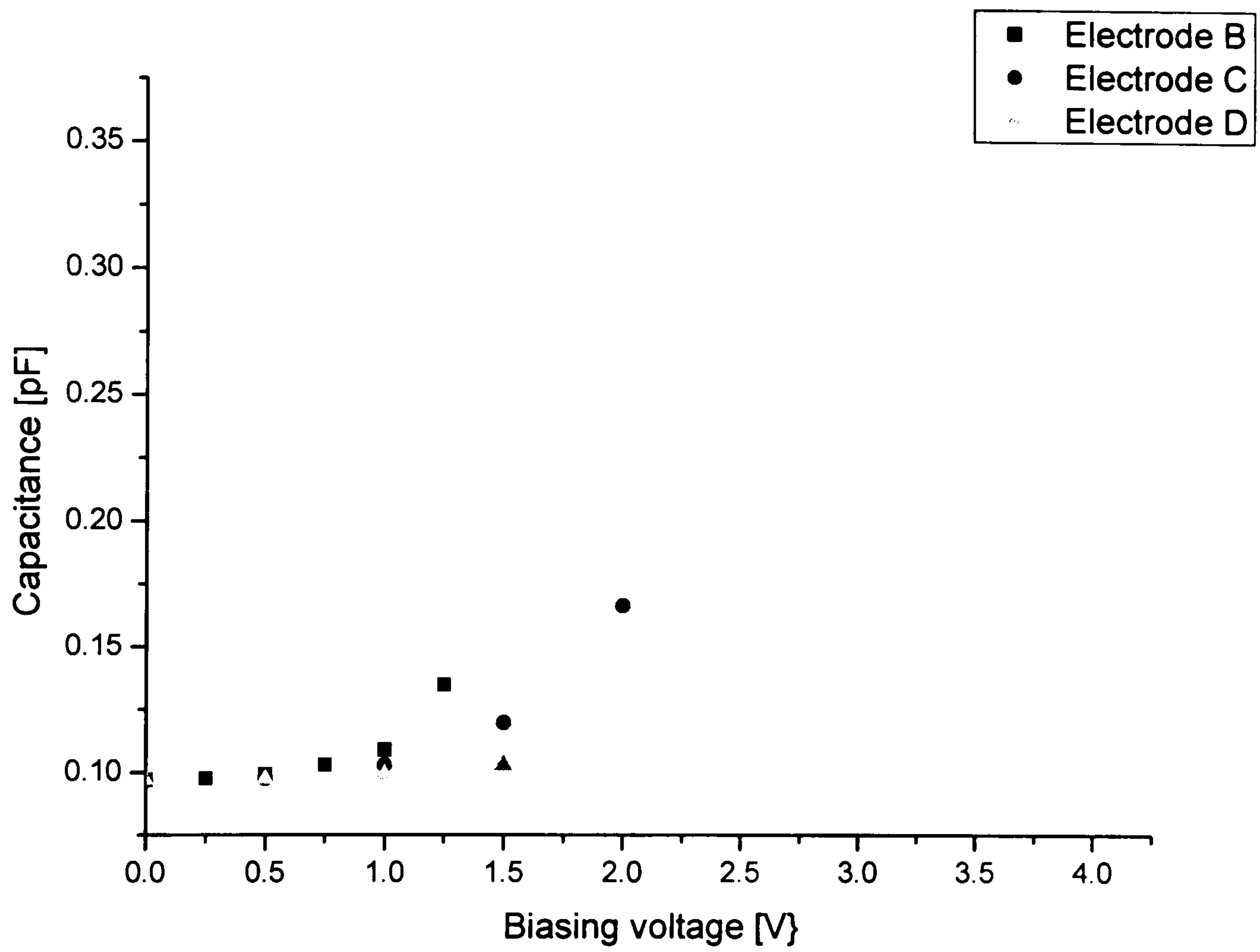


Fig. 3.20 The capacitance tuning characteristics of device 6 with electrode B, C and D used individually for biasing.

When only electrode C, which is nearer to the clamping point than B, is biased. In this case the maximum tuning ratio prior to pull-in is 1.72:1. This is a further improvement. However, the peak tuning voltage has increased from 1V to 2V.

Using only electrode D for biasing, pull-in occurs after the capacitive electrodes have made contact and has therefore been eradicated. This, in principle, enables any capacitive gap to be set which leads to an infinite tuning ratio.

Fig. 3.21 shows the displacement of the device subject a range of electrode D biasing voltages. The simulations have been performed using only a single electrode for actuation. However, applying a voltage to each electrode in turn could create discrete capacitances. This would form the basis of a digital variable capacitor.

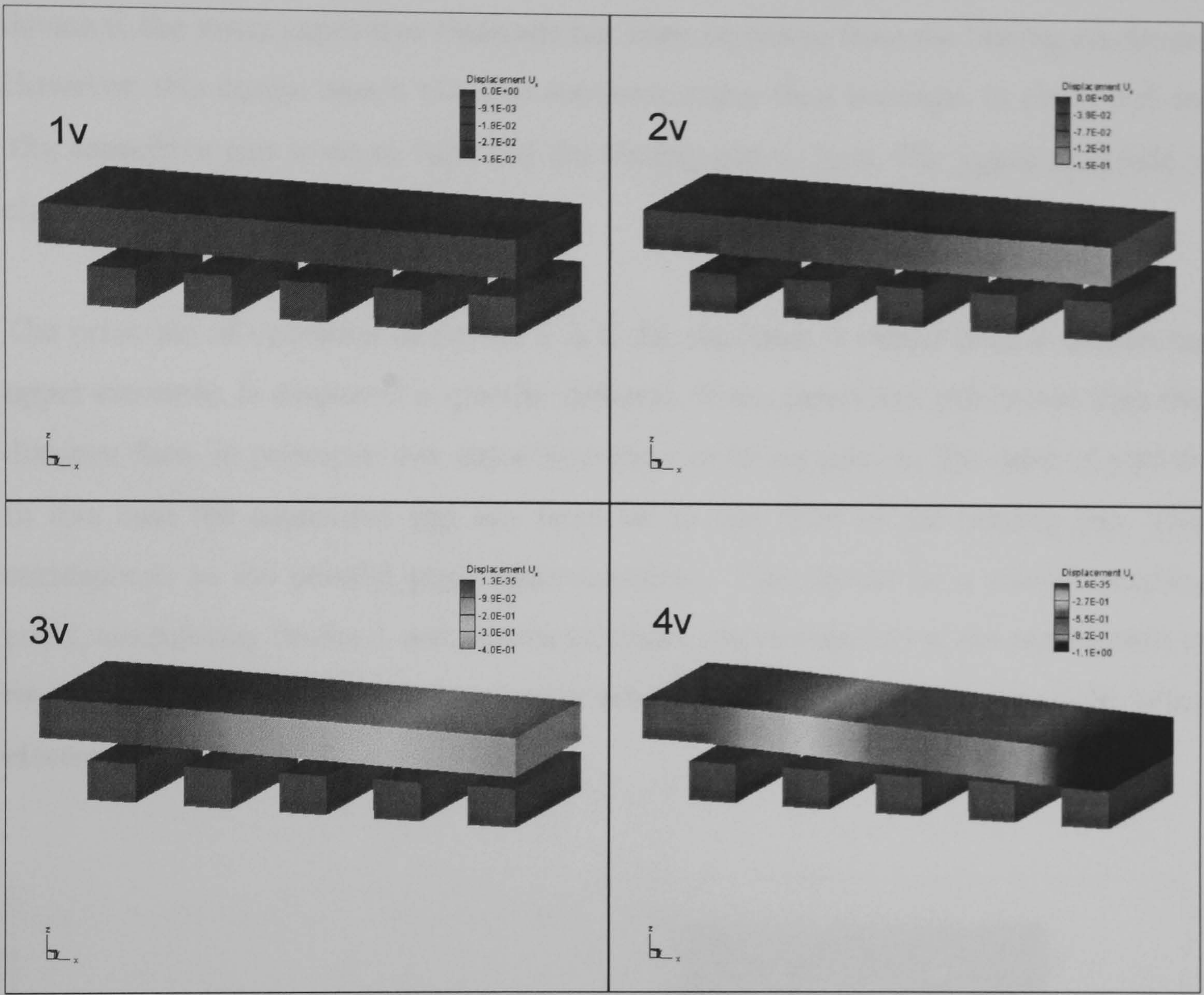


Fig. 3.21 The deformation of device 6 subject to a range of biasing voltages on electrode D. In the 4V case, the upper electrode has displaced through electrode A. Displacement units are μm.

The cost of using leverage bending is twofold. First, the force required to deflect the beam increases with proximity to the clamping point. This can lead to higher control voltages. Second, the separation of the capacitive and biasing electrodes consumes more substrate space leading to larger devices. However, it should be reiterated that the benefit is a potentially infinite tuning ratio.

3.3.7 Device 7: Stepped upper electrode

Device 7, shown in fig. 3.22, introduces a step into the upper electrode. As with device 6, the lower capacitive electrode has been separated from the biasing electrode. However, this design uses a two-gap structure, rather than leverage, to avoid pull-in. The capacitive gap is set to $1\mu m$ and the biasing gap to $3\mu m$. The upper electrode is clamped on all four sides.

The principle of operation of device 7 is if the capacitor is biased to pull-in then the upper electrode is displaced a specific distance. If the capacitive gap is less than this distance then, in principle, any capacitive gap can be set prior to the onset of pull-in. In this case the capacitive gap has been set to one third of the biasing gap. This corresponds to the parallel plate approximations. This should be a reliable starting point, considering device 1 was shown to deform more than this at the centre prior to the onset of pull-in and some leverage is occurring due to the separation of the lower electrodes.

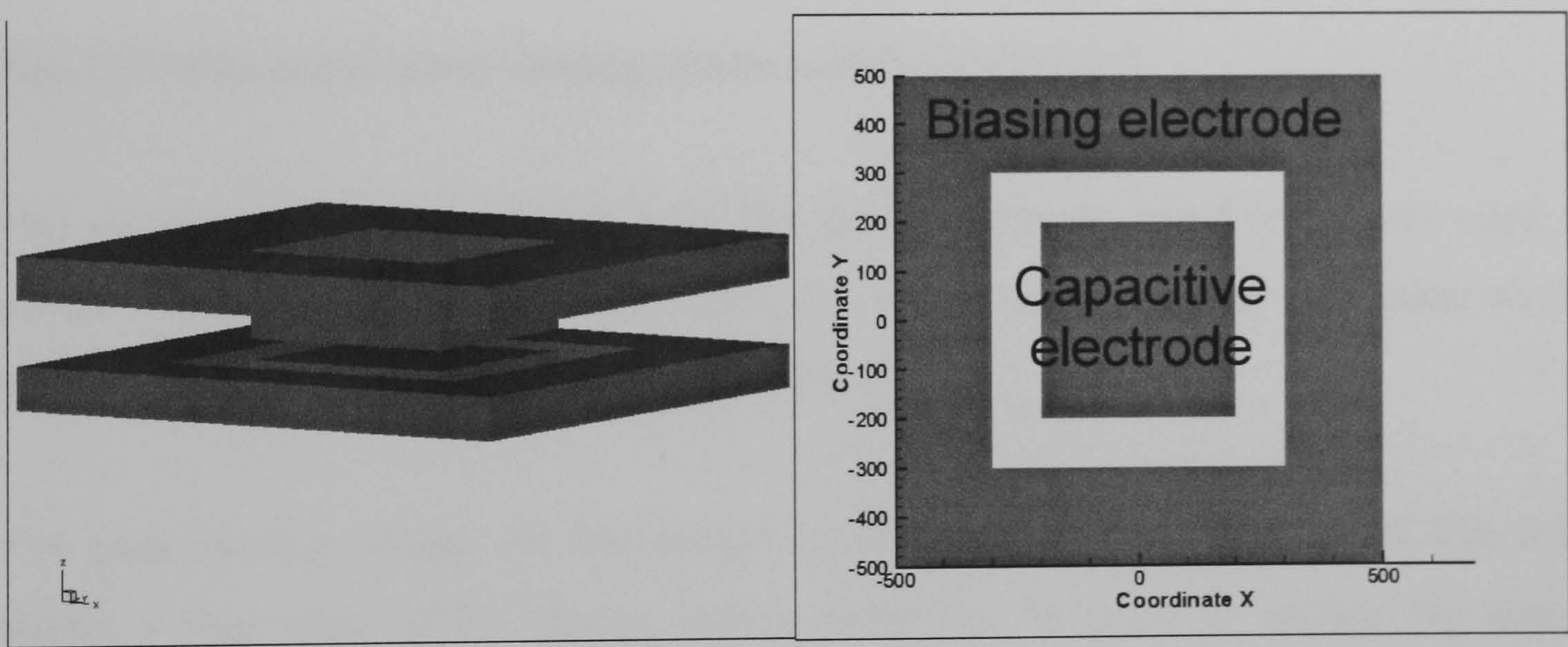


Fig. 3.22 Dimensions of device 7. The biasing gap is set to $3\mu m$ and the capacitive gap to $1\mu m$.

Fig. 3.23 confirms the validity of this approach by showing the capacitance tuning characteristic of this device. Capacitive electrode contact is occurring prior to pull-in which leads to an unrestricted tuning range.

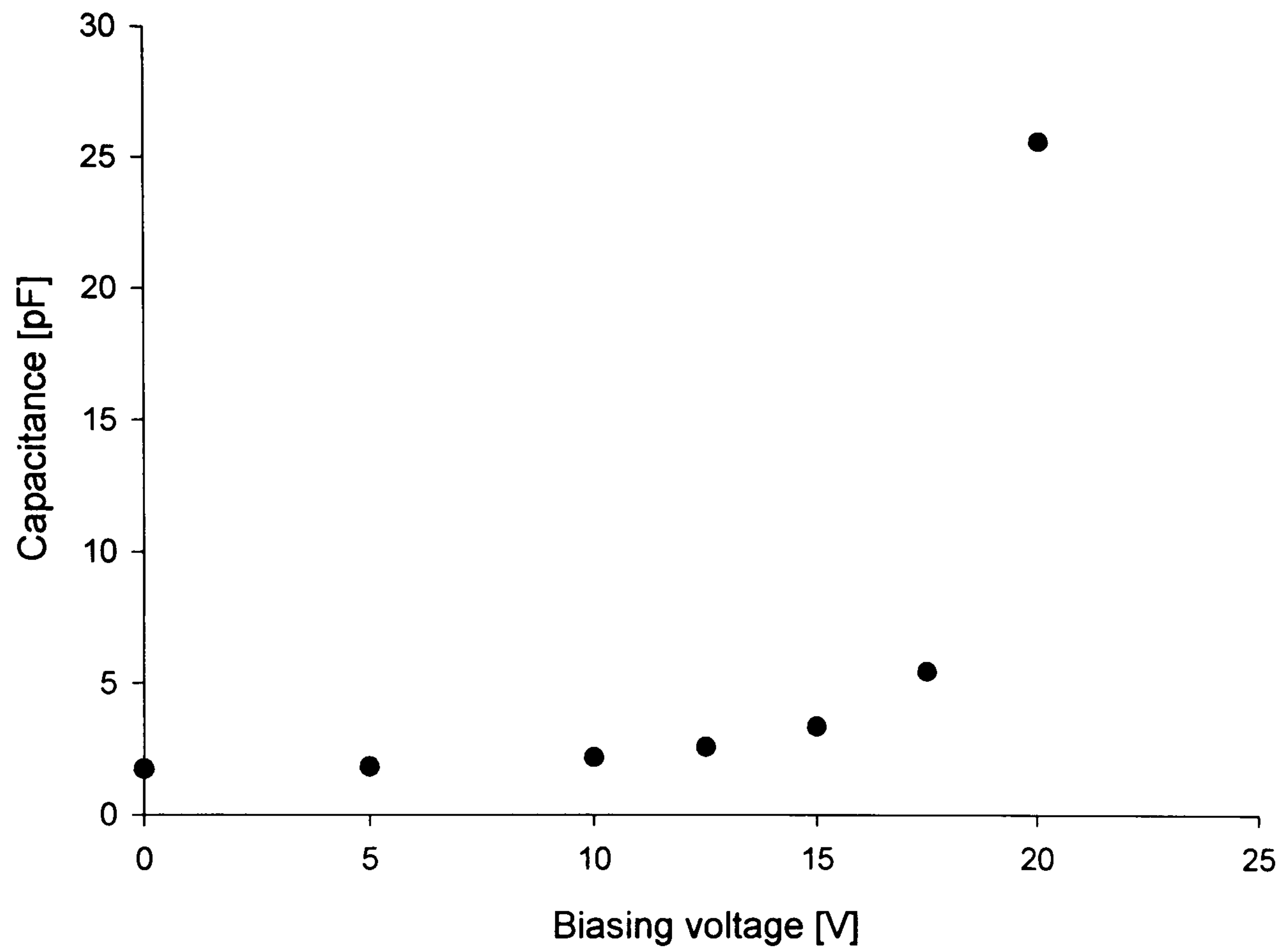


Fig. 3.23 The capacitance tuning characteristic of device 7.

The advantage of this approach over the purely leverage based avoidance used in device 6 is that the biasing and capacitive electrodes can be close to each other on the substrate. This allows for a more compact device.

The peak biasing voltage for this device is 20V prior to electrode contact. Fig. 3.24 shows a side view of the device during actuation. In order to reduce the tuning voltage, the biasing electrode area could be enlarged, the upper electrode shape modified to reduce the restoring spring force (as in device 3), the upper electrode thickness reduced or the electrode gaps decreased. The final decision on such a change depends on fabrication considerations. The next section will discuss the fabrication issues in parallel with the simulations.

This two-gap micromachined capacitor forms the basis of the simulations in the next section. However, instead of using a stepped upper electrode the two-gaps are achieved by using different lower electrode thicknesses.

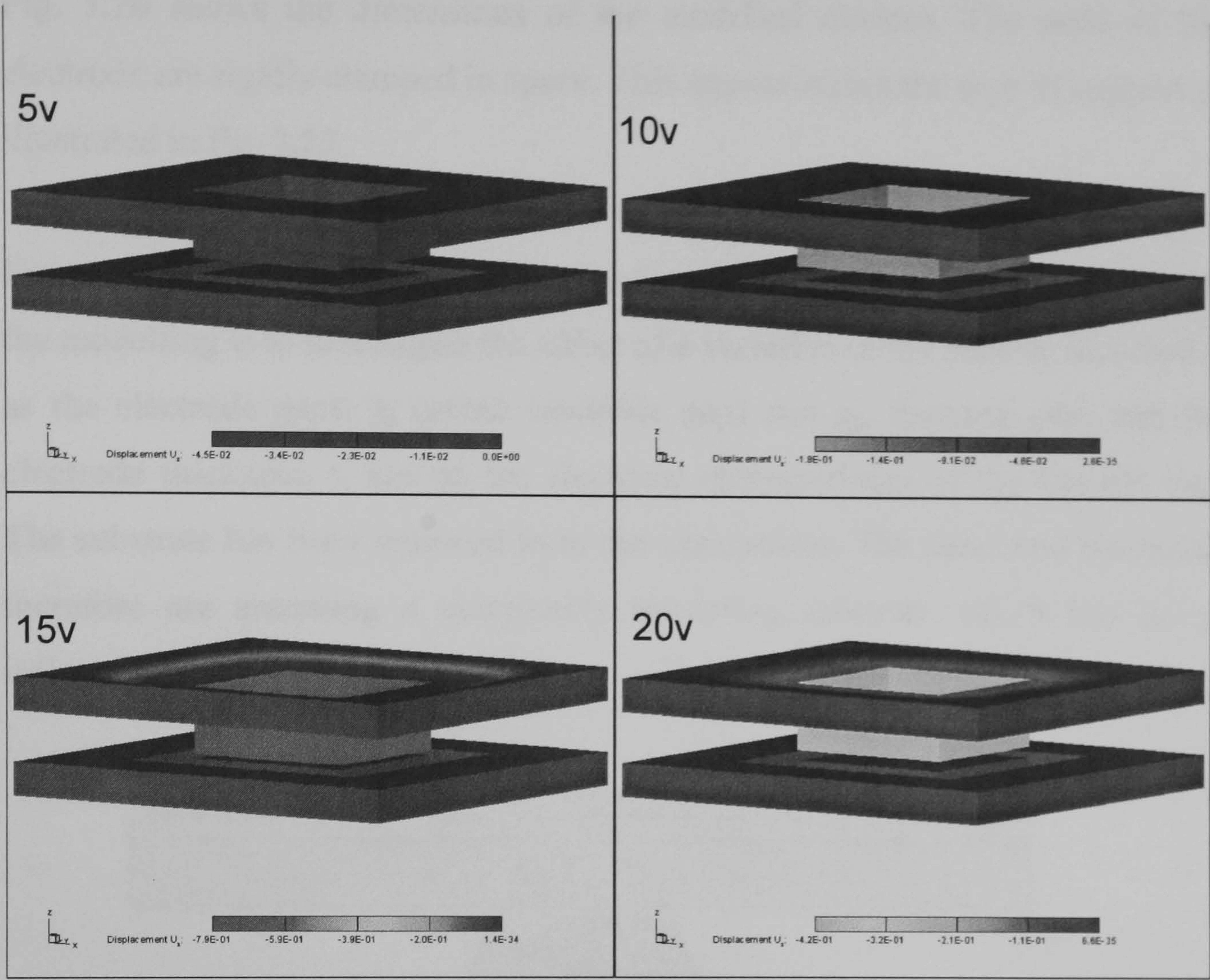


Fig. 3.24 The deformation of device 7 subject to various biasing voltages. Displacement units are μm.

3.4 Simulating the two-gap widely tunable capacitor

In the previous sections, the tuning limitations associated with any single-gap two electrode capacitor were highlighted. The side view of a two-gap approach is shown in fig. 3.25. The central capacitive sense electrode is thicker than the outer biasing electrodes. This enables two gaps to be achieved.

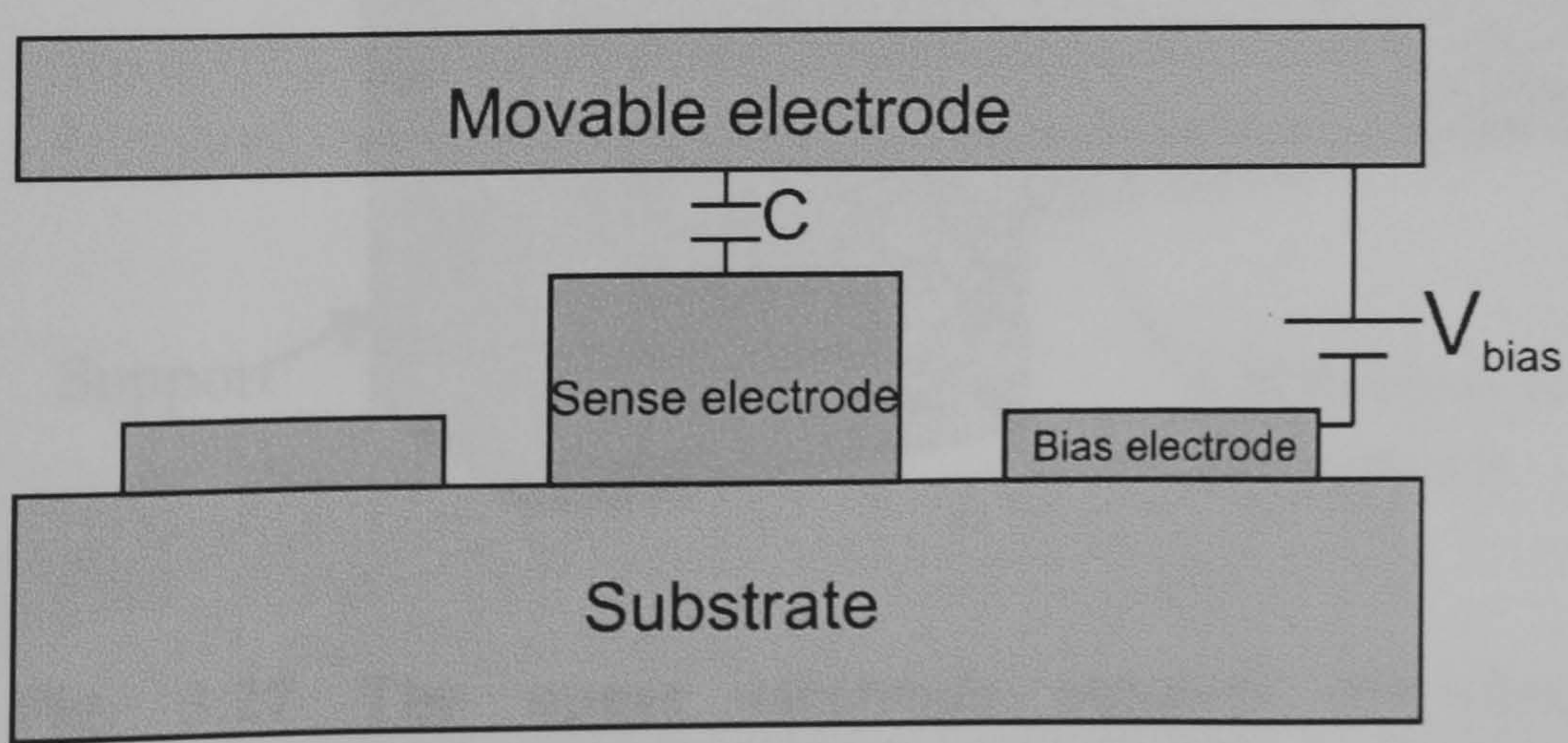


Fig 3.25 The structure of a two-gap tunable capacitor.

Fig. 3.26 shows the dimensions of the modelled devices. The ends of the upper electrode are rigidly clamped in space. This approximates the type of support structure illustrated in fig. 3.27.

For modelling purposes the device area dimensions remain fixed. Instead, the focus of the modelling is to investigate the effect of a variation of the vertical dimensions, such as the electrode gaps, g_s (sense electrode gap) and g_d, (biasing gap) and the upper electrode thickness, t, has on the electrical characteristics of the tunable capacitors. The substrate has been removed from the simulations. The simulated electrical results therefore are assuming a completely insulating substrate which has no parasitic influence.

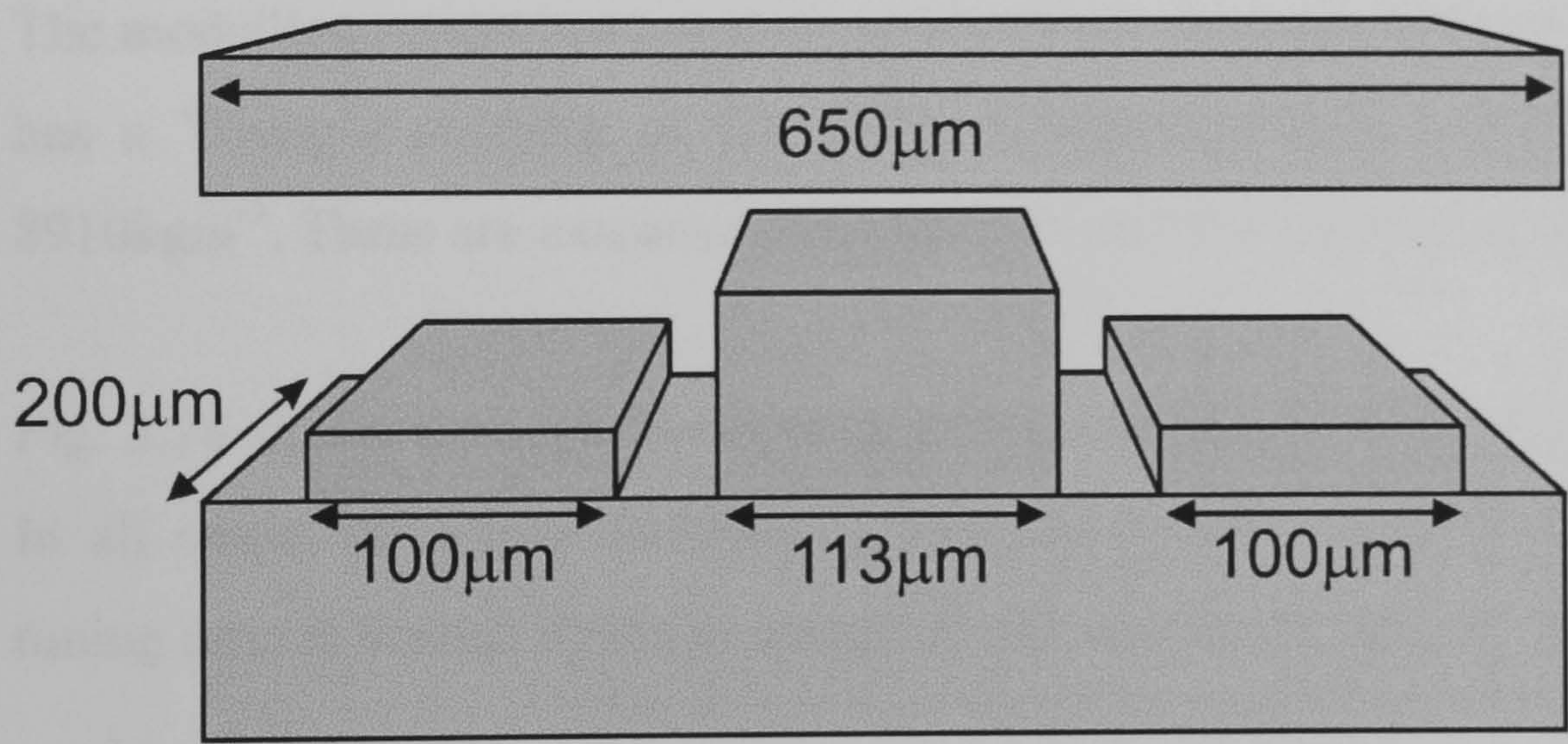


Fig. 3.26 The horizontal dimensions of the modelled devices.

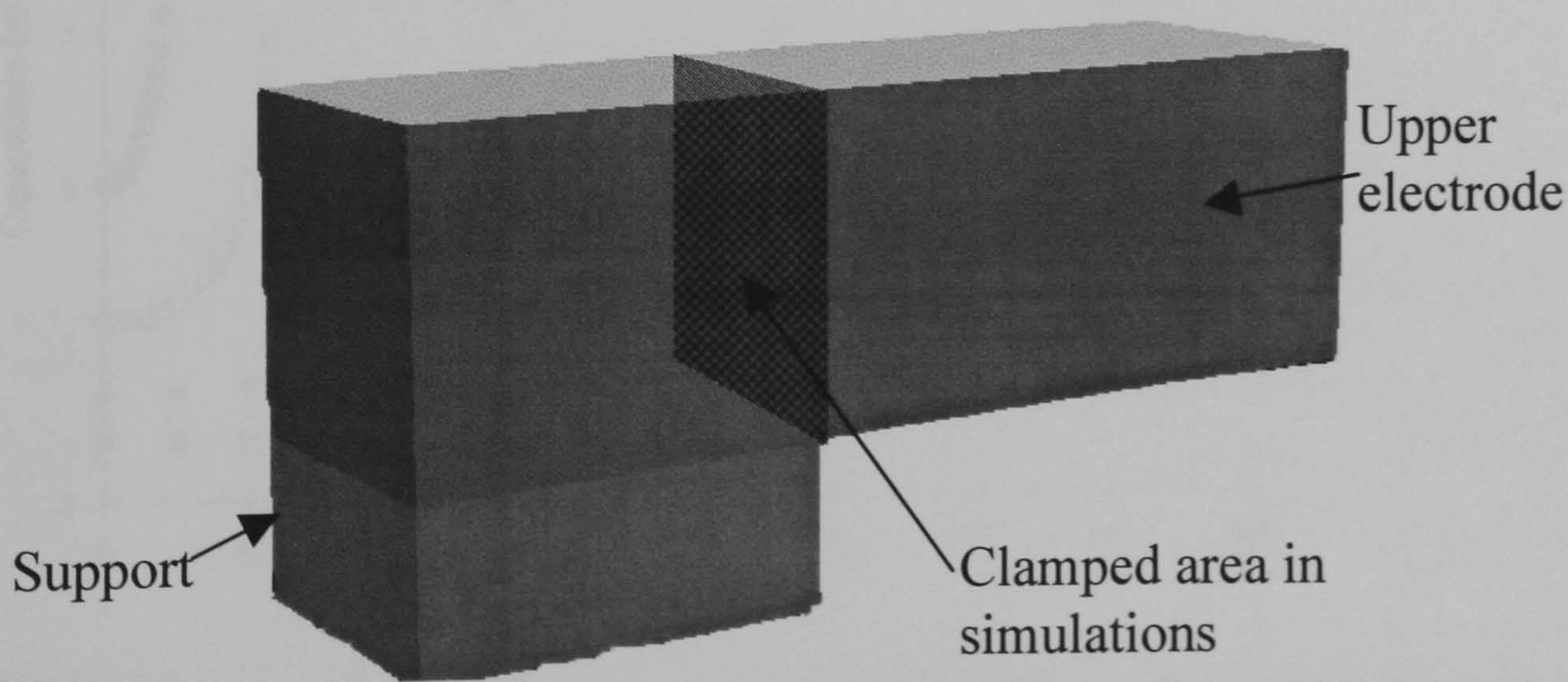


Fig. 3.27 The upper electrode support arrangement. The simulations approximate this support by clamping the upper electrode in the shaded region

The area of the upper electrode is primarily determined by device fabrication considerations. Larger areas introduce stiction failure at the device release stage and occupy valuable chip area.

The modelling results attainable from the variation of the vertical dimensions enable the designer to choose a suitable operating voltage and unbiased capacitance value. The choice of fabrication technique, which includes evaluating the need for additional planarisation techniques, depends on the surface topology. The upper electrode does not include etch holes in the modelled devices. The configuration of these etch holes in the completed device is subject to change during the optimisation of the fabrication process and hence cannot readily be pre-determined.

The modelling results are based on an all nickel structure. In these simulations, nickel has a Young's modulus of 220.5GPa, a Poisson's ratio of 0.3 and a density of 8910kgm^{-3}. These are extracted from Coventorware's material property database.

Fig. 3.28 shows the capacitance tuning characteristics for a range of gap dimensions. In all cases, the upper electrode is 3μm thick. From a modelling perspective, the tuning ratio is limited by the precision of the control voltage prior to electrode contact.

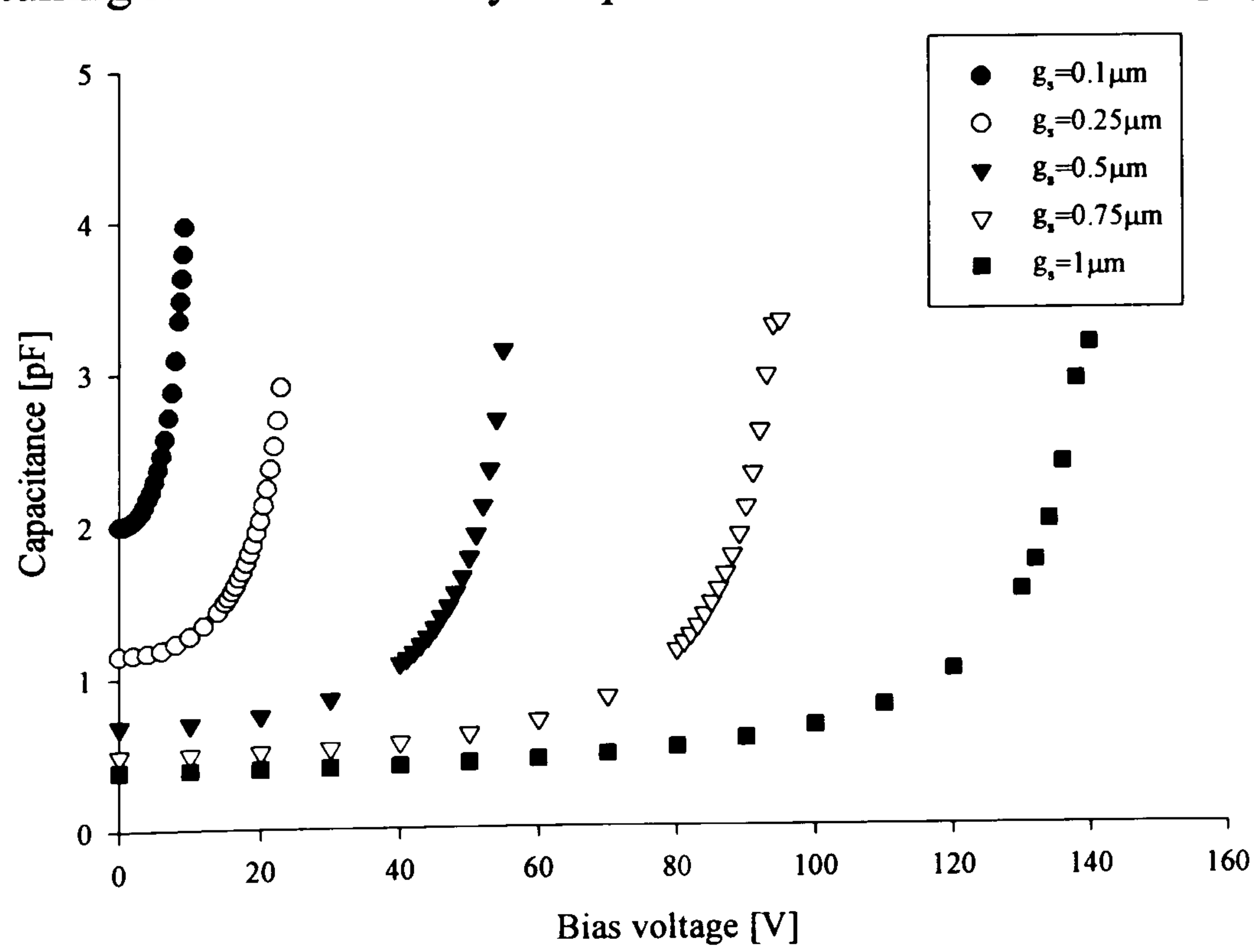


Fig. 3.28 The modelled capacitance-bias voltage characteristics of the two-gap capacitor for a range of initial sense/top electrode spacings, g_s. In all cases g_d is set at three times g_s. The top electrode thickness is 3μm. This assumes zero residual stress.

This electrical characteristic forces the capacitor to work at the extreme of its bias voltage for a significant capacitance variation to be achieved. The stability of the capacitance is therefore extremely reliant on the stability of the bias voltage.

The effect of the RF voltage across the sense electrode on the performance of the capacitor cannot be discounted. Although pull-in due to the DC bias has been overcome, the RF voltage could cause the upper electrode to pull-in. Fig. 3.29 shows the maximum root mean squared (rms) RF voltage which can be applied to the sense electrode prior to pull-in for a tunable capacitor with g_s=0.5μm, g_d=1.5μm and t=3μm.

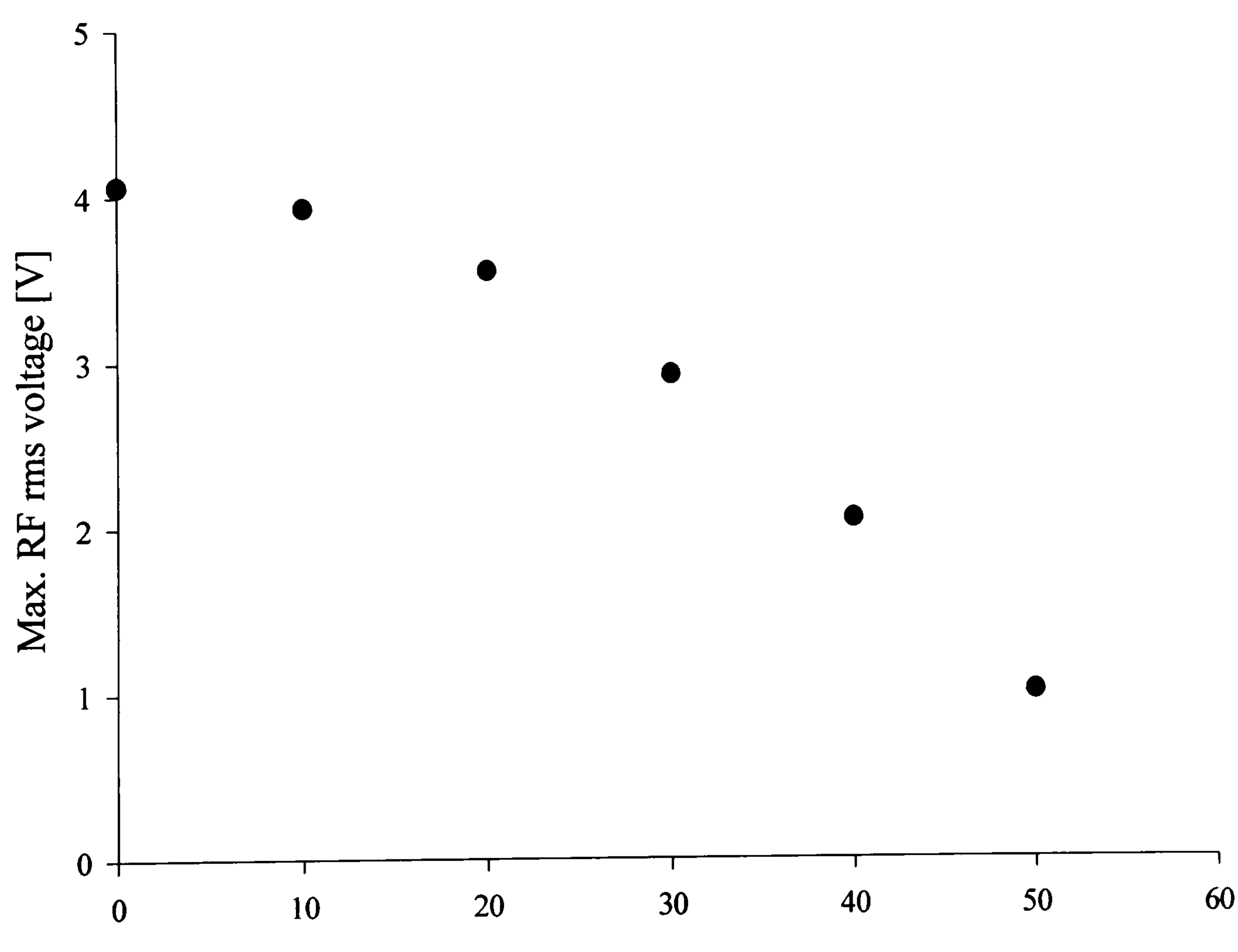


Fig. 3.29 The modelled maximum rms RF voltage which can be applied to the sense electrode prior to pull-in for a tunable capacitor (g_s=0.5μm, g_d=1.5μm and t=3μm) under a range of bias conditions. This assume zero residual stress.

When the bias voltage is applied the electrode spacing is reduced and consequently the maximum RF voltage achievable before pull-in occurs also reduces. Therefore, the preferred region of operation, which shows the largest capacitive change, is also the region where the smallest RF voltage can be accommodated. This introduces an additional constraint on the practical device operation.

By altering the electrode gaps, the initial capacitance value can be set by the designer. As the gap is increased, the unbiased capacitance decreases but the magnitude of the bias voltage increases.

Fig. 3.30 shows the effect of varying the upper electrode thickness on the electrical characteristics of the tunable capacitor. A reduction in the upper electrode thickness enables the designer to reduce the required bias voltage for a given unbiased capacitance.

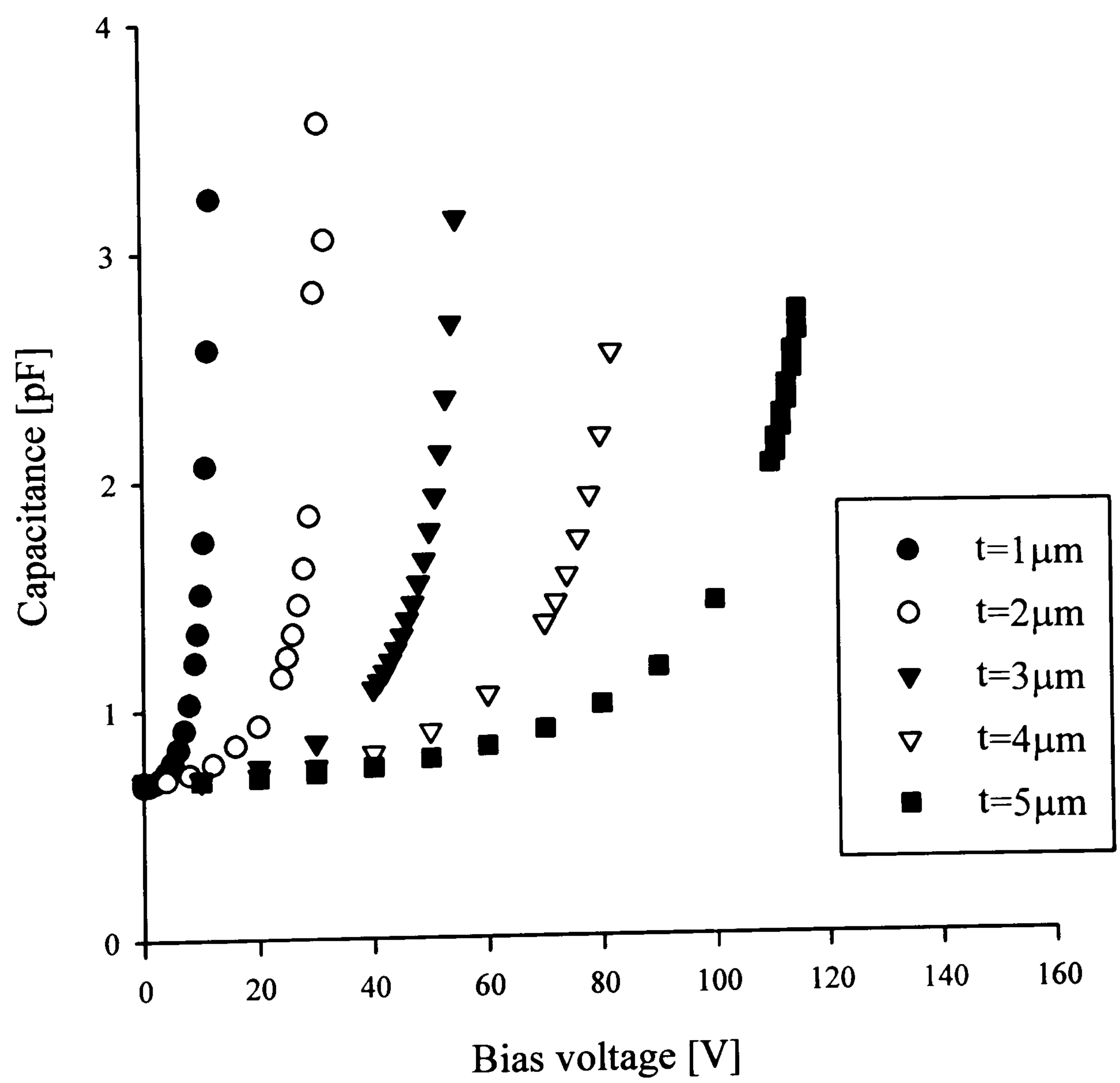


Fig. 3.30 The modelled effect of varying the thickness of the upper electrode, t, of a capacitor (g_s=0.5μm and g_d=1.5μm). This assumes zero residual stress.

Fig. 3.31 shows the mechanical resonant frequency variation over a range of upper electrode thicknesses for the device modelled in fig. 3.29. In all cases the magnitude of the resonant frequencies is in the kHz range. This is an essential characteristic of the device, which will typically be subject to RF signals in the GHz range. The upper electrode is mechanically damped such that a stable capacitance is maintained when an RF signal is applied.

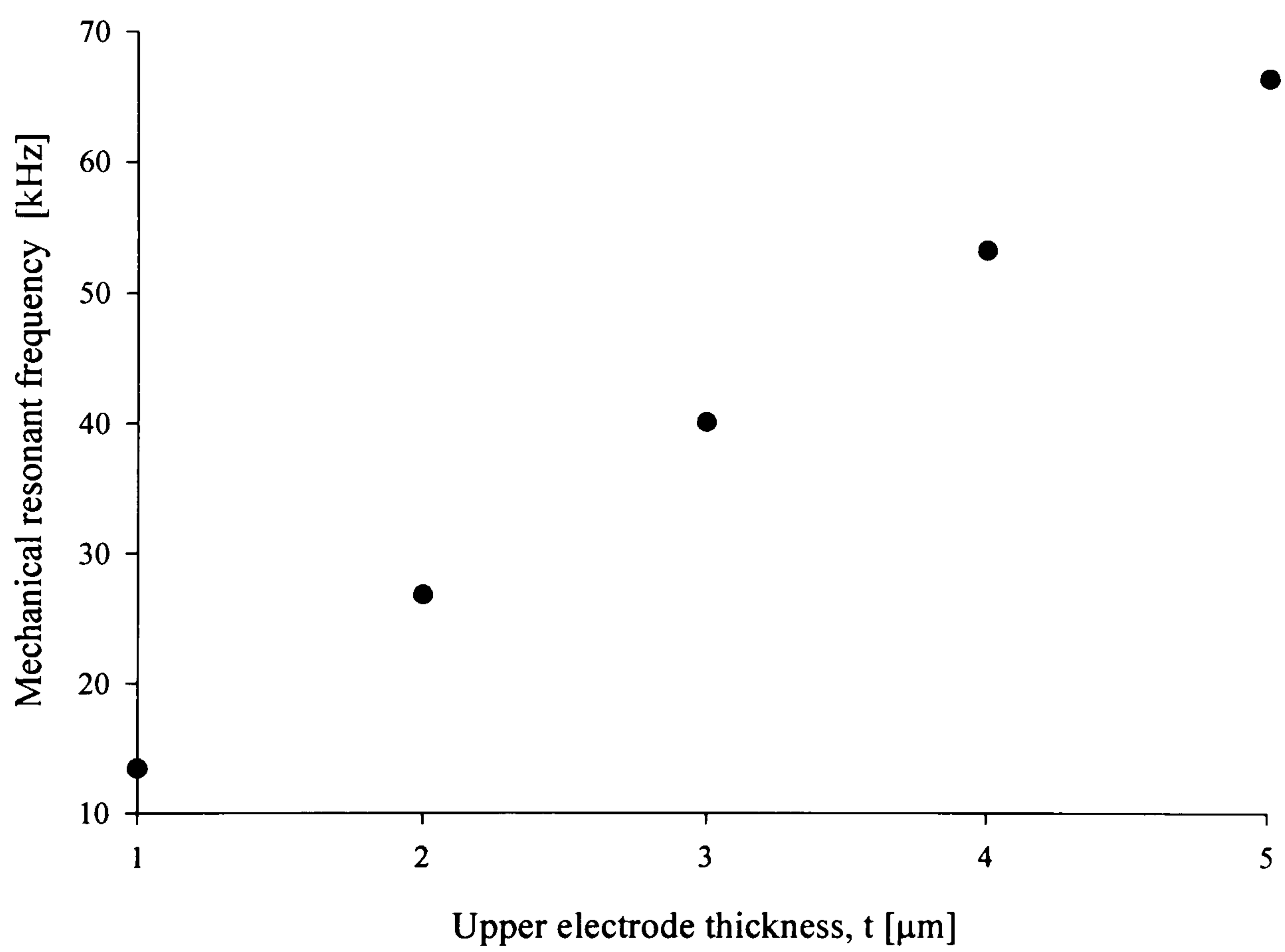


Fig. 3.31 The modelled mechanical resonant frequency of the device for a range of upper electrode thicknesses for devices with g_s=0.5μm and g_d=1.5μm. This assumes zero residual stress.

The device specification can be obtained by choosing an electrode gap to set a desired unbiased capacitance. Then variation of the upper electrode thickness establishes a preferred control voltage. However from a fabrication perspective, the situation is not as straightforward. The maximum biasing voltage is limited by the dielectric breakdown of air. If the air gaps are below 5μm, then Paschen's Law [90] elevates the breakdown voltage. However, microdischarge and eventually full breakdown will still occur with increasing bias voltage. This limits the technique of increasing the upper electrode thickness to increase the tuning voltage.

The deformation of the thicker and hence stiffer upper electrode introduces additional stress on the supports. This has ramifications for the long-term reliability of the devices.

A reduction in the upper electrode thickness introduces a different set of device problems. With the decrease in the spring constant, the upper electrode is more susceptible to permanent stiction failure. In addition, any residual stress in the upper electrode becomes a more significant part of the thin film properties. This can produce at worst buckling when under compressive stress, and at best an elevated control voltage when tensile.

Fig. 3.32 simulates the effect of residual stress in the upper electrode on the biasing voltage required to cause sense/upper electrode contact. Negative stress is defined as compressive and positive stress as tensile. The simulated device has g_s=0.1μm, g_d= 0.3μm and t=3μm.

In the tensile case, the contact voltage is observed to increase as the tensile stress increases. The compressive situation, however, shows a fall off in contact voltage which effectively stops the device being tunable for compressive stress greater than 25MPa. This is, however, assuming that the compressive stress has not caused the device to buckle after release.

If stresses in the upper electrode introduce an upward curvature into the released devices it causes a deviation from the parallel plate arrangement. Fig. 3.33 shows a modelled device with upper electrode curvature and no biasing voltage. The maximum sense electrode gap is now $g_s + \Delta g_s$, where Δg_s represents the increase in gap caused by upper electrode curvature.

In Coventorware, a device has been simulated with g_s=0.1μm, g_d= 0.3μm and t=3μm. The application of a force, Fc, to the top electrode, as indicated in fig. 3.33, has simulated the type of curvature that could be caused by a residual compressive stress.

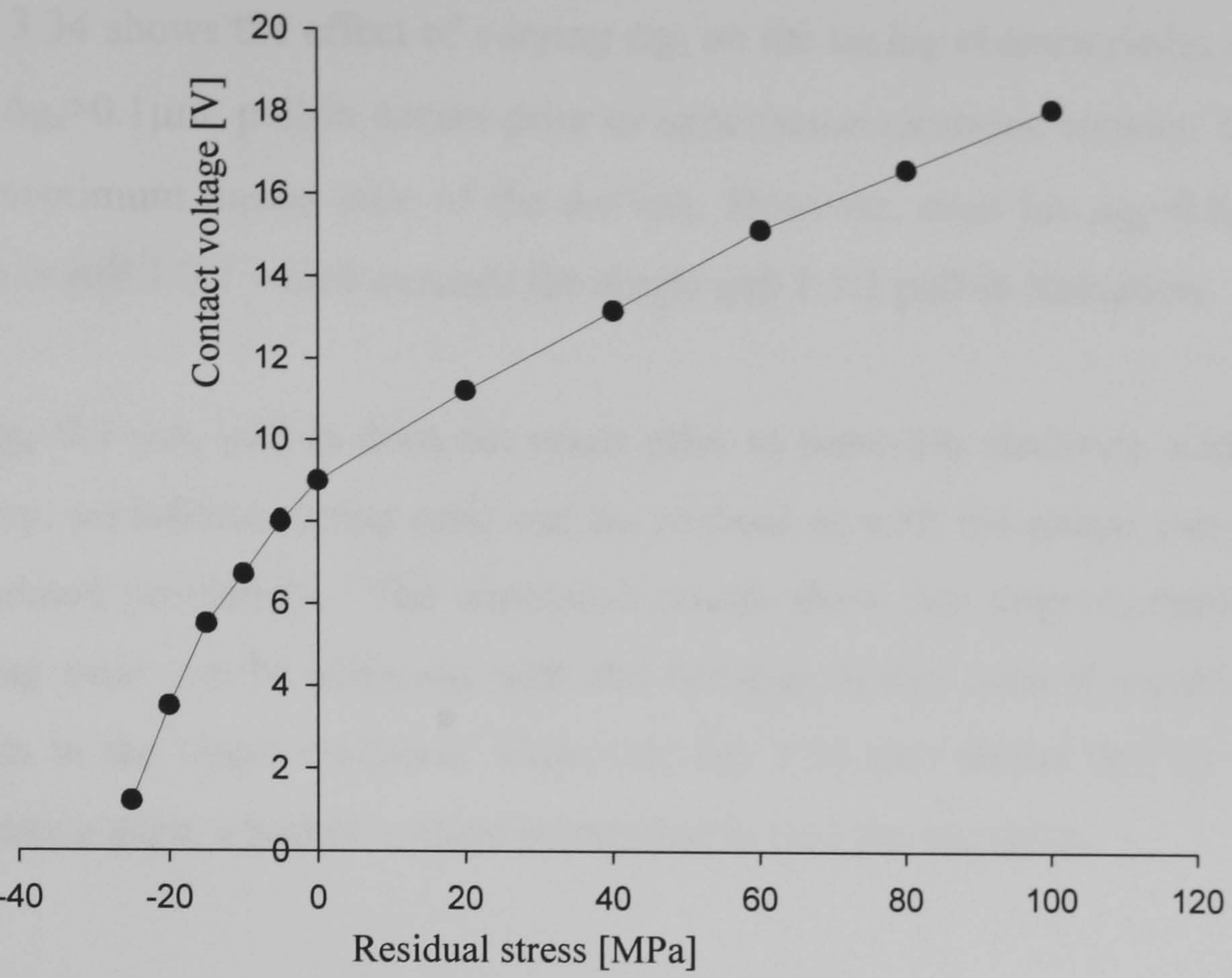


Fig 3.32 The simulated effect on the electrode contact voltage of residual stress in the upper electrode. Tensile and compressive stresses are represented by the positive and negative regimes respectively. The simulated device has g_s=0.1μm, g_d= 0.3μm and t=3μm and has zero residual stress gradient.

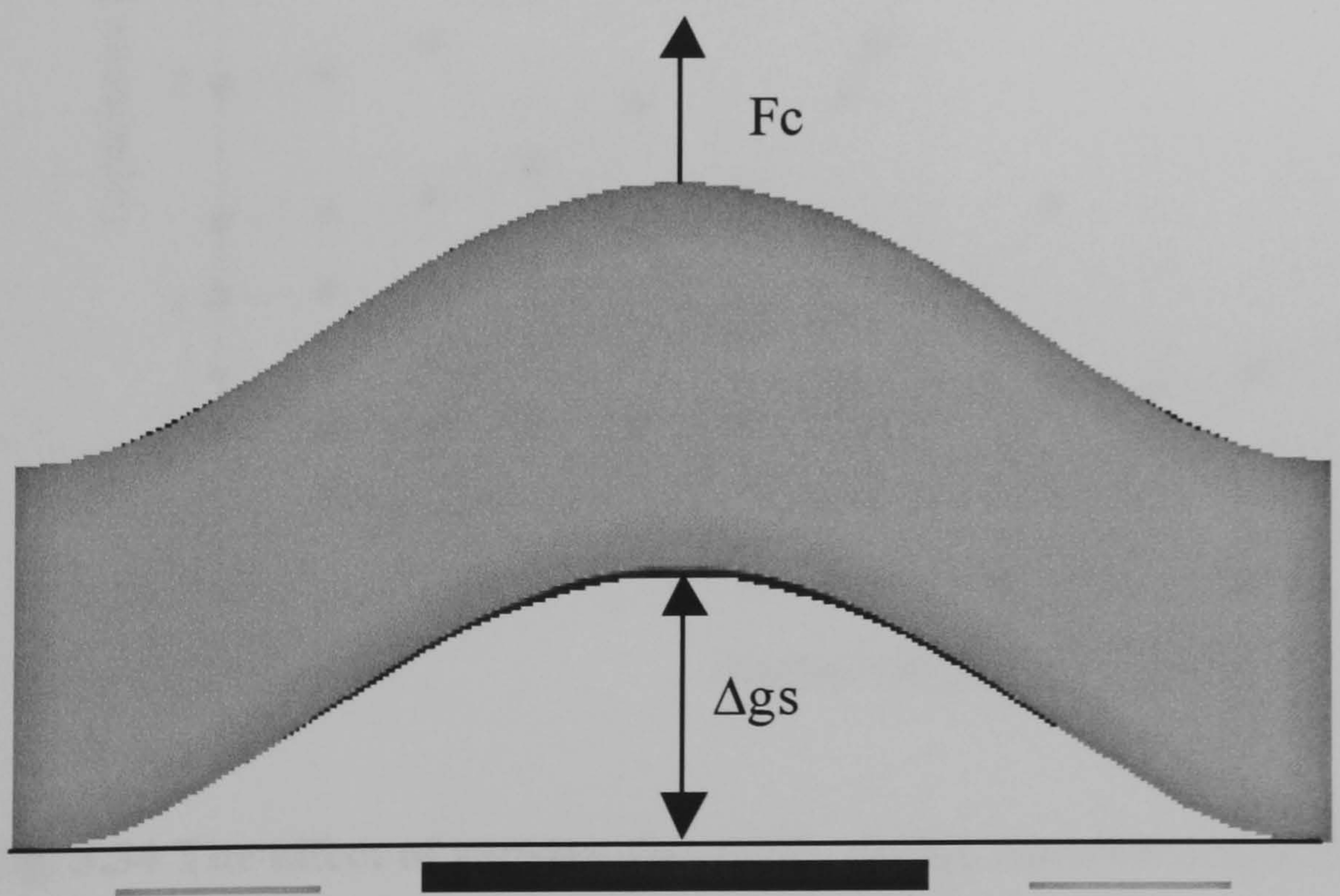


Fig. 3.33 An unbiased two-gap capacitor with a force, F_c, applied to the upper electrode. Δg_s is the maximum increase in upper/sense electrode gap caused by this deformation.

Fig. 3.34 shows the effect of varying Δg_s on the tuning characteristics of the devices. For Δg_s>0.1 μm, pull-in occurs prior to upper/sense electrode contact. This is limiting the maximum tuning ratio of the devices. However, even for Δg_s=0.8 μm the tuning ratio is still 1.9:1 which exceeds the single-gap 1.5:1 pull-in limitation.

If Δg_s<0.1 μm, pull-in does not occur prior to sense/top electrode contact. Hence, in theory, an infinite tuning ratio can be attained as with the planar two-gap structures simulated previously. The simulated results show that improvements on the 1.5:1 tuning ratio can be achieved with the two-gap design even if significant curvature exists in the upper electrode. However, fig. 3.34 also shows that by increasing the electrode gaps, a higher voltage is required to tune the capacitor.

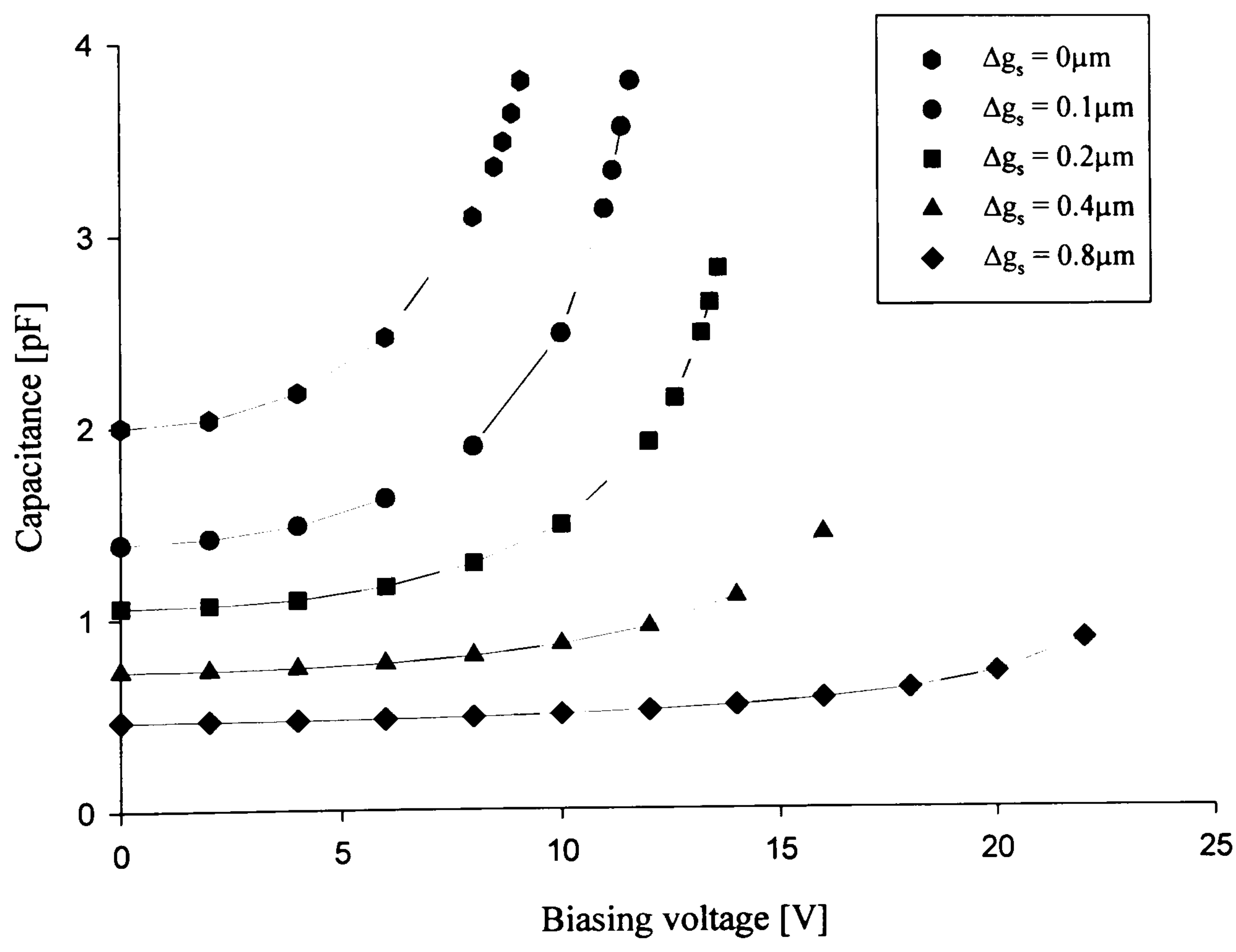


Fig. 3.34 The effect of varying Δg_s on the tuning characteristics of the capacitor.

3.5 Chapter Summary

- Coventorware is a commercial finite element analysis (FEA) package specifically developed for the simulation of micromachined devices. Computer simulation tools aim to minimise cleanroom processing and the associated costs during product development.

- Pull-in can limit the tuning range of electrostatically biased micromachined capacitors. In an ideal parallel plate, single-gap capacitor the maximum tuning ratio can be shown to be 1.5:1

- Leverage bending by separating the bias and capacitive electrodes can provide significant tuning range benefits. First, the force required to deflect the beam increases with proximity to the clamping point. This can lead to higher control voltages. Second, the separation of the capacitive and biasing electrodes consumes more substrate space leading to larger devices.

- The advantage of the two-gap approach over the purely leverage based avoidance used in device 6 is that the biasing and capacitive electrodes can be close to each other on the substrate. This allows for a more compact device.

- The effect of gap dimensions, upper electrode thickness, RF voltage and thin film stress on the tuning performance of the two-gap structure has been modelled using Coventorware.

- An important consideration of the two-gap structure is that to achieve very high tuning ratios the gap needs to be made very small. This introduces additional considerations such as surface topology which are not effectively simulated by Coventorware.

Chapter 4

Surface micromachining methodology

Surface micromachining can lead to substrate independent devices. It is therefore ideal for RF MEMS fabrication, where integration with existing ICs is a significant goal. This chapter details the techniques used to fabricate surface micromachined devices at Durham. Deposition, photolithography, patterning and metrology techniques will be identified and discussed. Later chapters will rely upon applications and modifications of these core techniques to fabricate micromachined RF devices.

4.1 An introduction to surface micromachining

Integration has been the driving force for the semiconductor industry over recent decades. In memory devices, for example, the primary objective has been to reduce the transistor gate length to enable more transistors to be fabricated on each chip. The reduction in gate and interconnect lengths enables both greater storage capacity and faster operation.

From a technological perspective this increased level of integration led by the memory industry has forced advances in photolithography, defect control, automated production and thin film deposition techniques.

In order to reduce manufacturing costs and maintain yield on small feature devices, an additional move in the industry has been towards larger wafer processing. 200 mm wafers are now commonplace with minimum gate lengths of 0.13μm regularly specified and 300mm wafers are used in the larger fabrication plants.

The micromachining industry has driving forces different from the IC industry. Minimum feature sizes tend to be larger than a micron. These dimensions are primarily dictated by structural and device mechanics rather than semiconductor electronics. This enables lower class cleanrooms, low cost contact photolithography and older manufacturing equipment to be employed.

From a university research and development perspective, micromachining is an excellent enabler to exploit existing equipment and cleanrooms which would be unable to compete in an industrial IC environment. Small-scale micromachining R&D does not require automated equipment, 300mm wafers or Class 1 cleanrooms.

However, in the long term it is imperative that these micromachining fabrication techniques can be integrated alongside existing integrated circuits. In RF MEMS this is particularly relevant because interconnect parasitics can negate the technological advantages of micromachined devices.

In order to integrate micromachined devices alongside existing integrated circuits common processing techniques need to be available. Surface micromachining [48] has been developed to produce devices with a near IC compatible process flow. The movable structures can, at least in principle, be fabricated onto an IC shared substrate.

Fig. 4.1 shows a simplified surface micromachined process flow. The structures are fabricated by depositing and patterning structural materials such as metals or polysilicon on top of a substrate. At the end of the processing one of the layers, known as a sacrificial layer is selectively etched. This releases the movable parts of the device. A typical process flow therefore consists of layer deposition, photolithographic patterning and etching. These are repeated for separate layers until the complete structure is formed.

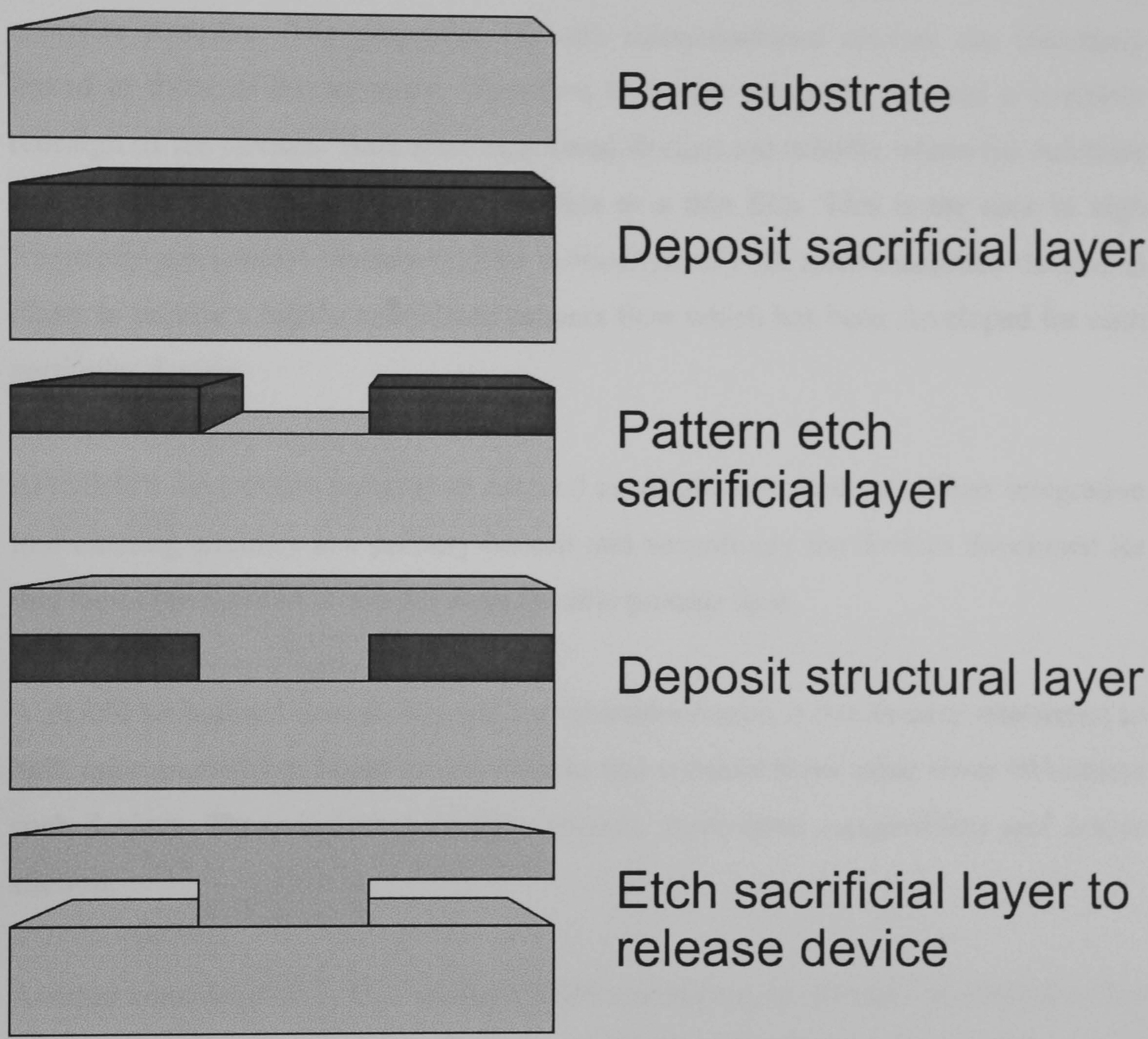


Fig. 4.1 A typical surface micromachining process flow

An important feature of surface micromachined devices is that they use the substrate primarily as a physical support rather than as an active mechanical element. Therefore the process flow can be made substrate independent. With care taken to avoid chemical incompatibility, substrates as diverse as silicon, glass and gallium arsenide could be used.

The devices could even be fabricated on top of an IC encapsulation layer such as polyimide. This flexibility is attractive to existing semiconductor companies when they are considering integrating micromachined devices with their microelectronic devices.

This contrasts with bulk micromachining, which uses the substrate as part of the movable structure. The properties of bulk micromachined devices are intimately linked to those of the substrate. Therefore to switch substrates requires a complete redesign of the devices. Bulk micromachined devices are suitable where the substrate can provide superior mechanical properties to a thin film. This is the case in high frequency mechanical resonators. The fabrication of bulk micromachined devices is likely to require a highly specialised process flow which has been developed for each particular device.

RF MEMS devices are unlikely to succeed as stand-alone elements. Their integration into existing circuitry is a primary benefit and accordingly the devices developed for this thesis have aimed to use the most flexible process flow.

It should be realised though that surface micromachining is not an easy alternative to bulk micromachining. Many new problems and considerations arise when fabricating such devices. These include thin film stresses, multi-layer compatibility and device stiction.

Another consideration is that, unlike CMOS techniques, no standard process flow has been universally adopted for surface micromachining. Some exist, however these tend to be tailored to specific structures and provide weaker performance when applied to an arena such as RF MEMS. As an example, consider the original MUMPS [91] process. It provides a standard platform surface micromachined polysilicon. Although polysilicon is an alternative to bulk micromachined silicon in some applications, in RF MEMS it is lossy at high frequencies.

4.2 Thin film deposition

This section describes three techniques which can be used to deposit thin metallic films for surface micromachined devices. These are evaporation, sputtering and electroplating. Each technique has its own benefits and applications. Combinations of these techniques such as evaporation and electroplating may be required to achieve a micromachining solution.

4.2.1 Evaporation

This technique relies upon a metal being heated high enough to produce a significant vapour pressure. The evaporant gas is allowed to condense onto the substrate requiring metallisation. This is performed under a high vacuum, typically 10^{-6} Torr or better, to ensure a large mean free path of the evaporant gas.

Two main routes exist to heat the metal. First, resistive evaporation is where the source is placed inside a tungsten filament. Current is passed through the filament and consequently the source is heated. This technique is effective for metals such as chrome, gold and aluminium.

The deposition rate is determined firstly by the source density and secondly by the current passing through the filament. Higher melting point metals therefore require high current passing through the filament.

However, when metals such as titanium and nickel need to be deposited the technique is ineffective. This is due to a eutectic mixture being formed between the tungsten and the source metal. The eutectic has a lower melting point than the tungsten and consequently the filament breaks.

One way around this is to place the source inside a carbon crucible, but this requires extremely high operating temperatures in the evaporator which could damage any organic sacrificial layers present on the substrate.

An alternative approach is to direct an electron beam (e-beam) at the source metal. This is illustrated in fig. 4.2. The e-beam, generated by thermionic emission from a filament, locally heats the source. Magnets surrounding the crucible are used to direct the e-beam.

The lower part of the source is in contact with a water-cooled copper crucible. Therefore this part of the source remains solid and cannot form a eutectic with the copper. The e-beam technique enables a wider range of materials to be deposited. The deposition rate/current required to deposit the source is determined by the thermal conductivity, specific heat capacity and the resistivity of the source.

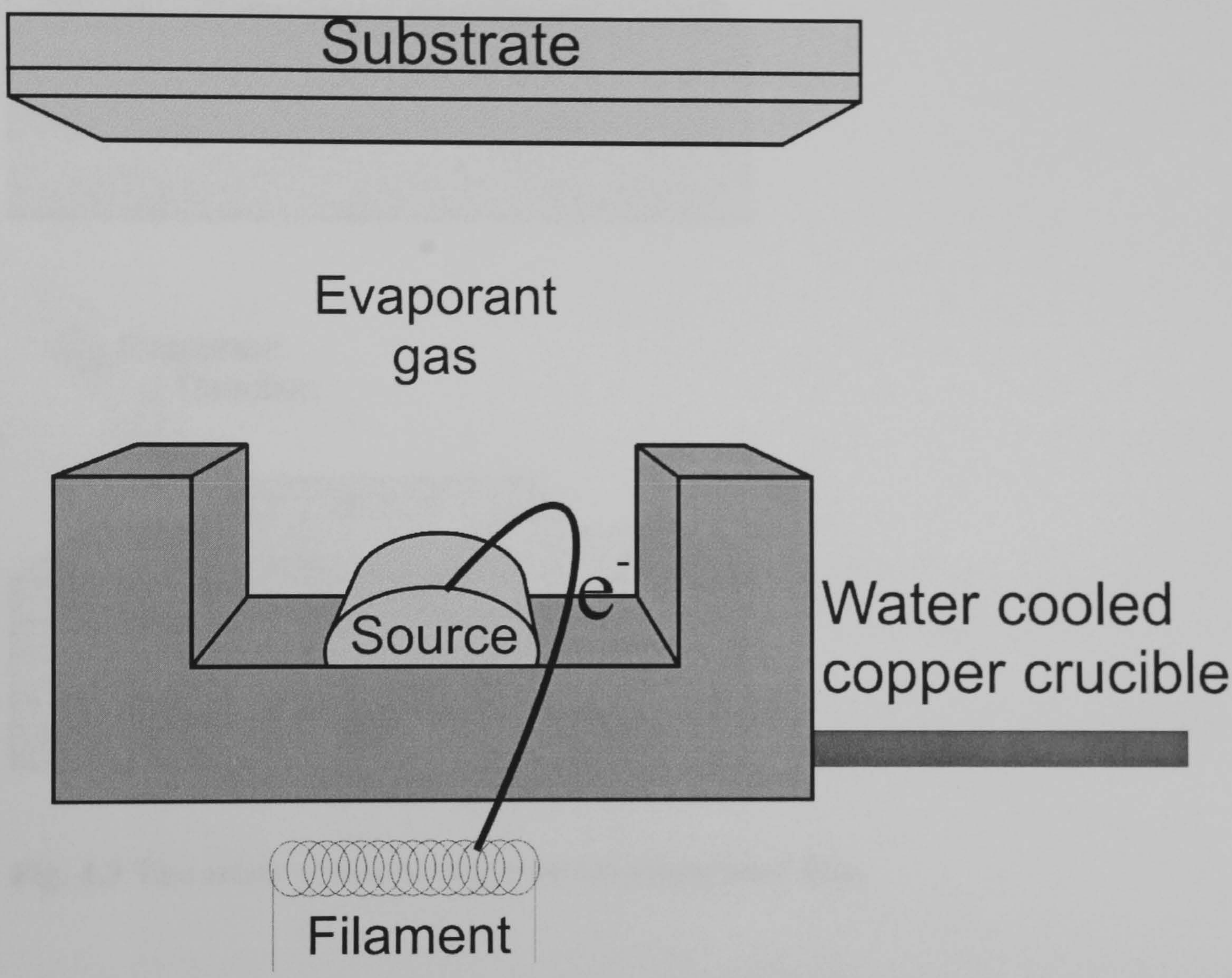


Fig. 4.2 Electron beam (e-beam) evaporation

Fig. 4.3 illustrates how an evaporated film coats a non-uniform surface when the source is considered to be at an angle to the substrate. The high vacuum minimises collisions of the evaporant gas in the chamber and hence the substrate is coated as if from a point source considered at a distance.

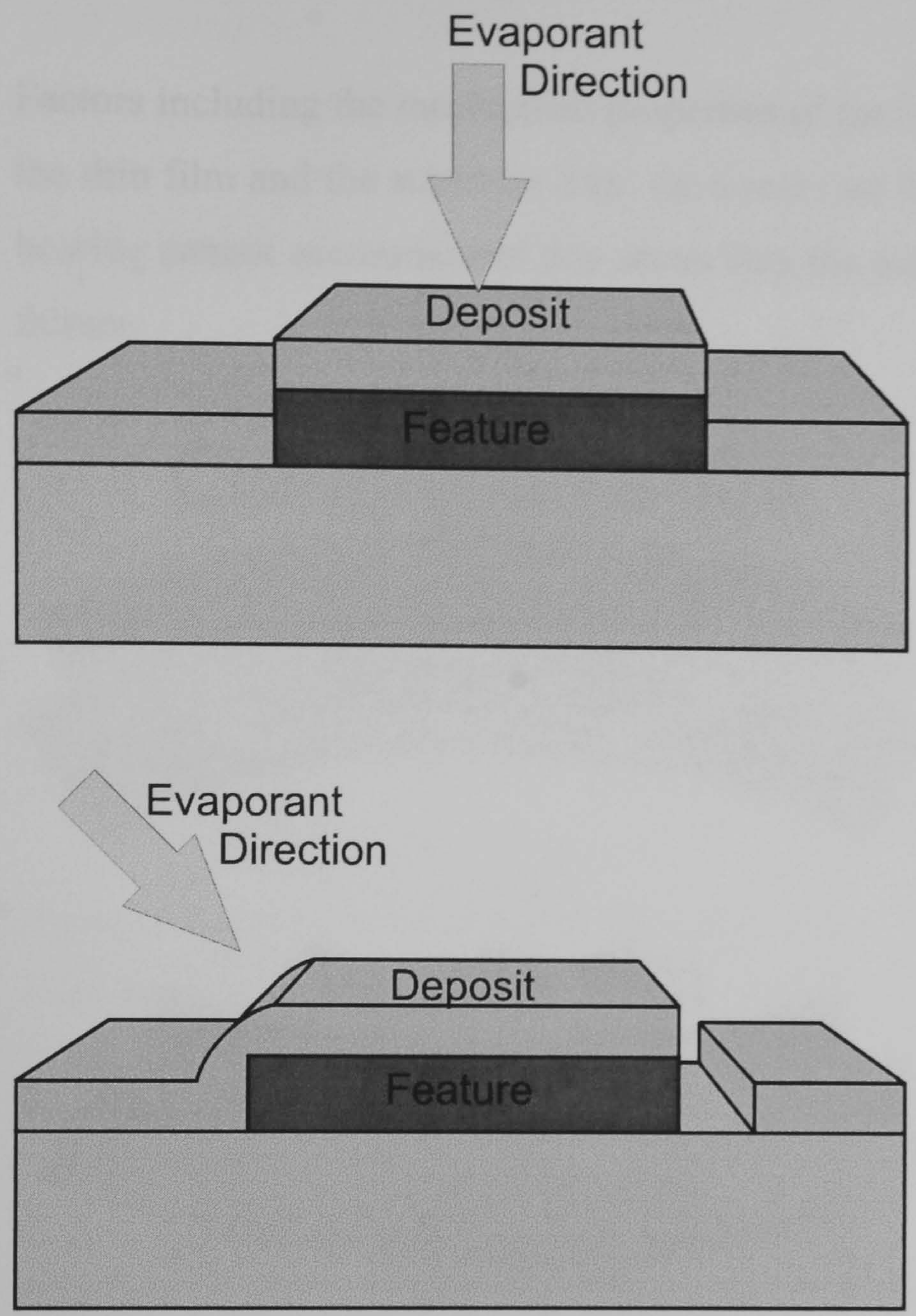


Fig. 4.3 The effect of source angle on an evaporated film.

The uniformity can be improved by increasing the distance between the source and the substrate. However, this reduces the deposition rate and increases metal consumption, which is important when valuable metals such as gold and platinum are deposited.

The benefits of evaporated films are apparent when dense high quality uniform depositions are required. The downside of this process is that high temperature evaporant gas contacts a cooler substrate to condense. This condensing causes the films to exhibit a higher stress when compared to lower temperature techniques. The tensile stress limits the deposition thickness.

The deposited film is attached to a substrate. If tensile stress occurs due to contraction during condensation then the film will pull against the substrate as shown in fig. 4.4 causing wafer bowing.

Factors including the mechanical properties of the substrate and the adhesion between the thin film and the substrate limit the stress that can be accommodated. If the wafer bowing cannot accommodate this stress then the thin film can fracture causing device failure.

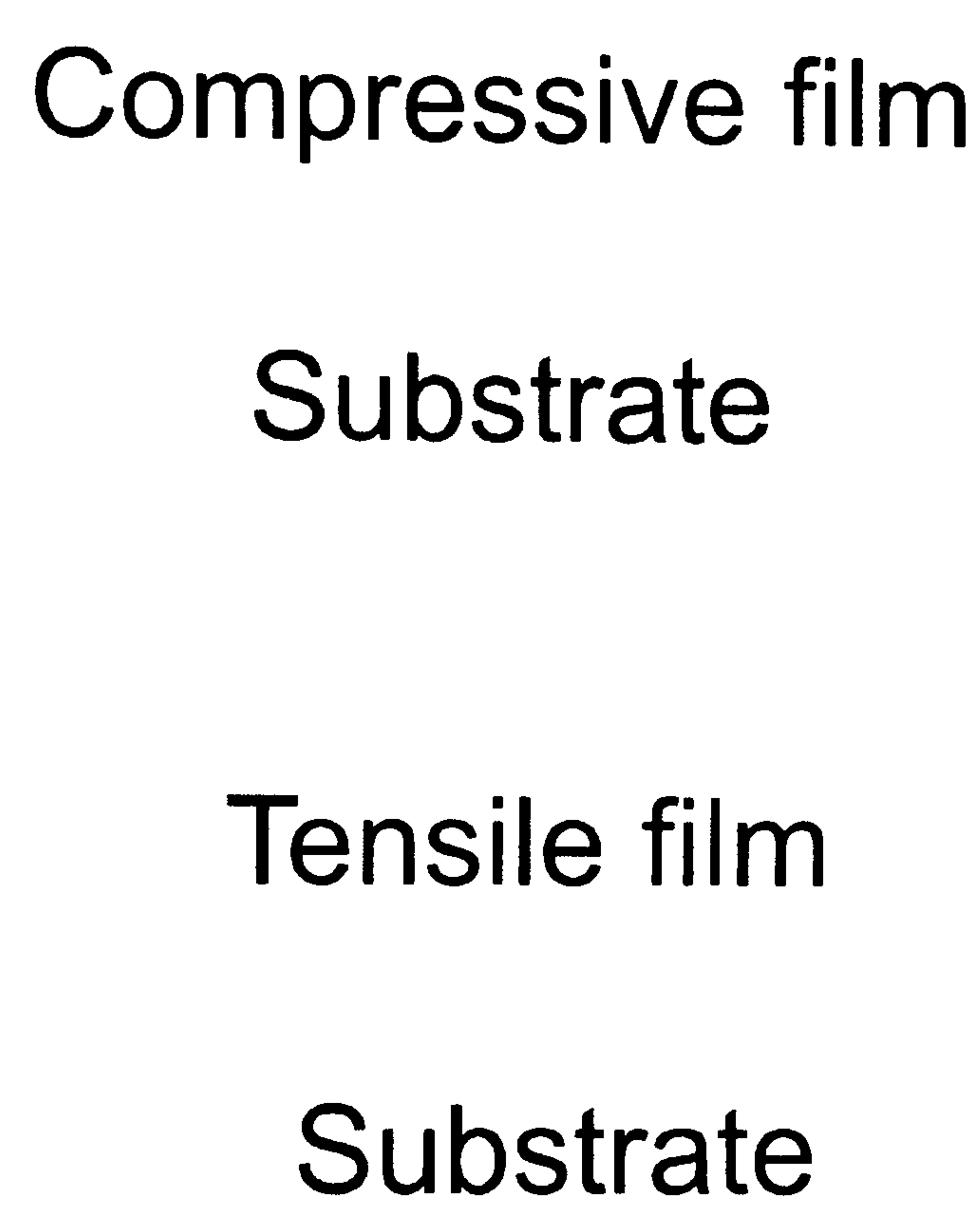


Fig. 4.4 The bowing effect of thin film stresses on a substrate.

Another important consideration is that if multi-layer evaporations are required then the stress in lower layers must also be considered because these will contribute to the overall stress on the wafer and will further limit the maximum thickness of an individual evaporation.

The thickness of the deposited films is measured by a thin film thickness monitor. This detects the resonant frequency change of a quartz crystal as metals are deposited onto it.

Since evaporation is fundamentally a high temperature process, care needs to be taken with organic films which may reflow during deposition. This can lead to stress fracturing. Evaporation is well suited to thin (0.5μm or less) film deposition and is well exploited in the fabrication flows of later chapters.

4.2.2 Sputtering

Sputtering, an alternative to evaporation, is a low temperature technique which enables lower stress and hence thicker films to be deposited. The principle of operation is that an argon plasma is generated in a vacuum chamber. This is directed at a target (the source material) and kinetic bombardment by the argon ions causes a displacement of the source material.

The displaced target material is then able to deposit onto the substrate. Sputtering produces a conformal coating as illustrated in fig. 4.5. Although the base pressure is comparable to evaporation (10^{-6} Torr or better), the operating pressure with argon in the system is typically only a few mTorr. This leads to more collisions and hence more scattering than in evaporation. The substrate is therefore coated from a range of directions leading to the conformal coating. In principle, films with a thickness of up to a few microns can be sputtered without stress fracture.

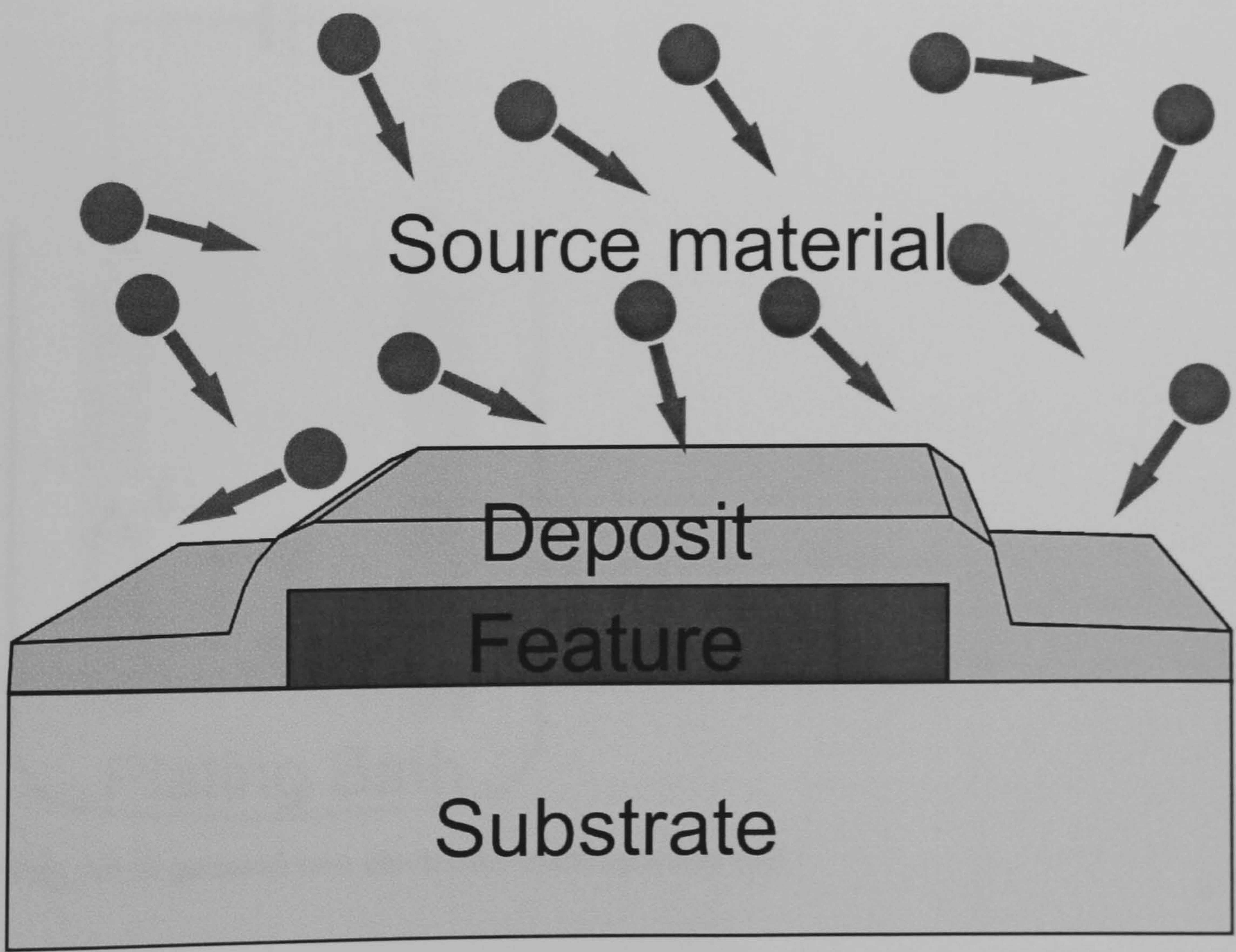


Fig. 4.5 The conformal nature of sputtered films due to random scattering.

4.2.3 Electroplating

Electroplating involves the transfer of a metal from a plating solution to a conductive substrate. In order to provide a sufficiently conductive substrate a thin metal seed may need to be sputtered or evaporated prior to electroplating.

Fig. 4.6 shows a general electroplating cell. There are two electrodes: A is the substrate and B is the metal to be deposited. A salt of B^+C^- is placed in solution. A voltage is applied across the two electrodes such that electrode A is negatively biased (the cathode) and electrode B is positively biased (the anode). In this situation the positively charged B^+ ions in solution are attracted to the cathode. On contact with the cathode an electron is transferred to reduce the ion and form a deposited metal B. At the cathode an electron is correspondingly removed to form a replacement B^+ ion. Replenishment of the electroplating bath has occurred and plating can continue until electrode B is fully dissolved.

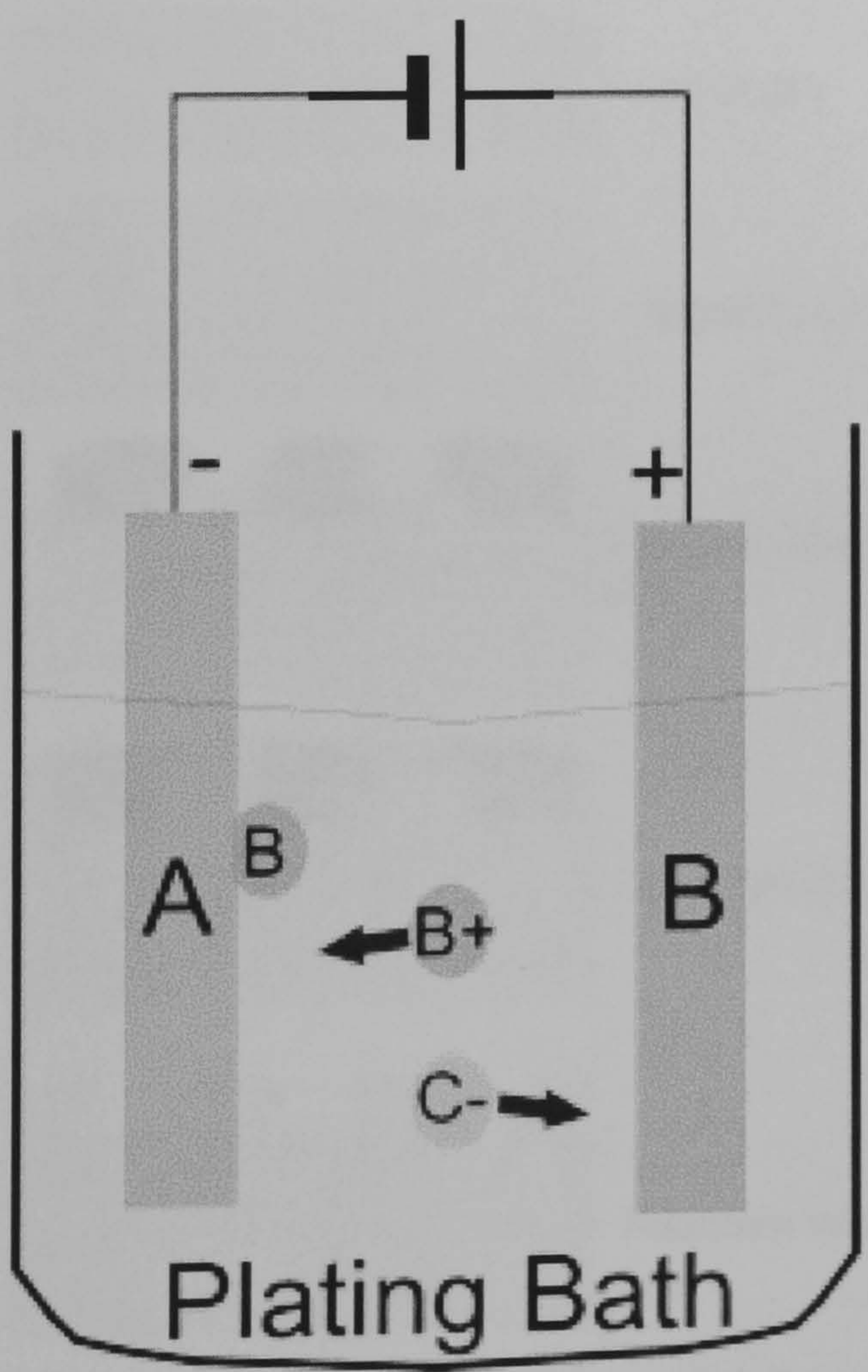


Fig. 4.6 A general two electrode electroplating cell.

Electroplating enables very low stress, and therefore thick, depositions to be performed. Nickel and gold electroplating are used for the devices in this thesis. The nickel electroplating follows the model presented in the previous paragraph. A nickel sulfamate bath [92] is used (400g/litre nickel sulfamate, 40g/litre boric acid, 1.5g/litre nickel chloride and 4g/litre sodium dodecyl sulphate). The bath needs to be maintained at between 50°C and 55°C to enable a low stress deposition.

The gold electroplating differs from the general model and is referred to as electroless. In electroless systems the gold plates out of the solution and no replenishment occurs from the anode. The plating bath is commercial Neutronex 309 [93] which is maintained at 40°C during deposition. The anode is platinum coated titanium.

Electroplating is particularly applicable to micromachining when plating occurs into a non-conductive mould, as illustrated in fig. 4.7. This is known as electroforming and enables thick metal structures to be formed on a substrate. Later chapters detail results from both gold and nickel electroplating.

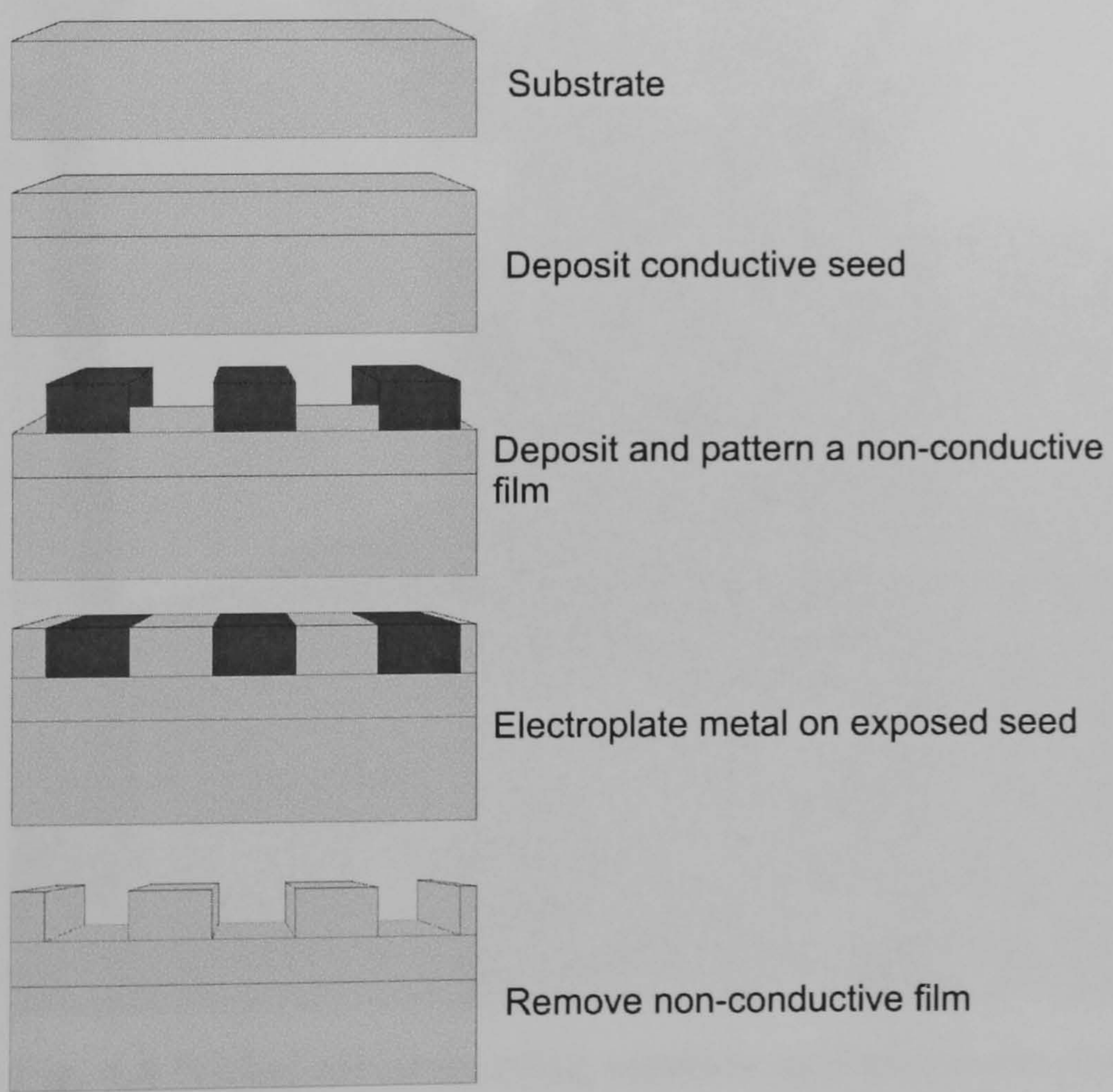


Fig. 4.7 Electroforming metal for surface micromachining

Fig 4.8 shows a photograph of the experimental set up for electroplating up to 2" wafers. A temperature controlled hotplate/stirrer is used to maintain the bath conditions during electroplating. Stirring is performed at 400rpm with a magnetic stirrer in the beaker. The nickel electrode (or platinum coated glass for gold electroplating) is held in place by a blue carrier. On the other blue carrier is the substrate to be electroplated. Crocodile clips are used to make electrical contacts to the electrodes. Photoresist is removed in these regions in advance of positioning the crocodile clips using a solvent such as acetone. A Keithley programmable current source is used for the electroplating.

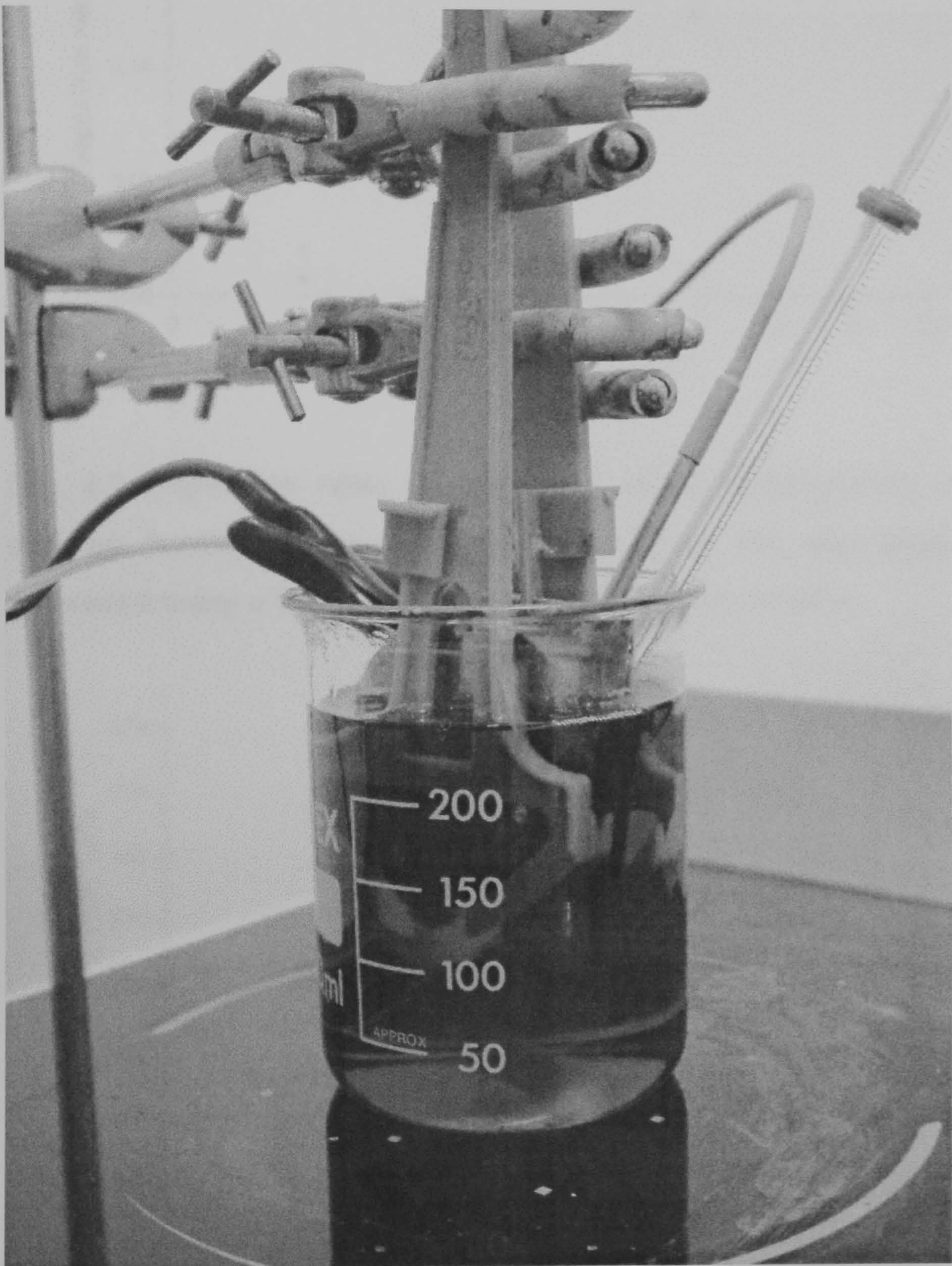


Fig. 4.8 Nickel electroplating solution and electrode setup.

Fig. 4.9 shows the deposition rates for gold and nickel electroplating. Higher current densities lead to increased rates. The surface roughness can also be determined by the current density as shown in fig. 4.10. Higher current densities lead to a faster deposition rate which, in turn, increases surface roughness.

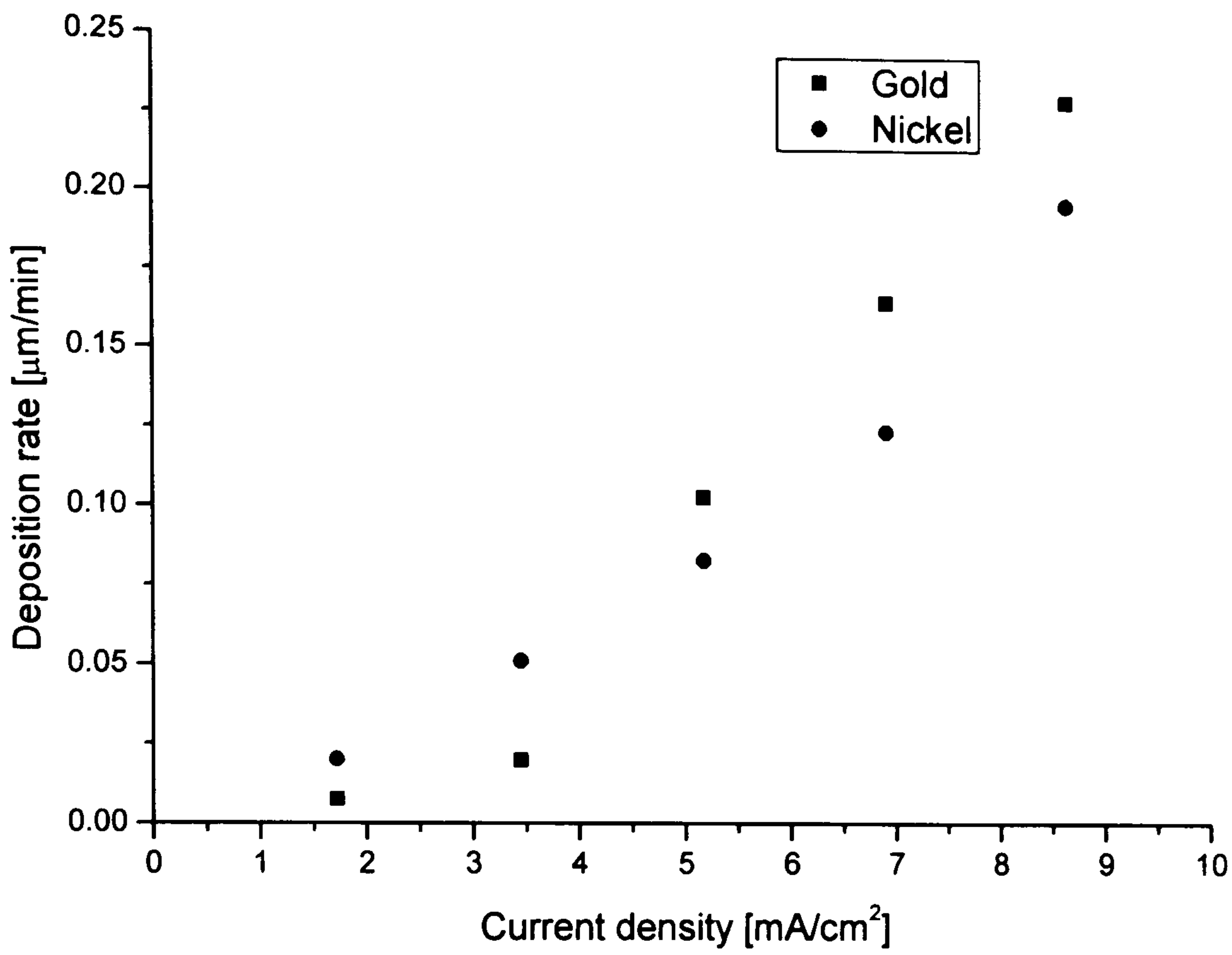


Fig. 4.9 Deposition rates for gold and nickel electroplating as a function of current density. These were calculated from the step heights which were measured using a Taylor-Hobson Talystep surface profiler.

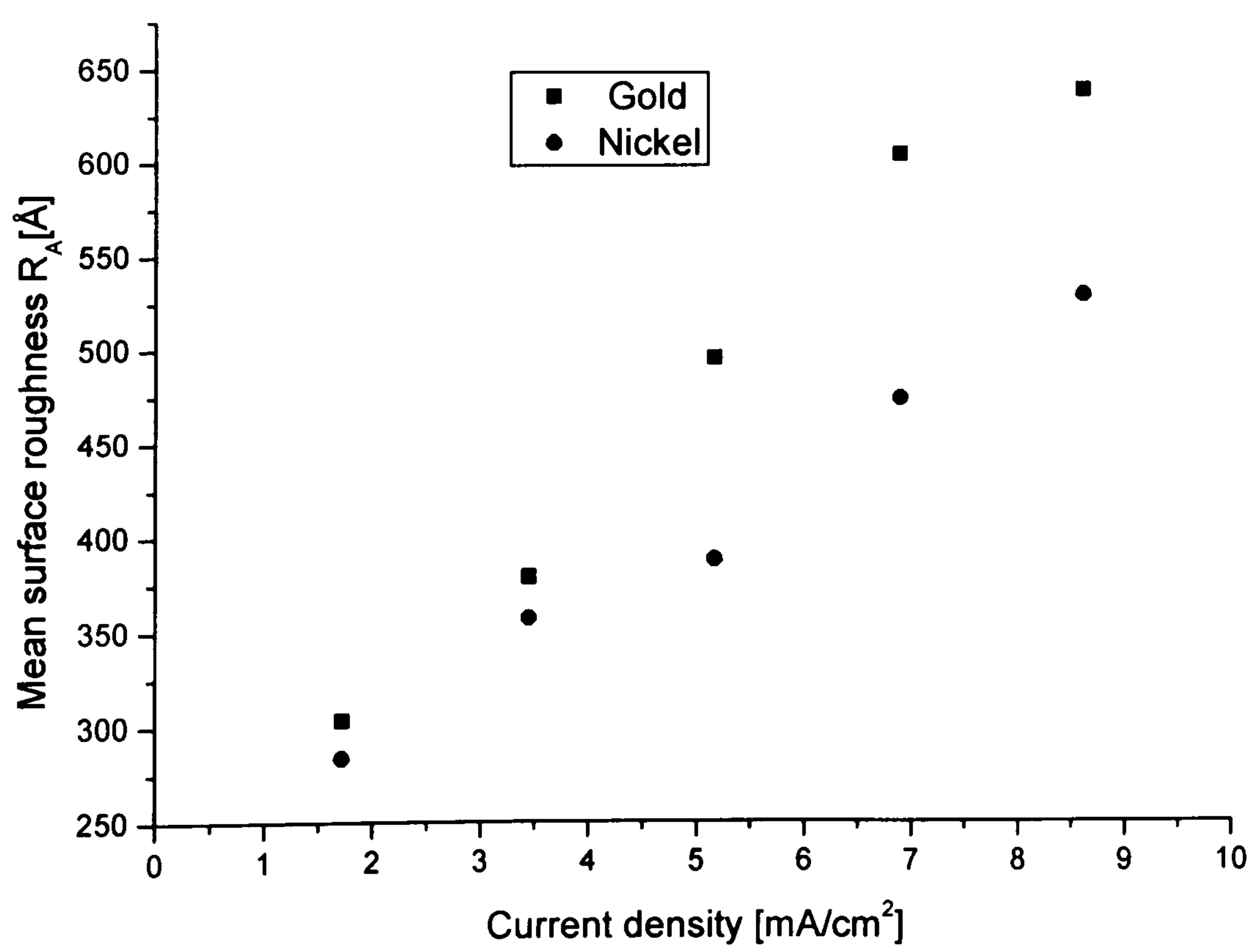


Fig. 4.10 Surface roughness as a function of current density for gold and nickel electroplating. This was measured using a Veeco Multimode AFM in contact mode.

4.3 Patterning of thin films

4.3.1 Mask design

Commercial e-beam or laser written masks typically cost several hundred pounds. They have a sub-micron resolution capability which is unnecessary for many MEMS applications. This section reports on the use of large format photography as an inexpensive alternative to commercially produced masks for feature sizes in excess of 20μm. The cost of a photoreduced mask is approximately £5.

Fig. 4.11 shows the experimental set up for mask fabrication. A large format Sinar camera is used. A printout of the mask on a transparent film is mounted onto a light box. A high resolution photographic glass plate is loaded into the camera and the image photographed. This reduces the light box image onto the photographic plate. Positive plates are used; therefore clear regions on the printout become dark on the plate and vice versa. The distance between the lens and the image determines the reduction factor.

Ultra high-resolution emulsions are available with grain sizes less than 0.03 μm. The grain size is not a limiting factor in the resolution of photoreduced masks. Vibration, focusing and contrast limit ultimate feature sizes. In order to reduce the effect of vibration and hence increase the maximum resolution the exposure times are minimised.

Exposure times can be minimised and contrast improved by illuminating the image to be photoreduced. Front illumination is difficult when good uniformity is required. Back illumination using a light box is a better alternative. Ordinary overhead transparency film limits the print resolution to 360 dpi. Special backlit film, supplied by ISCA Jet, enables the full resolution of a modern inkjet printer to be exploited.

Masks can be designed in CorelDraw. These are printed using an Epson 1290 super A3 printer which has a resolution of 2880 x 720 dpi. In practice, the minimum reliable feature size printable on this printer is 100μm.

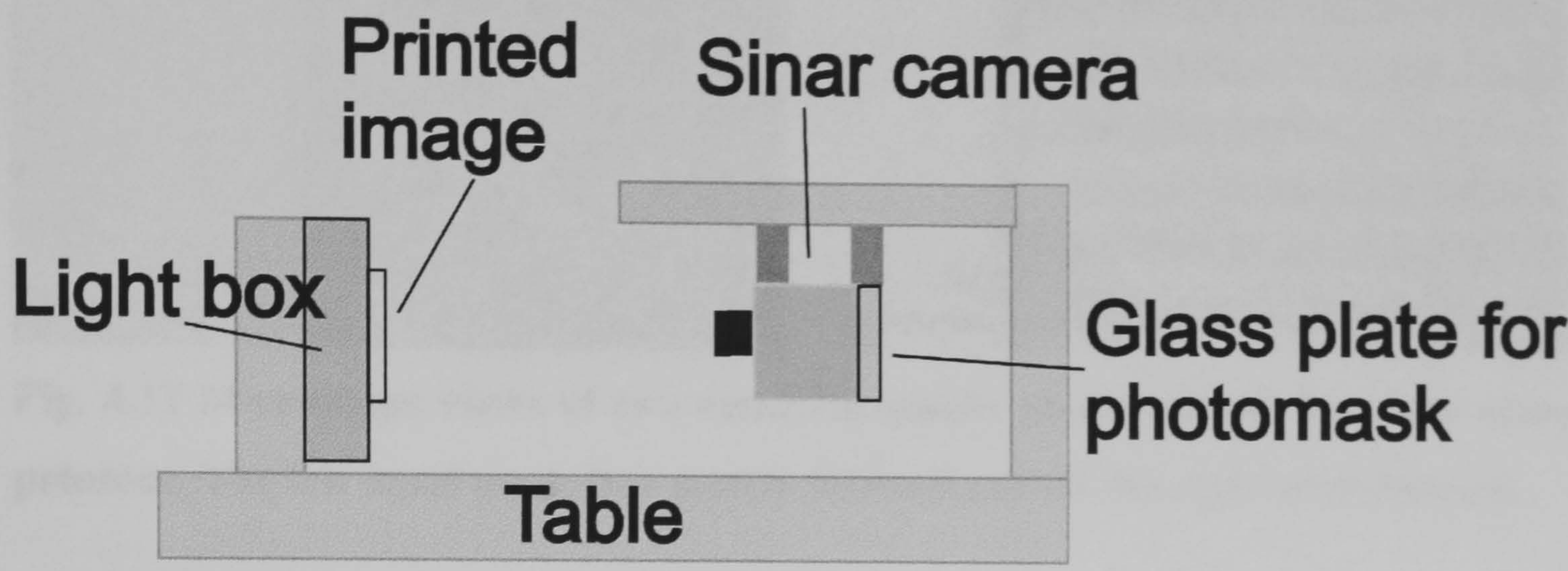


Fig. 4.11 Photoreduction set up for emulsion masks. The spacing between the lens and light box determines the reduction factor.

Apart from resolution, the photoreduced mask area needs to cover the wafer to be patterned. For the lens available on the Sinar camera a super A3 printout is required to provide good coverage of 2" wafers for up to 10 times reduction.

In principle a super A3 light box could be used to provide back illumination: however, this was found ineffective. At the end of the fluorescent tubes, the intensity of the light is reduced. This affects the film exposure and can alter the feature sizes. Instead an A2 light box is used and the printout mounted at the centre.

Focusing is performed at a wide aperture (F4.5) but the lens is stopped down (F16) during exposure. This increases the depth of focus and ensures that the features remain in focus. If the back plane of camera is not parallel to the light box then, although the lens can accommodate the focal differences, the effect is to alter the reduction factor across the mask. Fig. 4.12 shows microscope images of two photoreduced emulsion masks. The mask on the left was poorly focused and has poor contrast and feature definition. The mask on the right was well focused and the signicant improvement in feature definition for the 40μm interdigitated fingers is clearly seen.

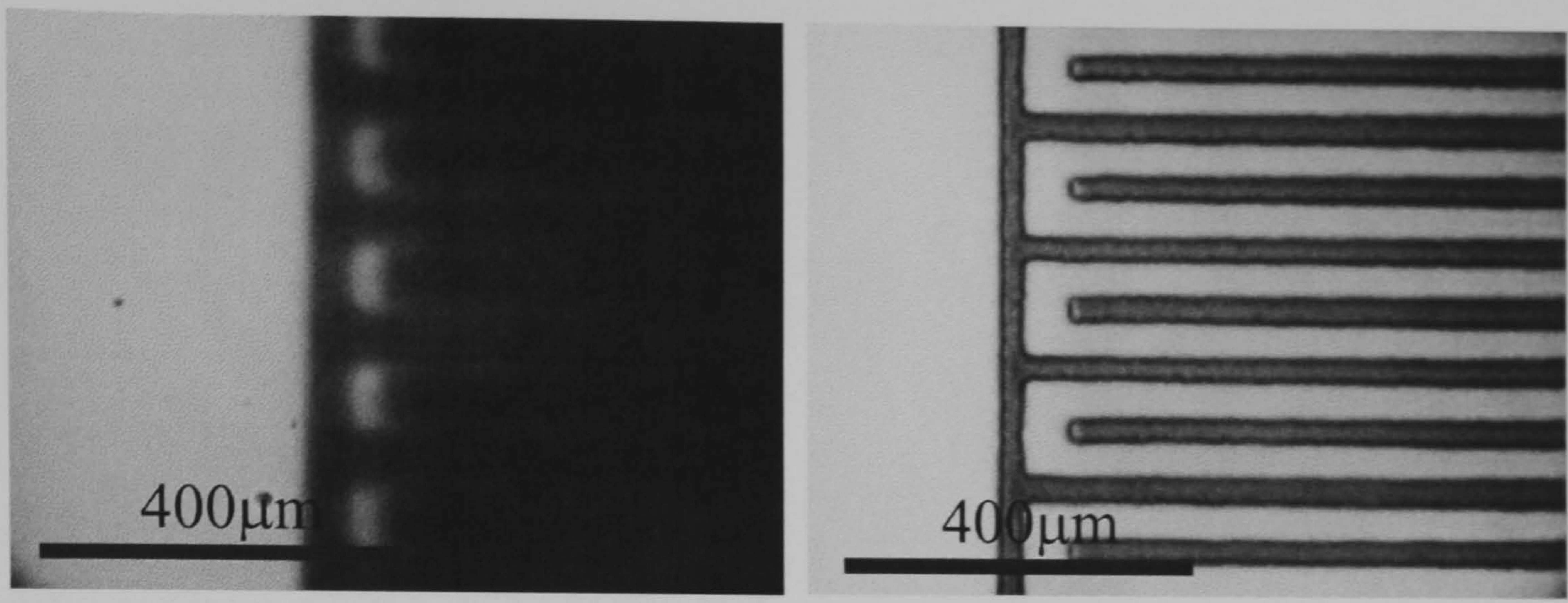


Fig. 4.12 Microscope views of two emulsion masks photoreduced from the same printout. The left hand mask was poorly focused and on the right well focused.

Originally 2.5" square Agfa millimask [94] green sensitive photographic plates were used for the mask fabrication. However, Slavich VRP-M plates [95] of the same size have been used as a replacement due to Agfa's discontinuation of plate film production in 2003. Table 4.1 shows the processing conditions for the photographic plates.

	Agfa millimask	Slavich VRP-M
Exposure	4.5 mins F16	4.5 mins F16
Development	4 mins 1:2 Developer	4 mins 1:5 Developer
Rinsing	DI water	DI water
Fixing	2 mins 1:5 Fixer	2 mins 1:5 Fixer

Table 4.1 Processing conditions for photoreduced masks (wet processing conditions obtained from manufacturer).

A reduction factor of between five and ten times can be used depending on the distance between the light box and the camera. Therefore to obtain a 20μm feature at ten times reduction, the printer needs to produce a 200μm line. Fig. 4.13 shows a 20μm photomask feature. The ripple on the edge of the emulsion regions emanates from the ripple on the printout.

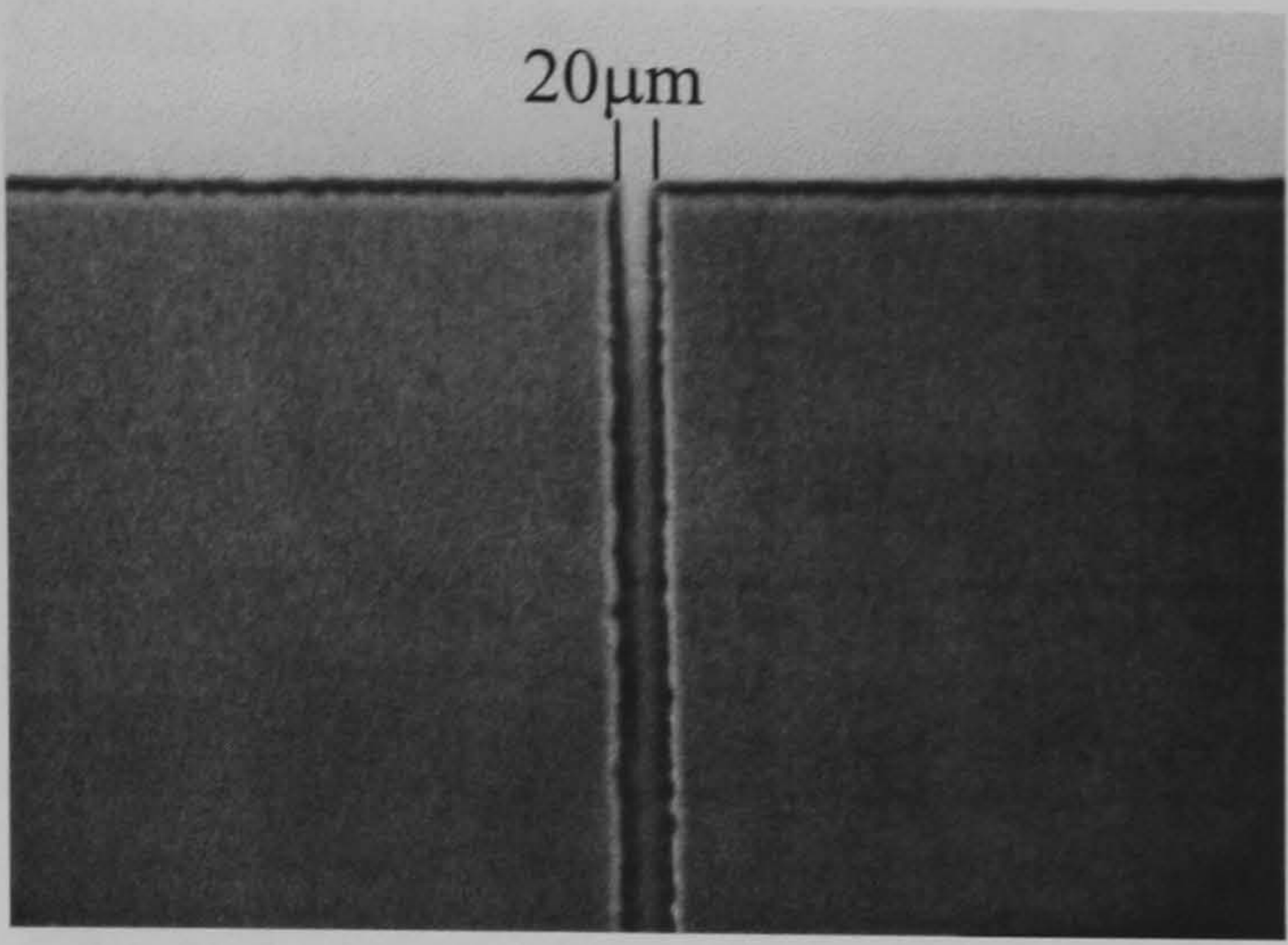


Fig. 4.13 Photograph of a 20μm feature on photoreduced emulsion masks.

An alternative process for larger feature sizes is direct printing which involves a contact print onto the photographic plate directly from the backlit film. This eliminates the reduction process and enables areas as large as the photographic plate to be exposed. However, feature sizes are determined by the printer and in the case of the Epson 1290 this is 100μm.

The 20μm minimum resolution reported for the photoreduction process refers to regular patterns, i.e. line-space-line. These are most susceptible to vibration because greying occurs and contrast is lost. The grey attenuates the UV exposed to the photoresist during photolithography and transfers a poor contrast image into the photoresist. When this occurs, the intended space/line ratio can be lost.

However, for well-spaced small features then vibration can be exploited to achieve sub 20μm results. Consider a black line on the printout surrounded by a clear region. On the photomask the line appears as a clear region surrounded by dark emulsion. If vibration occurs then the clear region, i.e. the line width, on the photomask will reduce in size. This has been exploited in chapter 6 to achieve 10μm etch holes.

4.3.2 Photolithography

Photolithography is integral to all microfabrication. At this stage the pattern is transferred from a mask to a photosensitive polymer, photoresist, on the substrate. Later stages can use the photoresist as a masking layer for etching patterns into thin films.

Contact photolithography is used at Durham with a Karl Suss MJB3 mask aligner. The contact process is illustrated in fig. 4.14. The photoresist is UV sensitive.

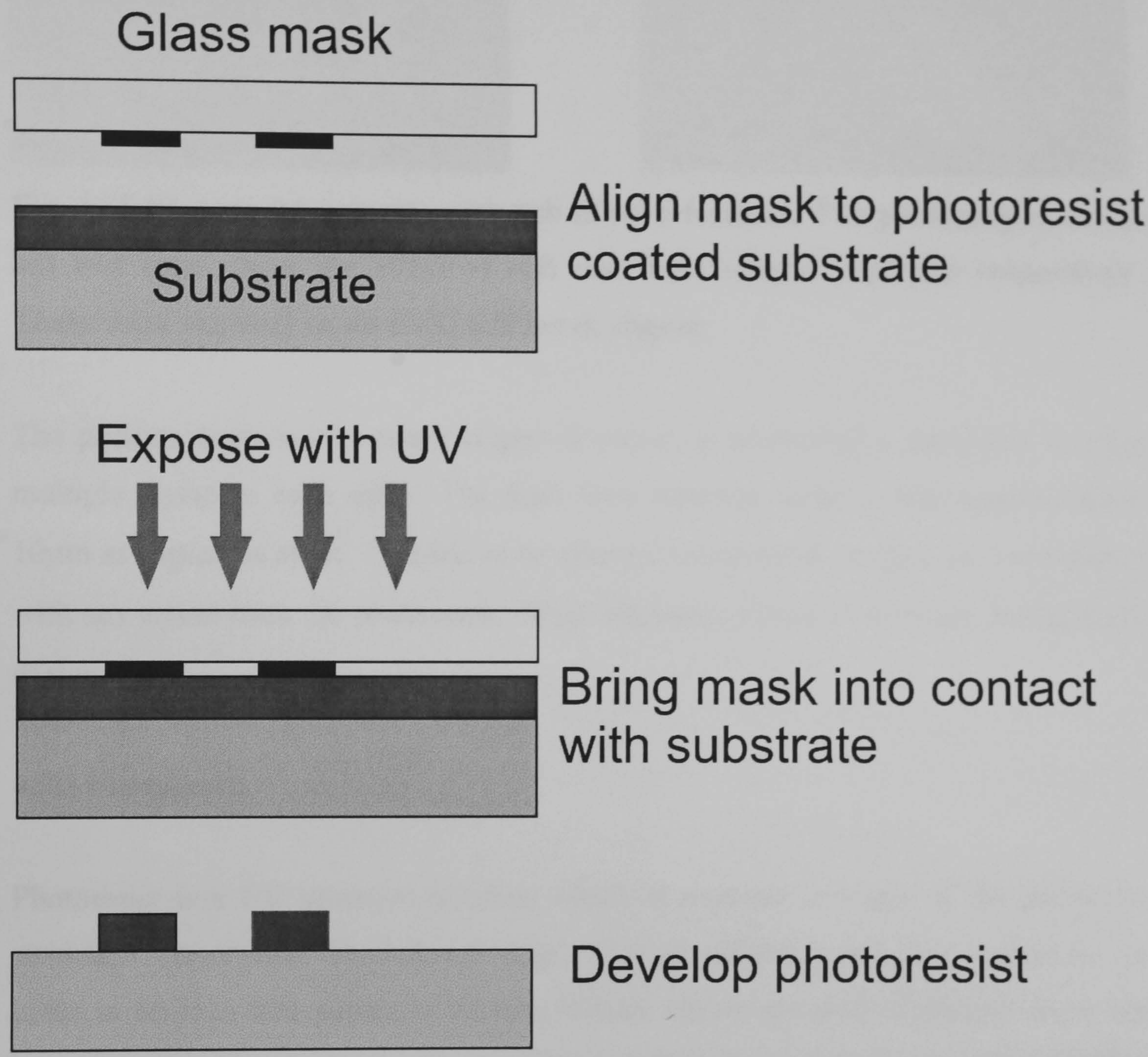
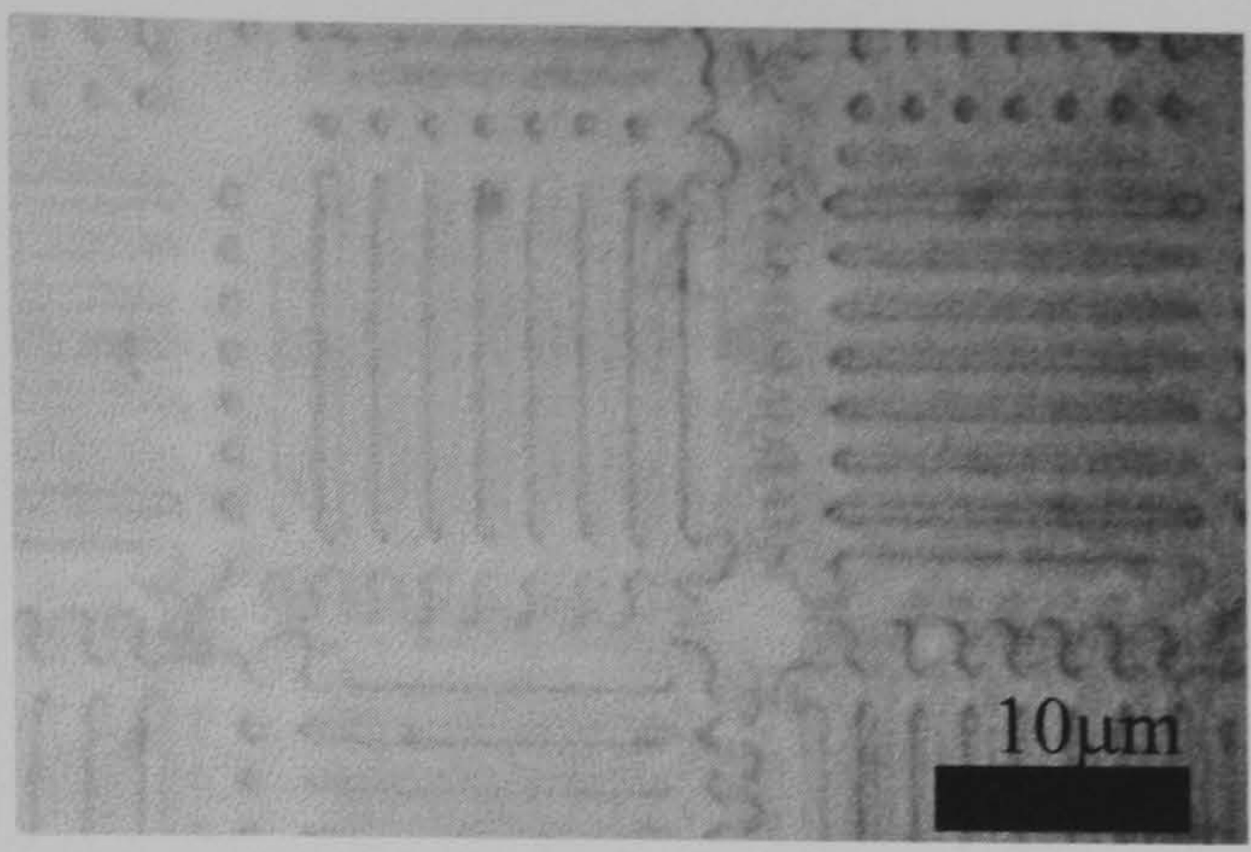


Fig. 4.14 Contact exposure for photolithographic patterning of a positive photoresist.

This is suitable for printing features over 0.7μm. For such small features though it is imperative that good contact is achieved between the substrate and the mask. Any gap can cause diffraction based interference which affects the photoresist pattern. This is illustrated in fig. 4.15 where two contact exposures into photoresist have been made. A commercially produced chrome mask has been used with lines of 0.7μm width. The first is using a soft contact where the substrate and mask are brought into physical contact. The second is using a hard contact mode where prior to contact a vacuum is pulled between the substrate and mask. In hard contact the interference patterns have been visibly reduced.



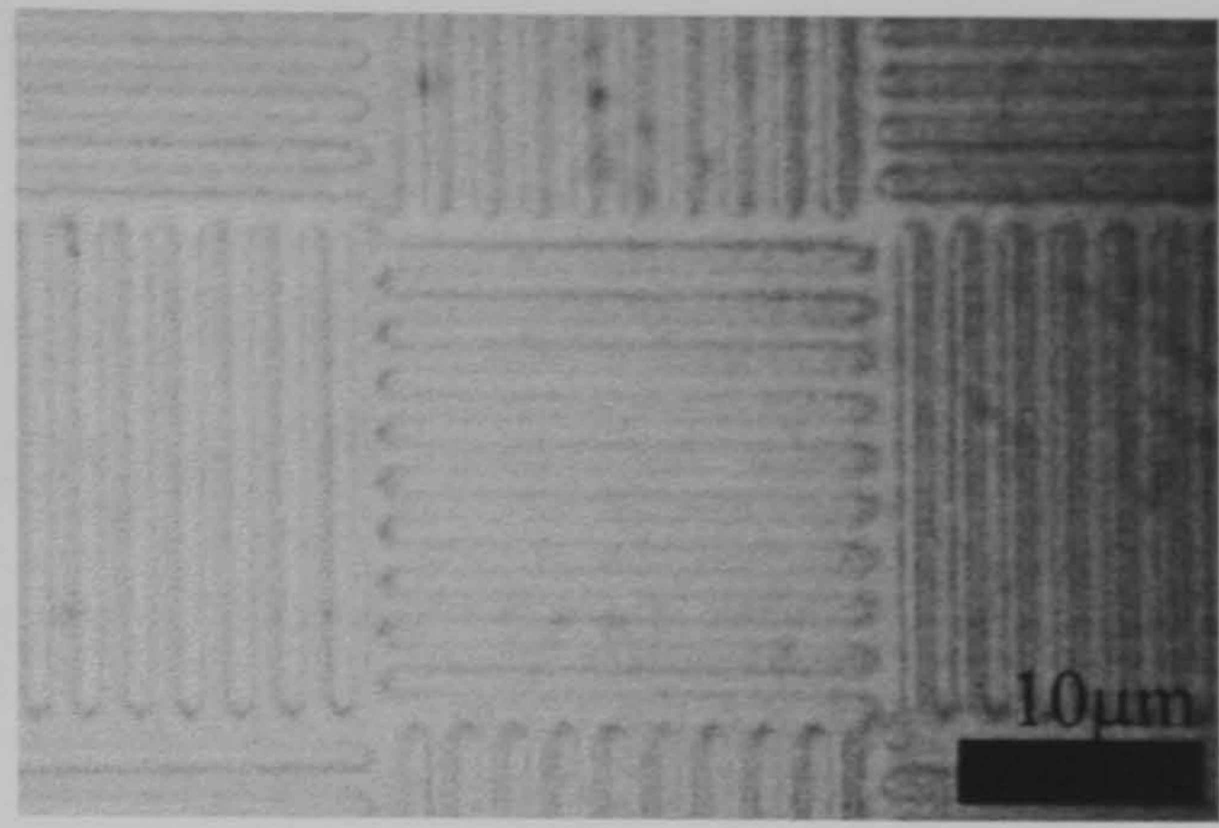


Fig. 4.15 Photoresist patterns with sub micron features. The photographs on the left and right show the effect of soft and hard contact exposure respectively. These were exposed on an EVG 620 mask aligner.

The primary purpose of a mask aligner however, is to provide a capability to align multiple layers to each other. The Karl Suss machine tends to slip approximately 10µm as contact is made. This has to be allowed for on mask designs. In combination with any errors from the photomask, 30µm allowances have to be made during mask design.

4.3.3 Photoresist

Photoresist is a UV sensitive polymer which is resistant to many of the chemicals used in IC processing. Thicknesses range from sub-micron to hundred of microns. In order to achieve fine pattern resolution thinner resists are used. Typically these are spun onto the substrate to provide a uniform coating. Spin-on resists are diluted with a solvent which must be baked off prior to exposure.

Positive resists are commonly used where the UV exposed regions are removed in developer and the unexposed regions remain on the substrate. The general considerations for a positive photoresist process are determined by the quality of the mask. With high contrast masks the photoresist should have a near vertical sidewall, which accurately represents the edge of the mask.

However, when exposing through a mask onto a reflective substrate back scattering of the UV causes side exposure. After development this causes the sidewall profile of the resist to deviate from the vertical.

4.3.4 S1813 & AZ4562 positive photoresist processing

S1813 and AZ4562 are both positive photoresists but differ in their thicknesses. The Shipley S1813 is 1.3μm thick when spun at 3700 rpm. The Clariant AZ4562 resist is 6.2μm at 3700 rpm. This thicker resist is well suited to act as a mould for electroforming [92, 96].

For standard processing of both resists, a pre-exposure soft bake of 2 minutes is performed on a 90°C vacuum hotplate. UV exposure times are longer for the thicker resist. Development is performed using a solution of one part sodium hydroxide based (AZ351B) developer to two parts of water.

In order to achieve additional chemical resistance, particularly on the S1813 resist which is used as an etch mask an additional bake at 120°C for up to 30 minutes may also be performed. This causes the resist to reflow. The reflow must be considered during surface micromachining. If the photoresist is to be used as a mould for electroforming, then the ideal vertical sidewalls of the resist and hence the formed pattern can be lost. This negates the advantages of using the thick resist.

After processing, these photoresists can be removed in acetone followed by an isopropyl alcohol (IPA) rinse and dry.

In some process flows the photoresist can be used a sacrificial layer and later metallisations may be deposited on top of the resist. If during deposition the temperature exceeds the soft bake temperature of the resist, then reflow can occur. This movement of a sub layer during deposition causes cracking of the deposited material.

If the photoresist remains after deposition and further layers need photolithographic patterning then reflow of the underlying resist can occur during soft bake of subsequent resists. This again can lead to cracking and device failure. In order to counter this, the underlying resist must be hard baked at a temperature which exceeds the highest temperature that the wafer will be exposed to during later processing.

4.4 Thin film etching

The photolithographic stage provides a substrate pattern using photoresist. In the etching stages this pattern is transferred to underlying materials. The etch technique depends on the material to be etched. Wet and dry etches are available.

4.4.1 Wet chemical etching

Wet etching relies upon a chemical attack of the underlying material. The etch chemistry is dependent on the material to be etched. In microfabrication it is desirable to be able to selectively etch a metal. Table 4.2 lists the wet etches for the materials used in this thesis.

Chromium etch	300g $K_3Fe(CN)_6$,150g NaOH in 1200 ml water.
Gold etch	$KI:I_2:H_20$ 4:1:8 by weight.
Nickel etch	10% conc. Nitric acid
Titanium etch	1:1 conc. HF:Ethanol
Oxide etch	10% conc. HF
Buffered oxide etch	$HF:NH_4OH$ 1:5 by volume.

Table 4.2 Wet etch recipes used in this thesis

The chromium etch is incompatible with positive photoresists. It is sodium hydroxide based and therefore acts as a developer. This incompatibility can be overcome by using an intermediate metal which has a photoresist compatible etchant. A layer of gold can be deposited on top of the chromium. First the gold is patterned, the photoresist is removed and then the chrome can be etched with the gold as a mask.

4.4.2 Dry etching

Dry plasma etching relies on the reactive nature of ionised gases such as oxygen. In a basic etcher, an RF plasma is formed between two electrodes. The substrate is placed on the grounded electrode. With a flow of gas through the system, reactive gas ions diffuse to the substrate and react to create a volatile product which is pumped away by the vacuum system. In this way the exposed substrate material is etched. This is generally isotropic.

To achieve anisotropy, a reactive ion etcher (RIE) is used. In an RIE the substrates are on a driven electrode which is much smaller than the ground electrode. This creates a DC bias which accelerates the ions towards the substrate. The lower pressure used in RIE also acts to make sure the incident ions impact normal to the substrate, increasing the degree of anisotropy of the etch.

4.5 Thin film thickness measurements

A Taylor-Hobson Talystep has been modified to measure the thickness of metals and photoresists. The modified Talystep directs its output to a computer via an analogue to digital converter (ADC) module. In keeping with the unmodified version, it can still be connected to a rectilinear chart recorder.

In operation, a stylus is either traversed across a groove in, or across the edge of, the deposit. A step in the vertical position of the stylus represents the height difference between the substrate and the deposit. The Talystep can perform a 2mm horizontal scan across a sample surface.

The device has been calibrated using grooves provided by Taylor-Hobson [97]. This is in accordance with the calibration technique for the rectilinear chart recorder. However, it has been noted that the output of the ADC is slightly temperature dependent. The temperature-regulated environment of a cleanroom eliminates this effect.

Fig. 4.16 shows an example output from the computer interfaced Talystep. The edge of an AZ4562 photoresist feature has been measured. The sharp drop in the ADC output curve shows the step height to be 7μm. The contact pressure of the tip can be reduced for soft material such as photoresists.

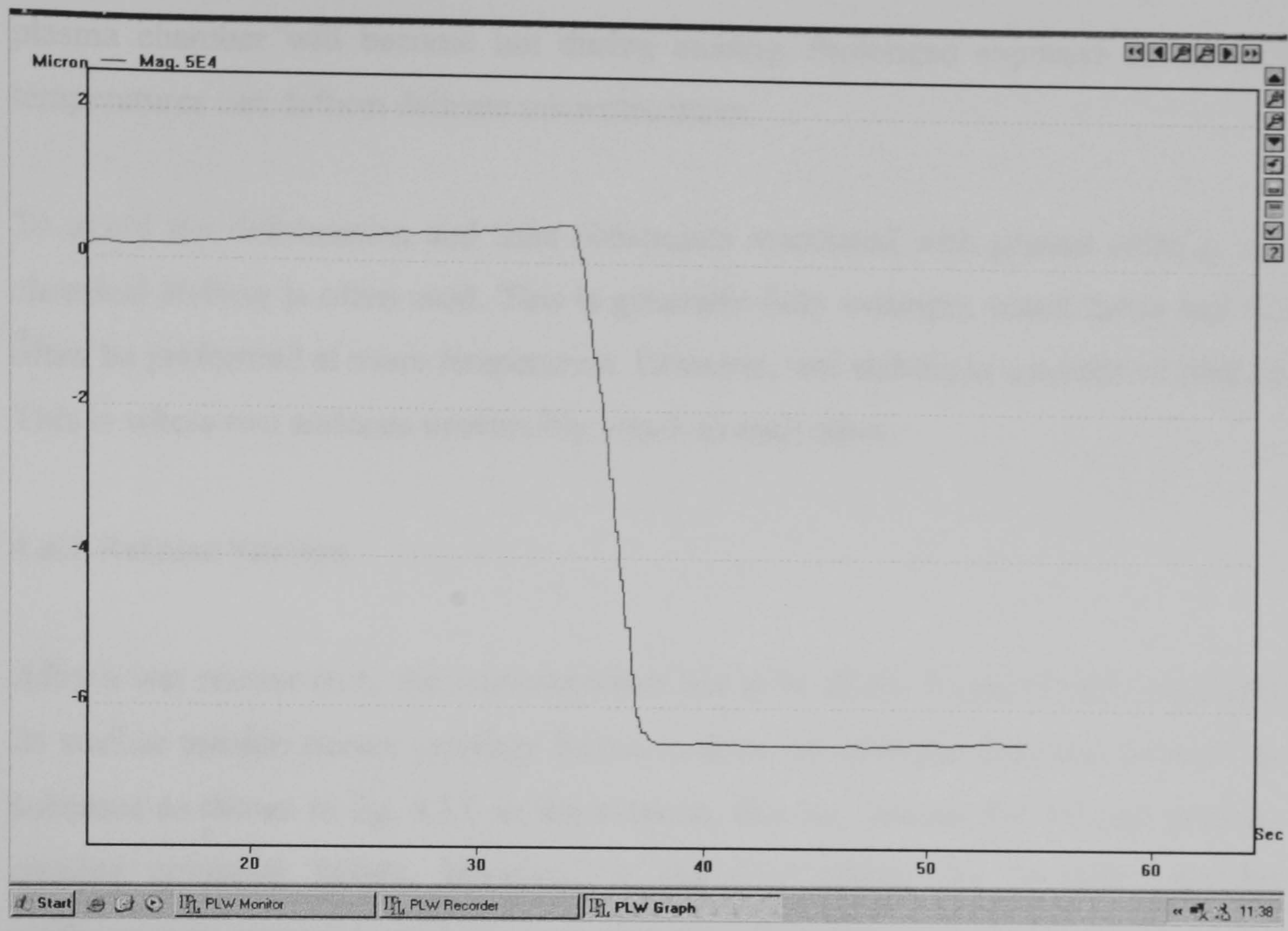


Fig. 4.16 The step height measurement of AZ4562 photoresist.

4.6 Sacrificial layer removal and stiction

This is the last stage in surface micromachining and is often the most challenging. The sacrificial layer has to be etched to leave a free standing microstructure. The etching can either be performed in wet conditions, such as in developer for photoresist, or in a dry plasma etcher.

An alternative to plasma etching for oxides is HF vapour phase etching which has been developed by Lee et al [98]. The associated dangers with this process have restricted its use. The advantage of the technique is that it avoids plasma damage and excessive substrate heating.

The disadvantage of dry plasma etching is that it is fairly slow, with etch rates typically less than a micron per minute. This is suitable for narrow cantilevers which may be only ten microns wide with a two micron air gap. However, larger structures can take many hours to release [99]. This is undesirable because the substrate and plasma chamber will become hot during etching. Prolonged exposure to elevated temperatures can deform delicate microstructures.

To avoid the deformation and time constraints associated with plasma etching, wet chemical etching is often used. This is generally fully isotropic, much faster and can often be performed at room temperature. However, wet etching is a source of stiction. This is where two surfaces irreversibly attach to each other.

4.6.1 Release Stiction

After a wet release etch, the microstructure has to be dried. As the liquid evaporates, its surface tension causes capillary forces to draw the movable structure towards the substrate as shown in fig. 4.17. In the extreme, this can fracture the delicate structure causing complete failure. However, it can also deform the movable structure sufficiently to cause it to make contact with the substrate.

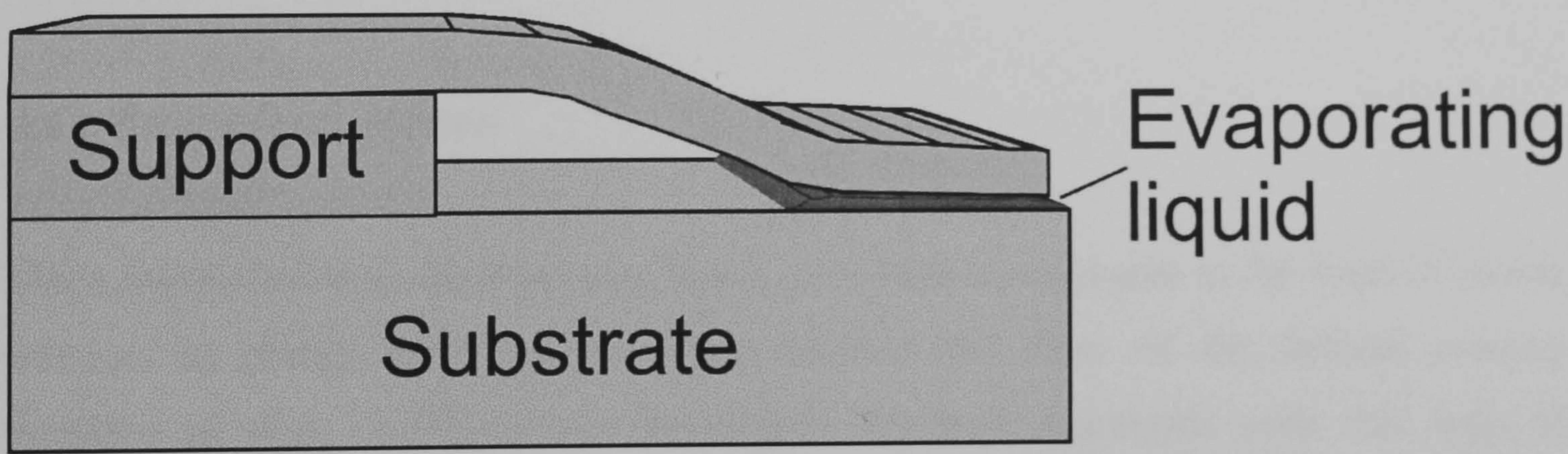


Fig. 4.17 Pull-down effect of evaporating liquid's concave meniscus.

When the liquid has completely evaporated, the structure can remain stuck to the substrate. This is known as release stiction [39, 100, 101]. It has been attributed variously to etch residues [102], residual stress gradients [103] and the condensation of water [104].

A wide range of techniques have been proposed to avoid stiction. These focus on removing or reducing the effect of surface tension [105]. Some groups have dried the structures from a liquid with a lower surface tension than water such as methanol or ethanol [106]. To further reduce the surface tension, the liquids have been heated.

In addition to the solvent rinse, supercritical carbon dioxide drying ($SCCO_2$) has been used [107]. To release microstructures, the rinse solvent has to be completely displaced by liquid CO_2. After this, the CO_2 is taken above its critical point and slowly released from the system. Therefore, the microstructure can be released without surface tension and the associated stiction.

Other techniques have been published, for example freeze - drying, in which the final etch rinse is frozen. It is then placed in a vacuum and sublimed directly from a solid to a gas avoiding the liquid state [92].

More exotic techniques such as hyperbranched polymers (HBP) have been proposed as another solution to stiction. The special characteristic of this type of polymer is that it does not exhibit a liquid phase. Suh et al [108] used spin on, solvent diluted, HBPs as sacrificial layers. Heating to 600°C in an oxygen atmosphere sublimes the sacrificial layer. However temperature related deformation of the microstructures was observed.

4.6.2 Post-release stiction

Once release stiction has been countered, the problem reappears in the form of in-use stiction. In humid environments water droplets can form on the devices causing surfaces to stick. Additionally, the micron spacings associated with this type of structure cause atomic attraction, in the form of Van der Waals forces [100], to become significant.

Regardless of the cause of post-release stiction, solutions have focused on coating the electrodes to form anti-stiction surfaces [41, 109-113] prior to release. If a coating is unsuitable, then the effect of stiction can be reduced by increasing surface roughness, to reduce contact area or using dimpled bump stops. As final solution some groups have worked on techniques for releasing stiction failed structures [114].

The devices fabricated in this thesis use a combination of high temperature solvent release alongside surface roughening to reduce stiction. This is detailed in the next chapter.

4.7 Chapter summary

- An important feature of surface micromachined devices is that they use the substrate primarily as a physical support rather than as an active mechanical element. Therefore the process flow can be made substrate independent.

- RF MEMS devices are not likely to succeed as stand-alone devices. Their integration into existing circuitry is a primary benefit and accordingly the devices developed for this thesis have aimed to use the most flexible process flow.

- Evaporated films are suitable when dense high quality uniform depositions are required. The films tend to exhibit a higher stress when compared to lower temperature techniques. This significantly limits the deposition thickness.

- Sputtering, an alternative to evaporation, is a low temperature technique which enables lower stress and hence thicker films to be deposited.

- Electroplating is particularly applicable to micromachining when plating occurs into a non-conductive mould. This is known as electroforming.

- Gold and nickel electroplating have been used throughout this thesis. Electroplated films can be near zero stress and enable films of tens of microns to be deposited. In electroplating, surface roughness can be determined by altering the current density.

- Commercial e-beam or laser written masks typically cost several hundred pounds. They have a sub-micron resolution capability which is unnecessary for many MEMS applications. Low cost photoreduction techniques have been used for this thesis. They are suitable for features as small as 20μm.

- Photolithography is integral to all microfabrication. At this stage the pattern is transferred from a mask to a photosensitive polymer, photoresist, on the substrate. Contact photolithography is used at Durham with a Karl Suss MJB3 mask aligner.

- S1813 and AZ4562 are both positive photoresists but differ in their thicknesses. The Shipley S1813 is 1.3μm thick when spun at 3700 rpm. The Clariant AZ4562 resist is 6.2μm at 3700 rpm. This thicker resist is well suited to act as a mould for electroforming.

- Wet etching relies upon a chemical attack of the underlying material. The etch chemistry is dependent on the material to be etched. In microfabrication it is desirable to be able to selectively etch a metal.

- The sacrificial layer has to be etched to leave a free standing microstructure. The etching can either be performed in wet conditions, such as in developer for photoresist, or in a dry plasma etcher.

- Stiction failure can occur after a wet release etch as the microstructure is dried. As the liquid evaporates, its surface tension causes capillary forces to draw the movable structure towards the substrate. A wide range of techniques have been proposed to avoid stiction. These focus on removing or reducing the effect of surface tension.

Chapter 5

Sacrificial layers for micromachined capacitors

CMOS designers can use standard cell libraries and processes for microelectronics fabrication. These standard processes do not exist for micromachining to the same degree. In many micromachining cases, standardisation would compromise performance for a particular device. Consequently, MEMS devices in the literature have been fabricated using a variety of techniques.

This lack of standardisation is a major issue when a new device process flow has to be developed. For surface micromachining, the choice of structural materials, sacrificial layer and substrate has to be carefully selected to obtain the desired device characteristics.

For the tunable capacitors and fixed inductors presented in this thesis, a key factor was that they would be compatible with a GaAs MMIC process flow for ultimate commercialisation. This significantly reduces available metallisation options and sacrificial layers.

A crucial feature of surface micromachined devices is the sacrificial layer. In order to achieve a wide tuning range in the capacitors presented in chapter 3, the upper electrode has to be biased to a near contact state with the lower electrode. Any residual etch residue in this air gap could impede the performance. Therefore the sacrificial layer must be cleanly etchable and provide a well-defined air gap.

This chapter focuses on the processing of two types of sacrificial layer which were potentially suitable for the widely tunable capacitor fabrication. Firstly, an organic sacrificial layer – photoresist – is presented. The appeal of spin-on organic layers includes a wide range of deposition thicknesses, good planarisation and low temperature wet etching.

The results, however, show commercially available photoresists were found to be inappropriate to form the capacitive gap due to residual deposits remaining after etch. In chapter 7, photoresist is used to form a thick interconnect to improve the RF performance of the capacitors and for suspending high Q inductors.

The second sacrificial layer presented in this chapter is titanium. It is readily deposited using either evaporation or sputtering and is etched using HF based solutions. This is advantageous because the Filtronic compatible metallisations of electroplated nickel and gold are resistant to HF. Titanium was found to be suitable for producing well defined clean air gaps in tunable capacitor structures.

5.1 Photoresist as a sacrificial layer

Commercial photoresist has been reported in the literature as an organic sacrificial layer [13, 83, 96]. Standard positive resists can usually be etched using solvents such as acetone, and alkaline solutions such as developer or aqueous sodium hydroxide.

An important feature of photoresist is that is photodefinable using standard lithographic techniques and by its nature it can be selectively etched away from standard structural materials used in MEMS.

In order to examine the possibility of using photoresist as a sacrificial layer a series of test structures had to be developed which would be comparable to those found in RF

MEMS, but at the same time be extremely basic to ensure a minimal number of process variables.

5.1.1 Micromachined test structures

Fig. 5.1 shows a side view of the fabrication process for the structures, which included membranes with sides of 250 μm, 500 μm and 1000 μm. 35 μm etch holes were used with a 35 μm pitch. A range of cantilevers with lengths up to 1000 μm and a width of 60 μm were also included. For these simplified devices some photoresist has to remain in the structure after release to act as a support. Therefore, the sacrificial layer etch is only partial.

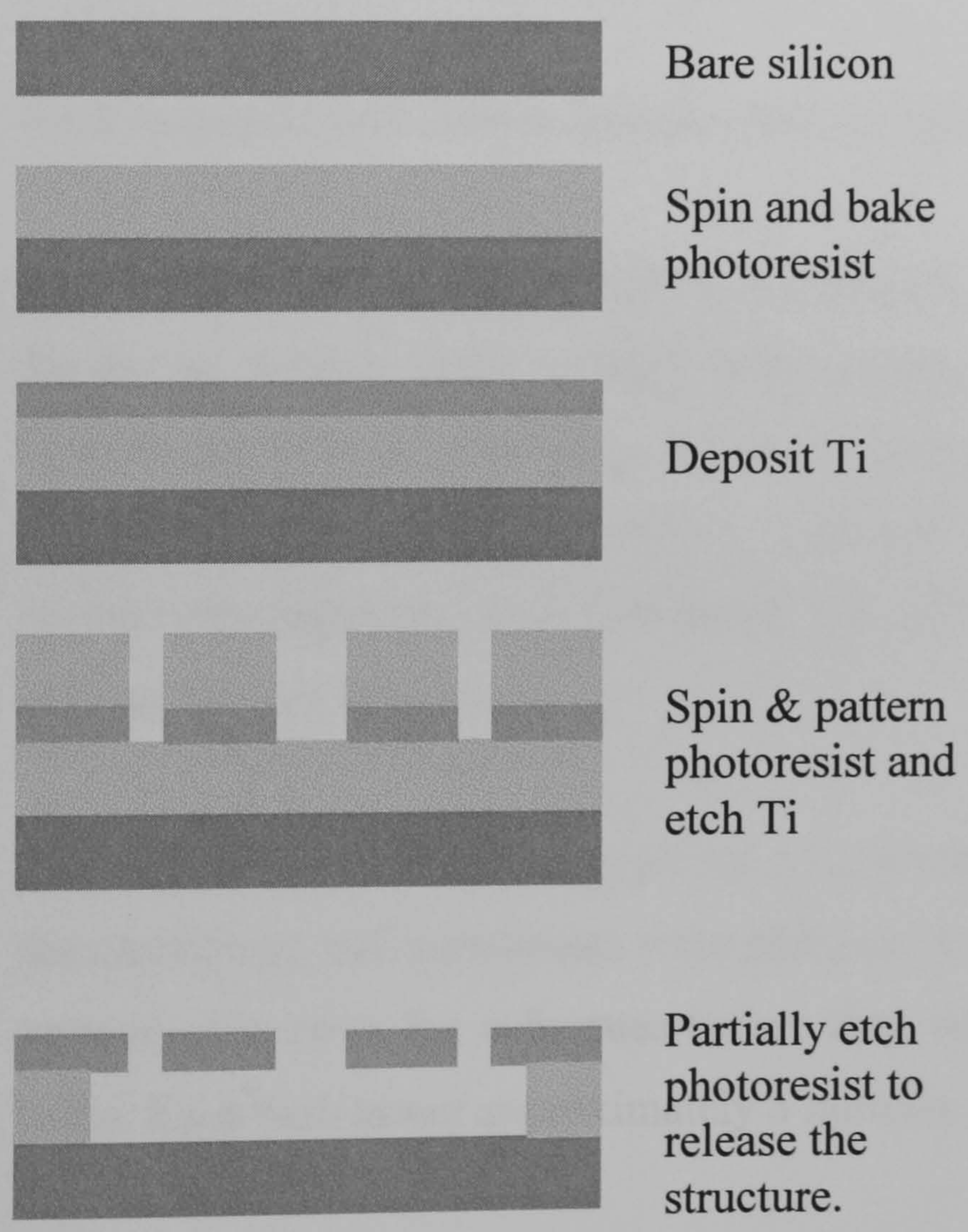


Fig. 5.1 The fabrication process flow for photoresist supported test membranes and cantilevers.

On a cleaned, degreased silicon wafer, a single layer of S1813 (1.3 μm thick after soft baking) was spun and soft baked at 80°C for 10 minutes, followed by a hard bake at

120°C for 20 minutes on a hotplate. 0.5 μm of titanium was sputtered onto the photoresist.

After sputtering, another layer of S1813 was spun onto the titanium, exposed with the test mask for 5 seconds and developed in 1:2 water:AZ351B developer for 30 seconds. The titanium was etched using a 50:50 solution of HF:ethanol at room temperature. This etch was found to produce rapid, clean etches without attacking the photoresist. Usually 10% HF is used [115], but it lifted off the cantilevers from the sacrificial photoresist due to excessive gas production.

Regardless of the choice of sacrificial layer, all wet etched devices are susceptible to stiction failure. Therefore in parallel to the identification of a suitable sacrificial layer, a suitable release mechanism had to be identified.

5.1.2 Supercritical carbon dioxide drying release

Supercritical carbon dioxide drying is a process regularly used in biological sciences for drying delicate tissue samples without causing surface tension damage. It is also suitable for MEMS processing: however, biological process chambers are generally too small to handle complete wafers. Consequently, prior to release, the wafers were scribed into segments of approximately 1cm by 2cm. The mask had been designed to account for this segmentation.

The scribed wafer pieces were placed in concentrated developer for 6-8 minutes until the cantilevers and membranes were observed to release. Three deionised water baths were used to rinse the substrates before they were transferred to a further three IPA baths. Each bath lasted approximately 5 minutes.

Traditionally, ethanol is used in $SCCO_2$ drying [107] but this was found to strip standard hard baked photoresist. The samples were placed into the critical point dryer (CPD) and liquid CO_2 was flushed through the system to substitute the IPA. After an hour of soaking in liquid CO_2, the system was reflushed and replenished with fresh liquid CO_2.

After replenishment, the dryer was heated and the liquid CO_2 taken to its critical point. The supercritical fluid was slowly bled from the dryer and the samples were removed. It is essential that the IPA is completely substituted as the solvent/supercritical fluid combination is extremely powerful at stripping organics, such as photoresist.

Fig. 5.2 shows a SEM image of the cantilever structures. Many of the cantilevers can be seen, in part, to be free from the substrate. This is a partial success as direct water drying was found to leave no free structures. The underlying reason behind the deformation of the cantilevers and the residue observed between the cantilevers will be explained in a later section.

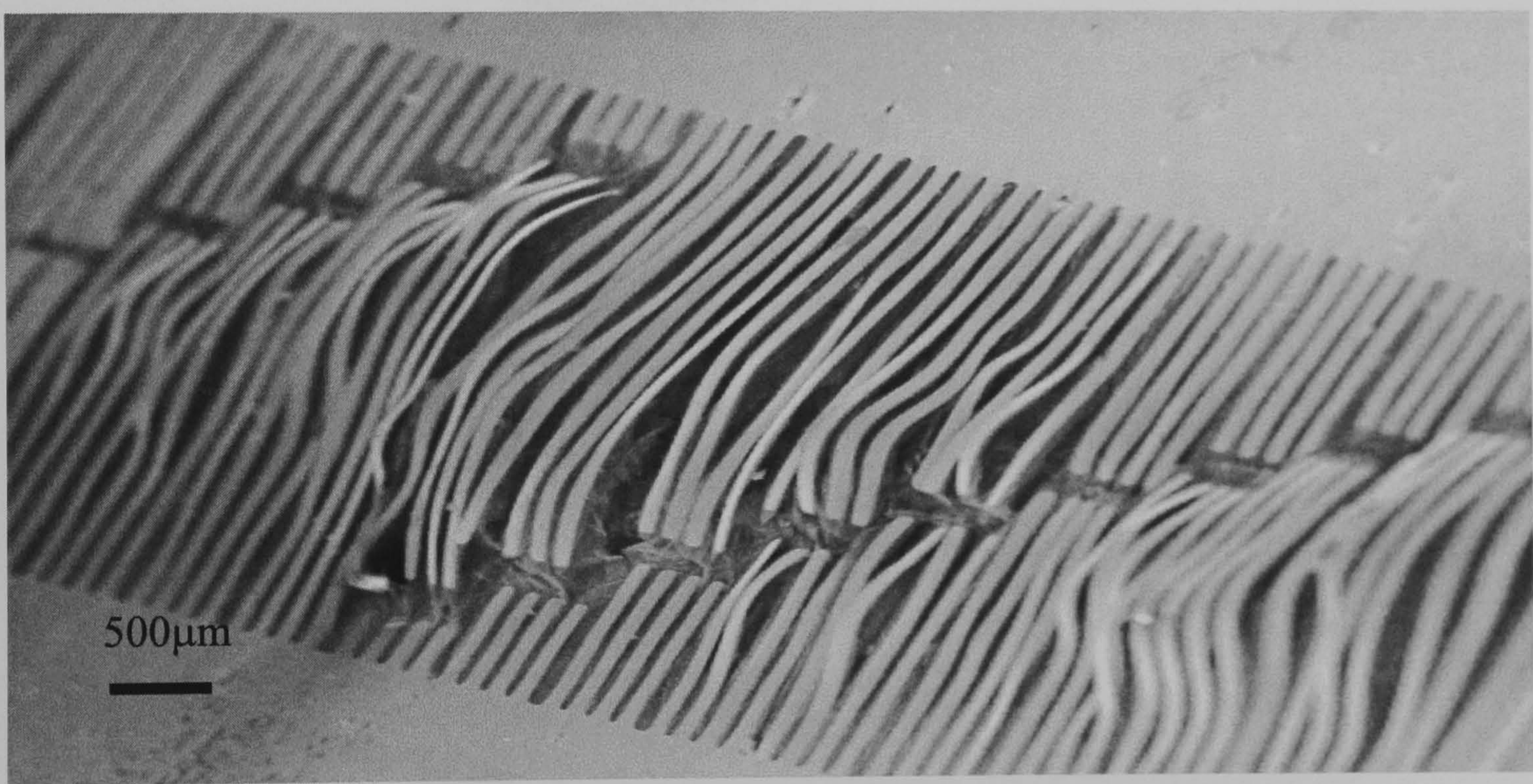


Fig. 5.2 Released titanium cantilevers after critical point drying.

Fig. 5.3 shows a SEM image of the etch holes on a released membrane. An air gap can clearly be seen under the central etch hole. This shows structural release. However, a key feature is the substance that fills and elevates out of the left hole in the image and appears to have collapsed in the central hole. At lower magnifications, as shown in fig. 5.4, this effect can be observed in many of the etch holes.

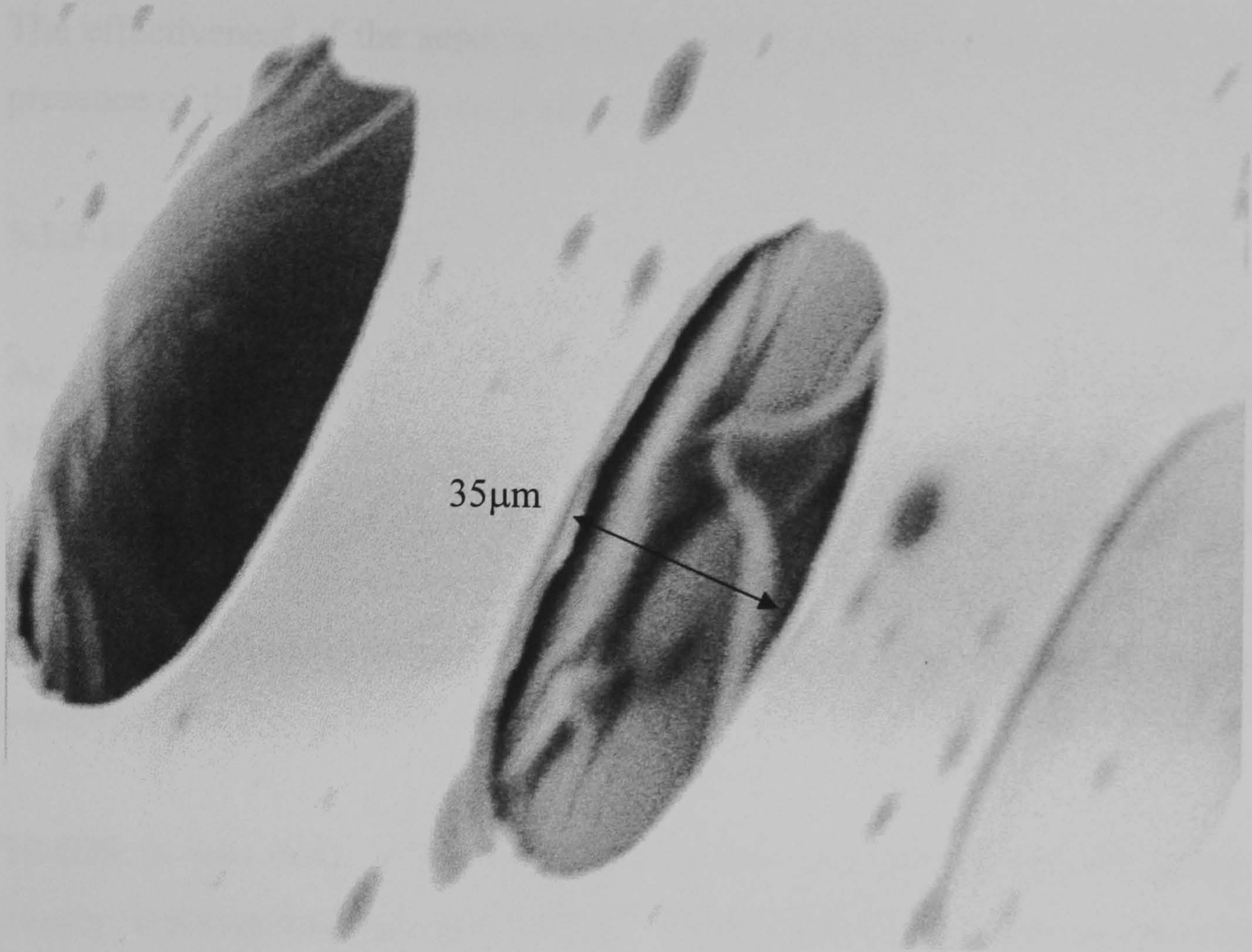


Fig. 5.3 Released titanium membrane after critical point drying.

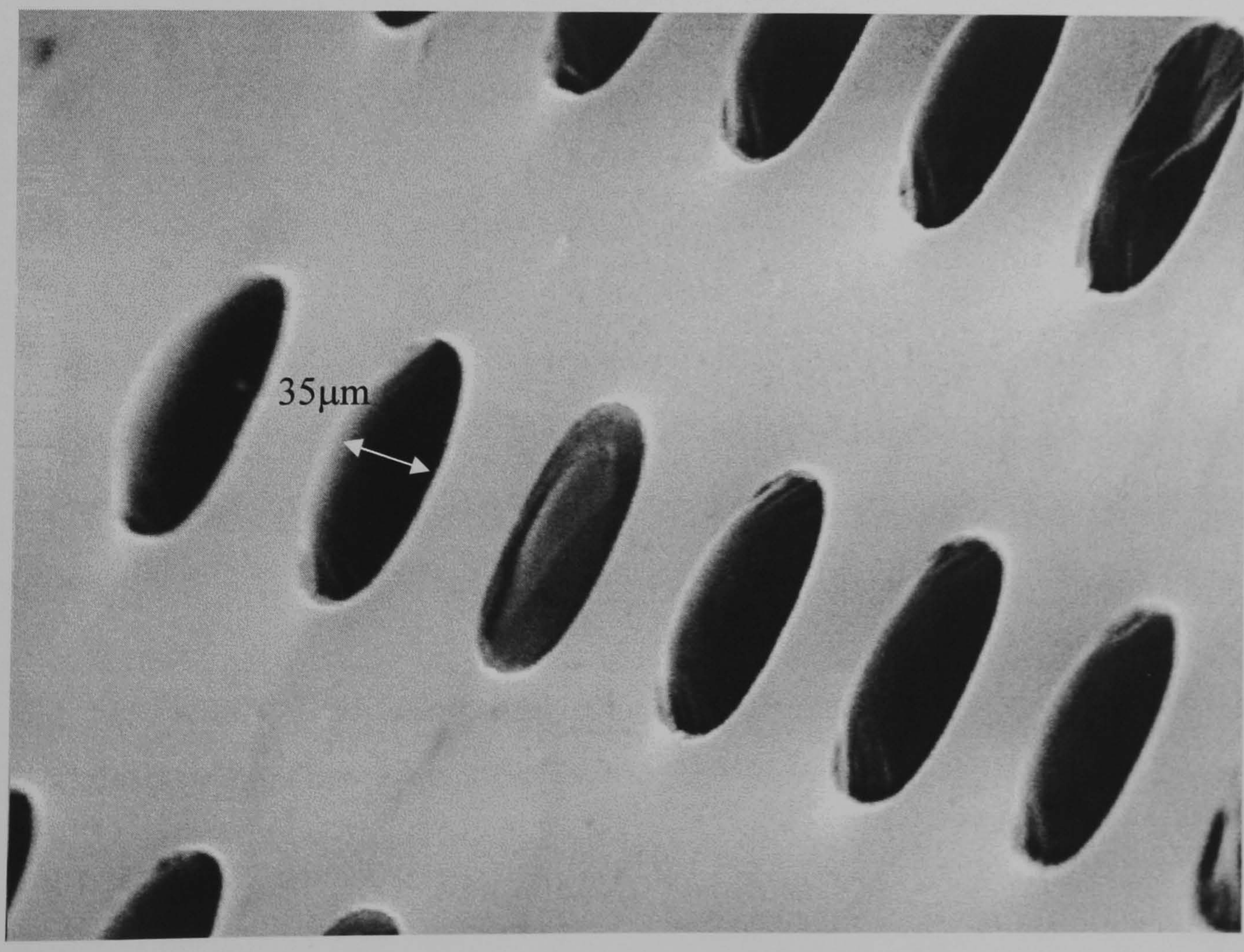


Fig. 5.4 Released titanium membrane showing unusual etch hole features after critical point drying

The effectiveness of the supercritical CO_2 drying appears to be uncertain due to the presence of this residue on the wafers.

5.1.3 HMDS drying

An alternative to supercritical CO_2 drying in biological sciences is a process known as HMDS, hexamethyldisilazane, drying [116]. HMDS has a surface tension of 18.2 dynes/cm compared to 23 dynes/cm for IPA [106], both at room temperature. The biological procedure starts with the sample in an ethanol bath. The ethanol is replaced by HMDS in a series of baths. After the ethanol has been completely displaced, the sample is allowed to air dry.

HMDS is also used in the semiconductor industry as a photoresist primer [117]. Firstly, it dehydrates the wafer surface. The elimination of surface moisture improves the adhesion and spinning properties of photoresist. Furthermore, it reacts with surface oxides to form a strong bond terminated in a methyl group. The methyl group bonds well to photoresists.

HMDS is therefore a photoresist compatible, low surface tension liquid used in the biological sciences as an alternative to $SCCO_2$ drying. These features indicate its suitability for MEMS sacrificial photoresist release.

Titanium test structures were prepared as for the $SCCO_2$ trial. After the IPA rinse, the wafer segments were placed in three baths of fresh HMDS each for about 10 minutes. Following the final bath, the wafers segments were removed and placed on a glass plate, and left at room temperature to dry.

Fig. 5.5 shows a SEM image from the end of a cantilever, after HMDS release. There is a clear air gap: however, the cantilever appears to have stuck on one side. Fig. 5.6 shows a SEM of a severed membrane. Again, the air gap is particularly clear.

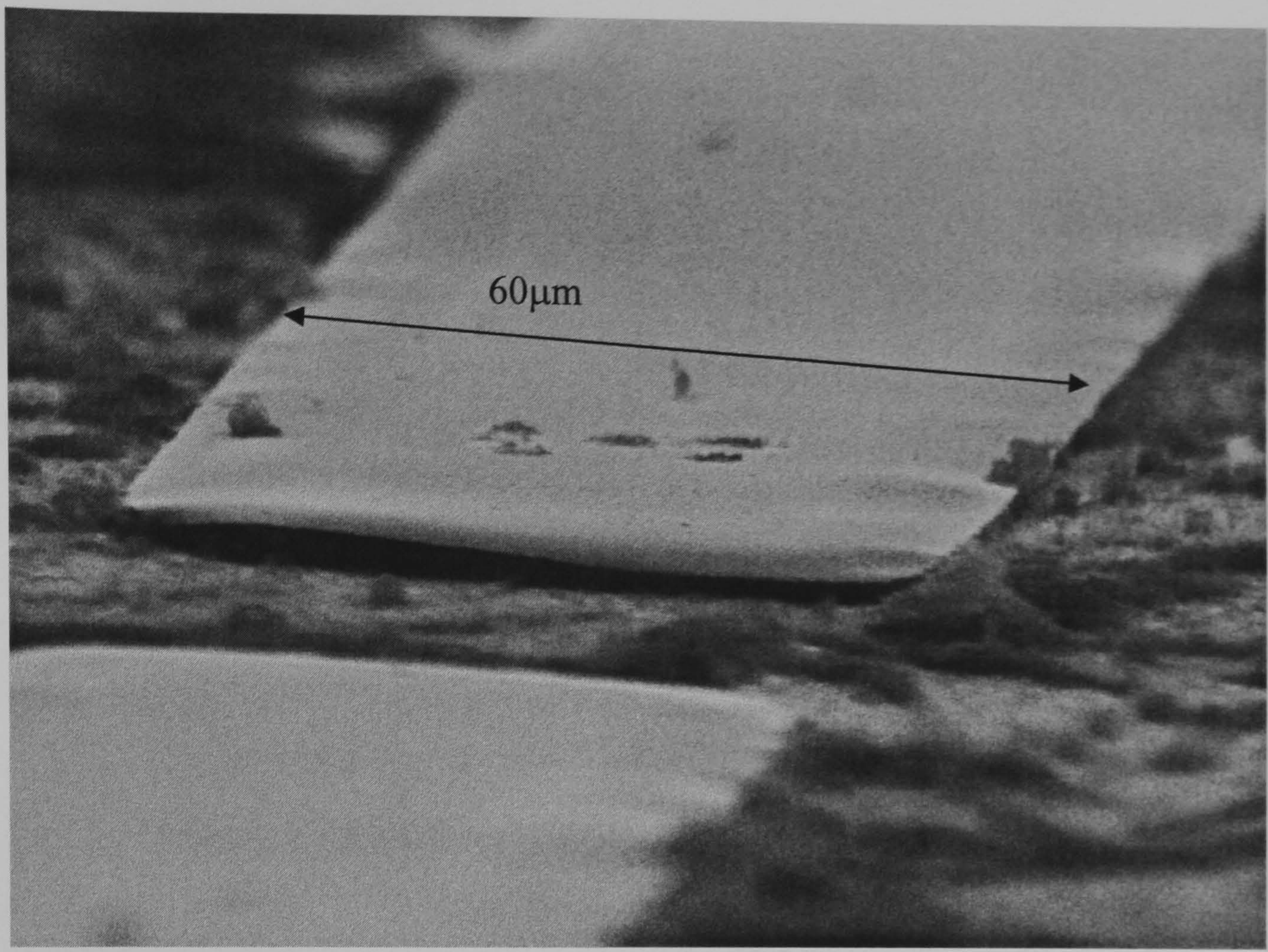


Fig. 5.5 SEM image of the end of a Ti cantilever after HMDS release

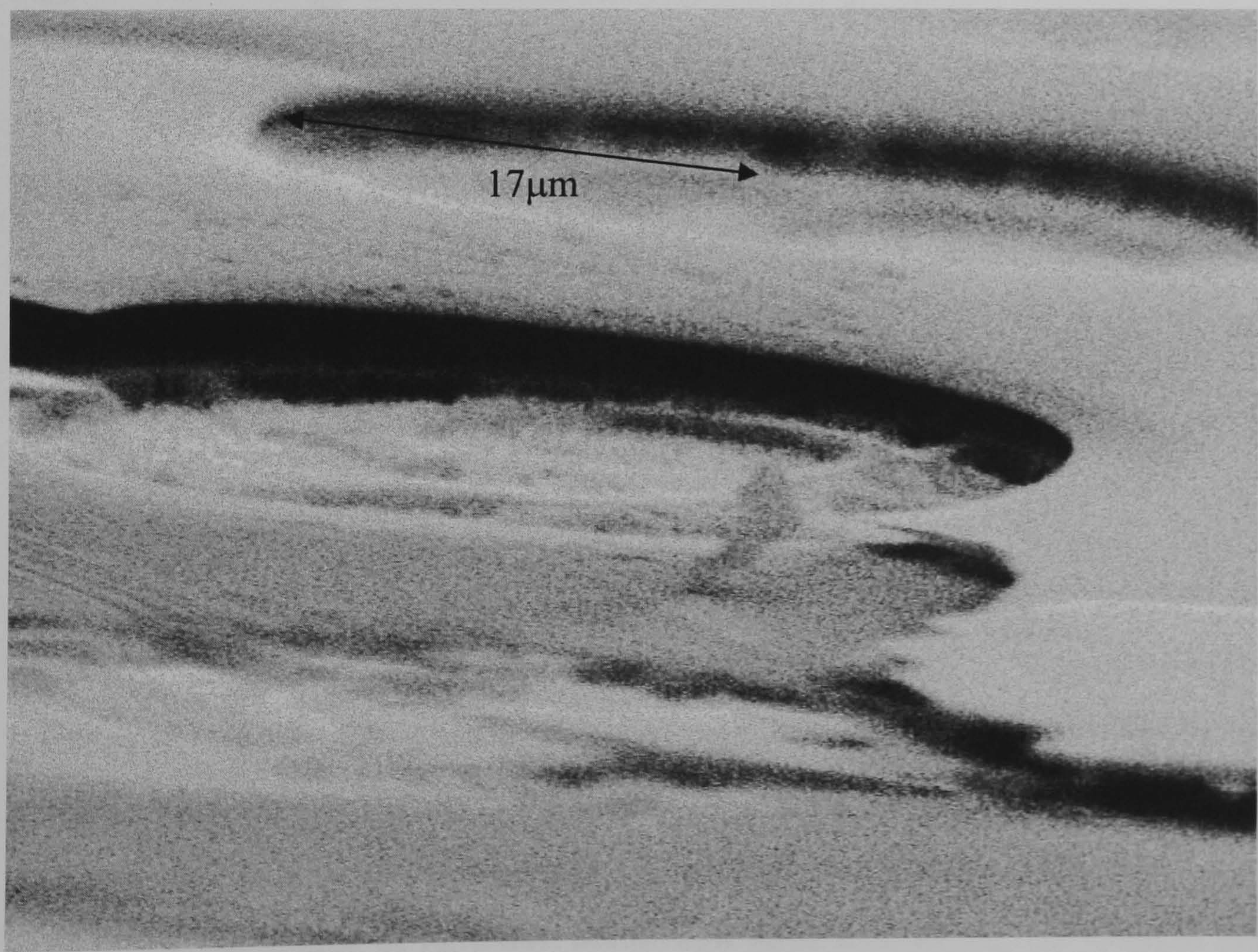


Fig. 5.6 SEM image of a severed Ti membrane after HMDS release.

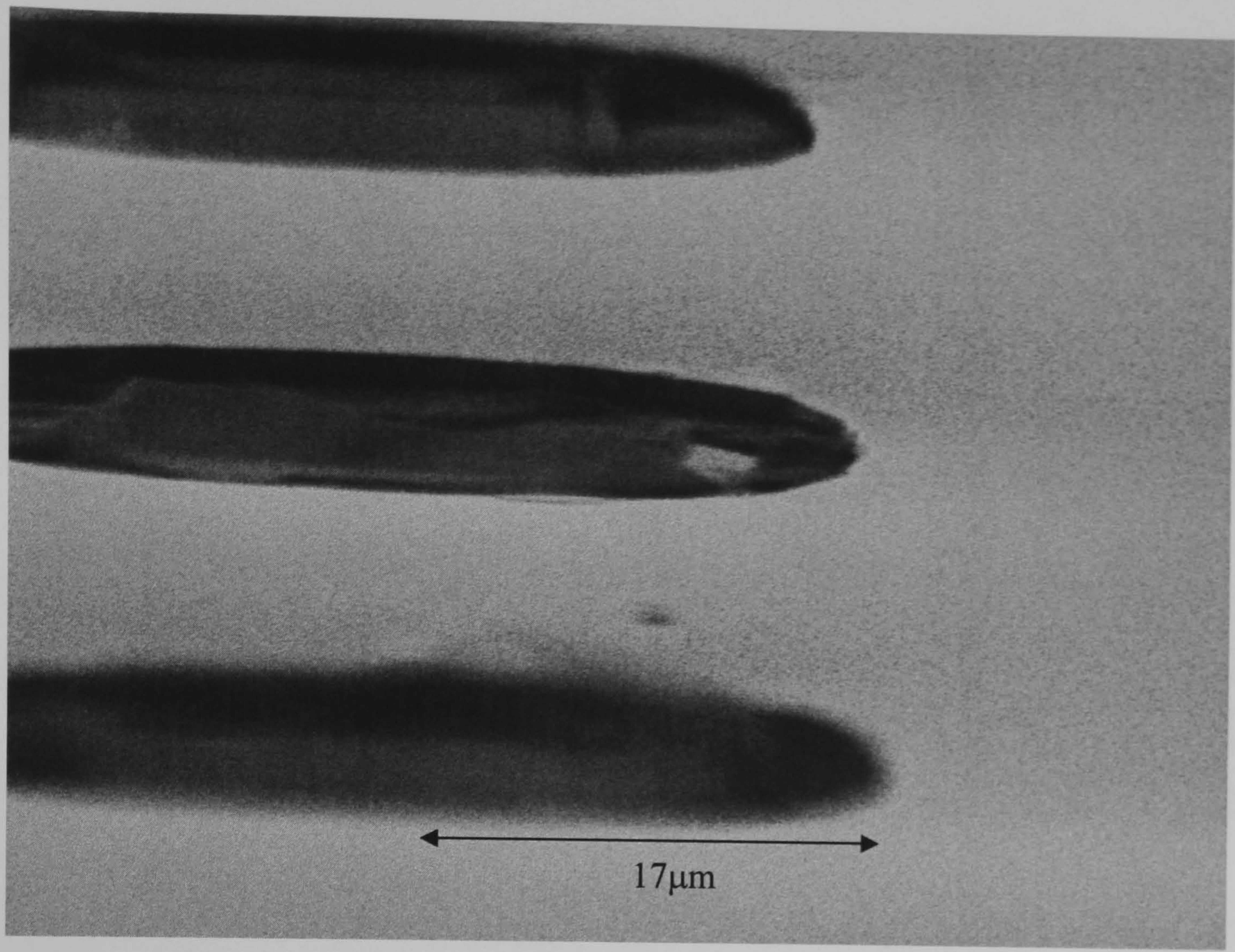


Fig. 5.7 SEM image of Ti membrane etch hole after HMDS release

Fig. 5.7 shows a SEM image of an unsevered etch hole in a titanium membrane, after HMDS release. In each of these figures, etch hole material is comparable to that observed after $SCCO_2$ drying. A test of the freedom of the membranes has been to gently load them with a probe. They have been observed to flex under the load prior to fracturing.

5.1.4 Photoresist residues

This section provides an insight into the causes and remedies for the unusual etch hole features observed after sacrificial photoresist release. The general approach to the problem has been to use different metals, deposition techniques, etch techniques and photoresists. It must be realised early on that many microstructures are very delicate. This limits the degree of agitation achievable after and during wet release. Ultrasonic agitation is therefore often ruled out as a solution.

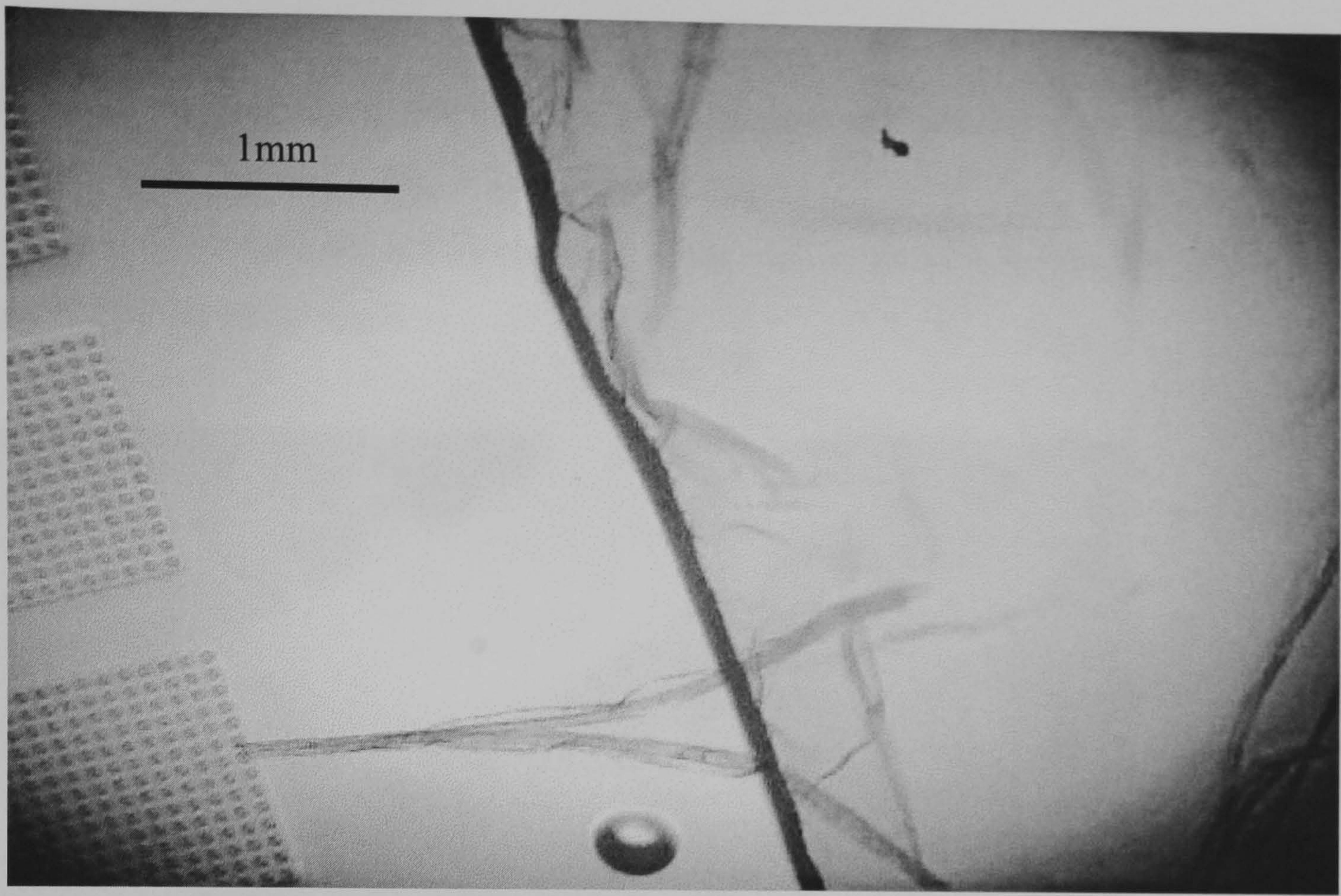


Fig. 5.8 Strands of material observed after sacrificial photoresist etching. The structures are in a deionised water bath.

Careful observation, under water, of the test samples immediately after release, using developer, showed fine strands of material emanating from the edges of large features. This is shown in fig. 5.8. These were floating and could be displaced by gentle agitation.

The observation of material after the first stage in the release process has important ramifications for its source. It eliminates the IPA, supercritical CO_2 or HMDS as the causes for its initial formation.

Plasma hardening occurs during the sputtering of titanium, this could lead to unetchable layers of photoresist. To eliminate this possibility, e-beam evaporation was used to deposit the titanium and the release process tested. This had no effect and the results were identical thus eliminating plasma hardening as an explanation.

Another strategy was to try different photoresist etchants. Identical results were obtained for releases using Microposit photoresist remover, sodium hydroxide (NaOH) solution and acetone. Consequently, this showed that the material is insoluble to standard photoresist etchants.

In order to investigate whether the phenomenon was restricted to titanium, other metals were deposited. Fig. 5.9 shows the material in the open spaces between e-beam evaporated aluminium cantilevers and in the etch holes of a membrane. Nickel also produced the same result.

Fig. 5.9 Strands of material observed after the sacrificial photoresist release of aluminium structures. The cantilevers are 60μm wide. The structures are in a deionised water bath.

To find out whether the problem was confined to S1813 photoresist, AZ5214E photoresist was used as the sacrificial layer with various combinations of deposition techniques, metals and etches. Again, the material was observed.

If the material is primarily organic then it is should be readily dissolved in a chemical solution known as 'bomb'. 'Bomb' is a 1:1 solution of hydrogen peroxide and concentrated sulphuric acid, which when mixed, produces an exothermic reaction which can reach temperatures of up to 75°C. At these temperatures it has been found to strip not only the floating material but also the photoresist. However, if it is allowed to cool to approximately 50°C it was found to etch the floating material with no significant photoresist etching.

If the samples were reactively ion etched prior to wet release, the material was observed not to form in open areas. This technique eliminates the type of floating strands observed in fig. 5.9. However, it is merely concealing the underlying problem. If the material has been previously observed in the exposed areas then one has to assume that it is present in the unexposed areas.

Fig. 5.10 shows a series of titanium cantilevers after release in developer. Fig. 5.11 shows the cantilevers after treatment in bomb. The cantilevers are observed to bend further after the bomb treatment. This indicates the presence of the material under the microstructures. The same effect has been observed for cantilevers that have undergone RIE prior to release.

Cantilever bending occurs because of a vertical stress gradient through the titanium. Typically metals are tensile, due to the method of deposition [118]. It is to be expected that at the interface between the photoresist, which is also tensile, some stress matching occurs. In thin films, the effect of interfacial stress matching can become significant. This suggests that the unidentified material forms at the photoresist/metal interface.

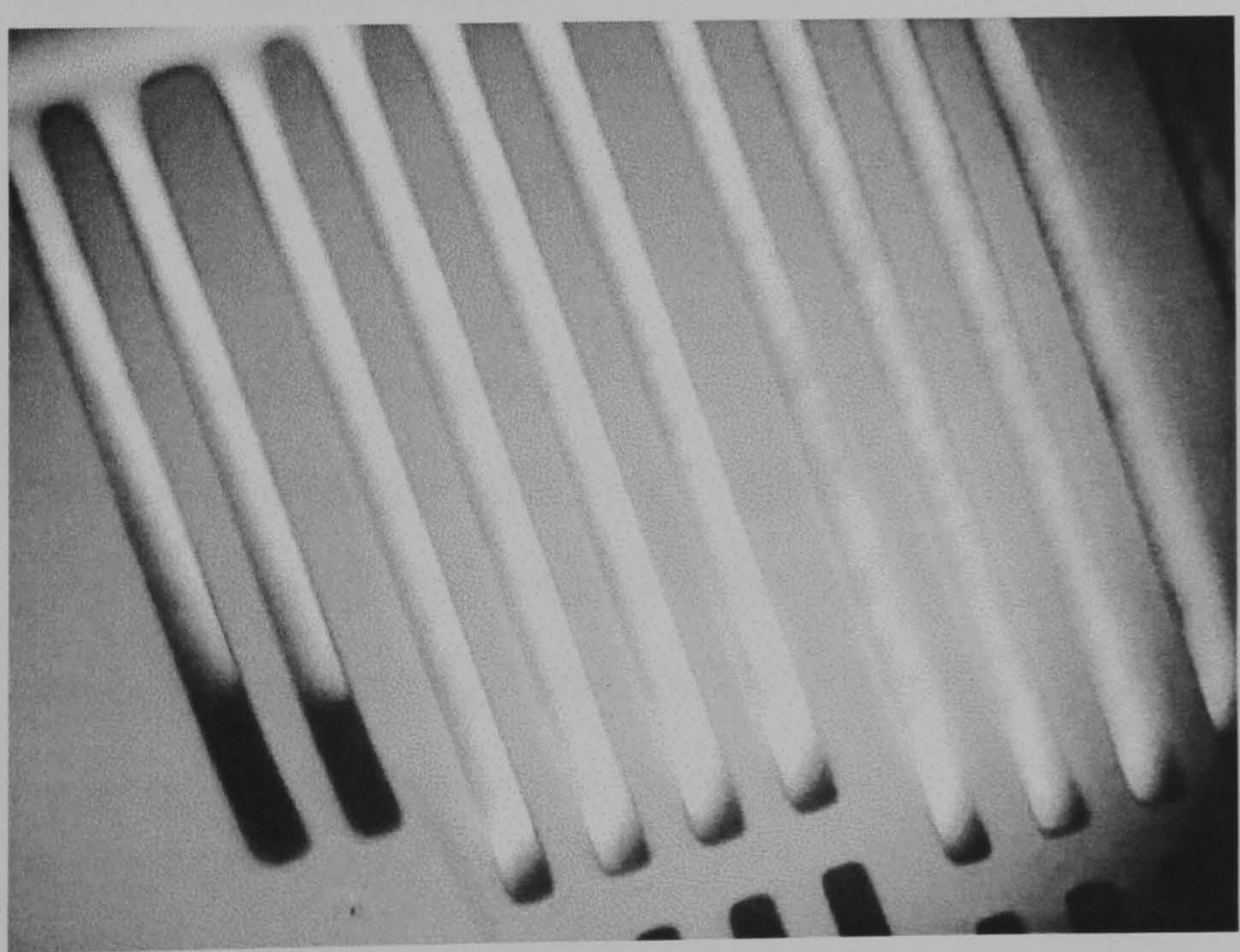


Fig. 5.10 Titanium (1μm thick, 60μm wide) cantilevers released after sacrificial photoresist etching. The cantilevers are in a deionised water bath.

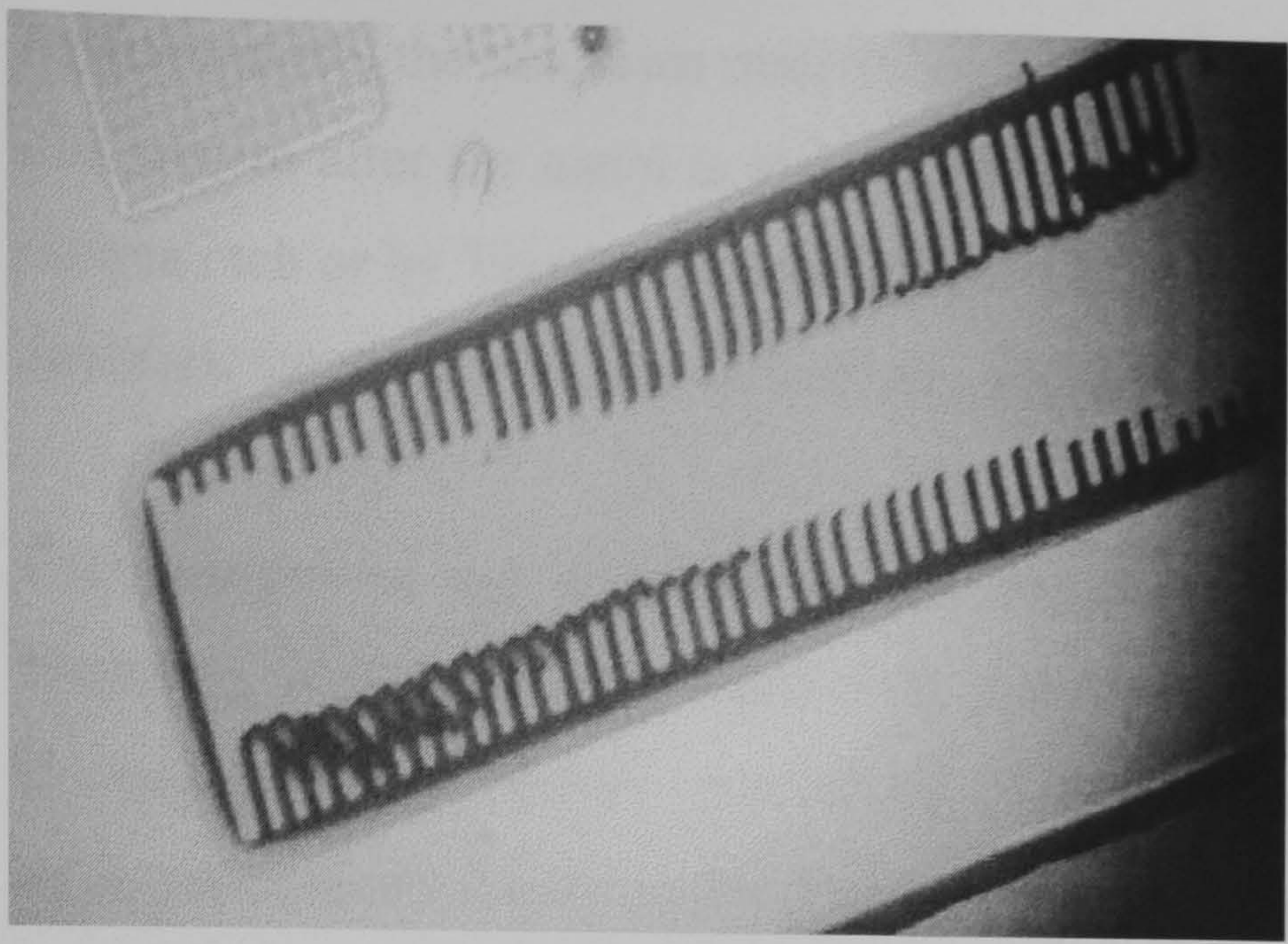


Fig. 5.11 Titanium (1μm thick, 60μm wide) cantilevers released after sacrificial photoresist etching followed by immersion in 'bomb' solution at 50°C. The cantilevers are in a deionised water bath.

For upward bending to occur, the top of cantilevers must have a higher tensile stress than the bottom. If stress matching is occurring, the photoresist should be less tensile than the top of the titanium. It is proposed therefore, that prior to 'bomb' etching the interfacial bonding layer is a significant contributor to the tensile stress of the titanium cantilever.

The interfacial bonding layer reduces the effect of the stress gradient through the metal. When, the remaining resist is removed, the effect of the stress gradient becomes significant and the degree of bending increases.

The cantilever bending is most prominent along the length. However, consider fig. 5.5 from the previous section. There is evidence of curvature across the width of a cantilever. This also explains the curvature of the cantilevers in fig. 5.2. If part of the stress compensating interface becomes detached from the cantilevers, then additional bending will occur in the areas of detachment.

The vertical stress gradient in the cantilever does not affect the metal membranes. Since these are clamped on all four sides, there should be no associated vertical bending with regards to the tensile stress gradient.

To summarise, the unknown material is formed at the photoresist/metal interface. It is still present after the metal is etched. This interface material can be removed in a dry plasma etch or by 'bomb' solution. 'Bomb' solution etches nickel and aluminium and is therefore unsuitable for microstructures formed using these metals.

The material is not observed on the topside of the metal after resist stripping. Titanium, nickel and aluminium will grow native oxides when exposed to the air. Consequently, photoresist spun on top of these metals will be bonding to the native oxide rather than directly to the metal, as occurs in vacuum deposition.

For adhesion to occur between the photoresist and the deposited metal, a bonding interface has to be formed. This layer can exhibit different etch properties to the bulk photoresist or titanium. It is therefore proposed that this interfacial bonding layer is the cause of the residue observed during and after sacrificial photoresist release.

The mechanism for the formation of the structures observed in the etch holes still requires explanation. It is known that the interfacial bonding layer is porous to etchants. This is indicated by the observation that the bulk photoresist can be etched. It is therefore reasonable to assume that it is also gas permeable.

After the bulk photoresist has been etched through the etch holes in the metal membranes, the structure will appear to be released. However, an interfacial layer will remain on the underside of the metal and will bridge the holes. As the HMDS dries or the supercritical CO_2 is bled, gas will escape out of the etch holes, passing through the gas permeable interface layer. The force of the escaping gas may stretch the interface layer past its elastic limit causing permanent deformation or even rupture. This model fits the results well.

If the metal membrane flexes during the release drying, as would be expected due to the finite surface tension of HMDS then the response of the underlying interface layer can potentially produce both negative and positive effects.

During release drying, if contact is made with the substrate or underlying metals then the interface layer may detach from the underlying metal, therefore avoiding stiction. After the structure has released, the interface material will remain in the cavity, with varying degrees of attachment to the metal. This introduces a significant uncertainty into long term device characteristics and reliability.

Insoluble photoresist interface polymers have been documented in the literature as photoresist scum [118]. This is common in sub-micron features where liquid agitation is less effective due to surface tension effects. Although the horizontal dimensions in MEMS are relaxed compared to the IC industry, vertical dimensions can be sub-micron. Consequently, it is to be expected that MEMS devices such as membranes will also suffer from scum problems. The issue is that, unlike in the IC industry, the scum is on the underside of features, hidden from view.

5.2 Titanium as a sacrificial layer

The organic scum found in photoresist sacrificial layers has rendered them unsuitable for the capacitive electrode gap of the tunable capacitor. Titanium has been previously reported as a sacrificial layer [92]. When compared to photoresist, titanium is a restrictive sacrificial layer. It is thickness limited and does not effectively planarise underlying topology. Titanium can be sputtered up to a thickness of a few microns and evaporated up to 0.5μm. After this stress fracturing and delamination occurs as shown in fig. 5.12.

Fig. 5.12 A stress fractured sputtered titanium film on silicon

These restrictions have to be carefully accounted for if titanum is used in a process flow. However the benefits, as will be shown in chapter 6, are exceptionally clean etching and compatibility with electroplated metals. Titanium shows excellent adhesion to glass and silicon and can also act as a conductive metal seed for electroplated nickel.

Fig. 5.13 illustrates a potential process flow using titanium for a bridge structure with electroplated nickel as the structural material. This process flow can not be directly used with electroless gold plating. As described in chapter 4, the electroplated gold preferentially plates onto itself. In order to replace the nickel with gold, a thin gold seed (10-20Å) must be deposited prior to plating.

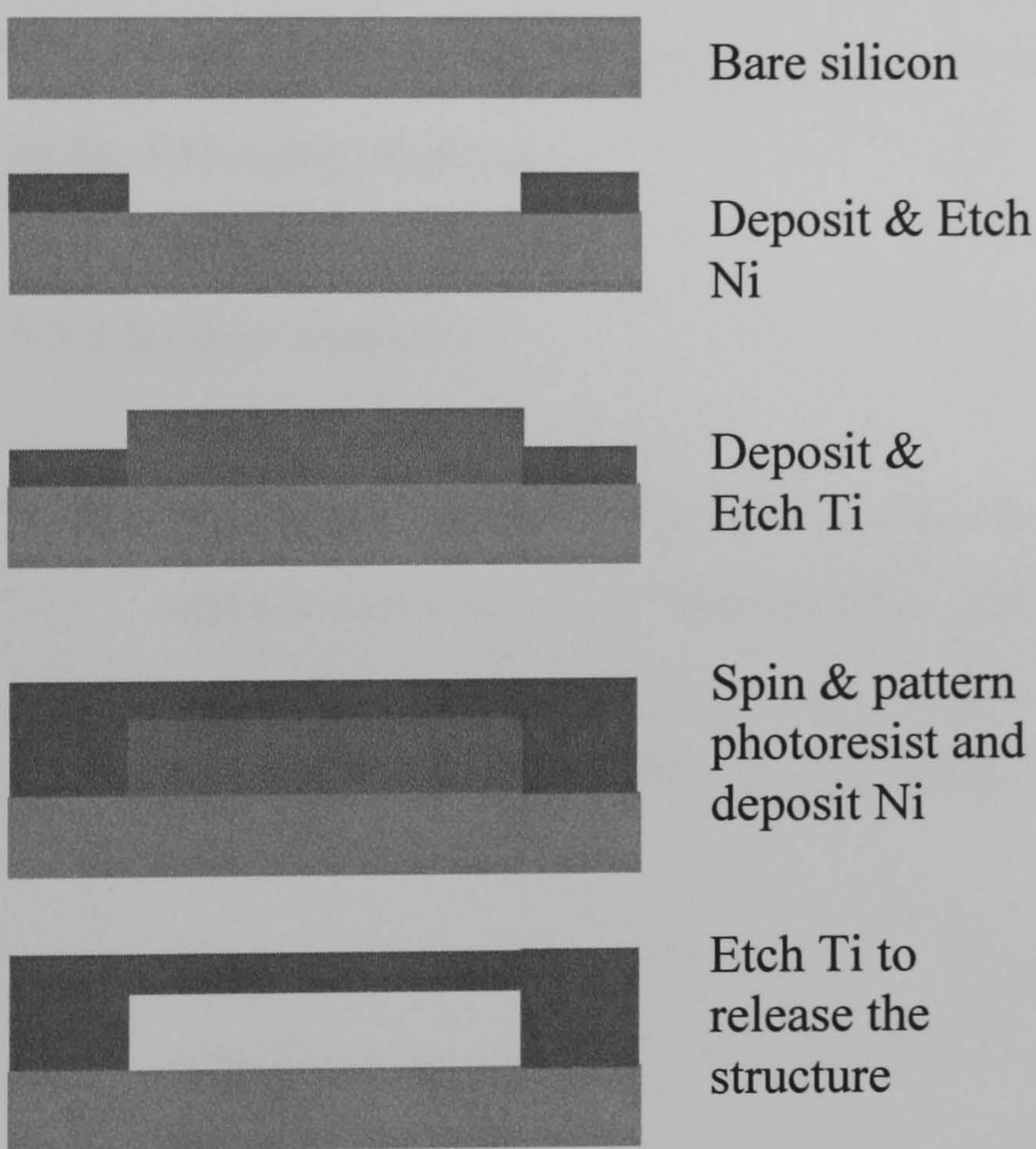


Fig. 5.13 A titanium sacrificial layer process flow to fabricate bridge structures using electroplated nickel.

Thin film metals exhibit a surface roughness associated with their grain structure [17]. This acts as a mould for electroplated metals. This roughness effectively reduces the metal to substrate contact area which decreases the likelihood of stiction failure.

A 1:1 solution of 42% HF and ethanol has been used to etch the sacrificial Ti at a rate of 10µm/min at 21°C. This is fast even for gaps as small as 0.1µm and the low surface tension of the solution enables it to effectively penetrate structures as wide as 200µm.

Unlike in the previous section a further option is available to release titanium sacrificial layer devices. A high temperature solvent bake has been found effective. This will be discussed in more detail in the next chapter. At elevated temperatures the surface tension of solvents such as isopropylalcohol (IPA) decreases. With titanium sacrificial layers, a high temperature (120°C) bake from IPA solution has been found effective at avoiding stiction.

Titanium is ideally suited to be a sacrificial layer for the widely tunable capacitors. Its clean etching and precise deposition at sub micron thicknesses will be exploited fully in the following chapters.

5.3 Chapter summary

- The widely tunable capacitor requires that the electrodes be in a near contact state to achieve a good tuning range. Any organic residue in this air gap of the capacitors could impede the performance. Therefore the sacrificial layer must be cleanly etchable leaving a well-defined gap.

- Commercial photoresist has been reported in the literature as an organic sacrificial layer. It is well suited for the definition of gaps in the order of a micron upwards. This was tested in conjunction with two stiction reducing drying techniques.

- Scanning electron microscopy revealed unusual etch hole features observed after sacrificial photoresist release.

- Insoluble photoresist interface polymers have been documented in the literature as photoresist scum. Although the horizontal dimensions in MEMS are relaxed compared to the IC industry, vertical dimensions can be sub-micron. Consequently, it is to be expected that MEMS devices such as membranes will also suffer from scum problems. The issue is that, unlike in the IC industry, the scum is on the underside of features, hidden from view.

- The organic nature of the scum was confirmed when it was found that the aggressive 1:1 solution of hydrogen peroxide and concentrated sulphuric acid was found to remove it. However, this etchant is incompatible with many metallisations and therefore its applicability is restrictive.

- Alternatively, titanium can be used as a sacrificial layer. It can be sputtered up to a thickness of a few microns and evaporated up to 0.5μm. After this stress fracturing and delamination occurs.

- A 1:1 solution of 42% HF and ethanol has been used to etch the sacrificial Ti at a rate of 10μm/min at 21°C. This is fast even for gaps as small as 0.1μm and the low surface tension of the solution enables it to effectively penetrate structures as wide as 200μm.

- Titanium is highly applicable as a sacrificial layer for the two-gap capacitor because it etches cleanly and is suitable for the formation of sub-micron gaps which are required to ensure a low tuning voltage.

Chapter 6

Widely tunable capacitors: Fabrication and testing

A range of processing techniques were available for the implementation of the tunable capacitor structures simulated in chapter 3. This chapter focuses on electroplated devices with titanium sacrificial layers. Two-gap tunable capacitors have been fabricated which have demonstrably wide tuning ranges.

The fabrication methodology relies upon a self-planarising approach. This, in principle, minimises deformation to the upper electrode structure caused by underlying structures. This is particularly important when using titanium as a sacrificial layer because it provides a conformal, non-planarising, coating.

In fabricating the devices, a primary aim was to minimise the unbiased capacitive gap. This enables a small biasing gap to be used. As demonstrated in chapter 3, smaller biasing gaps reduce the tuning voltages required to actuate the device. This permits thicker metallisations to be applied to the upper electrode without impeding device performance.

The use of small gaps produces high aspect ratio devices. Therefore, during deformation, the centre of the upper capacitive plate is acting in its optimum parallel plate configuration.

In addition to detailing fabrication processes and electrical results, this chapter presents the key factors which influence device yield. These include processing problems such as poor adhesion and stress induced curvature.

Furthermore, the localised topology of the capacitive plates has been studied using an atomic force microscope (AFM). This provides an insight into the meshing of the capacitive plates during actuation.

6.1 Fabrication methodology

Many fabrication techniques and materials have been presented in previous chapters. These provide a toolkit for the implementation of widely tunable two-gap capacitors. However, the fabrication of complex micromachined structures requires these techniques to be combined, which introduces additional considerations.

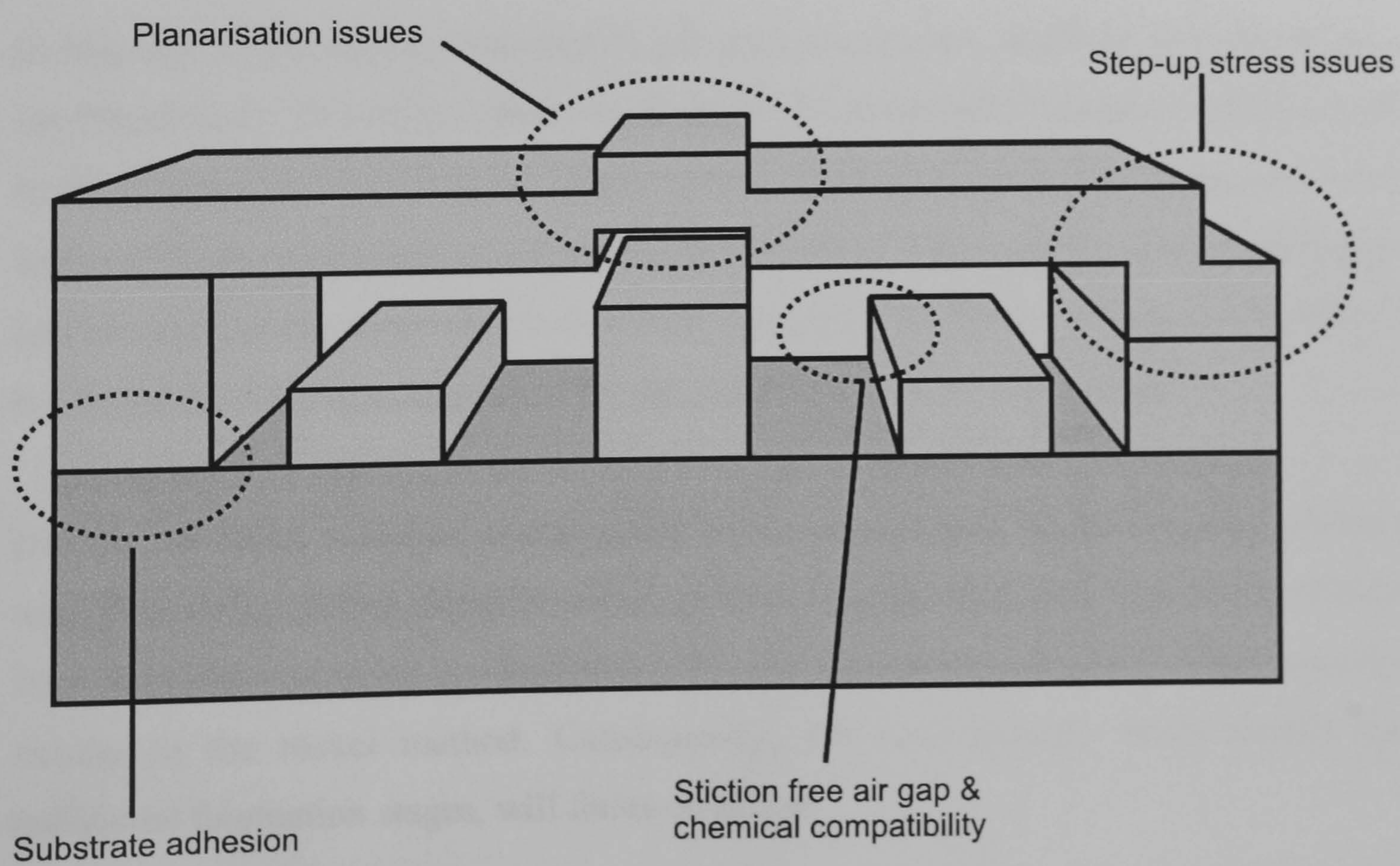


Fig. 6.1 General fabrication considerations for the two-gap capacitor

Fig. 6.1 shows the two-gap capacitor approach and includes notation of the key points to consider when implementing a process flow. A primary consideration is the self-compatibility of the flow. This is from both a chemical etch and mechanical perspective. For example, the structural metals need to be inert to the sacrificial layer etchant. From a mechanical perspective, the total stress on the wafer at any given point during process must not cause structural cracking or delamination. The micromachined structure needs to be well attached to the substrate for effective operation.

A further consideration is the planarity of the fabricated structures. This can be a problem for surface micromachined devices. Conformal sacrificial layers such as titanium do not provide effective planarisation. Non-planar topology passes through to the upper metallisations in the device. The presence of non-planar features in a free membrane or beam introduces additional mechanical considerations which can influence device performance. Chemical mechanical polishing is available for planarising multilayer metallised devices. However, it was deemed unnecessary for this work after the development of the 'etch and fill' planarisation technique discussed in the next section.

In response to the results presented in the previous chapter, titanium was chosen as a sacrificial layer. Thin film stresses associated with evaporated titanium typically limit its thickness to less than 0.5μm. This is suitable for the two-gap structure where a well controlled sub-micron gap is a key objective. A thick, low resistive loss metallisation can be used for the upper electrode without elevating the tuning voltages. In addition, it provides a better approximation for the ideal parallel plate tuning case.

For the structural material, electroplated nickel was chosen because it can produce near zero stress plating deposits under optimum conditions [119]. Devices have also been demonstrated using electroplated gold. The fabrication of these is fundamentally similar to the nickel method. Consequently, the next section, which details the individual fabrication stages, will focus on nickel.

6.2 Fabrication implementation

The general approach is a self-planarising, 'etch and fill technique', shown in fig. 6.2. As an example, when the central electrode needs to be plated, photoresist is used to mask the wafer everywhere except for over the central electrode zone. HF:ethanol is used to etch titanium in this exposed region. This is a very aggressive etchant and will rapidly undercut the photoresist as shown. The remaining photoresist is used to define the area for the electroplated metal to fill the cavity.

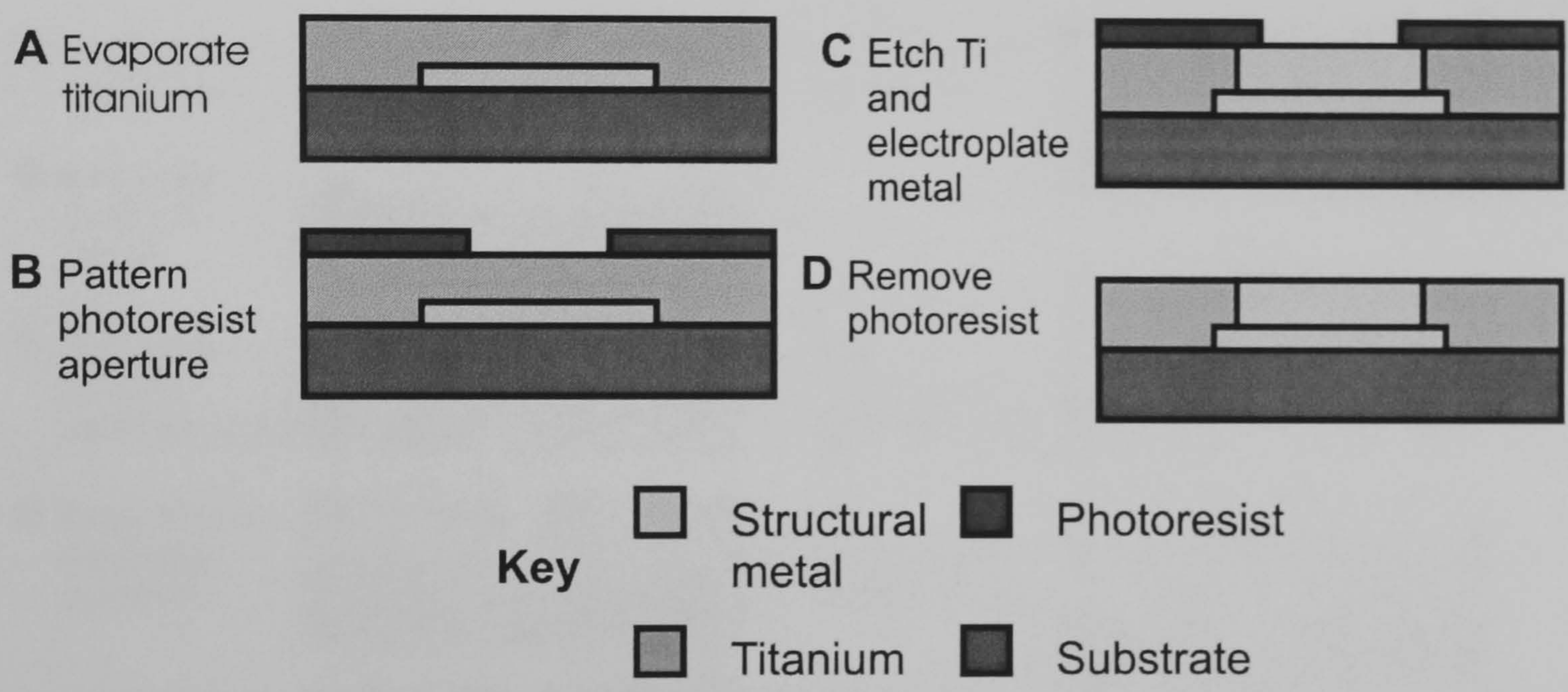


Fig. 6.2 The 'etch and fill' self-planarisation technique.

Partial photoresist undercut presents a very convenient method of ensuring that the electroplating thickness does not exceed the cavity thickness. If overplating occurs (fig. 6.2 C), a secondary ridge will be visible on the electrodeposit after the photoresist is removed. This has been used extensively to provide a rapid visual check of plating effectiveness during device fabrication.

Particular importance is paid to overplating because when working with small wafers and primarily dark field masks, the plating current has to be controlled precisely to ensure effective thin deposits. For this reason, it was found best to optimise the current density for each mask used. Although more time consuming, it produces better results. Evidence of the overplating ridge will be shown in the SEM defect studies presented later in this chapter.

Fig. 6.3 provides an illustration of the general process used to fabricate the two-gap tunable capacitors in this chapter. All fabrication starts on a clean substrate. The cleaning protocol consists of exposure to 'bomb' solution (1:1 H_2O_2:conc. H_2SO_4). Although very exothermic on mixing, the solution tends to cool after a few minutes. To counter this, the substrates are boiled in bomb solution on a hotplate for at least 30 minutes. For silicon, the native oxide is removed in 10% HF solution. The overall effect of this process is to provide effective removal of grease and contaminants. If present on a substrate these act to degrade thin film adhesion.

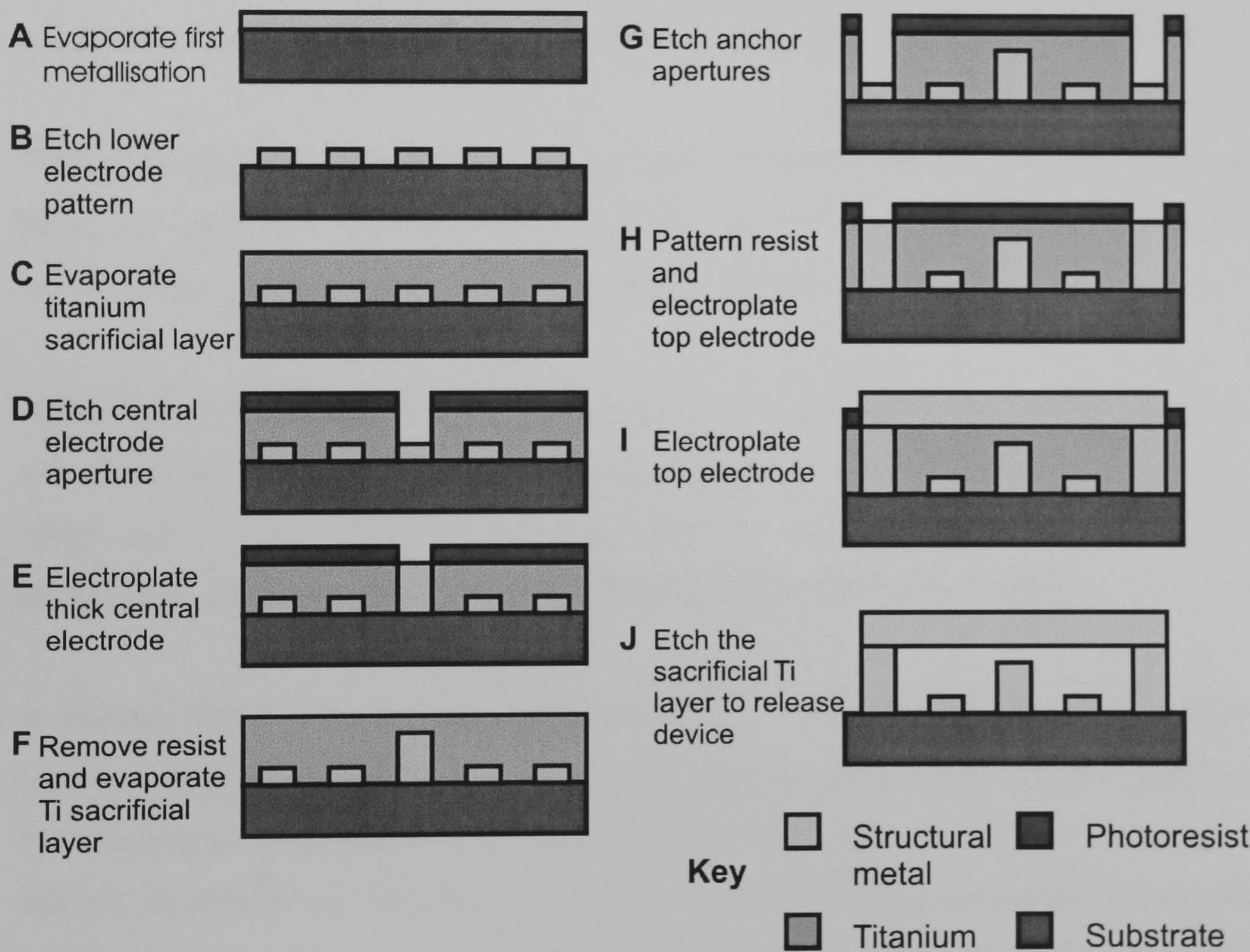


Fig. 6.3 The general fabrication process for two-gap capacitors

Although nickel will adhere to silicon much better than, for example, gold, it was found advantageous to include a thin seed layer of titanium (approximately 10Å) to enhance the adhesion. This stage has to be well controlled because sharing a seed with a sacrificial layer is potentially extremely problematic.

The seed has to be sufficiently thin to block the sacrificial etchant by surface tension. Furthermore the metal on top has to be sufficiently thick to block penetration by the etchant. The aggressive HF:ethanol solution requires very thin seeds of titanium to be effectively blocked. It can etch where other, higher viscosity, water based etchants could not.

A second consideration, with regard to the thickness of the first nickel metallisation is its effect on the self-planarisation approach. This first stage introduces non-planarity into the sacrificial layer (fig 6.3 A&B). This is unavoidable but can be minimised by ensuring that the metallisation is relatively thin. The implications for this with respect to RF losses will be detailed in the next chapter. However, purely for an electromechanical demonstration of wide tunability, this is less important. As a consequence of this, metallisation thicknesses between 300Å and 500Å were used.

From an electroplating uniformity perspective, the use of a thin nickel layer is not an issue for ensuring a uniform current density. The first layer of sacrificial titanium increases the effective metallisation thickness to 2000Å (fig. 6.3 C).

After this first sacrificial layer is deposited by evaporation, the central electrode aperture is etched (fig. 6.3 D). For a two-gap capacitor the aperture is then filled with electroplated nickel. However, this stage provides some flexibility because by not electroplating, a stepped top electrode capacitor design can be fabricated.

A second layer of evaporated titanium (1000Å) is deposited to form the central capacitive gap (fig. 6.3 F). At this stage, the anchors are formed using the 'etch and fill' technique. After these have been electroformed, the top electrode pattern is defined in photoresist. The first generation of nickel devices presented in the next section include etch holes to minimise release times. Later devices have had these removed since the sacrificial etch time was found to be sufficiently short (less than ten minutes) without them.

Classical electroforming requires the photoresist mould to be at least as thick as the electrodeposit. This is undesirable in many applications where the wafer stress is already high due to underlying layers. Once the electrodeposit exceeds the thickness of the mould, it becomes laterally unconstrained leading to overplating. In the capacitor structure this effectively reduces etch hole size and enlarges the top electrode area.

After the top electrode has been electroformed, the S1813 photoresist mould is removed in acetone. The device is now ready for release (fig. 6.3 J). Release of the titanium sacrificial layer requires immersion in HF:ethanol typically for several minutes depending on the electrode configuration. After this, the wafer is transferred to water to provide a primary rinse of the etchant. Then it is transferred to an acetone bath for wafer dehydration. This requires a minimum of two acetone baths with at least 5 minutes in each bath.

Finally, the wafer is transferred to an isopropyl alcohol bath. This was found to provide a much cleaner release than acetone when transferred to a high temperature (120°C) for final wafer drying.

If the first acetone stages are too short or only a single bath is used, the wafer will not dry instantly. Instead, droplets of liquid will be evident. This is not good because the slow drying droplets can leave residue on the wafer. Second, the drying liquid is likely to be water, which has a much high surface tension than the flash evaporated solvent. Therefore the devices are more susceptible to stiction failure. Final bake is typically performed on the 120°C hotplate for longer than 30 minutes to ensure thorough wafer drying.

From a device fabrication perspective this represents the full process flow prior to test. As mentioned previously, the individual stages are optimised to a particular set of masks or devices but the flow and key dimensions are still maintained.

The masks used for the devices in this chapter vary depending on final electrode configuration. Apart from the first mask which is used to define the lower electrode structure all of the masks are dark field. The use of dark field masks is a feature of the self-planarising 'etch and fill' approach. However, the effective alignment of these masks is imperative. Early devices suffered due to misalignment defects. The most critical alignment is for the central electrode and anchor apertures.

Fig. 6.5 illustrates the effect of a deviation from good alignment. As can be seen, if the aperture is partially opened to one side of the nickel electroplating seed, a metal free void is created.

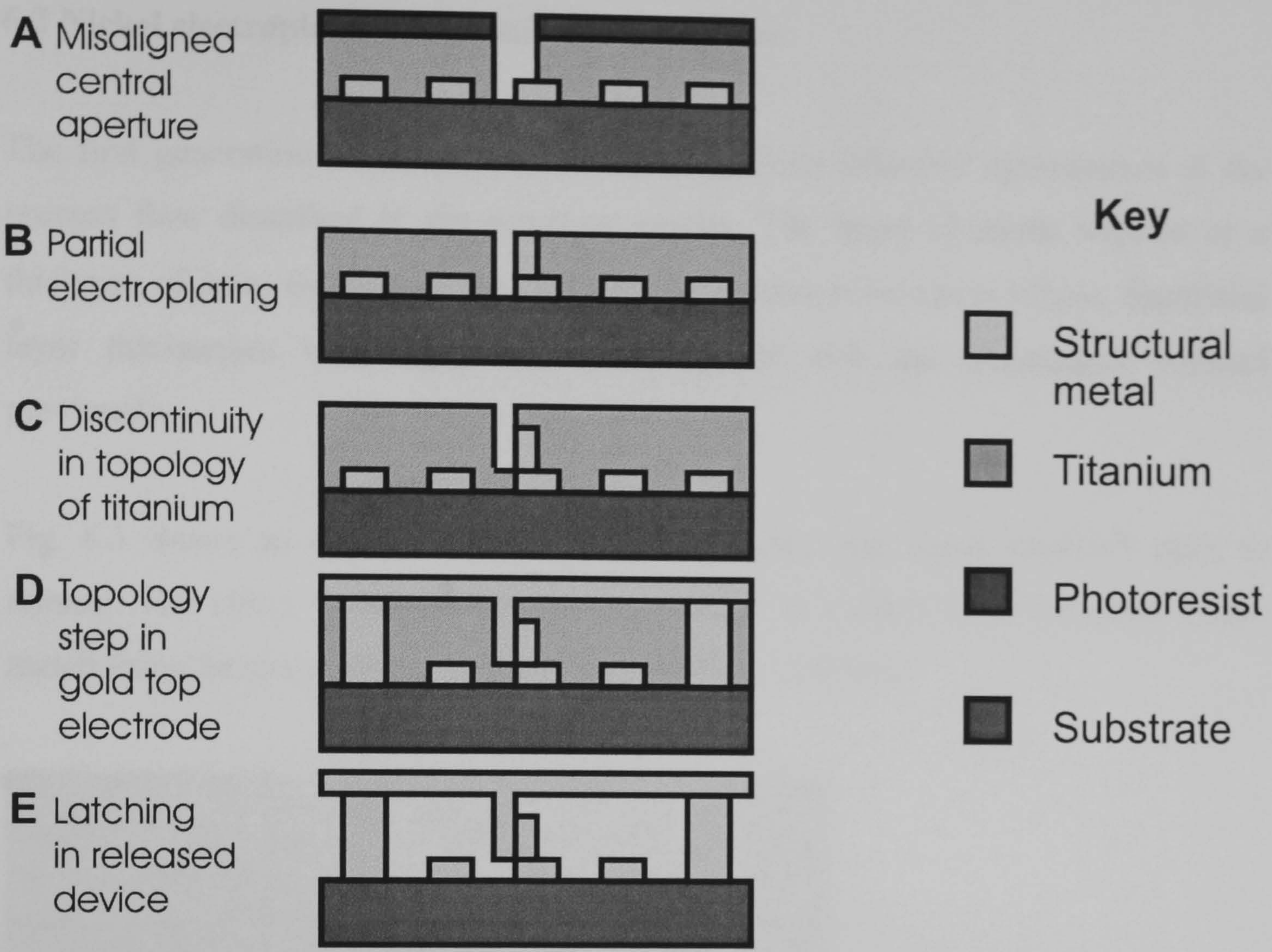


Fig. 6.5 The effect of central electrode misalignment on upper electrode topology

If a stepped upper electrode design is required then this misalignment can be accommodated since the next sacrificial layer will cover the void and provide effective plating for subsequent layers. However, for a thick central electrode design, the consequences of misalignment are more serious. The capacitor essentially becomes a mixture of the stepped electrode and the thick central electrode designs. This causes a sharp dip in the upper electrode which acts a side latch bump stop thereby limiting device performance.

All the masks used for fabrication are photoemulsion based, as described in chapter 4. Whilst providing good feature sizes for the application, the mask to mask alignment capability across a wafer is not as good as that for an e-beam written chrome mask. Consequently, alignment allowances have to be included in the central electrode. The electroplating void is deliberately smaller than the underlying metal seed.

6.3 Nickel electroplated widely tunable capacitors

The first generation of nickel devices represented considerable optimisation of the process flow described in the previous section. The upper electrode was set to a thickness of 3μm, the anchors to 0.3μm and the central electrode to 0.2μm. Sacrificial layer thicknesses were deposited in accordance with the dimensions outlined previously.

Fig. 6.5 shows an electron micrograph of an anchor and upper electrode prior to release. The effect of the self-planarising process is evident from the good height match from the electroplated nickel to the sacrificial titanium.

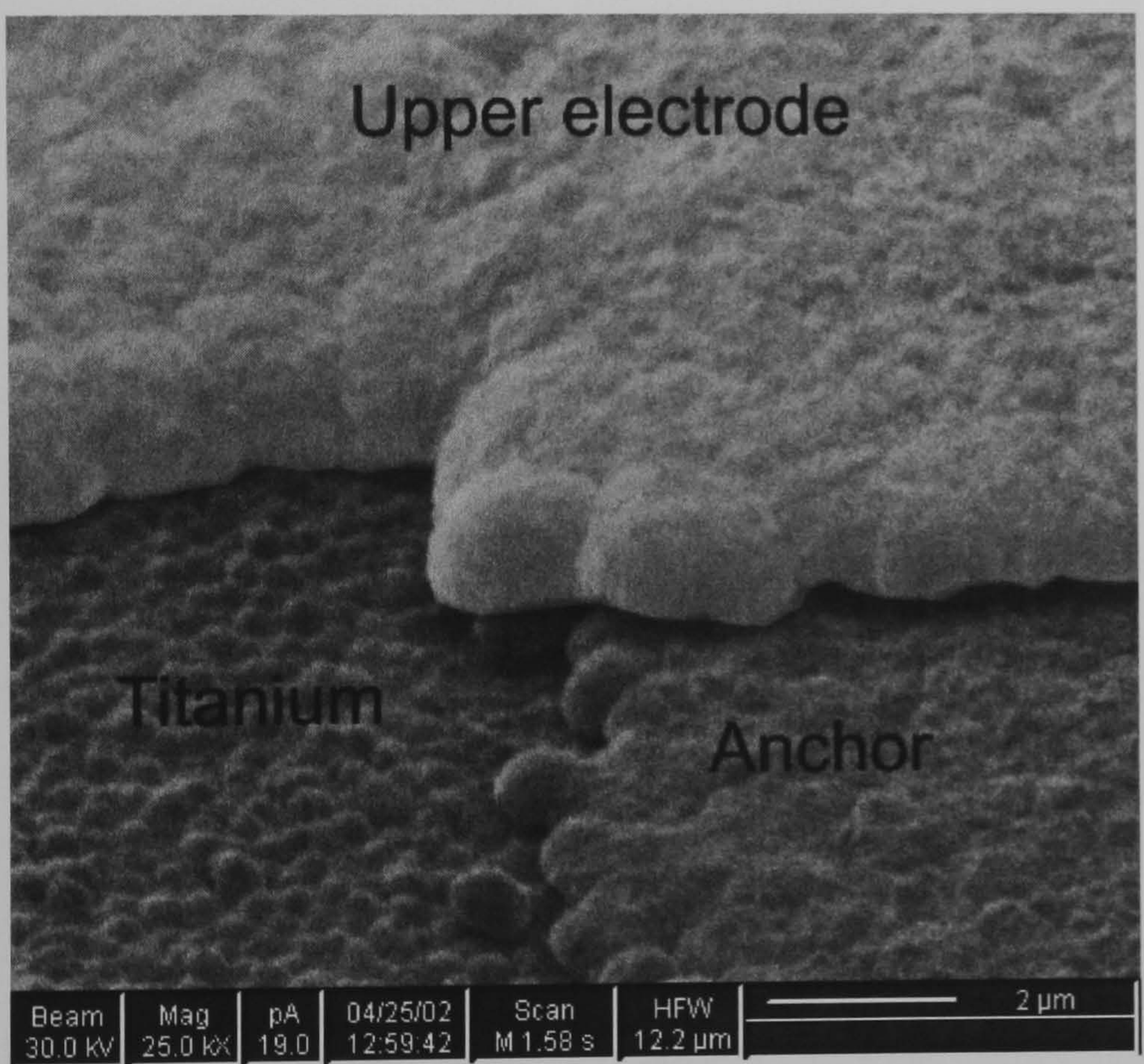


Fig. 6.5 A SEM image of an unreleased device in the anchor region.

Fig. 6.6 shows a microscope photograph of a fabricated device. The total device footprint is approximately 1000μm wide. The substrate is p-type silicon with a resistivity of 70 Ω cm.

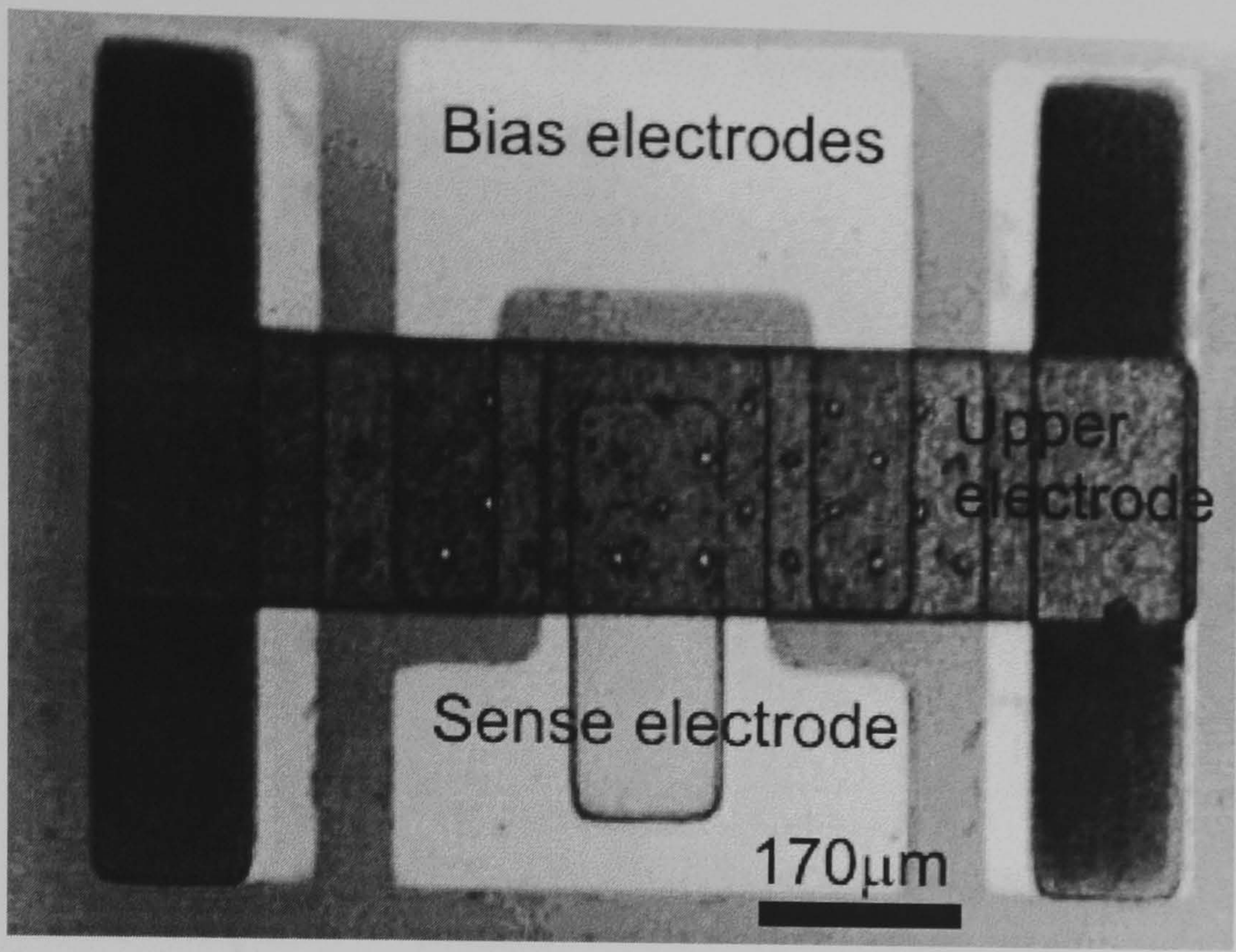


Fig. 6.6 A microscope view of a fabricated nickel device.

In order to test the electromechanical response of this device, a Boonton 72B capacitance meter was used in conjunction with a DC voltage source and a probe station. This meter measures capacitance using a signal frequency of 1 MHz.

A result of the relatively low measurement frequency is that the measured tuning characteristic includes a parasitic capacitance associated with the substrate. The effects of the leads can be removed by zeroing the device after all but one of the capacitive probes is in contact with the substrate.

This parasitic capacitance has the effect of reducing the apparent tuning range at these frequencies. The parasitic effect is less significant at the GHz testing frequencies or on the insulating substrates detailed in the next chapter.

Fig. 6.7 shows a capacitance – voltage tuning characteristic from the nickel capacitor. This has a tuning ratio of 5.1:1 from an unbiased capacitance of 0.7pF. These initial results represented state of the art for the two-gap structure. The tail-off associated at the end of the tuning range is unexpected when compared to the simulated device responses. The simulated results are for a planar 0.1μm device and one with an additional 0.1μm of curvature representing a stressed state. The simulations are in the correct regime, however, they only represent a simplification of the device topology as will be identified in later sections.

As will be shown in the SEM studies in the next section, some curvature can exist in the upper electrode. This causes deviation from the ideal two-gap situation. The simulations in chapter 3 showed that this could be accommodated without significantly restricting the maximum tuning ratio.

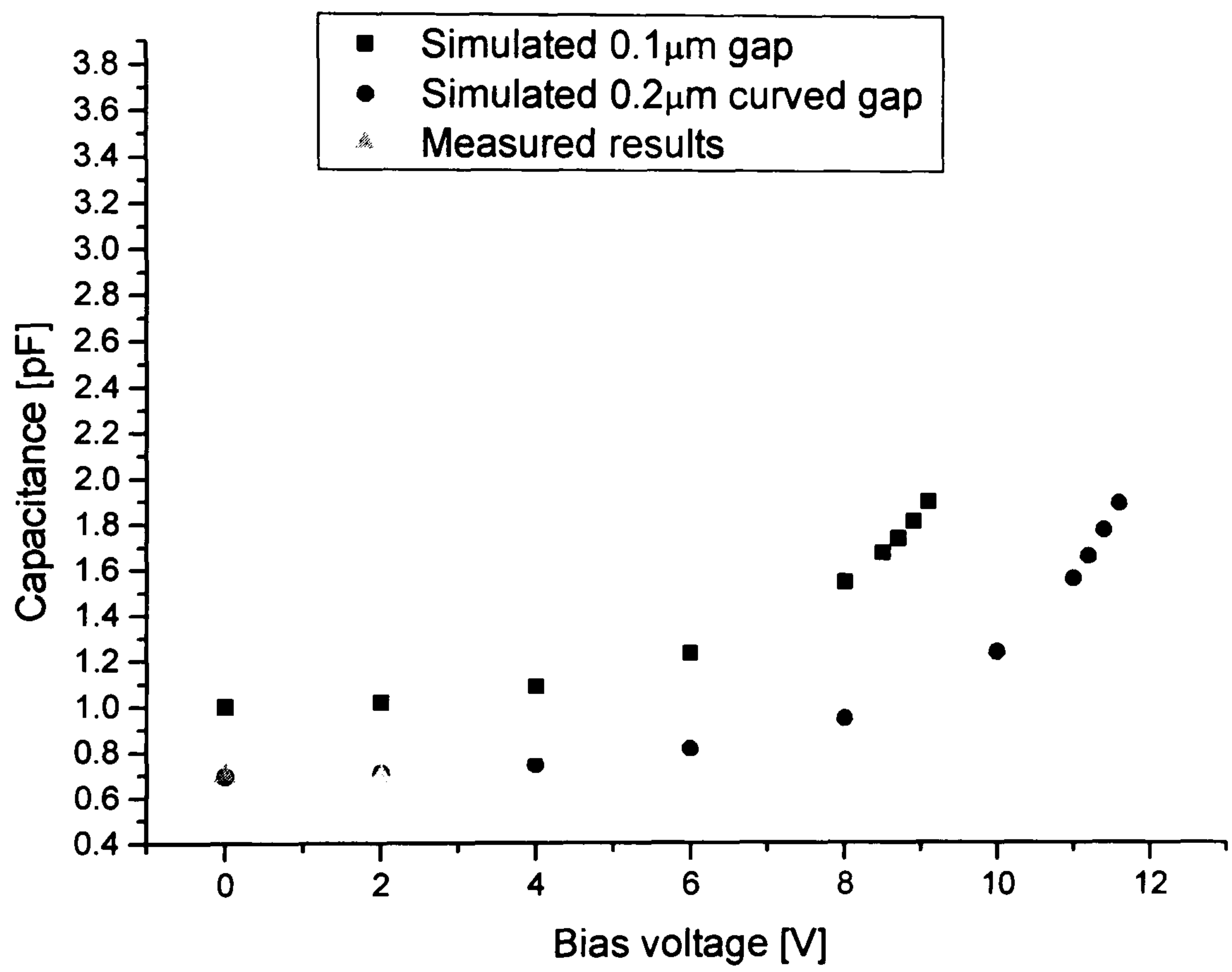


Fig. 6.7 C-V characteristic of a nickel electroplated two-gap tunable capacitor compared to simulated values.

However, the effect of any bowing, in conjunction with the step introduced from the first nickel seed stage, means that at the end of the tuning range, the upper electrode can contact the edge of the bias electrodes before good contact can be achieved with the central electrode.

In order to confirm that the central electrodes could be brought into contact with the upper electrode, a probe tip was placed on the centre of the upper electrode. As the probe was lowered contact could be made between the central and upper electrodes which shorted the capacitor.

Extremely high tuning voltages, followed by contact or dielectric breakdown can cause catastrophic device failure. This is shown in fig. 6.8. The device has shorted with a high current passing through and melting the structural nickel.

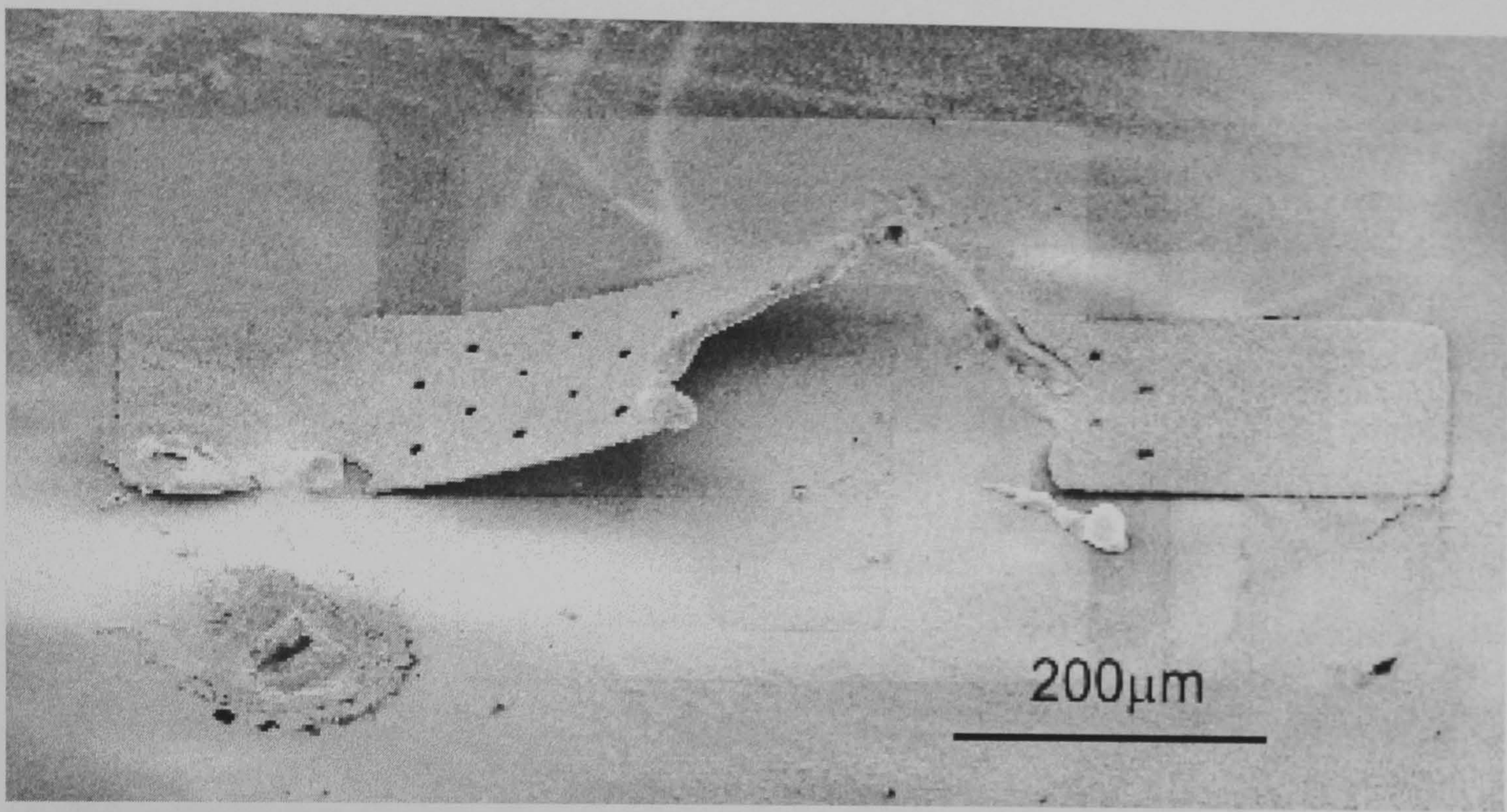


Fig. 6.8 A nickel micromachined capacitor after high current shorting and subsequent upper electrode melting.

6.4 Gold electroplated widely tunable capacitors

The long term applicability of surface micromachining technique for RF MEMS relies upon the use of low resistivity structural metals such as gold. The nickel process flow was developed first because of the ready availability and low cost of the nickel electroplating solution. Electroless gold plating is significantly more expensive. However, thick electroplated gold structures are used in the MMIC industry for air bridges. From an integration perspective, the pursuit of an effective gold process was desirable.

Gold electroplating methodology has been covered in chapter 4. However, the process flow in section 6.2 needs some modifications for the successful implementation of gold capacitors.

The most important is a change in the first metallisation, from evaporated nickel to 100Å of chromium followed by 300Å of gold. Gold was electroplated for the capacitive electrodes and supports using Neutronex 309 electroless solution at 40°C. Unlike nickel, gold electroplates poorly onto titanium. Consequently, 100Å of gold was evaporated onto the second layer of sacrificial titanium to act as a plating seed. This layer was removed prior to the release etching in the HF:ethanol solution.

When compared to the electroformed nickel, electroless gold exhibits relatively high compressive stress. This can be enough to lead to significant buckling. Fig. 6.9 shows a SEM image of an extremely buckled upper electrode. The gap in this case is of the order of tens of microns. This type of extreme buckling is also visible in the optical micrographs shown in fig. 6.10. The lighter region in the centre of the membrane shows the buckling point.

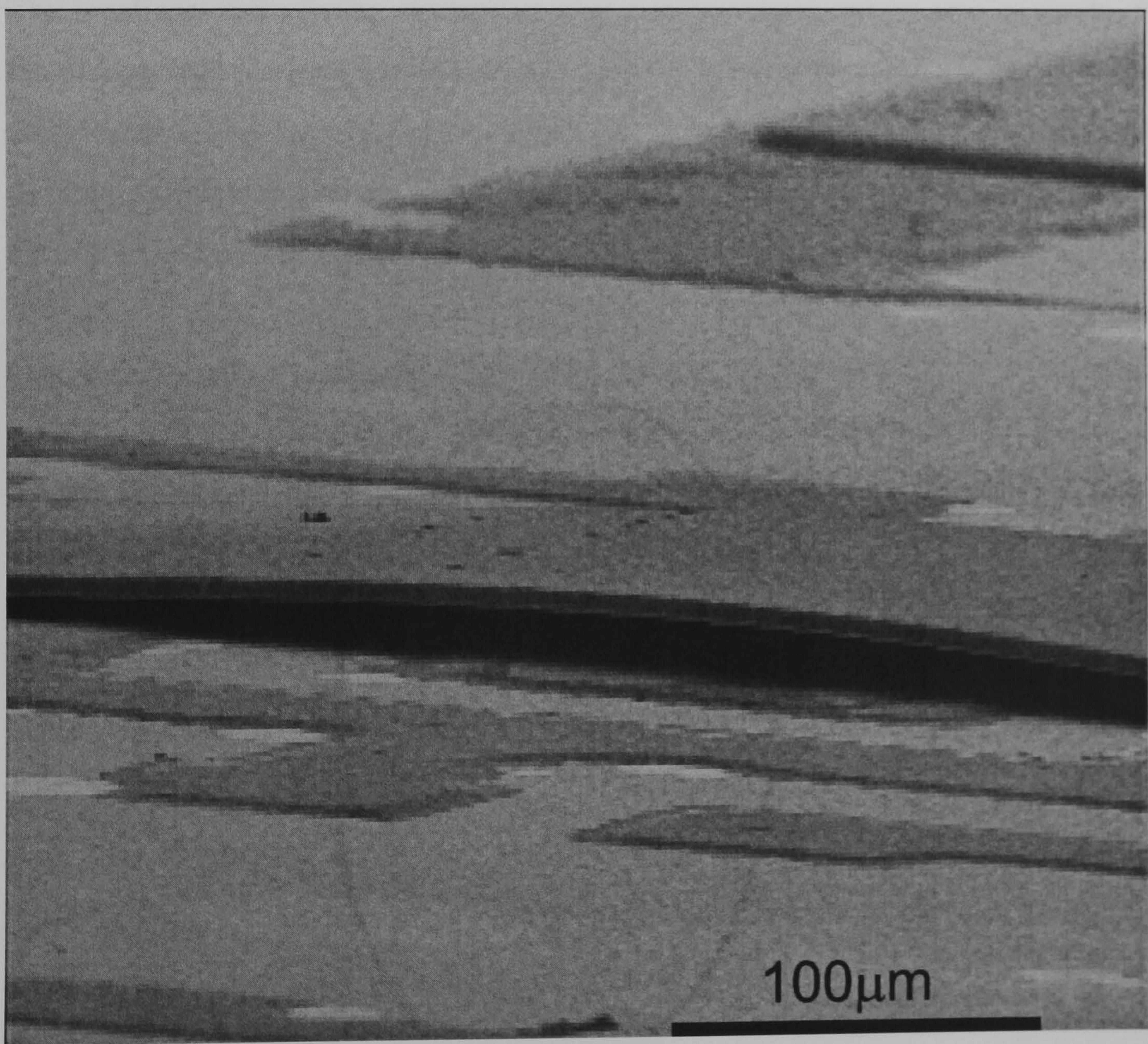


Fig. 6.9 An electron micrograph of a buckled gold upper electrode.

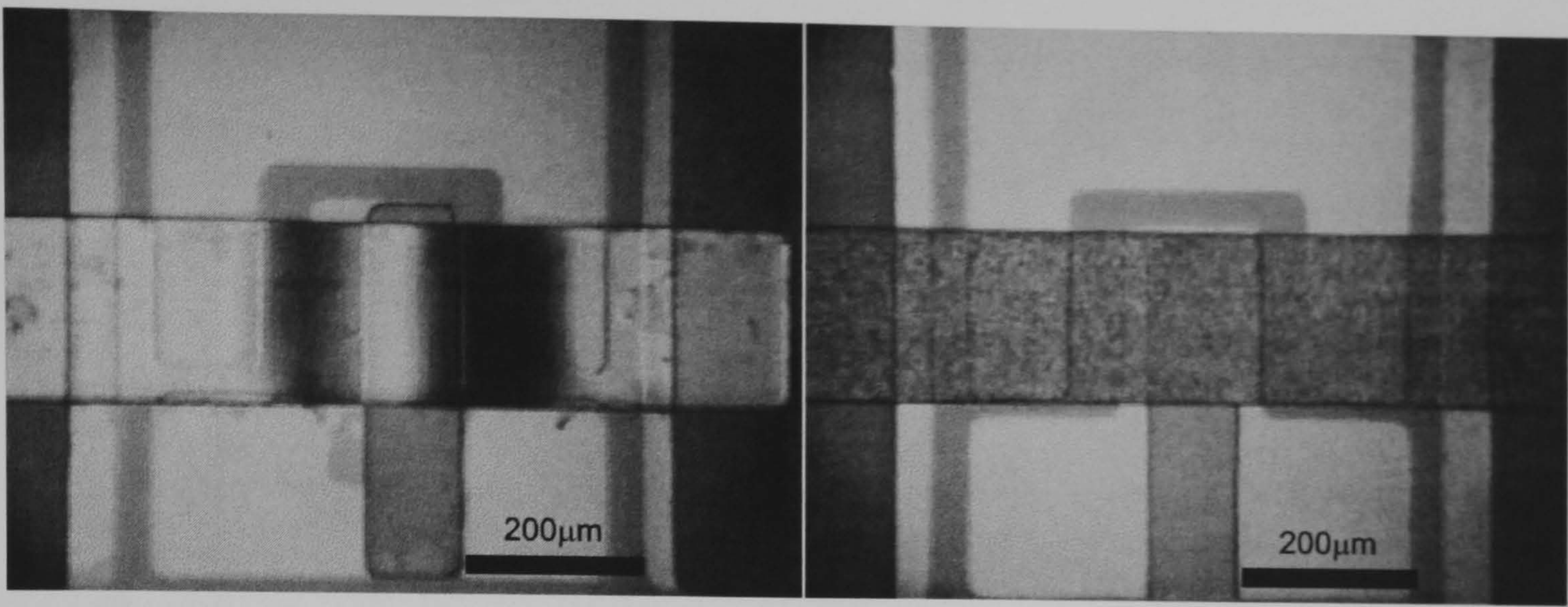


Fig. 6.10 An optical microscope image of a buckled gold upper electrode (left) and successfully fabricated gold device (right).

The localised stress in the electroless gold can be minimised by two methods. First, the plating bath temperature has to be at least 40°C. Second, as described in chapter 4, a high current density leading to a rapid plating rate must be used. This produces a rougher but lower stress deposit. However, at very high current densities edge definition and feature scale uniformity can be lost.

Fig. 6.11 shows a measured capacitance-voltage tuning characteristic from a gold tunable capacitor. The tuning voltage is higher than that required for the nickel device in the previous section. A peak tuning voltage of 30V is used. The next section will present results which confirm that in released devices, even with a small stress related curvature, the tuning voltage is elevated. Any curvature associated with the upper electrode acts to reinforce the upper electrode structure and enlarge the biasing gaps leading to a higher tuning voltage.

A second observation is an increase in the unbiased capacitance. When compared to the nickel capacitor structure in 6.3, a lower resistivity substrate of n-type silicon (1-10 Ω cm) has been used. This increases the parasitic capacitance to ground. However, even with the increased parasitic capacitance, the tuning ratio for the gold device is 7.3:1 which exceeds that of the nickel device.

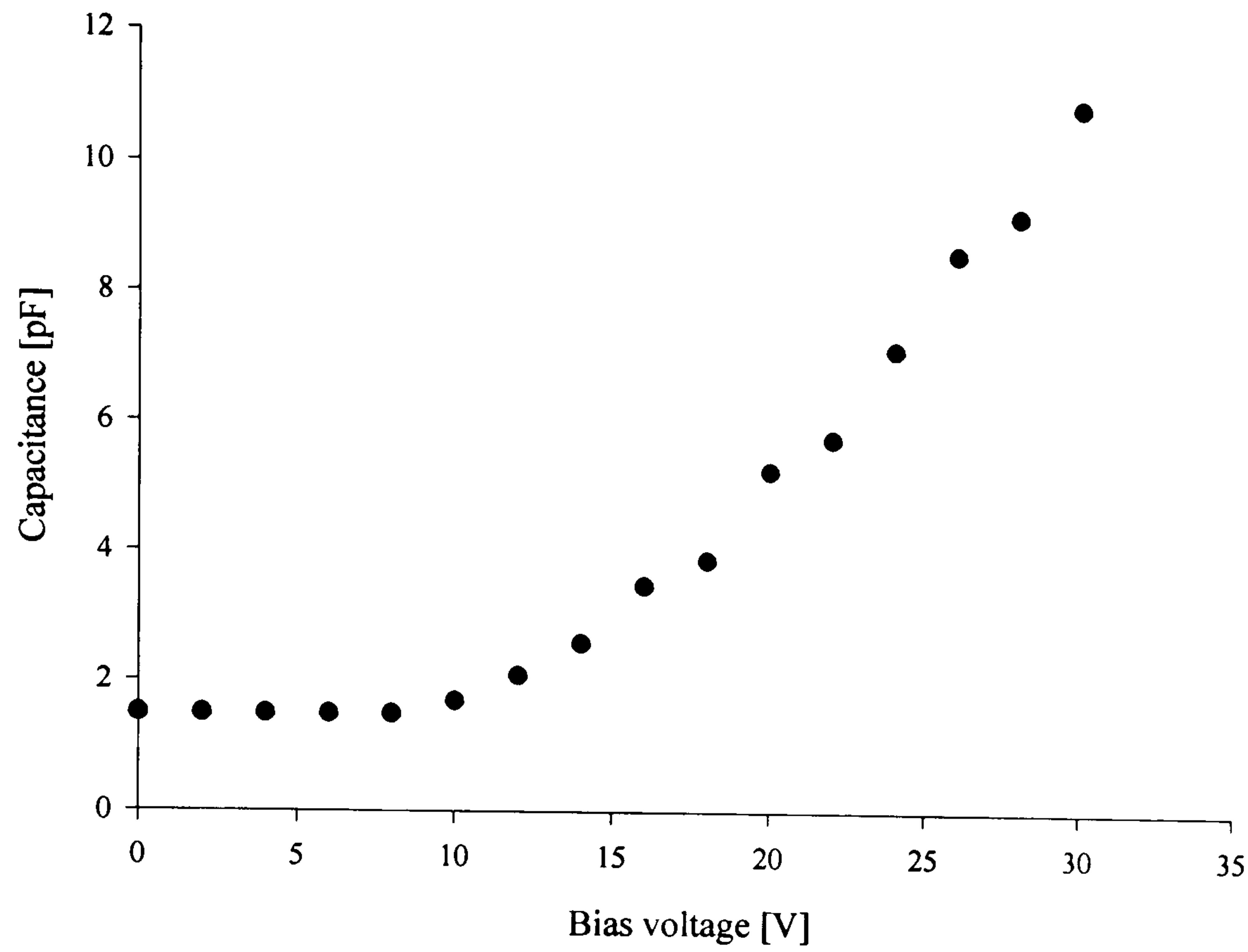


Fig. 6.11 C-V characteristic of a gold electroplated two-gap tunable capacitor.

6.5 The effect of device topology and processing on performance

The aim of this section is to examine the effect of a change on the process conditions on both yield and performance. The full stabilisation of processing conditions outside a commercial manufacturing environment is very difficult. In a university environment, typically chemicals are used for longer and fabrication equipment can drift out of specification.

A range of wafers was produced with devices subject to various processing conditions. Particular focus was paid to the variation in the central electrode plating conditions. However, in the course of this work many of the other variables and issues associated with the fabrication of a multilayer surface micromachined structure were identified.

This variety of nickel capacitors differs from those in section 6.3. First, the upper electrode thickness has been increased to 5μm. The etch holes have been removed because device release without etch holes can be achieved in less than 10 minutes. A pad configuration has been used which is compatible with the on wafer probing used in the next section. Initially, three types of device will be considered. They represent a stepped upper electrode, a thick central electrode device and a bowing stepped upper electrode.

6.5.1 Stepped upper electrode device

The devices presented in sections 6.3 and 6.4 used a thick central electrode structure. By not plating nickel in step E of fig. 6.3, the two gaps can be formed by using a stepped upper electrode. A high aspect ratio is maintained and, in theory, according to the simulated results there should be little variation in the device performance providing the stress in the upper electrode does not cause significant bowing.

Fig. 6.12 shows a SEM image of the sense electrode region in this stepped device. The transition from the biasing gap to the capacitive gap can be seen clearly. It demonstrates a clear step in the upper electrode as intended. Fig. 6.13 shows a bias gap electron micrograph. When compared to fig. 6.12 the gap is maintained which indicates negligible bowing.

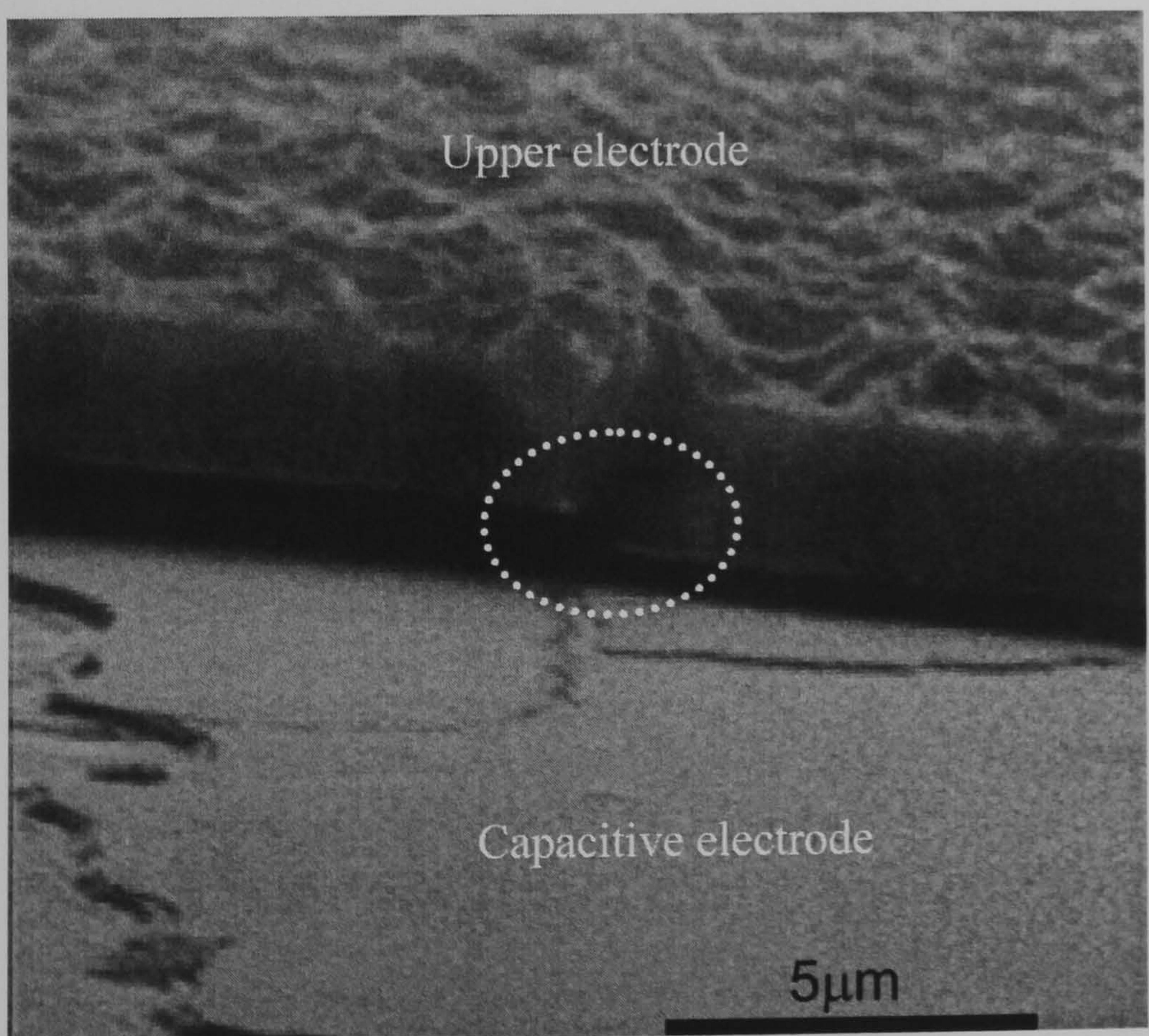


Fig. 6.12 A SEM image of the capacitive electrode region of stepped upper electrode capacitor. The step in the upper electrode is circled.

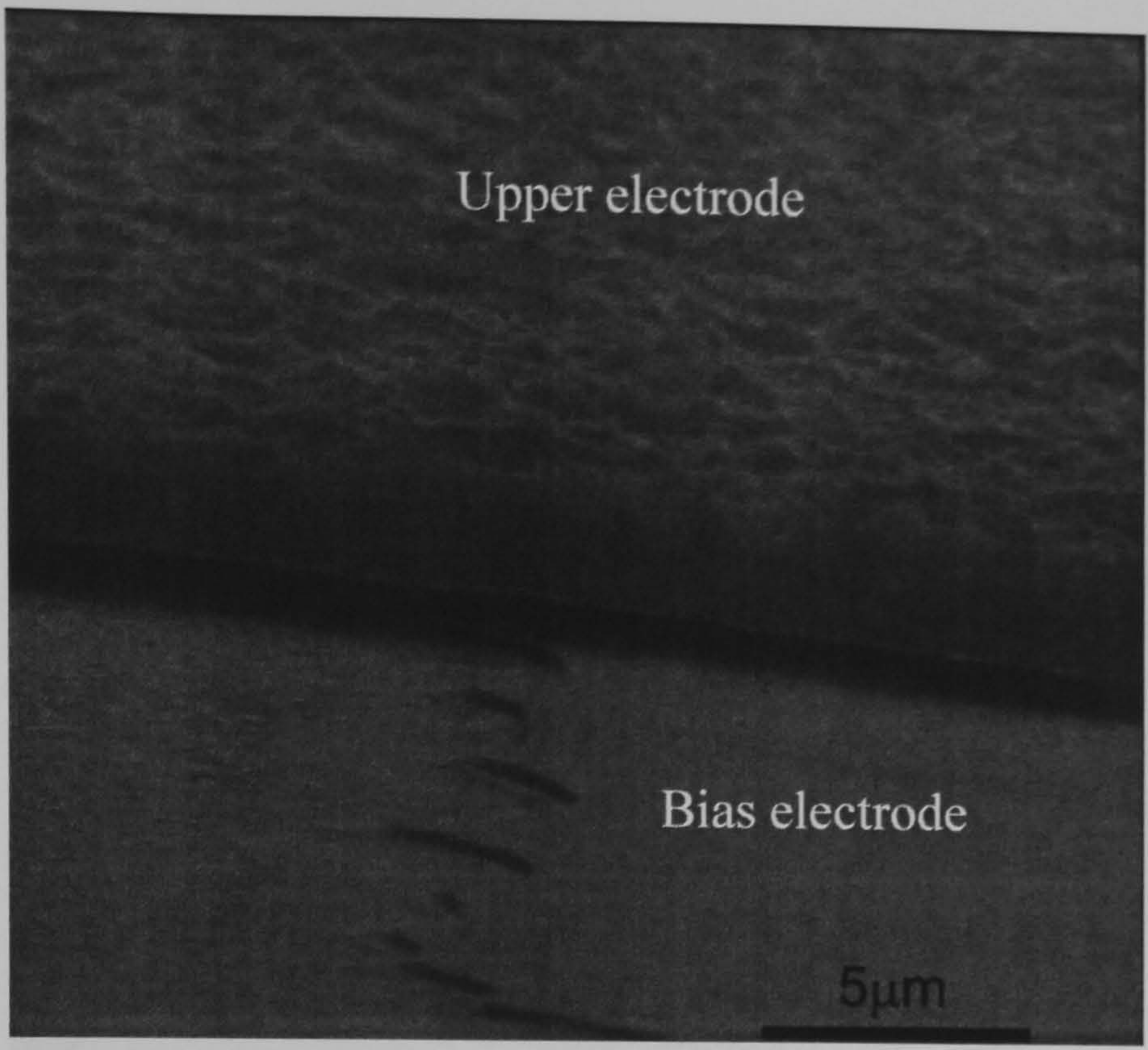


Fig. 6.13 A SEM image of the bias electrode region of stepped capacitor.

Fig. 6.14 shows the electrical tuning response of this capacitor. A maximum tuning voltage of 5V gives a tuning ratio of 4.3:1 from an unbiased capacitance of 1.19pF. The tuning response is comparable to the nickel device in section 6.3.

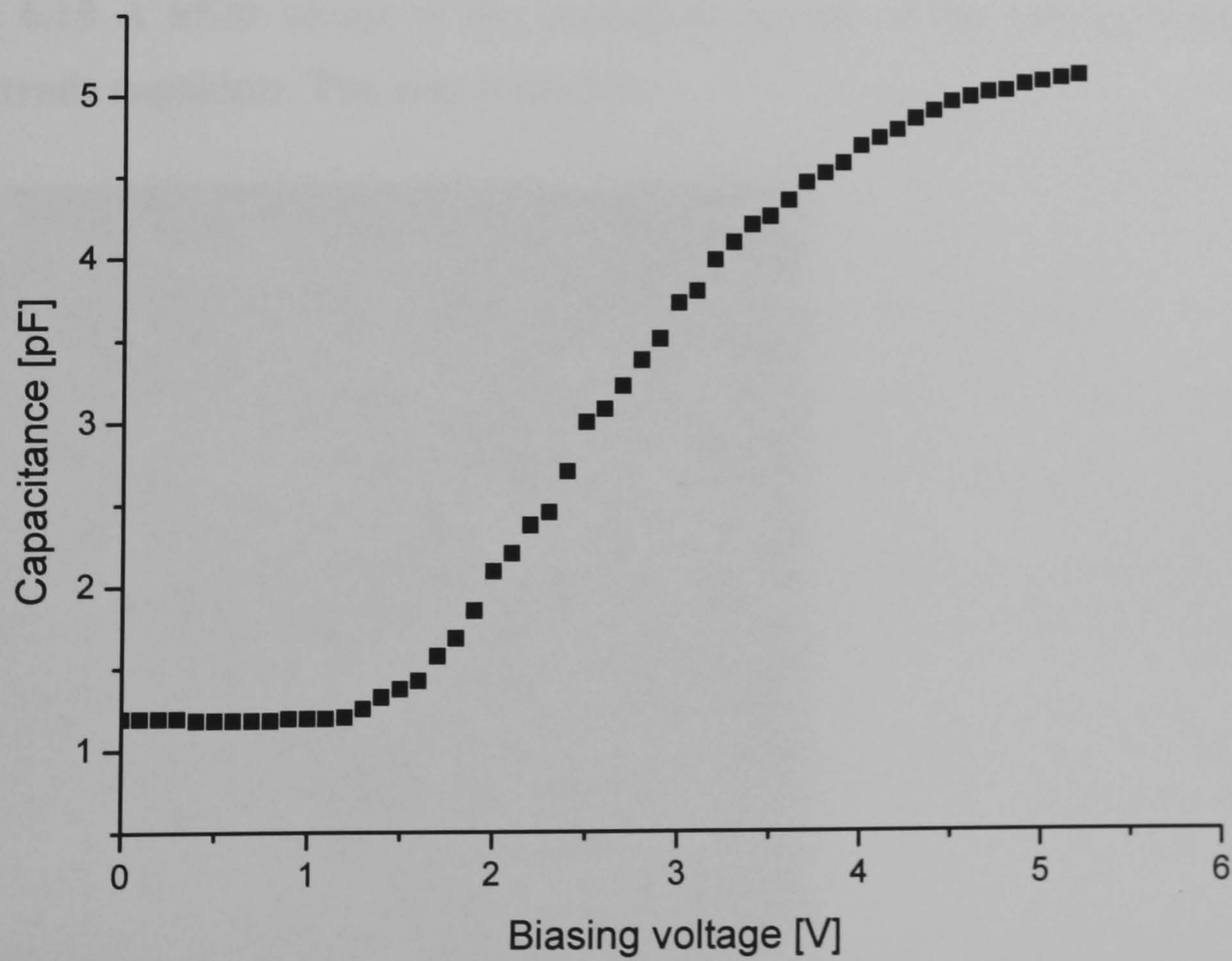


Fig. 6.14 The electrical tuning characteristic of the stepped capacitor.

6.5.2 Bowing upper electrode

This device is essentially the same as in the previous section but the upper electrode stress is higher which leads to additional bowing. Fig. 6.15 shows the step in the capacitive electrode region but the gap is greater than that found in fig. 6.12. This is further evident when compared to the bias electrode gap shown in fig. 6.16.

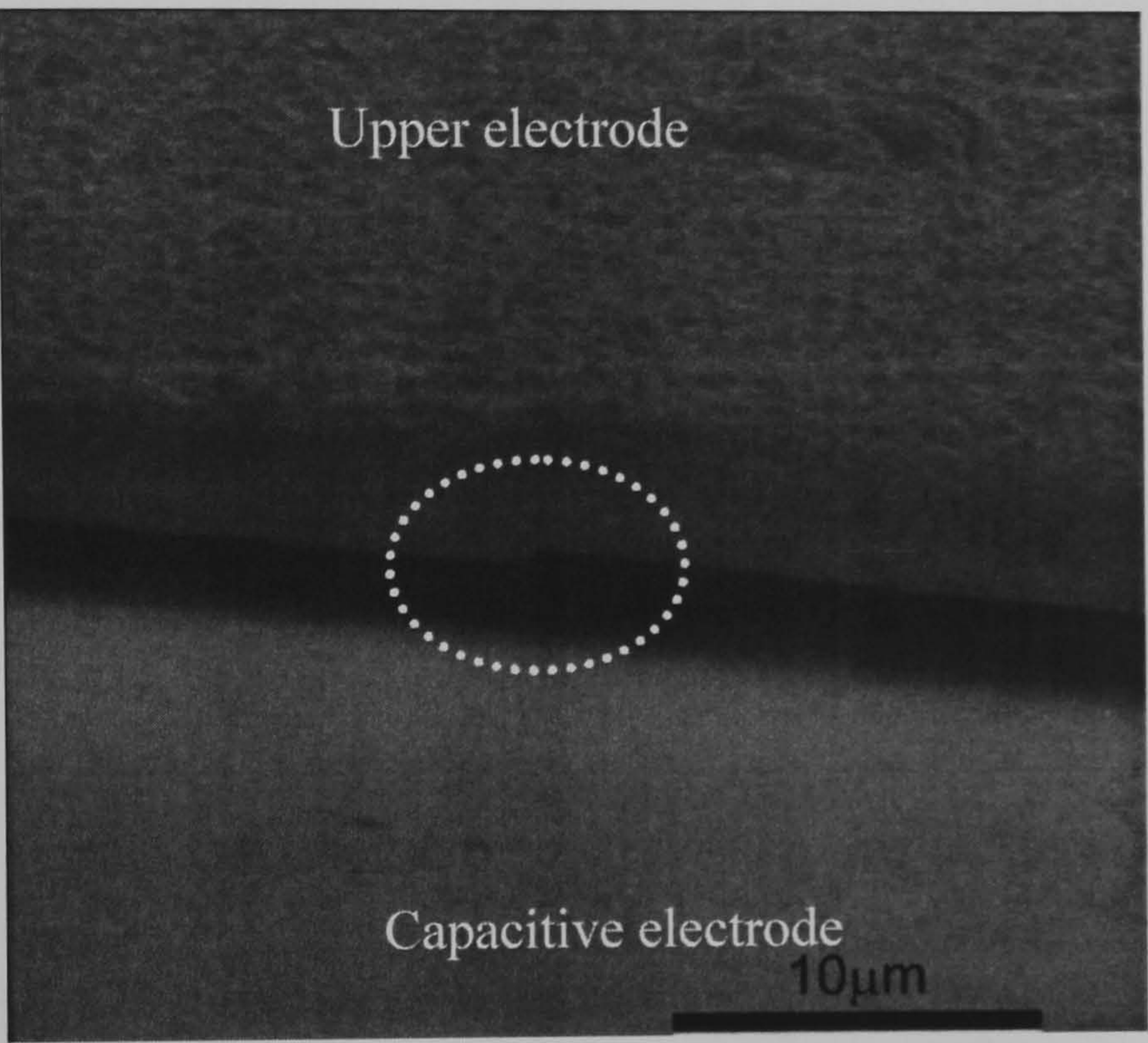


Fig. 6.15 A SEM image of the capacitive region of the bowing stepped upper electrode capacitor. The step is circled.

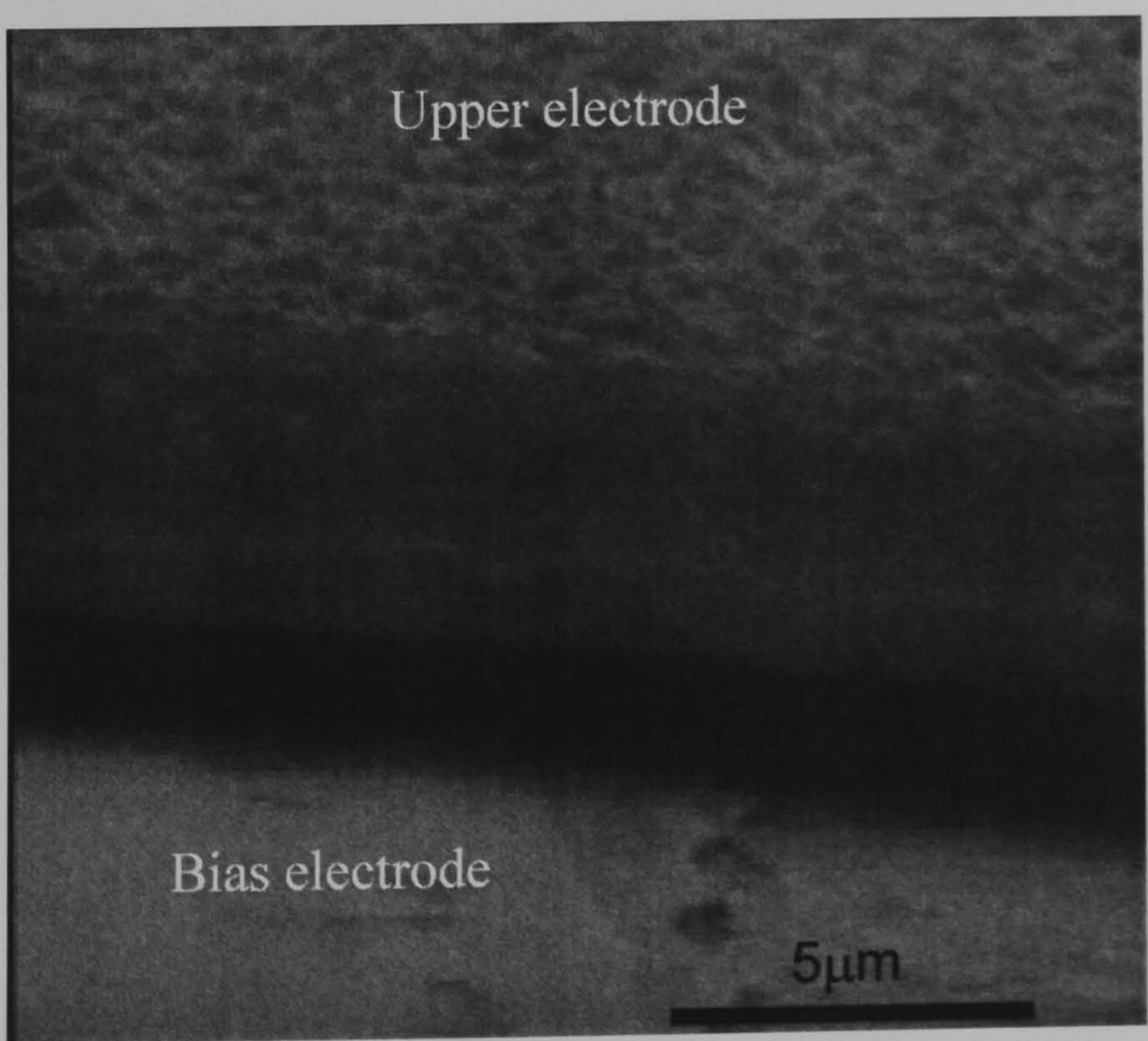


Fig. 6.16 A SEM image of the bias gap region of the bowing stepped upper electrode capacitor.

In line with the results from the gold structure, earlier, the electrical tuning charactistic shown in fig. 6.17 requires a higher biasing voltage. A tuning ratio of 3:1 is achieved from an initial capacitance of 0.84pF for a peak voltage of 30V.

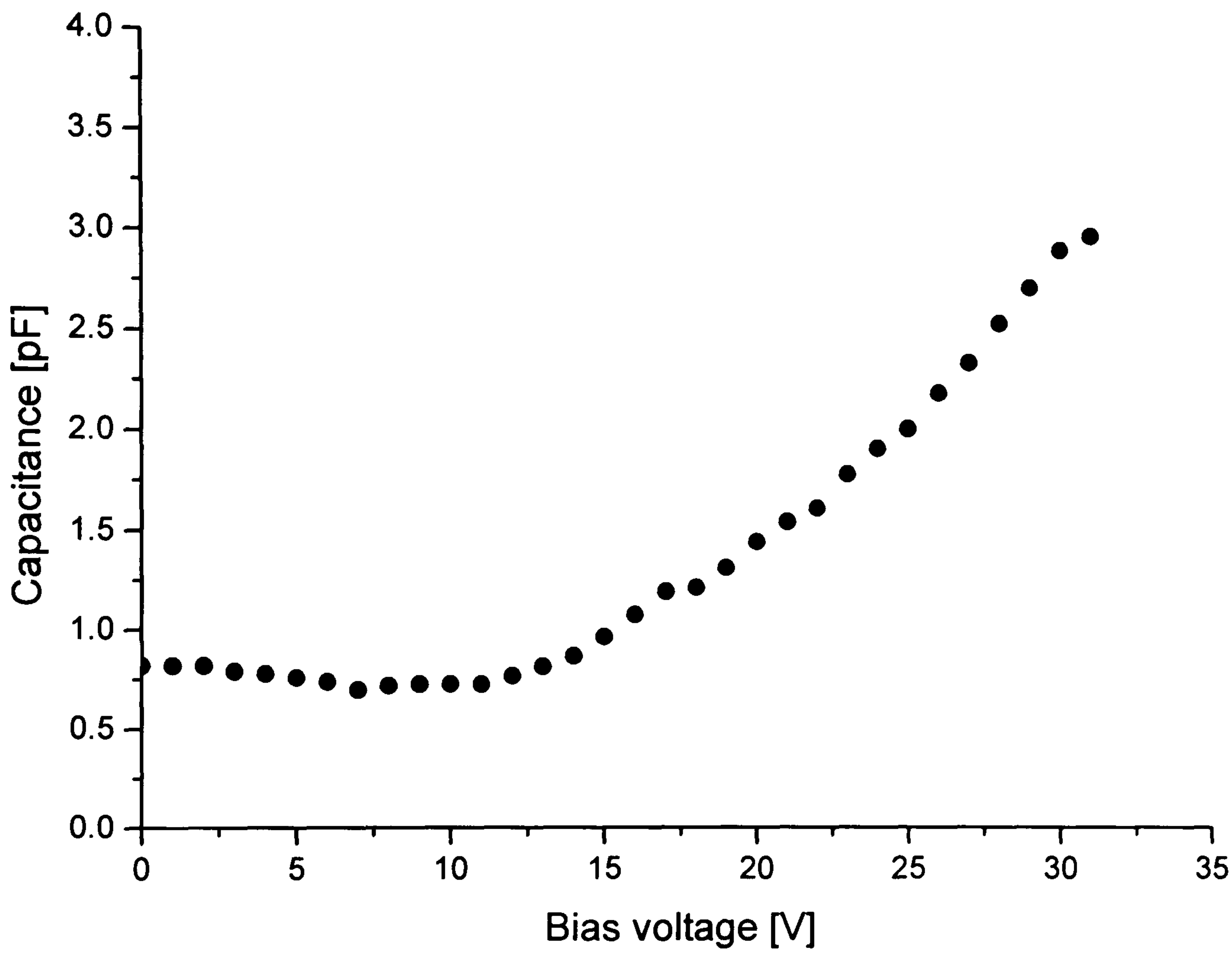


Fig. 6.17 Electrical tuning characteristic of the bowed upper electrode capacitor.

6.5.3 Thick central electrode device

This device is from a fabrication perspective comparable to the devices in the previous sections with a thick central electrode. Fig. 6.18 shows a side SEM view of the thick central electrode. Unlike, the stepped structures, the step in the upper electrode is no longer visible. This is an ideal case for a thick central electrode structure.

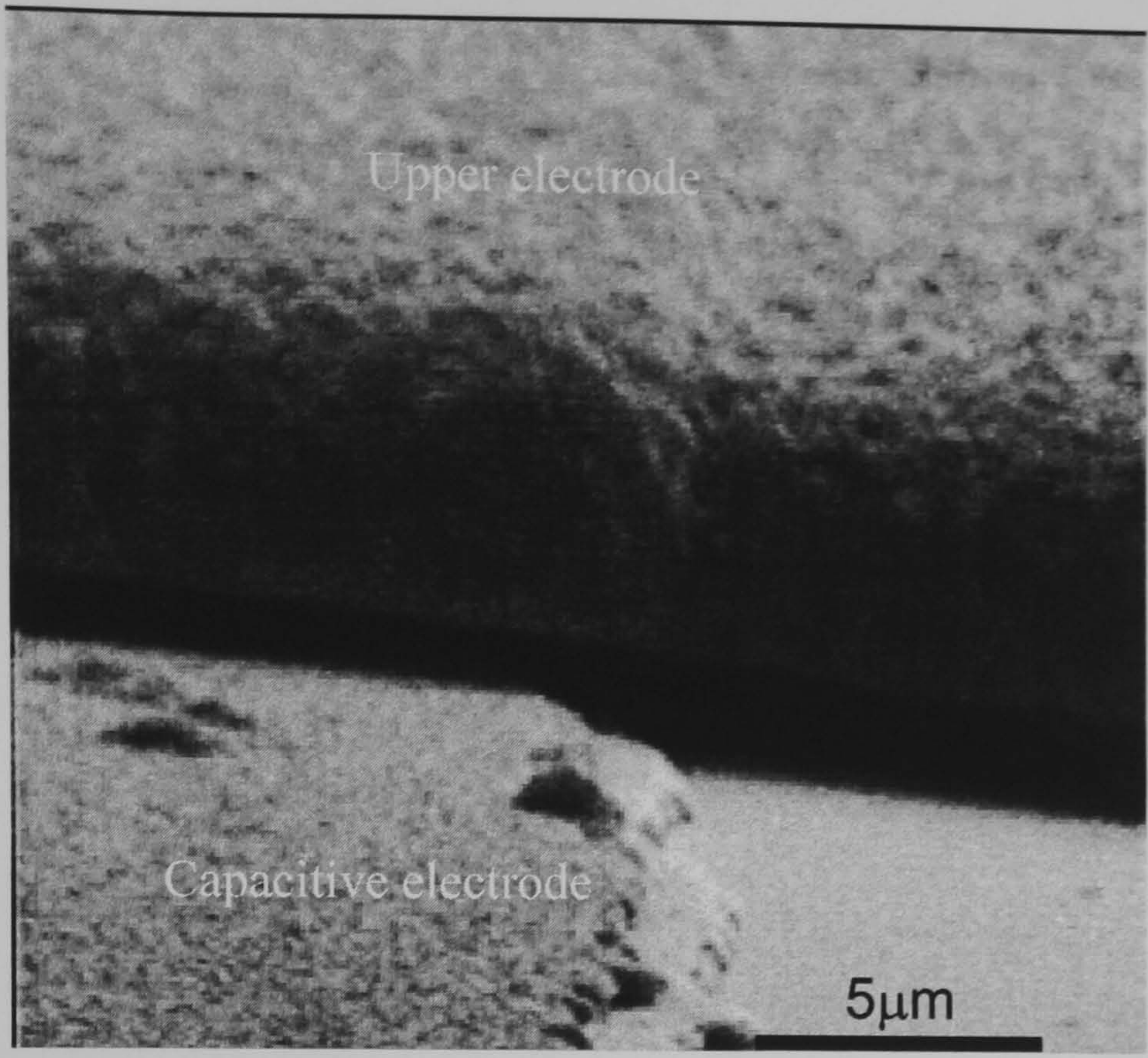


Fig. 6.18 A SEM image of the capacitive electrode area of thick central electrode device

Fig. 6.19 shows the bias voltage gap. Fig. 6.20 shows the tuning characteristic of the device. As minimal bowing is evident in the upper electrode again low voltage tuning can be achieved. A tuning ratio of 4:1 from an unbiased capacitance of 1.29pF is achieved for a bias voltage of 5V.

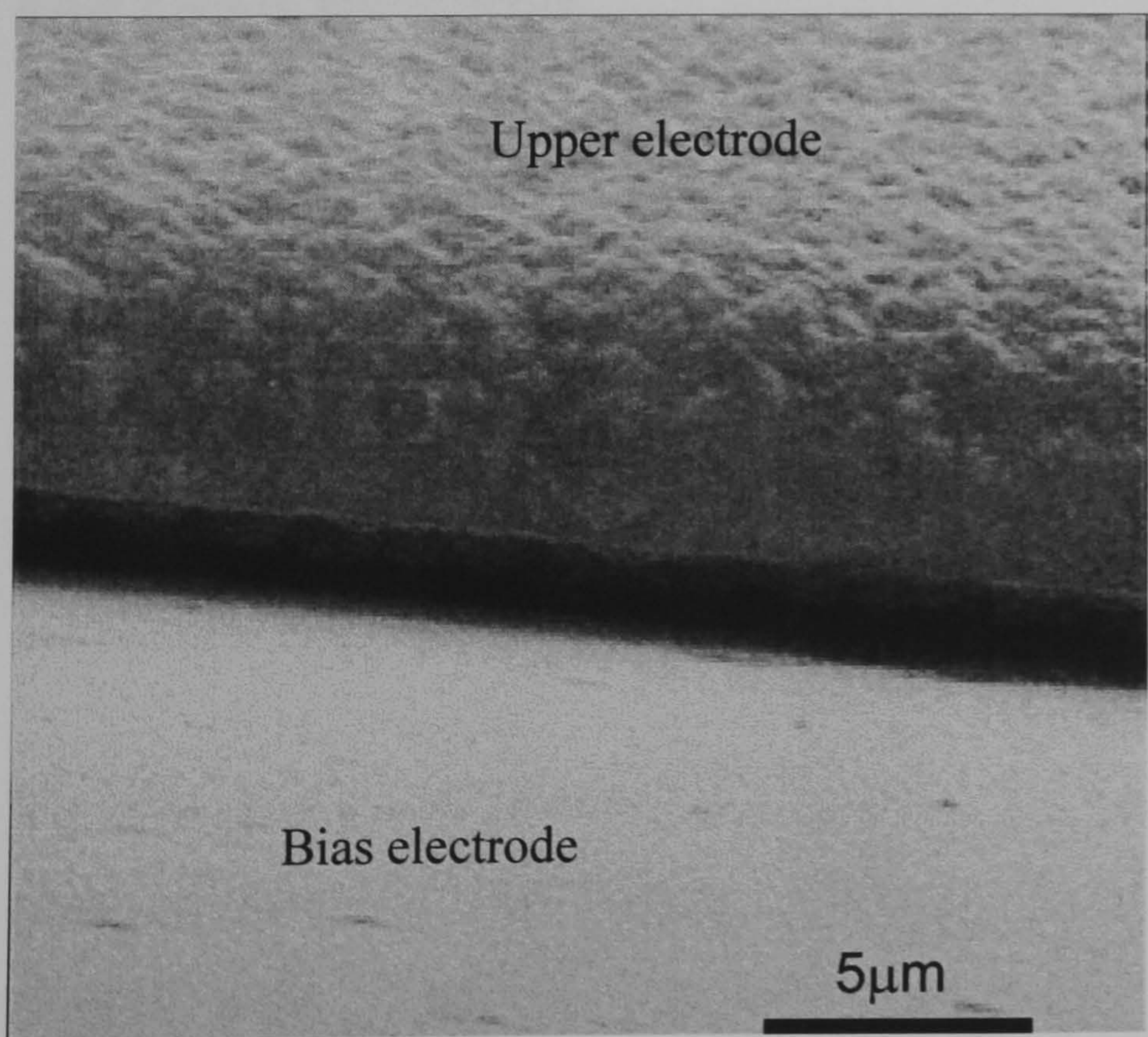


Fig. 6.19 A SEM image of the bias electrode area of thick central electrode device

These three devices were extracted from high yield wafers. The following section examines key failure mechanisms for the devices.

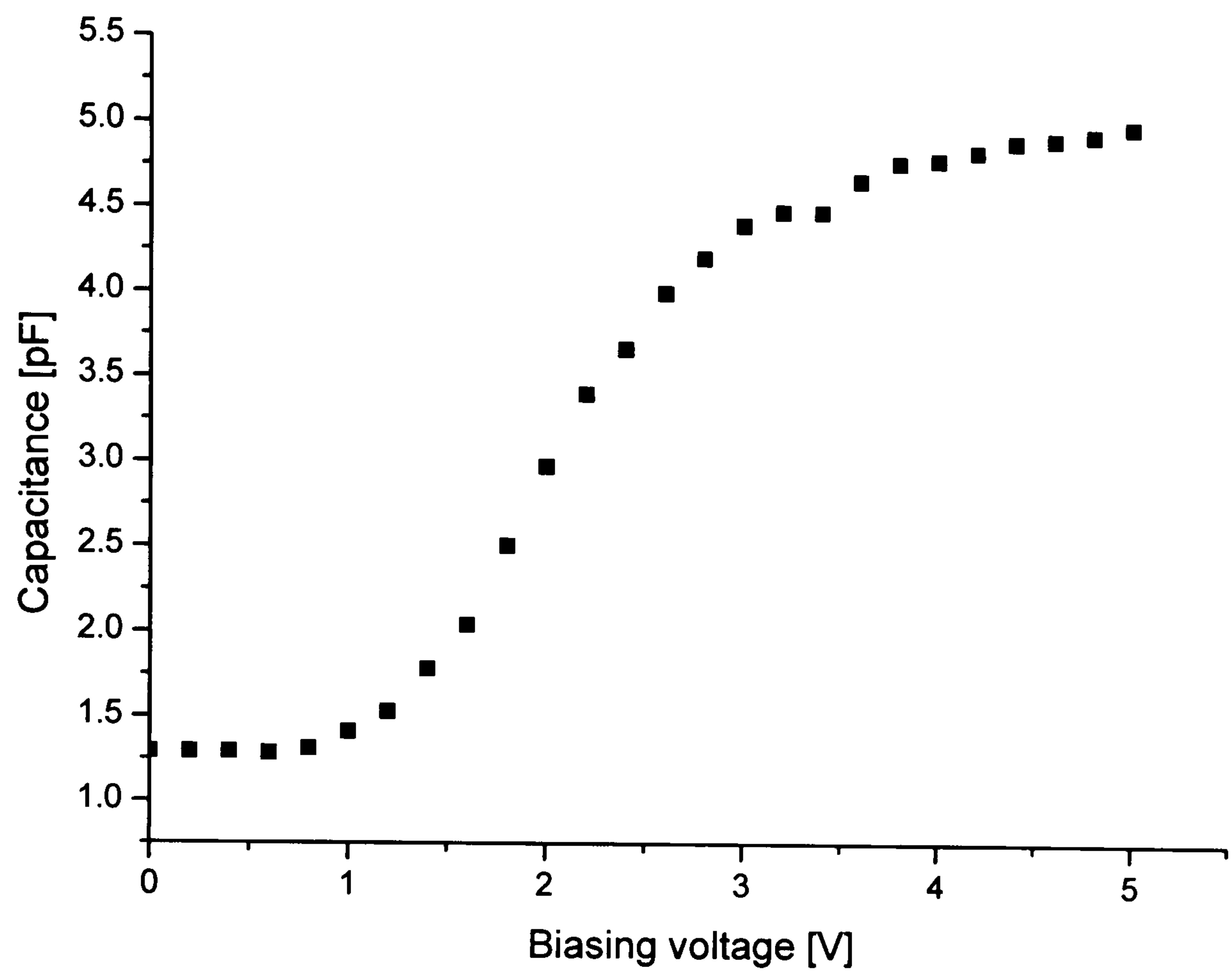


Fig. 6.20 Electrical tuning characteristic of the thick central electrode capacitor

6.5.4 Failure mechanisms

6.5.4.1 Adhesion failure

Adhesion failure at any processing stage introduces a considerable weakness into the device. If the adhesion of the anchors to the substrate is poor then the devices will detach from the substrate during release etch. Alternatively, adhesion can be poor between the electroplated and the evaporated metals causing delamination.

Fig. 6.21 shows a SEM view of the anchors delaminating. Adhesion failure is often observed if organic scum remains on the plating seed. The effect is to increase the electrode gaps.

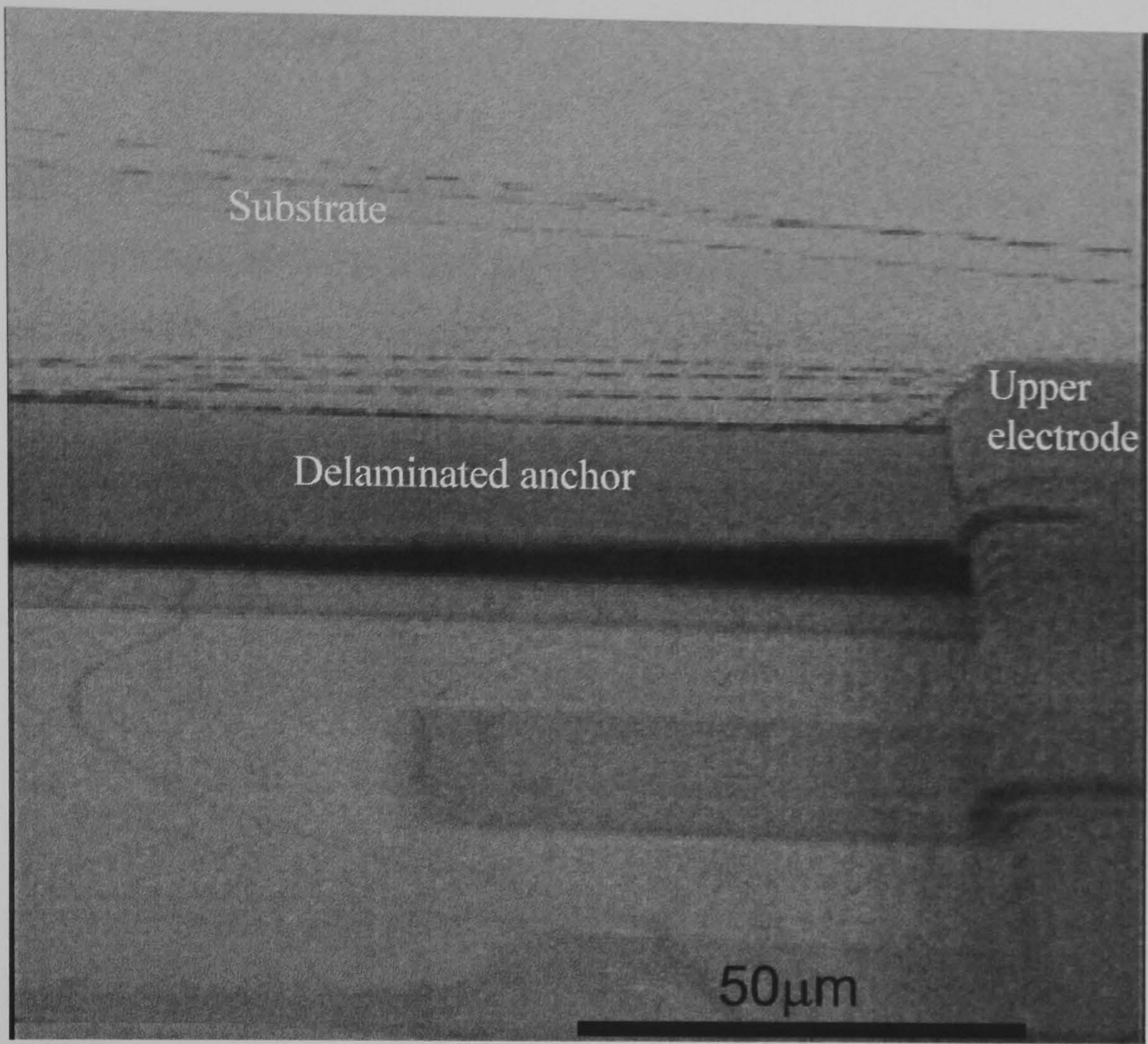


Fig. 6.21 A SEM image of delaminated anchors in a micromachined capacitor.

Delamination can also occur if the substrate fails during wafer dicing. In fig. 6.22 the silicon substrate has cleaved through a device, causing the anchors to fail.

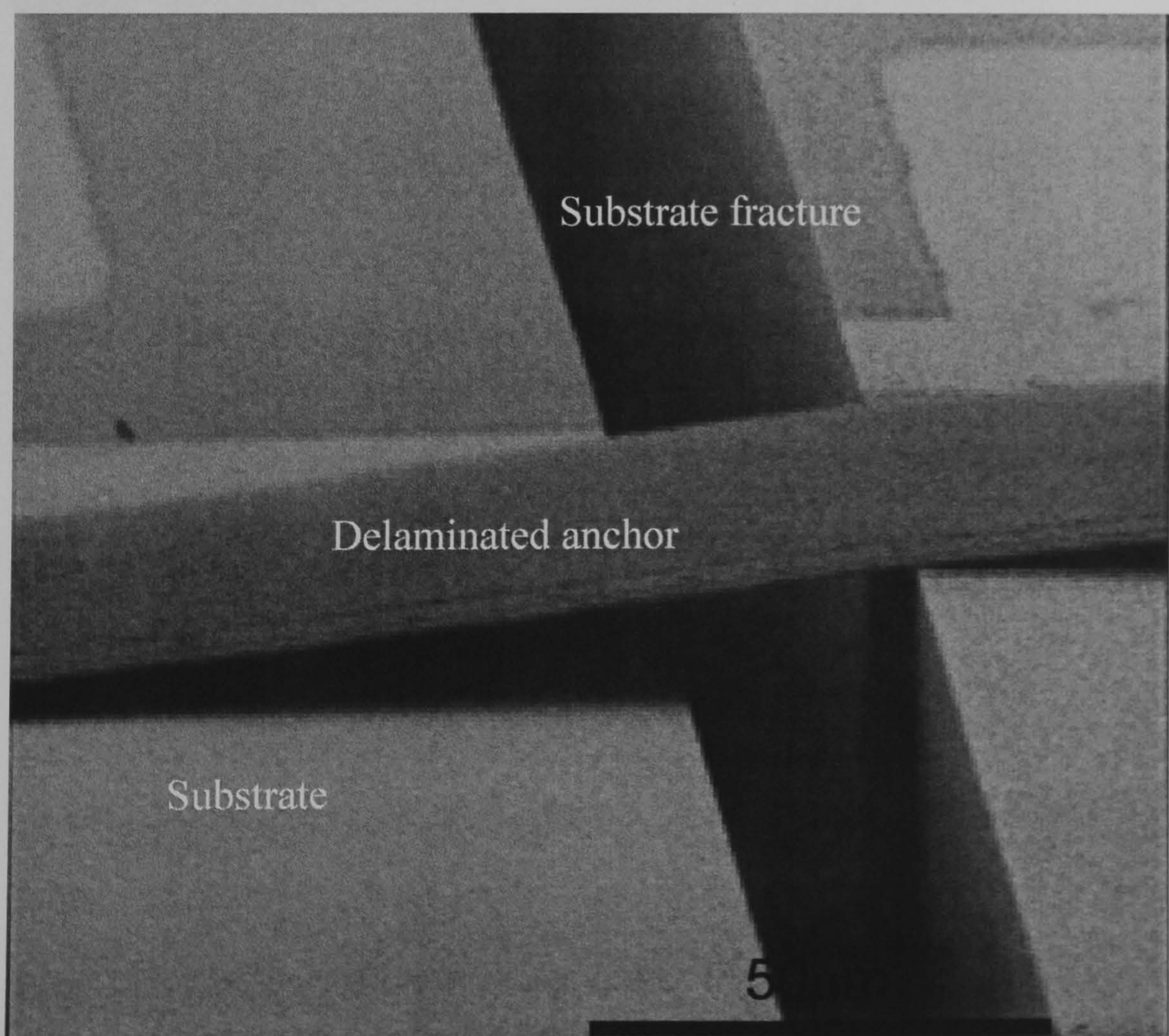


Fig. 6.22 A SEM image of delaminated anchors in a micromachined capacitor

6.5.4.2 Overplating

As described previously, a relatively simple technique was used to identify overplating. Since the etching of the titanium aperture causes underetching of the photoresist, a stepped ring exists in the electroplating deposit if it exceeds the thickness of the titanium.

Fig. 6.23 shows an electron micrograph of an overplated anchor. Anchor overplating is preferable to underplating because a step up in the top electrode, as shown in fig. 6.1, is avoided. A step up in the top electrode can introduce additional stress [120].

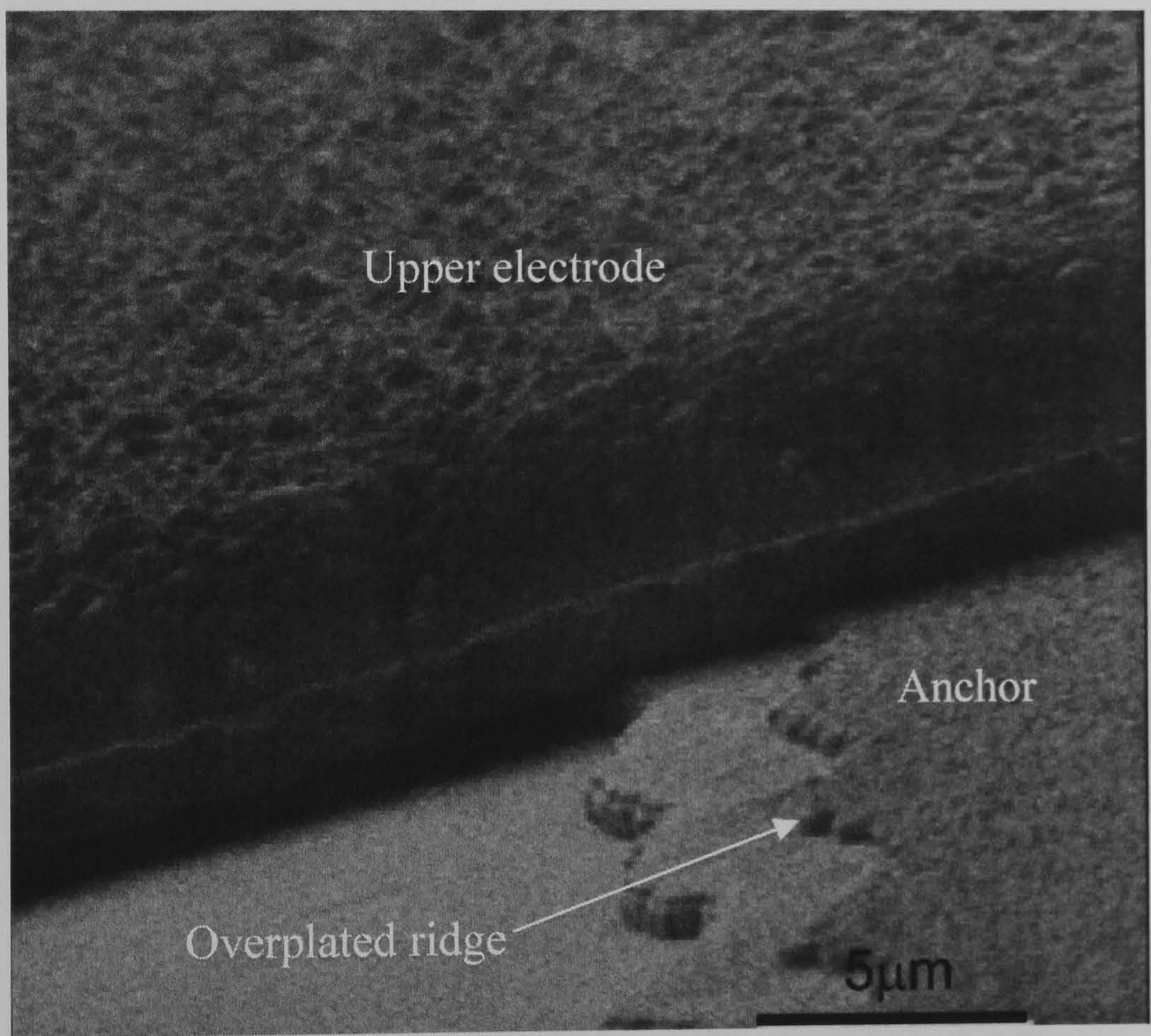


Fig. 6.23 A SEM image of the anchor region of a capacitor. In the bottom right the electroplated anchor can be seen. It has been overplated as indicated by the secondary ridge.

However, when overplating is applied to the central electrode, the effect on device performance was found to be catastrophic. The electron micrograph in fig. 6.24 shows the upper electrode resting on the overplated lower electrode causing shorting.

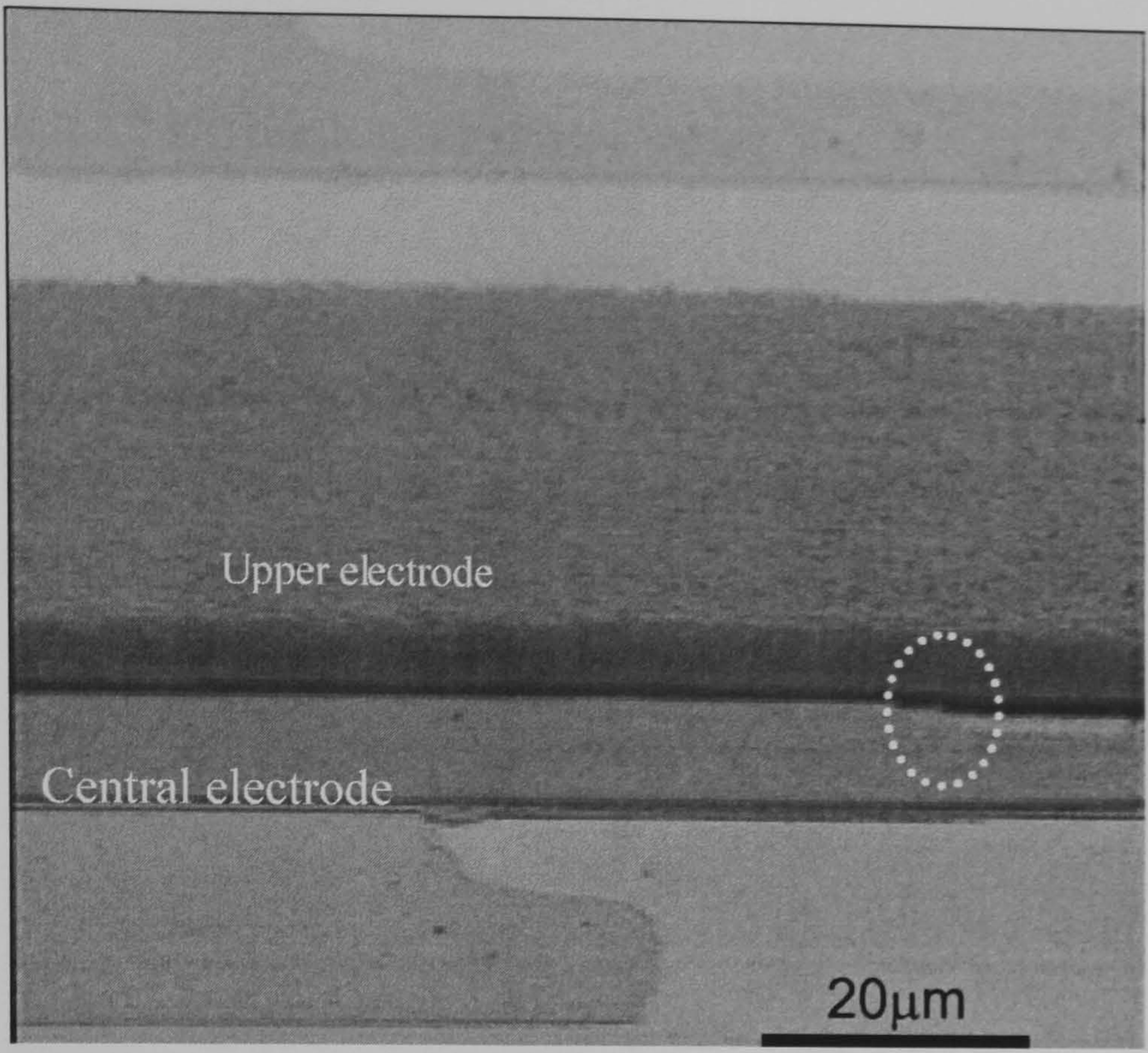


Fig. 6.24 A SEM image of an overplated central electrode. The ridge is circled.

6.5.4.3 Organic residue

Organic residue from photoresist contaminants is a further source of device failure. Inadequate removal of photoresist in stage B, in fig. 6.3, can lead to problems later on in processing. Electroplating initially can only occur through pinholes in the residue. This leads to uneven electroplating as shown on the lower electrode in fig. 6.25.

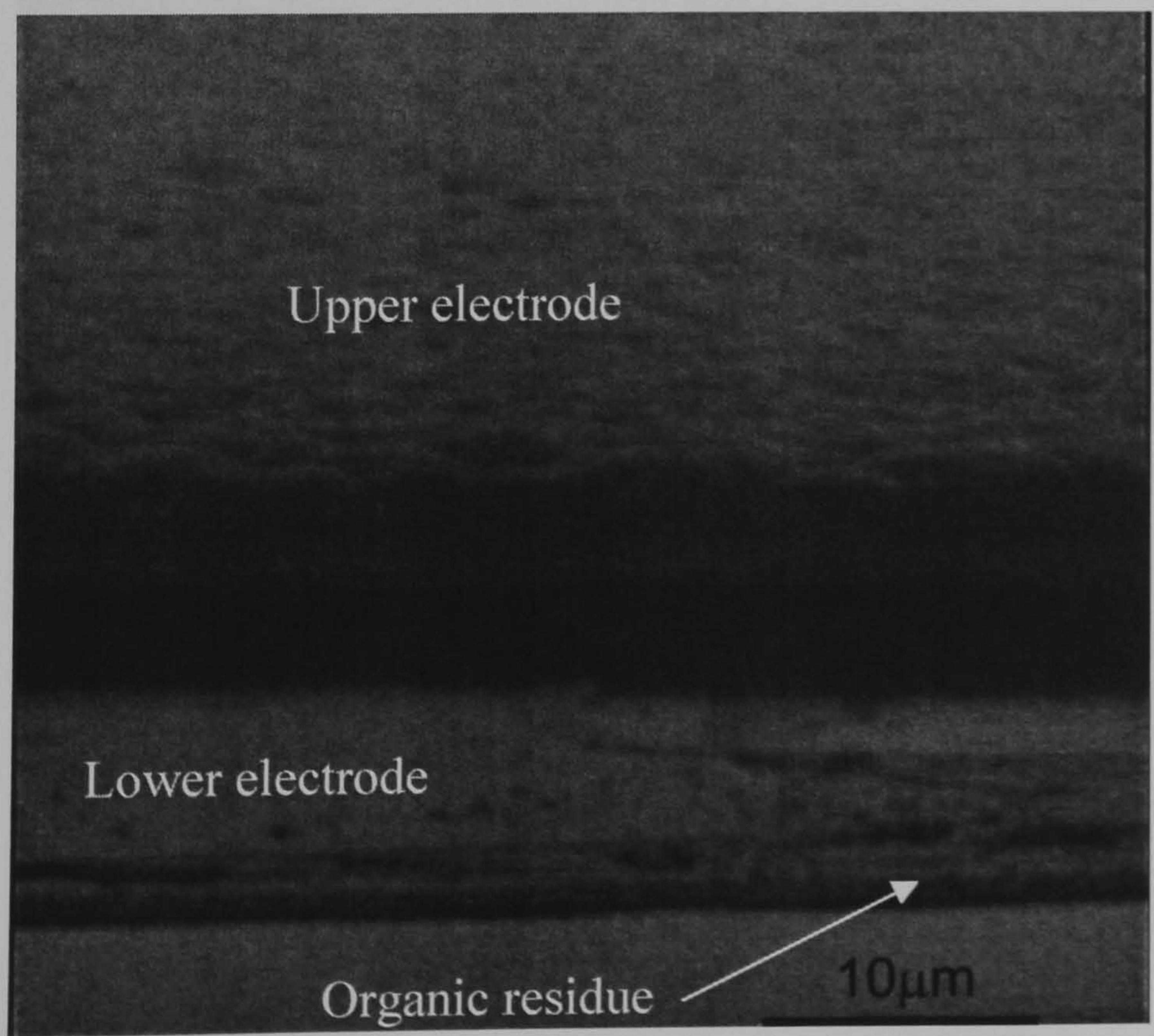


Fig. 6.25 This SEM image shows evidence of uneven plating on the lower electrode due to inadequate photoresist scum removal.

6.5.4.4 Extreme compressive stress

High stress compressive buckling was evident in early gold devices. However, ageing electroplating solutions or very low current densities can also lead to stress buckling of the nickel devices. This is shown in fig. 6.26.

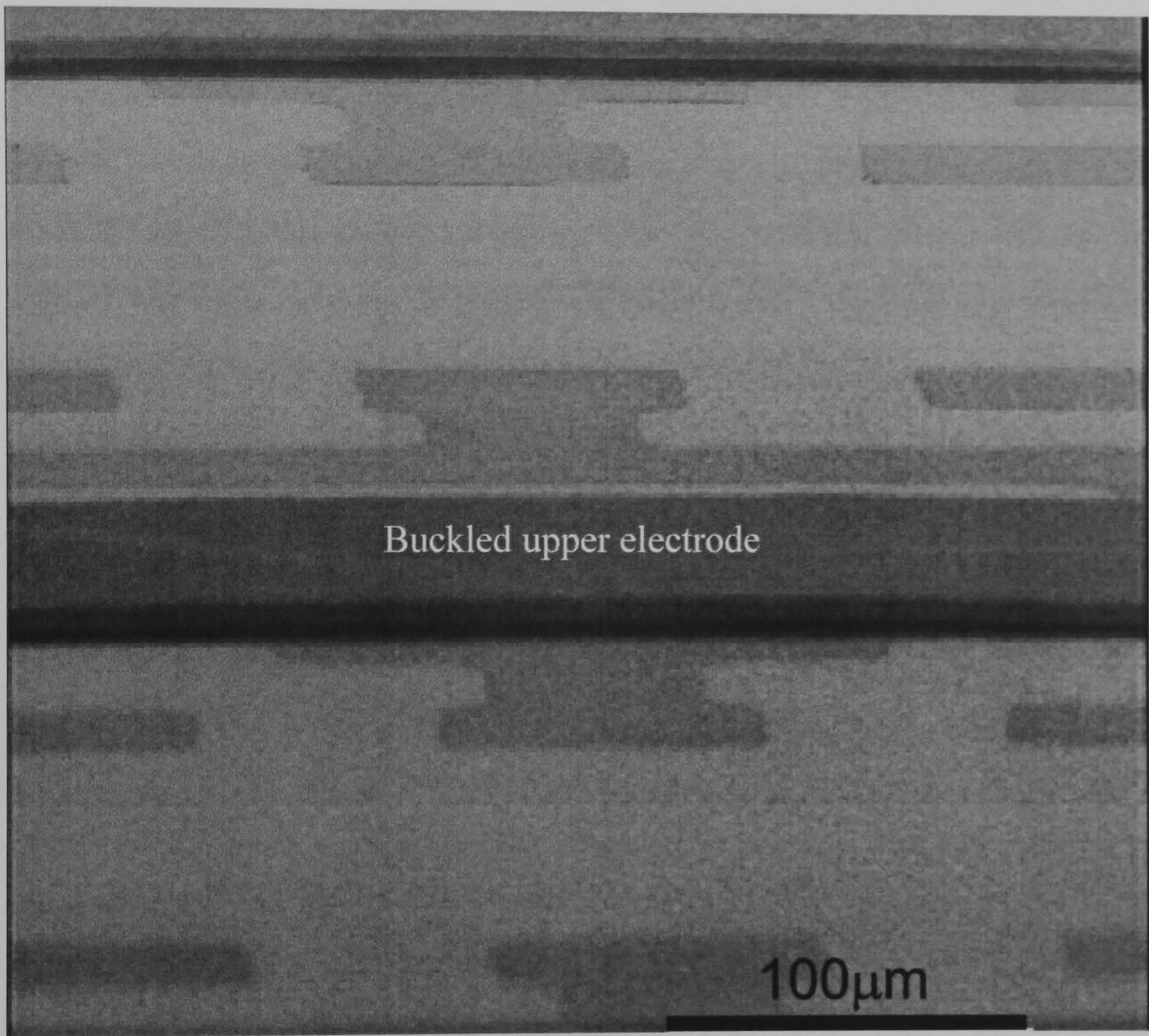


Fig. 6.26 A SEM image showing buckling of nickel devices

6.5.4.5 Stiction

Stiction failure is commonplace in surface micromachined devices. In use stiction is not a primary consideration for the capacitor because the electrodes should not contact during normal device operation. However, release stiction is an important consideration especially with sub micron gaps.

The HF:ethanol approach was chosen because the low surface tension of the ethanol enables deep penetration into high aspect ratio structures. This is confirmed by the relatively fast release of the devices presented in this chapter. However, in addition to surface tension, the topology of the closely spaced surfaces is an important consideration.

Stiction is related to contact area. Large area planar surfaces present a significantly increased chance of stiction failure due to large contacting surfaces. The aim of this section is to detail the transfer of topology through a capacitive structure. This analysis enables an insight to be gained into the microscopic topology.

In order to examine the topology transfer three primary zones of the capacitor have been studied using atomic force microscopy (AFM). These are the topside of the central electrode, the underside of the upper electrode over the central electrode and the underside of the upper electrode over a silicon region.

A Veeco Multimode AFM was used in contact mode. It has a relatively small maximum scan area of 13.5μm. Consequently, it is not feasible to track identical feature areas through the structure. However, general trends in surface roughness and topology characteristics are studied.

Surface roughness analysis in-situ of the underside of the upper electrode is currently not technically possible. To obtain this data the upper electrodes were lifted off the substrate using adhesive tape, and then examined with the AFM. Fig. 6.27 shows the underside of the nickel upper electrode in the region above the bare silicon. In this case the mean surface roughness is 73Å. This roughness is primarily associated with the 3000Å of evaporated titanium.

This shows that the finite surface roughness of the titanium transfers through to the underside of the upper electrode. Fig. 6.28 shows the surface topology of an electroplated nickel central electrode. A smooth metal grain is evident from the AFM scan. The mean surface roughness is 230Å.

Fig. 6.29 shows an AFM scan of the underside of the upper electrode in the region above the central electrode. This is essentially an inverted version of fig 6.28 with the lower electrode grain still visible. However, in addition the localised roughness associated with the evaporated titanium is also present, superimposed onto the grain pattern of the electroplated metal. The mean surface roughness in this region is 170Å.

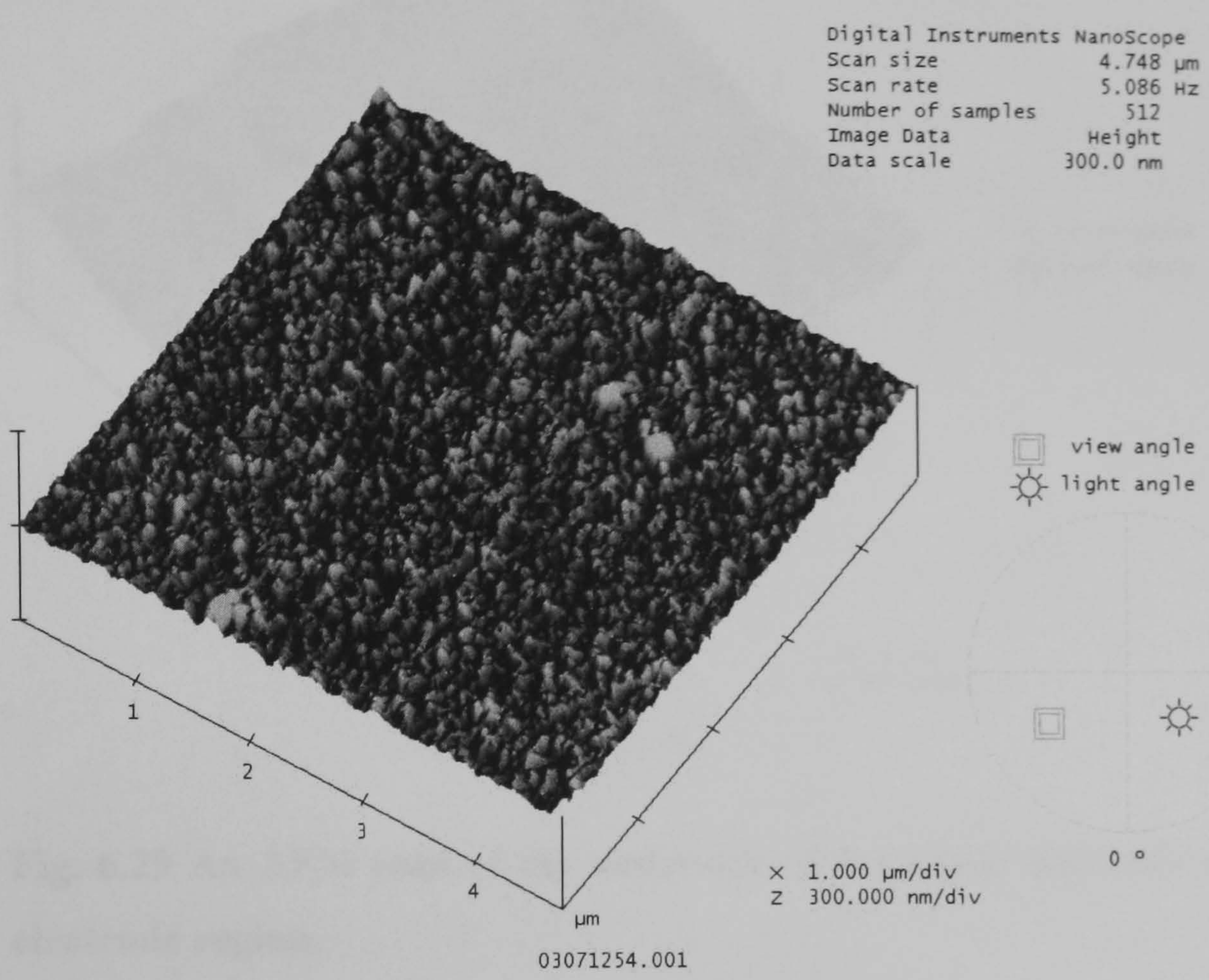


Fig. 6.27 The surface topology of the underside of the nickel upper electrode in the region above bare silicon

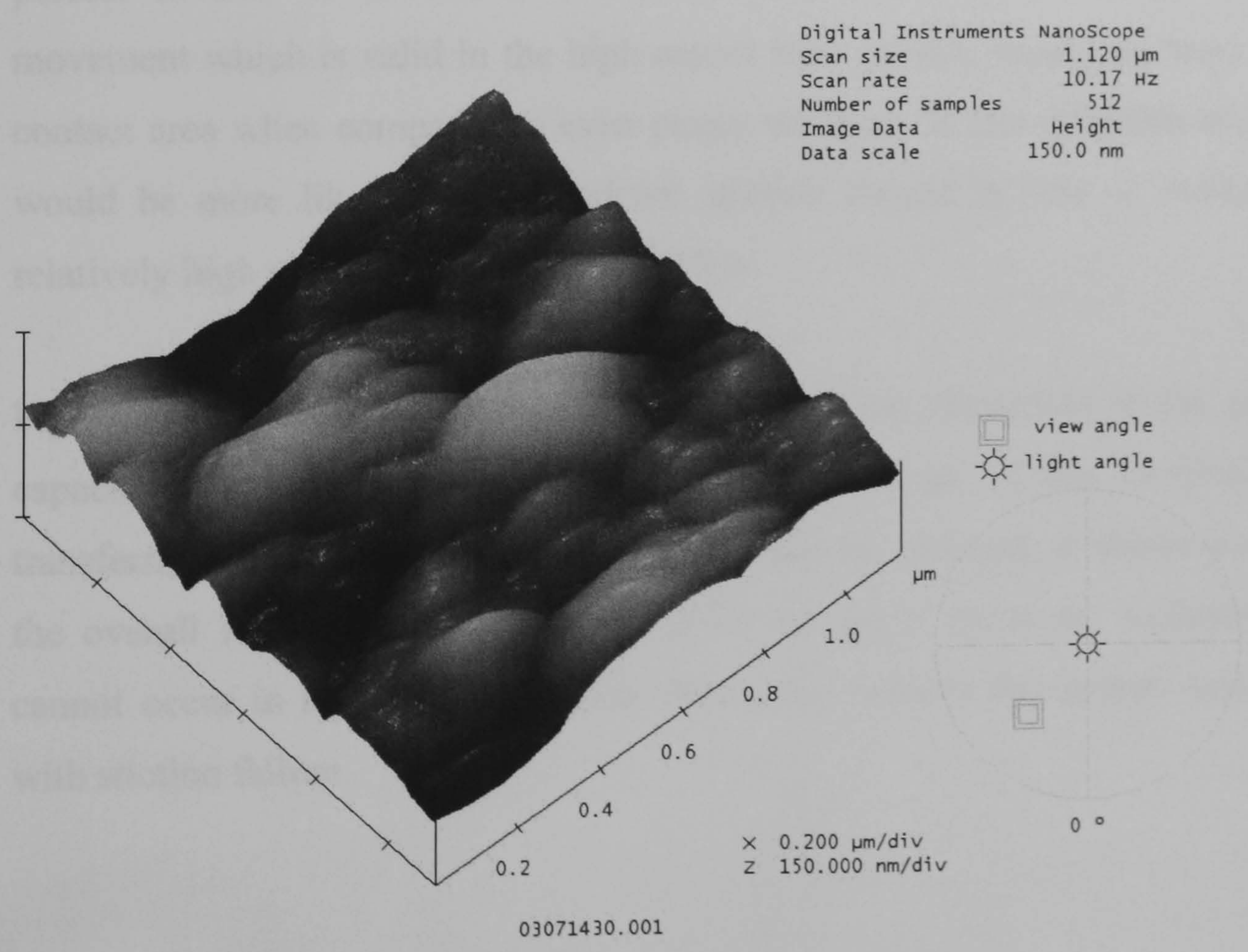


Fig. 6.28 An AFM scan of the electroplated nickel central electrode

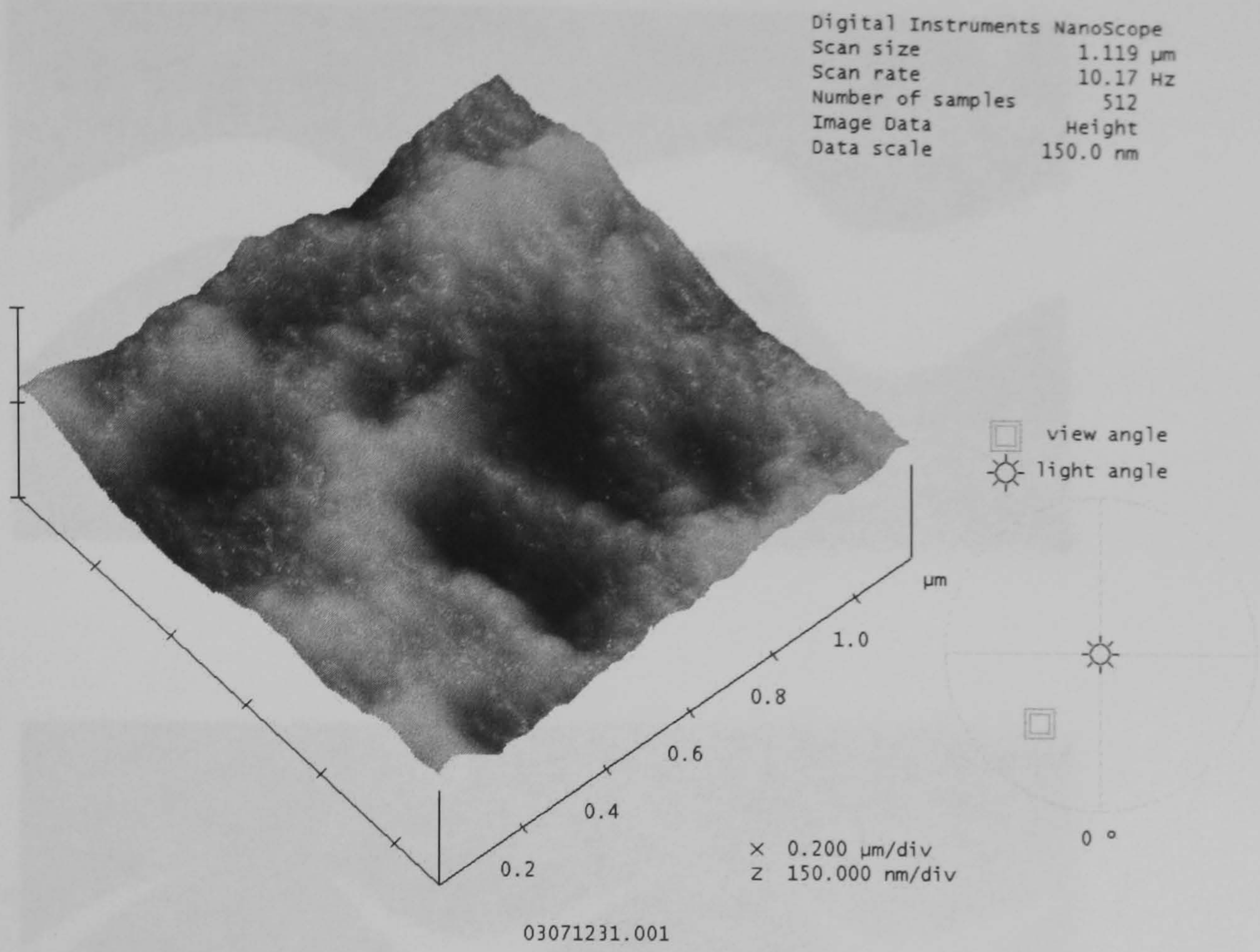


Fig. 6.29 An AFM scan of the underside of the upper electrode over the central electrode region.

Without the effect of the titanium sacrificial layer, the upper electrode would be a perfect inverse of the lower electrode. This in effect, assuming parallel plate movement which is valid in the high aspect ratio regime, would increase the surface contact area when compared to even planar surfaces. In this situation stiction failure would be more likely. Instead, release stiction should be low as indicated by the relatively high yields achieved of up to 95%.

Fig. 6.30 illustrates the model proposed for surface interaction in the electroplated capacitive structures. It shows the localised topology of the sacrificial titanium transferring to the underside of the upper electrode. Second, it shows a reduction in the overall surface roughness observed in the upper electrode. Complete meshing cannot occur in this situation which effectively reduces the contact area associated with stiction failure.

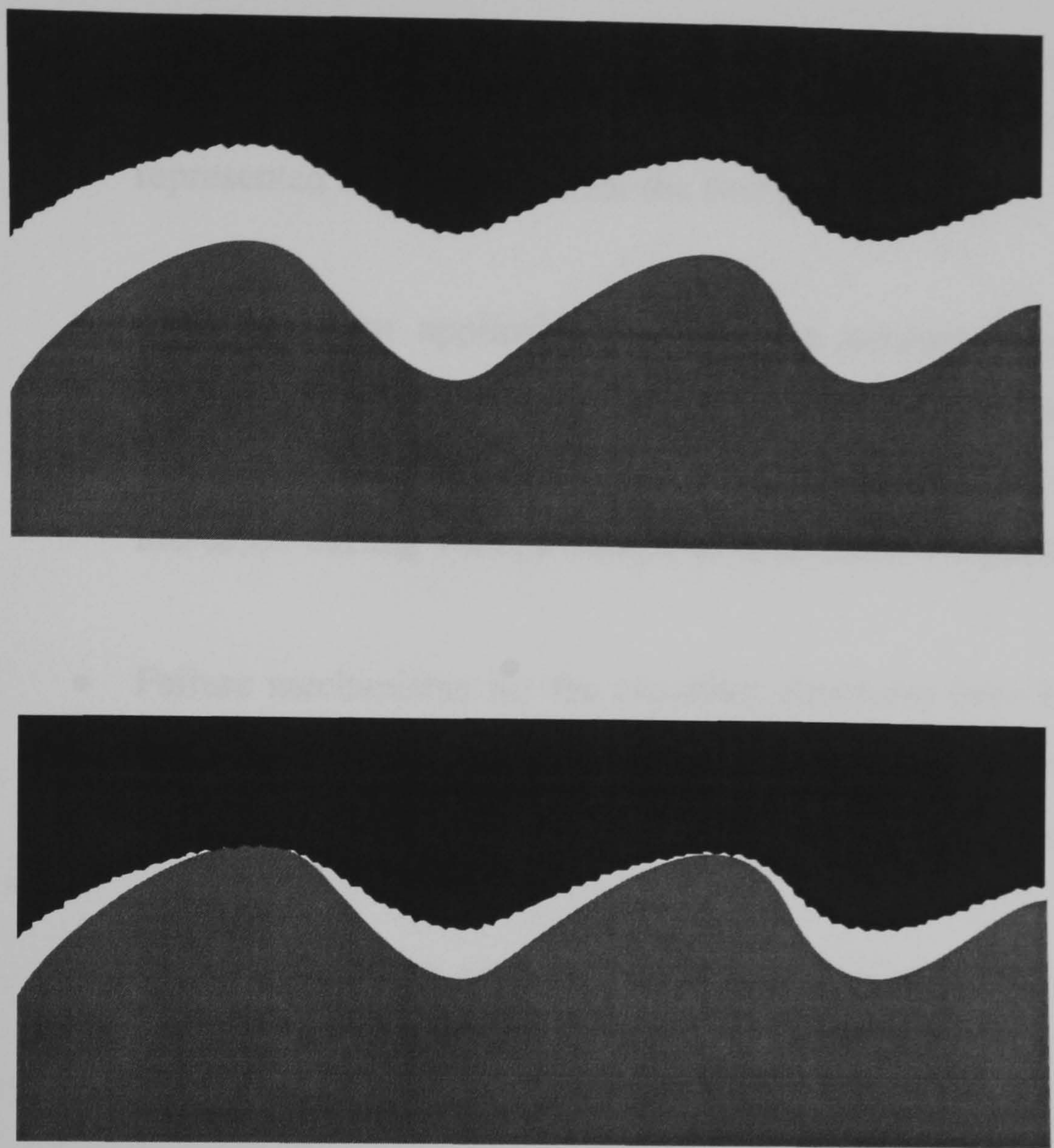


Fig. 6.30 An illustration of the surface topology of the electroformed capacitor with an electroplated central electrode.

6.6 Chapter summary

- Smaller biasing gaps reduce the tuning voltages required to actuate the device. This permits thicker metallisations to be applied to the upper electrode without impeding device performance.

- The use of small gaps produces high aspect ratio devices. Therefore, during deformation, the centre of the upper capacitive plate is acting in its optimum parallel plate configuration.

- A self-planarising, 'etch and fill technique' has been developed which uses electroplated metals for structural layers and titanium as a sacrificial layer.

- A two-gap nickel capacitor with a thick central electrode demonstrated a tuning ratio of 5.1:1 from an unbiased capacitance of 0.7pF. At the time this represented state of the art for the two-gap structure.

- The long term applicability of surface micromachining technique for RF MEMS relies upon the use of low resistivity structural metals such as gold. The tuning ratio for the gold device was 7.3:1 but at the expense of an increased biasing voltage compared to the nickel capacitor.

- Failure mechanisms for the capacitor structures have been identified through the use of electron microscopy. These include adhesion failure, over electroplating of the central electrode and organic residue.

- Without the effect of the titanium sacrificial layer, the upper electrode would be a perfect inverse of the lower electrode. This in effect, assuming parallel plate movement which is valid in the high aspect ratio regime, would increase the surface contact area when compared to even planar surfaces. In this situation stiction failure would be more likely. Instead, release stiction should be low as indicated by the high yields achieved of up to 95%.

Chapter 7

RF testing of tunable capacitors and inductors

As detailed in chapter 2, the primary application arena for the widely tunable capacitor is likely to be as part of an *LC* tank in tunable filters and voltage controlled oscillators. By using air as a dielectric, low loss performance should be achievable into the GHz regime. However, the use of air dielectrics alone does not ensure a good RF performance. Other factors, such as the substrate and metallisation, introduce losses into the performance.

Previous chapters focused on the tuning range of the two-gap design. This chapter reports on the RF properties of the devices. The important figure of merit for RF MEMS capacitors and inductors is the quality factor, Q. A high Q is indicative of a low loss device. This leads to sharper tuning peaks and significantly enhances the application opportunities for RF MEMS based devices.

In this chapter, the quality factor results for the capacitor design presented in the chapter 6 are reported. Alternative designs have been developed which use thicker metallisations to minimise RF losses in order to facilitate high Q operation. These process flows enable suspended inductors to be fabricated alongside the capacitors, which opens up the route to primary RF MEMS device integration.

7.1 Quality factor extraction from scattering parameters

The electrical quality factor, Q, can be calculated from the complex impedance as shown in eqn. (7.1).

$$Q = \frac{\Im z}{\Re z} \qquad \textbf{- (7.1)}$$

where $\Re z$ and $\Im z$ are the real and imaginary components of the complex impedance, Z, respectively.

Vector Network Analysers which are used to determine the RF response of a device, typically use scattering parameters instead of complex impedance. Therefore, the complex impedance, and hence Q, has to be derived from these parameters. Extraction from the scattering parameter, S_{11} can be achieved through eqn. (7.2).

$$Z = Z_0 \frac{1+S_{11}}{1-S_{11}} \quad \textbf{- (7.2)}$$

where Z is the complex impedance, Z_0 is the characteristic impedance and S_{11} is the reflected scattering parameter. Eqn. (7.3) shows Z in terms of the real, $\Re_{S11}$, and imaginary, $\Im_{S11}$, components of S_{11}.

$$Z = Z_0 \frac{1-\Re_{S11}{}^2 - \Im_{S11}{}^2}{(1-\Re_{S11})^2 + \Im_{S11}{}^2} + jZ_0 \frac{2\Im_{S11}{}^2}{(1-\Re_{S11})^2 + \Im_{S11}{}^2} \quad \textbf{- (7.3)}$$

Eqn. (7.4) shows the simplification that can be made when eqn. (7.3) is combined with eqn. 7.1, to provide a solution for Q in terms of the real, $\Re_{S11}$, and imaginary, $\Im_{S11}$, components of S_{11}.

$$Q = \frac{2\Im_{S11}}{1-(\Re_{S11}^{\ 2} + \Im_{S11}^{\ 2})} \qquad \textbf{- (7.4)}$$

As with S_{11}, the quality factor is a frequency dependent quantity. Since this equation has been derived from the general definition of electrical quality factor in eqn. 7.2, it is applicable to both capacitors and inductors.

7.2 Quality factor measurements for thin interconnect tunable capacitors

The first set of capacitors to be tested were fabricated in accordance with all gold designs in chapter 6, section 6.5. These were tested, at Filtronic, using an Agilent 8720ES vector network analyser with a Cascade Microtech probe station. An ISS standard calibration substrate was used to remove the parasitic effects of the probes from the results.

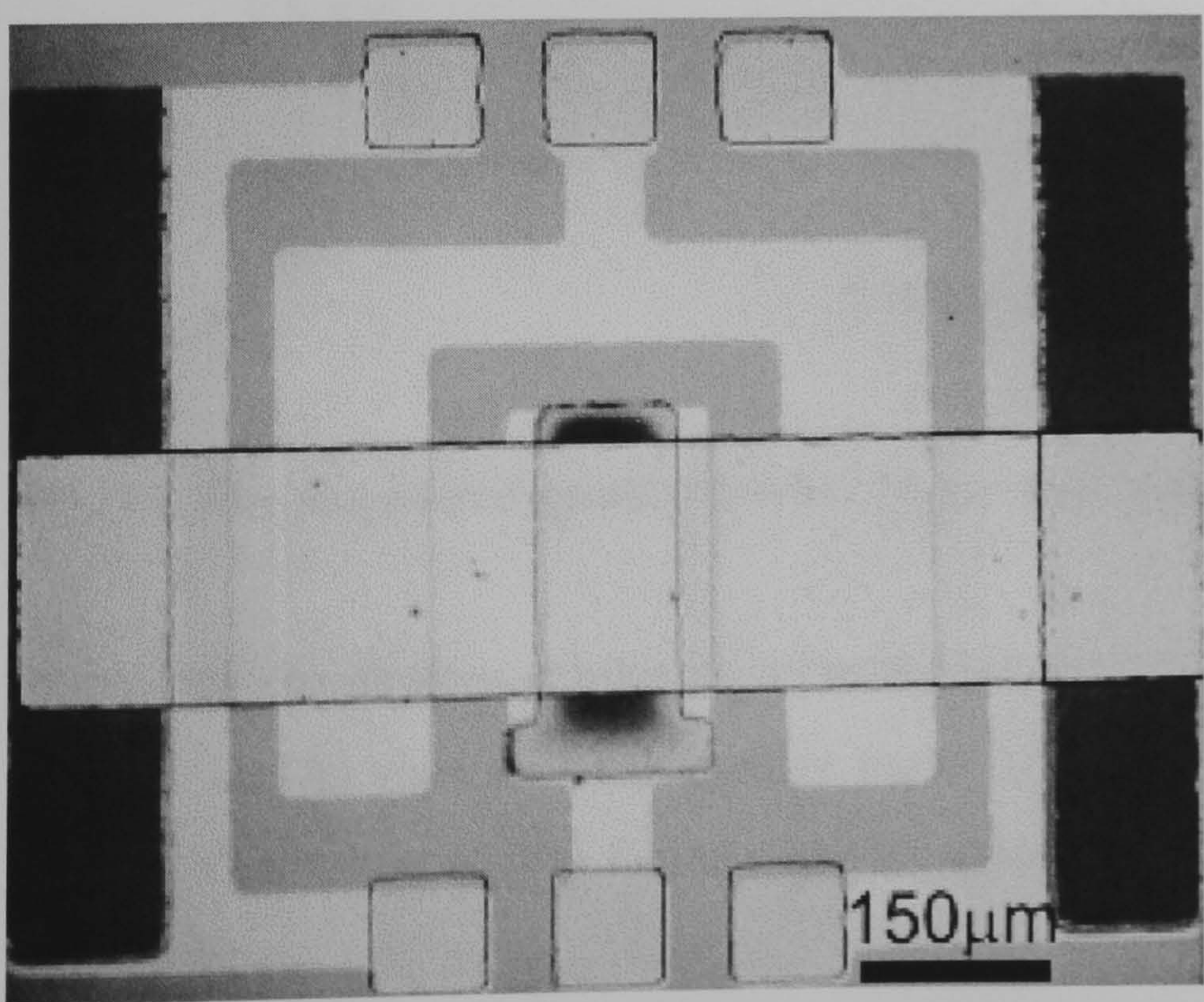


Fig. 7.1 A microscope view of a ground signal ground pad configuration on an all gold micromachined capacitor.

The devices were modified with the additional electroplating of thick gold pads. The interconnect pad structure is shown in fig. 7.1. This is a coplanar waveguide configuration with two ground pads either side of a signal line. These pads are 2 μm thick gold and spaced at 150μm to enable a Picoprobe GSG-150 RF probe to be used. Fig. 7.2 shows the extracted Q from four devices (A-D), which were tested on the same wafer.

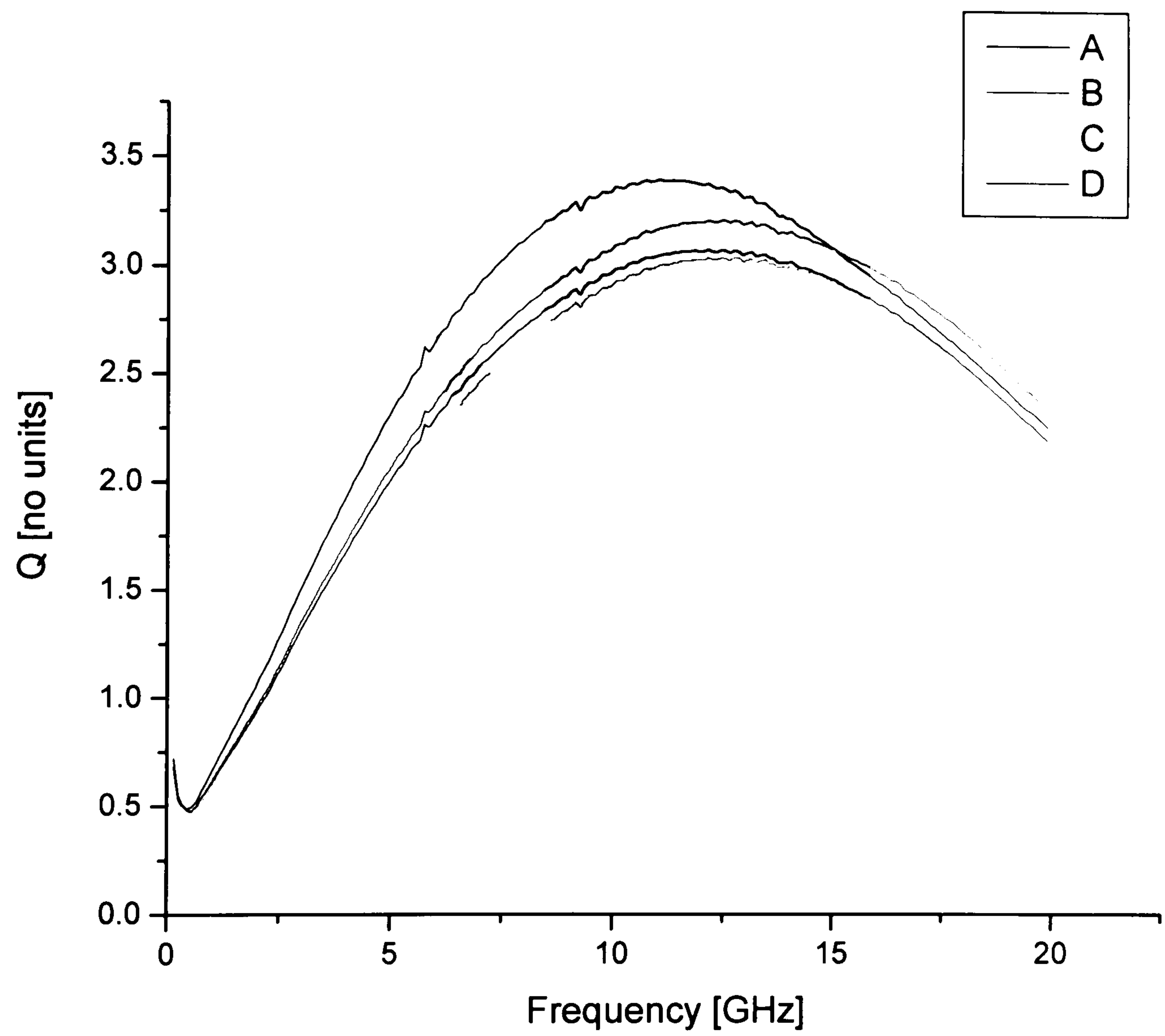


Fig. 7.2 The measured quality factor, *Q*, for four gold tunable capacitors.

In general, the devices exhibit highly comparable frequency responses. However, the best device (A) shows a peak quality factor is 3.4 at 11.4 GHz for a capacitance of 0.24pF. This a low quality factor when compared to the literature values presented in chapter 2.

This can be partially explained by the use of low resistivity silicon which introduces loss, especially at low frequencies. However, the next section will identify the interconnect thickness as being a further contributing factor.

7.3 Interconnect thickness and skin depth

The devices in section 7.2 showed a peak Q in the 11 to 12 GHz regime. This is fairly high for the peak to occur - typically the low GHz range has been reported elsewhere. The reason for placing the peak here is that several factors determine the frequency dependence of Q.

As detailed in chapter 2, Q, for a capacitor, can also be expressed as shown in (7.5).

$$Q = \frac{1}{wCR} \qquad \text{- (7.5)}$$

where w is the oscillation angular frequency, R is the equivalent series resistance and C is the capacitance. The equation shows that the quality factor will decrease with increasing frequency.

A second consideration is the R term. This represents resistive losses. In a DC conduction state, the current is distributed evenly throughout the metal. However, at RF, the current becomes increasingly localised to the edge of the conductor. The skin depth, δ, which can be calculated using eqn. 7.6, represents the penetration of signal into the conductor line.

$$\delta = \sqrt{\frac{2}{\mu_r \mu_0 \sigma \omega}} \qquad \text{- (7.6)}$$

where μ_r is the relative permeability, μ_0 is the permeability of free space, σ is the electrical conductivity and ω is the oscillation angular frequency.

Generally, μ_r, is unity. However, nickel has μ_r of 100 [121]. Fig. 7.3 shows the skin depth for gold and nickel conductors in the low GHz regime. Even though gold has a higher conductivity than nickel, it shows higher skin depths due to its low relative permeability.

Therefore to minimise losses in the 1 GHz region, the thickness of a gold conductor must exceed the skin depth of 2.4 μm. The devices in section 7.2 have a minimum interconnect thickness of 0.04 μm. This acts as a resistive bottleneck and therefore only at high frequencies (over 10 GHz) are the losses associated with skin depth minimised.

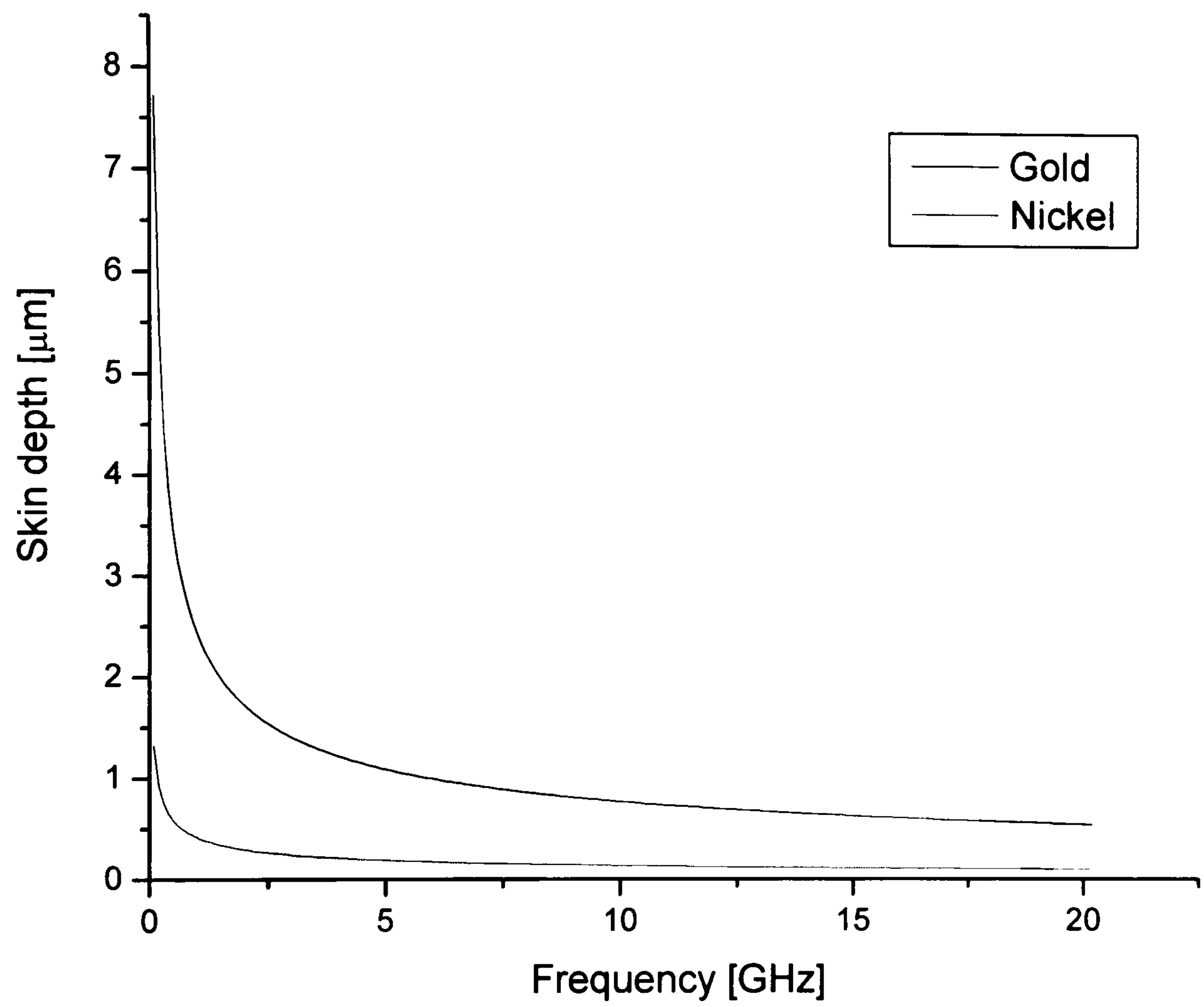


Fig. 7.3 Calculated skin depth for gold and nickel conductors as a function of frequency.

At low frequencies, the skin depth exceeds the metallisation thickness and dominates resistive losses. This acts to suppress the quality factor. These losses reduce with increasing frequency, which effectively elevates Q. However, in parallel, Q is falling away due to increasing frequency. Therefore, a point is reached between optimally low resistive losses and peak frequency dependent Q.

In order to achieve the highest quality factor this optimum frequency has to be as low as possible. Therefore, it follows that the skin depth related losses have to be minimised.

Ideally, the interconnect and metallisation thicknesses should exceed the skin depth at the low frequency. Due to the limitations of the self-planarising process presented in chapter 6, the interconnect cannot be significantly increased above its 0.04μm thickness without impeding the device planarisation. This is illustrated in fig. 7.4.

If the interconnect thickness becomes in the order of the sacrificial layer then the topology can be extreme (from the perspective of this device). Furthermore, the limitations with the maximum evaporated titanium thickness limit its applicability to form thick interconnect without stress fracturing. The devices presented in the following sections have a modified process flow which enables the interconnect thickness to be increased to 6.2μm.

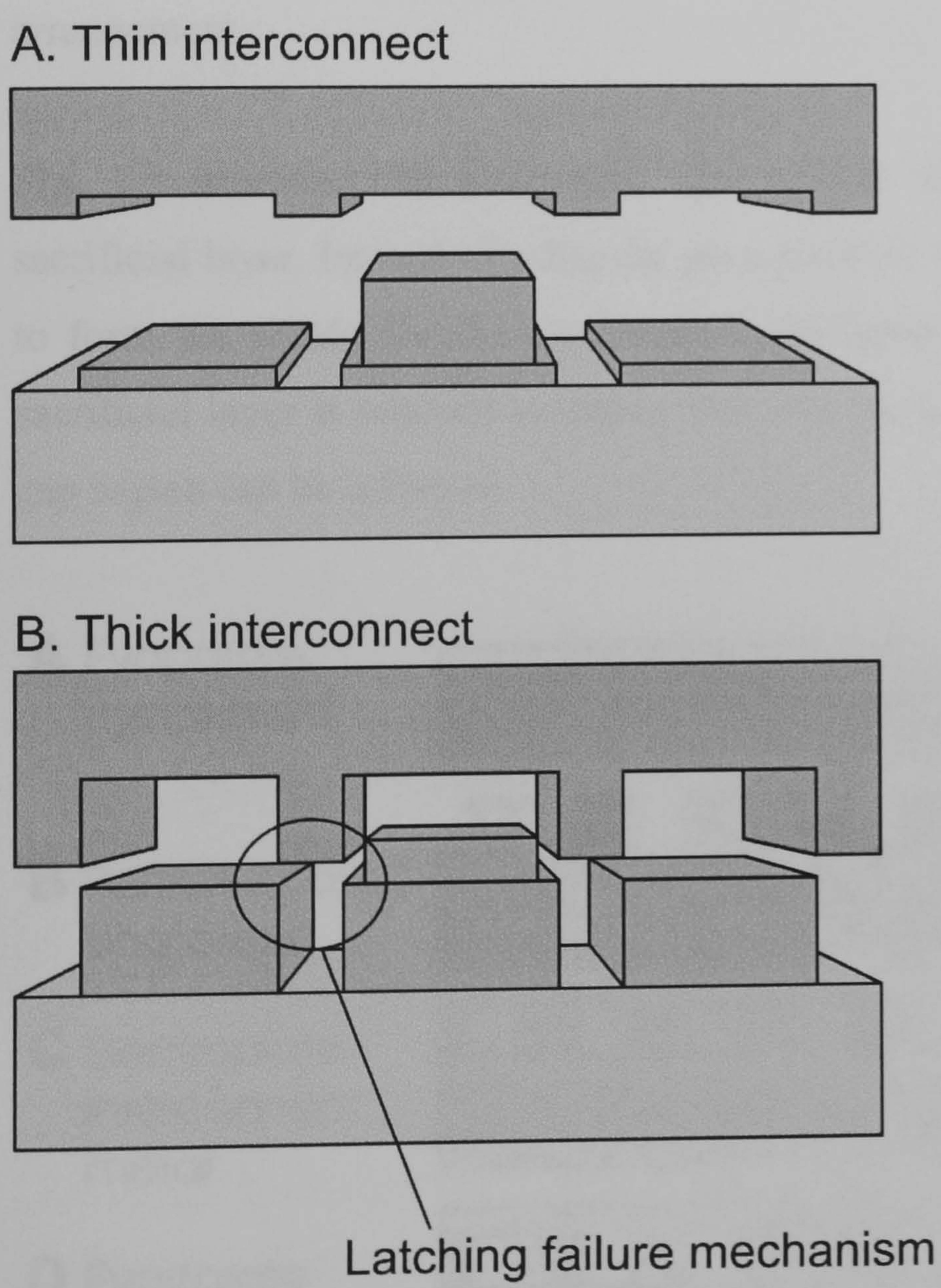


Fig. 7.4 The interconnect thickness for the process in chapter 6 is limited due to latching effects. In A and B, the interconnect is thin and thick respectively relative to the electrode gaps.

7.4 Dual sacrificial layer approach

As discussed in the previous section, the applicability of titanium as a sacrificial layer for the formation of thick interconnect (several microns) is poor because of its high stress nature. Classically, for this application, a low organic stress mould such as photoresist is suitable.

The problems with photoresist as a direct sacrificial layer were identified in chapter 5. This showed that organic scum remained after sacrificial layer etching, and photoresist was therefore deemed unsuitable for use in critical air gaps. The two-gap capacitor requires that the capacitive electrodes are brought into close contact to provide a wide tuning range. Organic scum could act to compromise this tuning arrangement.

Fig. 7.5 illustrates an alternative approach to fabrication, which utilises a dual sacrificial layer. Instead of using the photoresist to form critical air gaps it only exists to form the mould for the interconnect and lower electrode anchors. The titanium sacrificial layer is retained to ensure that organic scum free etching of the critical air gap region can be achieved.

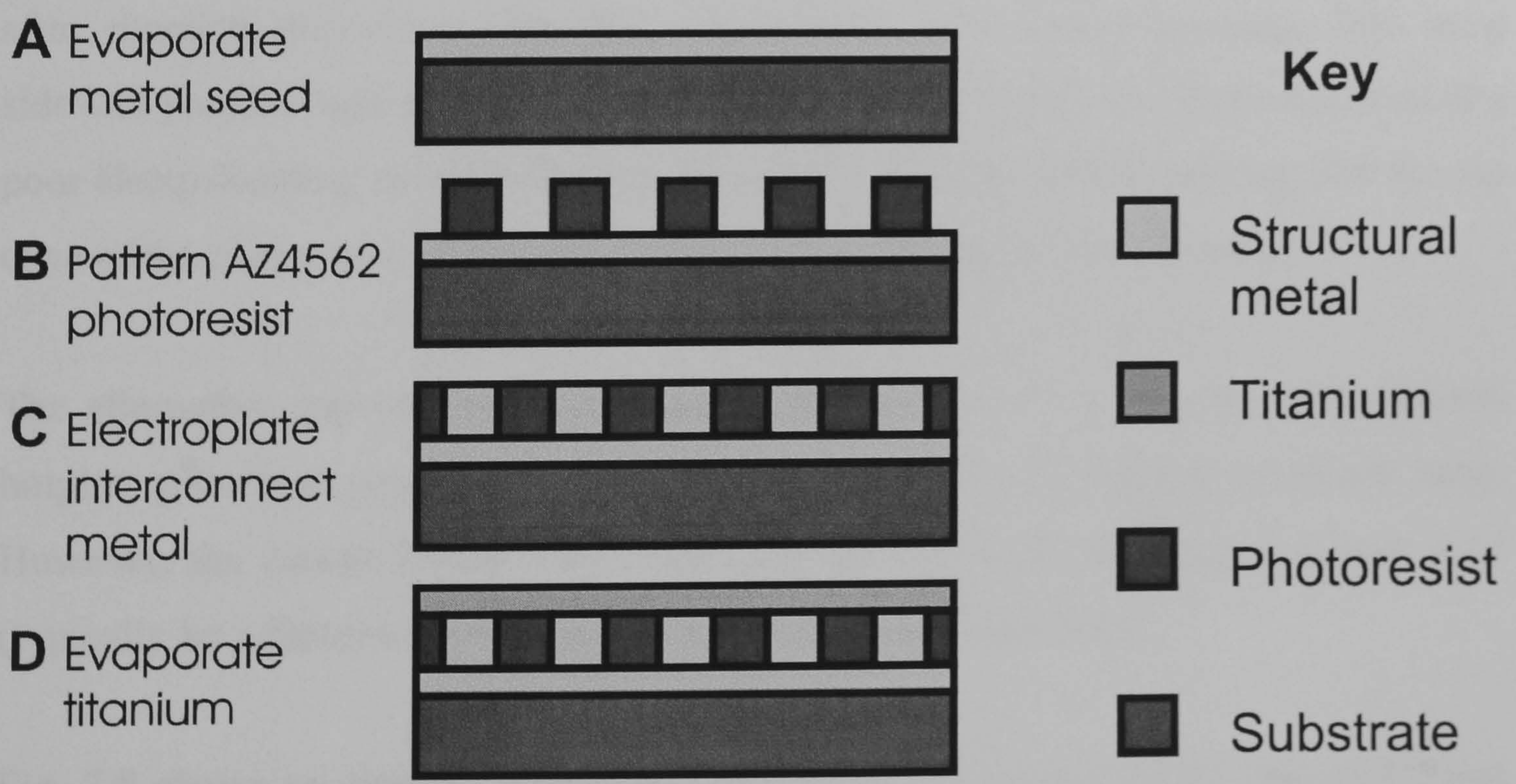


Fig. 7.5 A dual sacrificial layer approach for thick interconnect devices.

The use of a thick photoresist such as Clariant's AZ4562, which typically spins to 6.2μm at 3700rpm, enables interconnect moulds to be used which exceed the RF skin depth. However, the implementation of a dual sacrificial layer process flow requires additional considerations. These include reflow of the organic layer during processing causing poor topology or stress fracturing and the chemical compatibility of the two layers. Furthermore, if photoresist is to serve a dual role as a sacrificial layer and a photolithographic layer then the latter needs to be removed from the former without causing damage.

The process flow in fig. 7.5 aims to combat many of these problems but this is at the expense of minimum feature definition. In particular, the sacrificial AZ4562 needs to be baked at an elevated temperature to avoid reflow during subsequent processing. The optimum processing conditions for AZ4562 require a 90°C soft bake on a vacuum hotplate for 5 minutes. Exposure times on a Karl Suss MJB3 mask aligner are typically 30 seconds for the photoemulsion masks.

Fig. 7.6 shows an electron micrograph of AZ4562 features after soft bake, exposure and development (in 1:2 AZ351B:H_2O). This however, has limited temperature stability, and fig. 7.7 shows an electron micrograph of the photoresist after 2 minutes at 120°C on a vacuum hotplate. The photoresist has reflowed. If this were to occur after titanium deposition then this would cause catastrophic cracking. The steep sidewall profiles have been lost. A consequence of this is that the photoresist acts as a poor electroforming mould with little chance of the electrodeposit joining with the top edge of the photoresist. This leads to significant topological discontinuities.

The alternative approach is to provide the 120°C bake for 2 minutes on a vacuum hotplate prior to exposure and development. This bake is in addition to the soft bake. However, the elevated bake temperature has the effect of increasing exposure time (typically by a factor of three) for comparable development times.

Fig. 7.8 shows an electron micrograph of AZ4562 photoresist which has undergone the high temperature pre-bake. Resist profiles are better than those in fig. 7.7. The longer exposure time in combination with photoemulsion masks leads to surface pitting on top of the photoresist. The photoemulsion does not provide a total UV block and hence normally unexposed regions can become partially exposed and developed for prolonged exposures. The compromise between temperature stability and feature definition is not perfect, and future thick resist development which can withstand high temperature processing and be relatively easily removed will hopefully improve this further.

Using the high temperature pre-bake, there is an improved possibility of the electroplated metal bridging the gap between the top of the resist and the top of the deposit. The sidewalls are not vertical but they do act to provide a partial lateral constrainment for the electrodeposit. In classical electroforming, the electrodeposit is constrained horizontally whilst free to form vertically. With angled photoresist sidewalls, the electrodeposit is unconstrained horizontally until it contacts the photoresist. In extreme cases, unconstrained electroforming leads to mushrooming as shown in fig. 7.9.

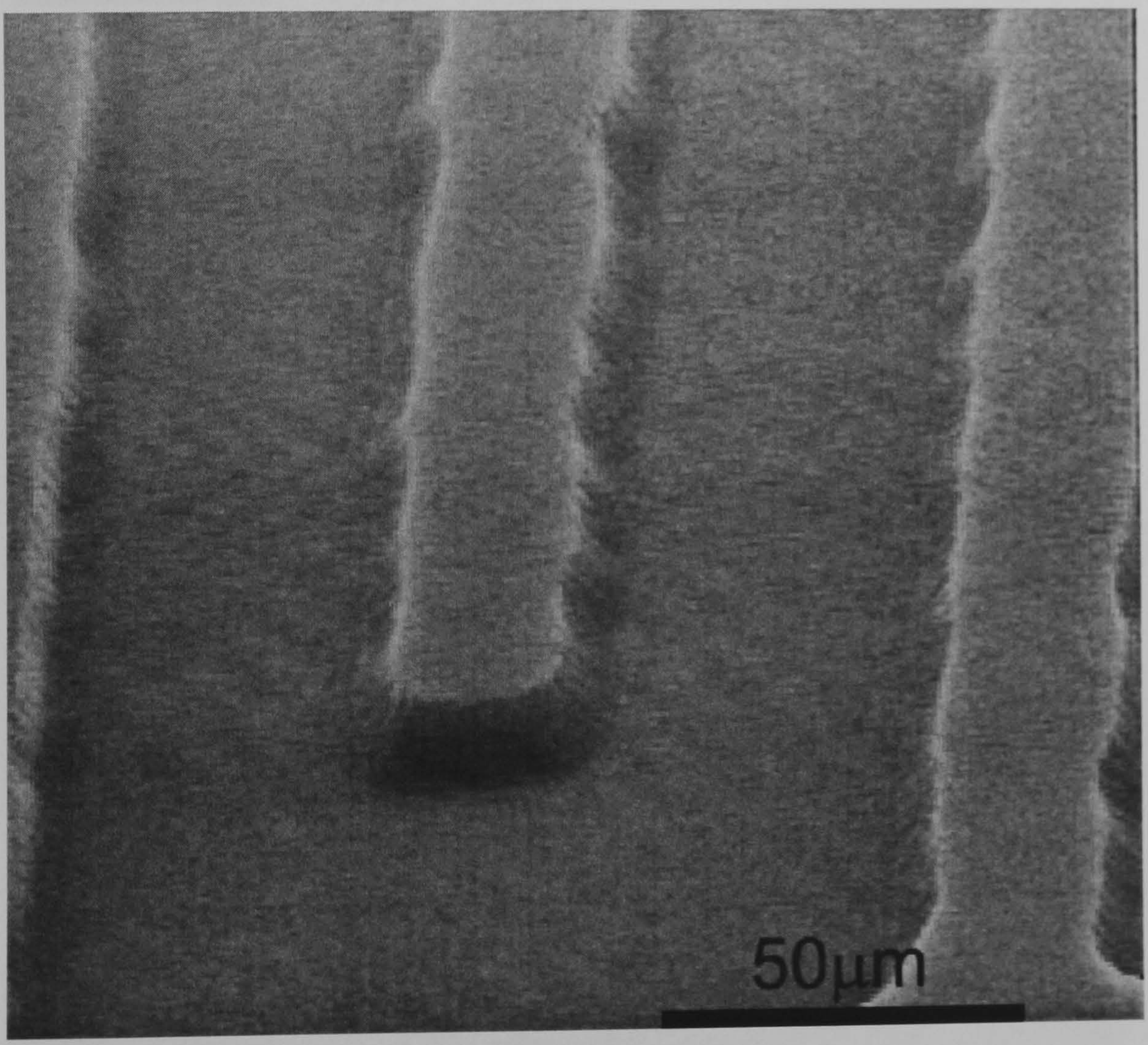


Fig. 7.6 Optimally exposed AZ4562 photoresist using a photoemulsion mask.

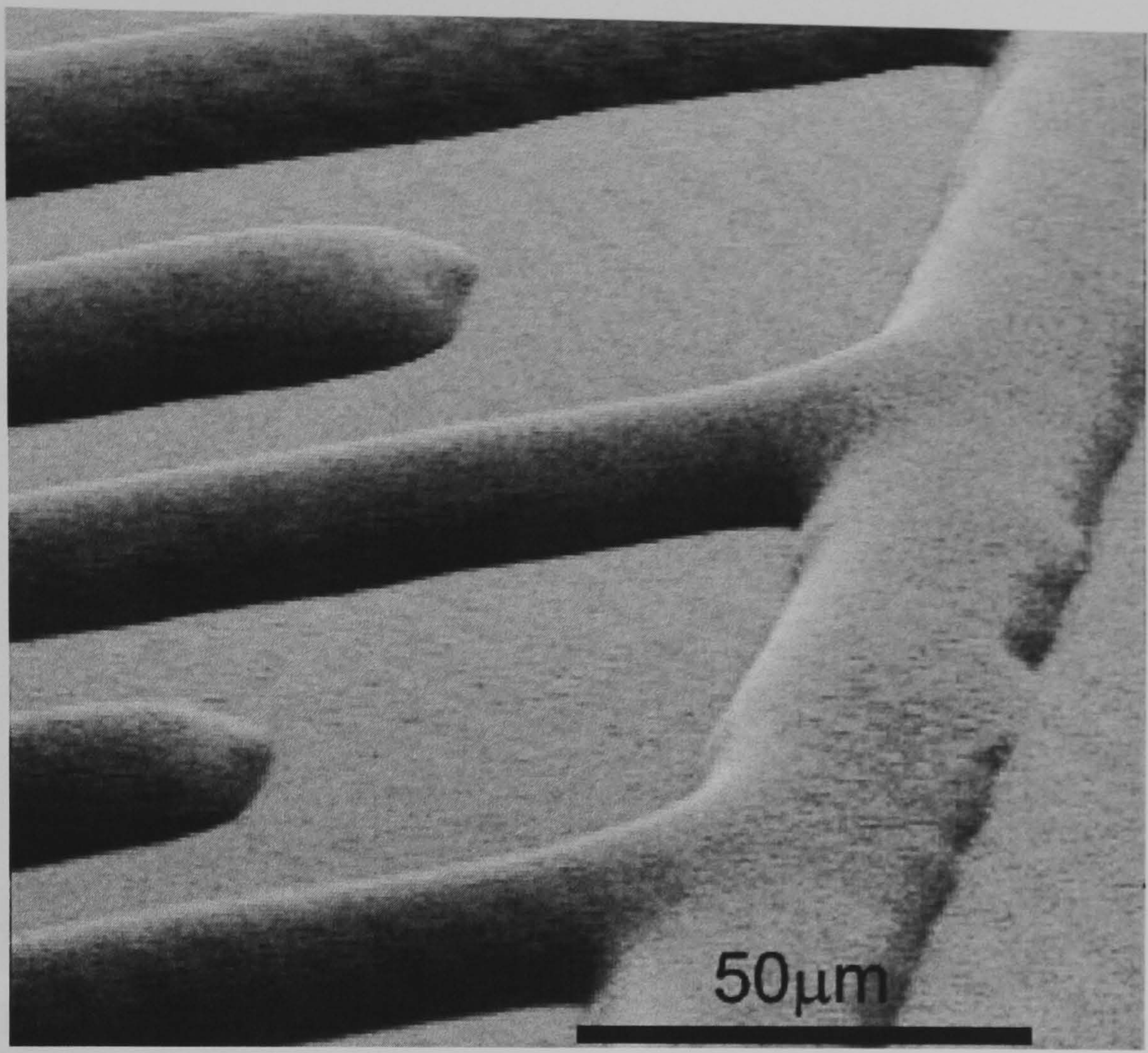


Fig. 7.7 AZ4562 photoresist after a hard bake reflow.

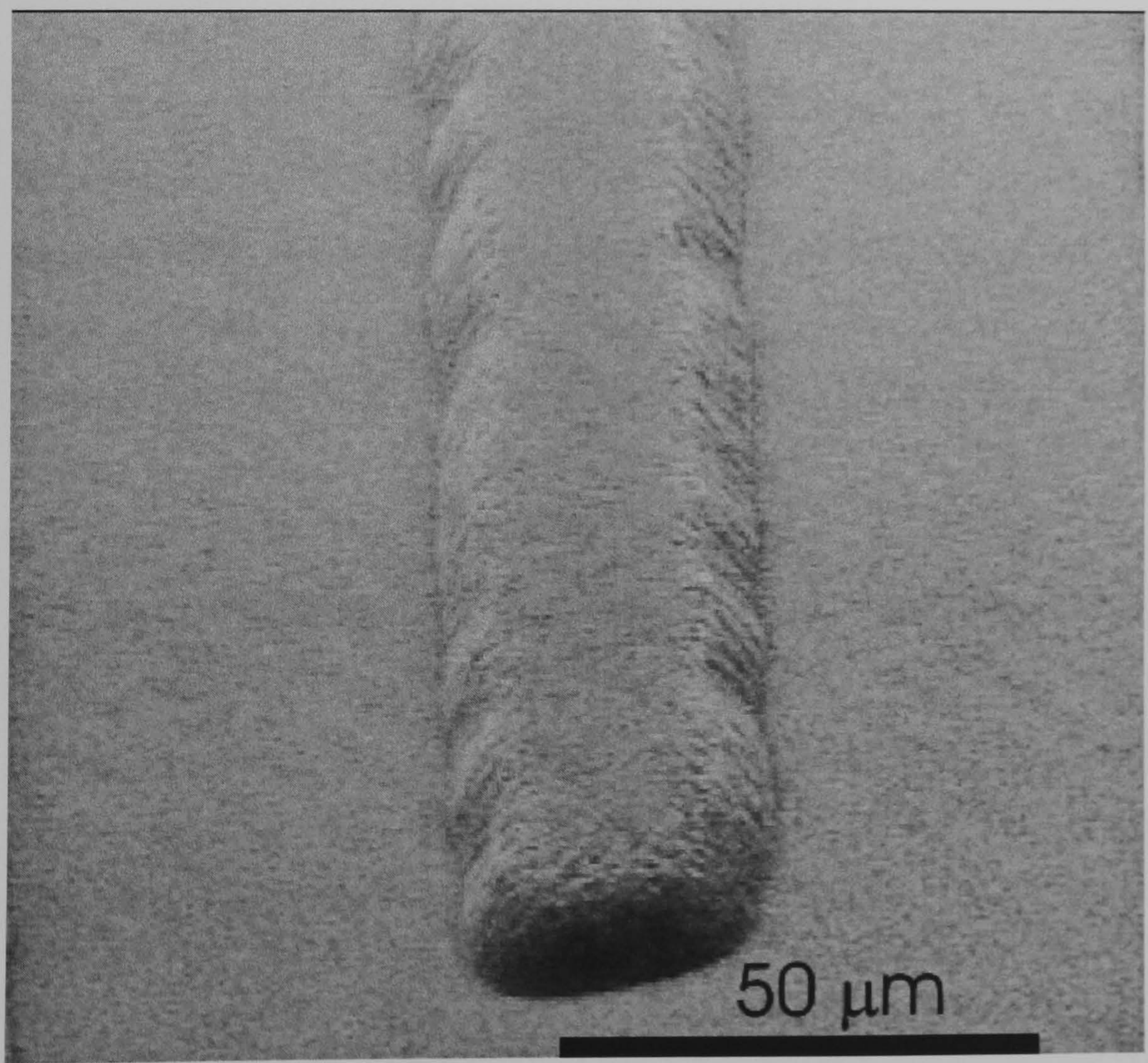


Fig. 7.8 AZ4562 photoresist after high temperature prebake. A longer exposure time is required and consequently pitting is evident on the photoresist.

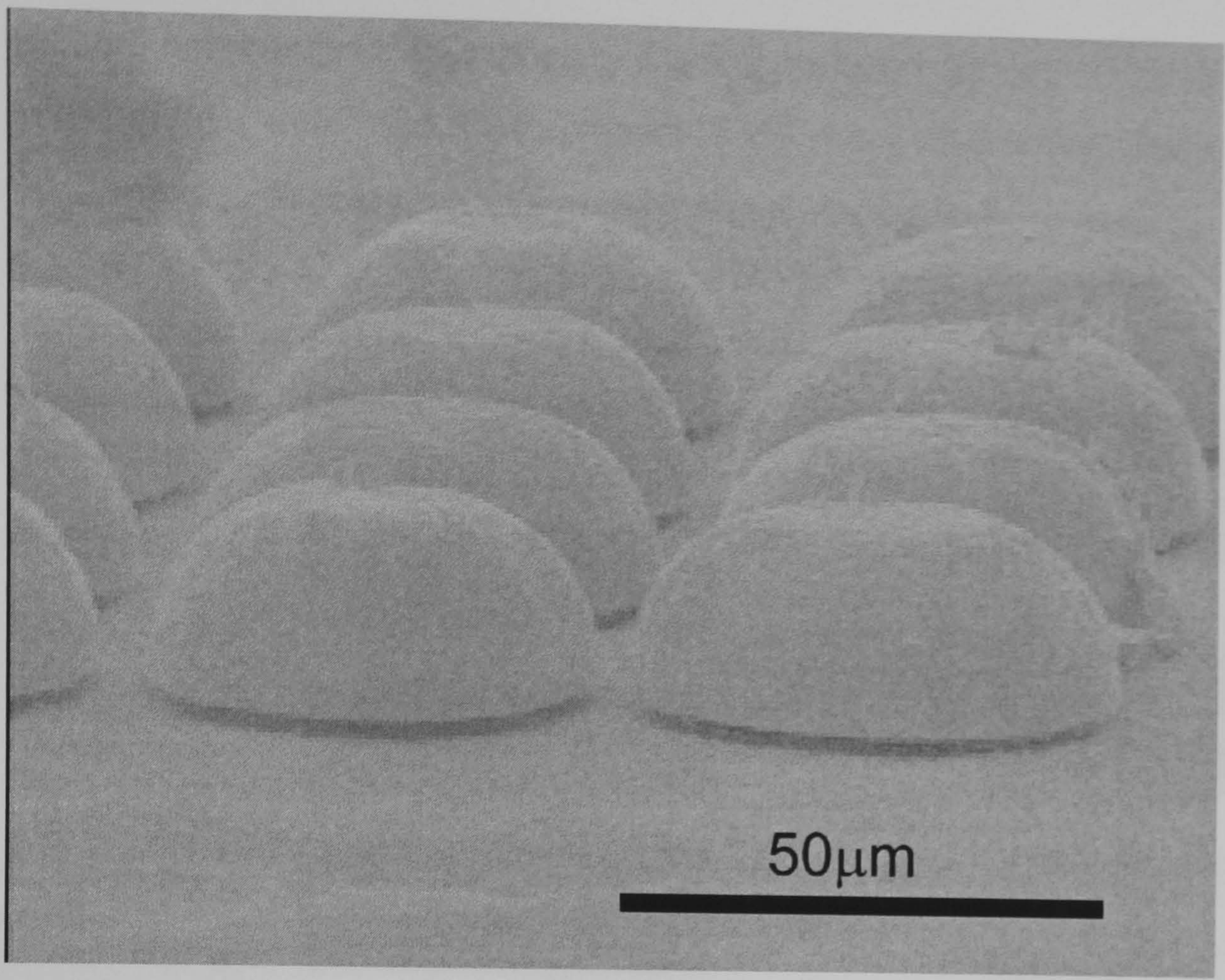


Fig. 7.9 This shows the effect of a completely unconstrained gold electroplating deposit. The mushroom effect is indicative of isotropic growth.

SU-8 was trialled as an alternative to AZ4562. It can provide excellent sidewall profiles and good temperature stability. However, this is at the expense of ease of removal. Removal techniques do exist but they rely upon a slow delamination/lift off process which is unsuitable in a partially enclosed capacitor structure. Attempts were made to develop interconnect structure which consisted of a series of 'fuses' connect each device. These fuses would be etched at a final stage of process to electrically release the devices.

The problem with this technique was found to be that ensuring a good uniform current density across the wafer is very difficult. Coiled inductor structures (which will be presented later) proved particularly troublesome where very little or no electroplating occurs at the centre of the coil because no connection could be made here in the first stages of processing.

Fig. 7.10 details the process flow for thick interconnect capacitors. First, 300Å/100Å of Cr/Au were e-beam evaporated to form a conductive plating seed on the substrate (fig. 7.10 A). Then AZ4562 photoresist was spun at 3700 rpm. The resist was first given a soft bake at 90°C for 5 minutes followed by a 120°C bake for 2 minutes on a vacuum hotplate prior to exposure. Typical exposure times of 90 secs on a Karl Suss MJB3 aligner were used. Development in 1:2 AZ351B developer:H_2O was performed for 2 minutes to ensure effective photoresist clearance through to the gold seed (fig. 7.10 B).

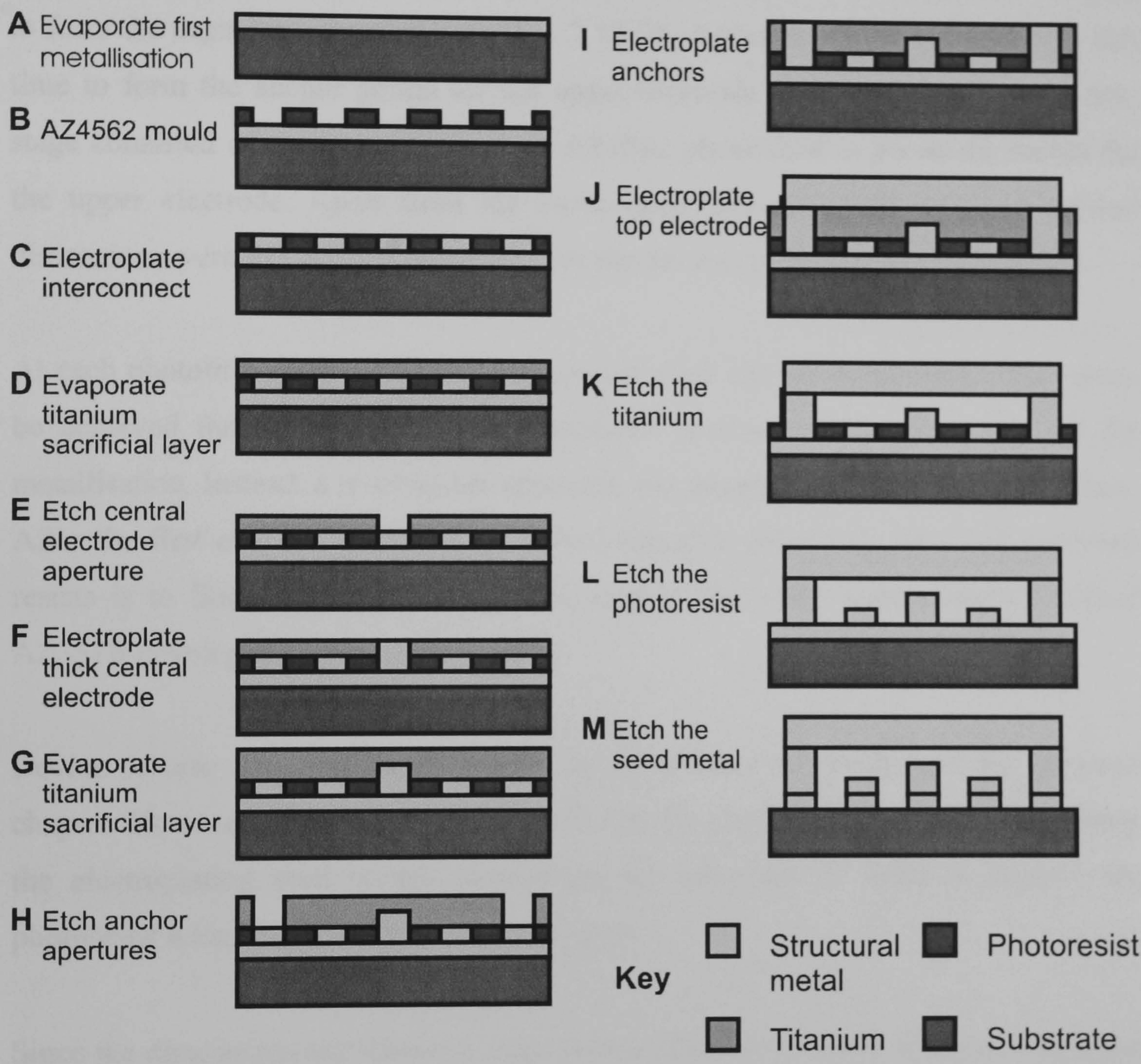


Fig. 7.10 Fabrication process flow for dual sacrificial layer micromachined capacitors.

Gold was electroplated into photoresist apertures until the gold deposit a) filled the aperture gap and b) reached the top of the photoresist (fig. 7.10 C). These measurements were primarily performed under the optical microscope.

In order to fully stabilise the photoresist an extended bake of 30 minutes at 90°C was performed. Subsequent fabrication consisted of an e-beam evaporation of 2000Å of titanium on to the photoresist and gold (fig. 7.10 D). This was followed by an HF etch over the sense electrode region to create the dual gap structure (fig. 7.10 E). Gold electroplating can be performed at this stage if a thick central electrode arrangement is required (fig. 7.10 F).

The next step was to e-beam evaporate 1000Å of titanium followed by 100Å of gold to form the capacitive electrode gap (fig. 7.10 G). Again, this is etched back, but this time to form the anchor points for the upper electrode (fig. 7.10 H & I). The next stage consisted of another deposition of AZ4562 photoresist to act as the mould for the upper electrode. Apart from the interconnect thickness, the area and vertical dimensions were the same as those used for the devices in chapter 6, section 6.5.

At each photolithographic stage the photoresist mask has to be removed. This cannot be achieved through standard etch procedures because solvent strips can lift the metallisation. Instead, a re-exposure approach was incorporated into the process flow. After the first evaporation the only method found to selectively removed patterned resists is to flood expose the wafer and develop the wafer using standard diluted AZ351B developer.

Device release was performed initially in HF:ethanol as detailed in the previous chapter. However, it is clear from fig. 7.10 that the photoresist and more importantly the electroplating seed is still present on the substrate. In order to remove the photoresist a long soak in acetone is performed.

Since the dimensions are relatively large with a channel thickness of 6.2 μm then this is a fairly rapid process, which can be achieved in under 5 minutes. The acetone soak is performed in an ultrasonic bath to minimise the presence of photoresist organic scum discussed in chapter 5. After the photoresist was removed, the electroplating seed can be removed in gold and chromium etching solutions. The wafers were returned to acetone followed by IPA for a high temperature release.

The key advantage of this process flow is the ability to be readily transferred to a range of substrates and the flexibility to produce thick, low loss, interconnect feeds. In the chapter 6 process flow, a prolonged exposure to HF:ethanol could cause delamination on a substrate such as glass. This is obviously undesirable because it impairs yield. The use of thick photoresist and underlying seed metallisation (which can be relatively thick because it does not influence overall planarisation) effectively isolate the substrate from any aggressive etchants.

Optical grade glass was used as a substrate. This is not cleanroom grade and therefore has to be degreased in Decon-90 prior to H_20_2:H_2SO_4 etch. Fig. 7.11 shows an electron micrograph of a fabricated device on glass without ultrasonic release during fabrication. The type of organic scum identified in the chapter 5 is prevalent.

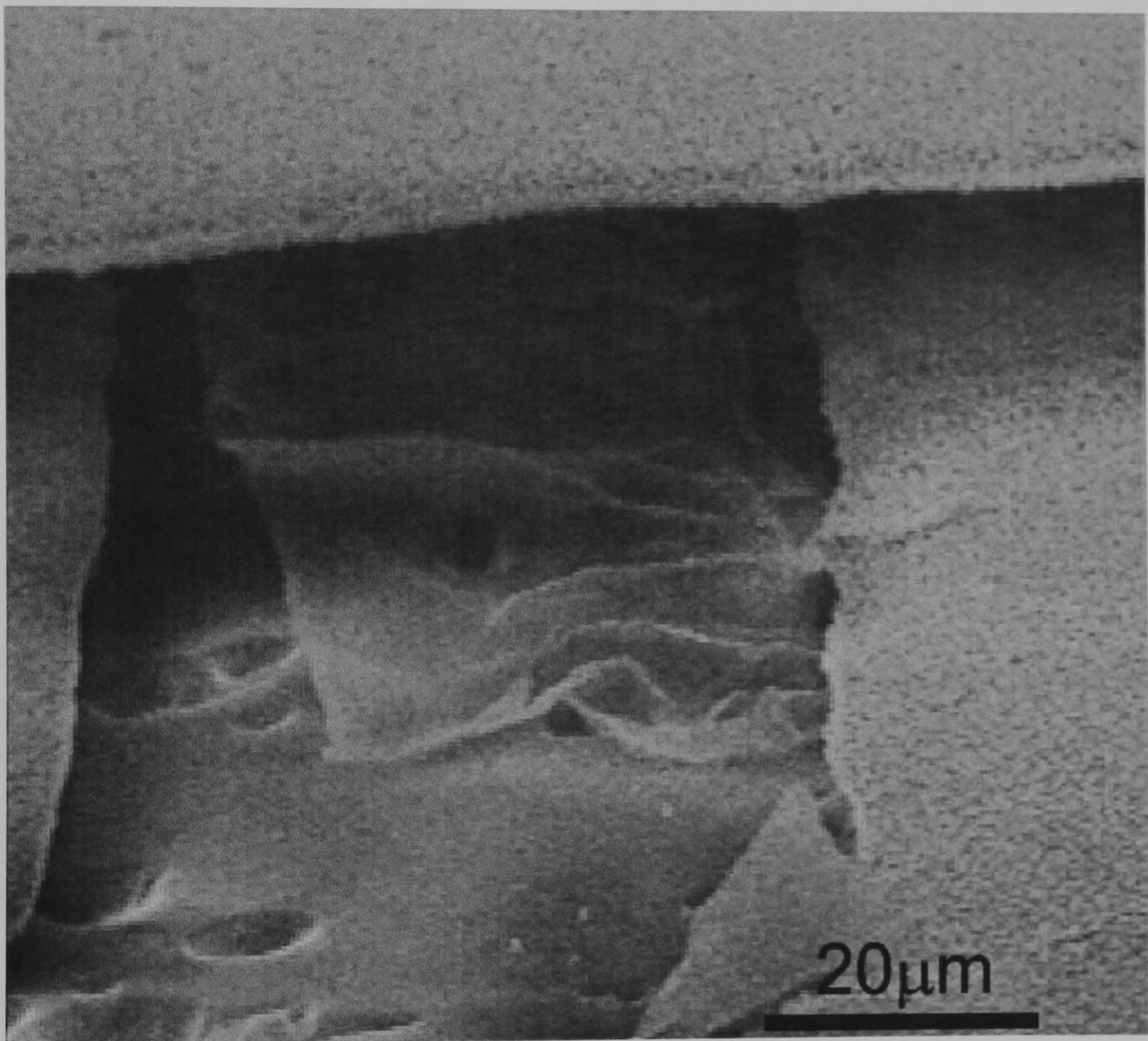


Fig. 7.11 An electron micrograph showing evidence of organic scum on a released gold capacitor. This has been fabricated on a glass substrate. Lack of ultrasonic agitation has been identified as the cause.

Fig. 7.12 shows a successfully fabricated thick interconnect gold device on a glass substrate without the photoresist scum evident in the previous device. The overplating required to achieve good planarisation is also visible in this figure.

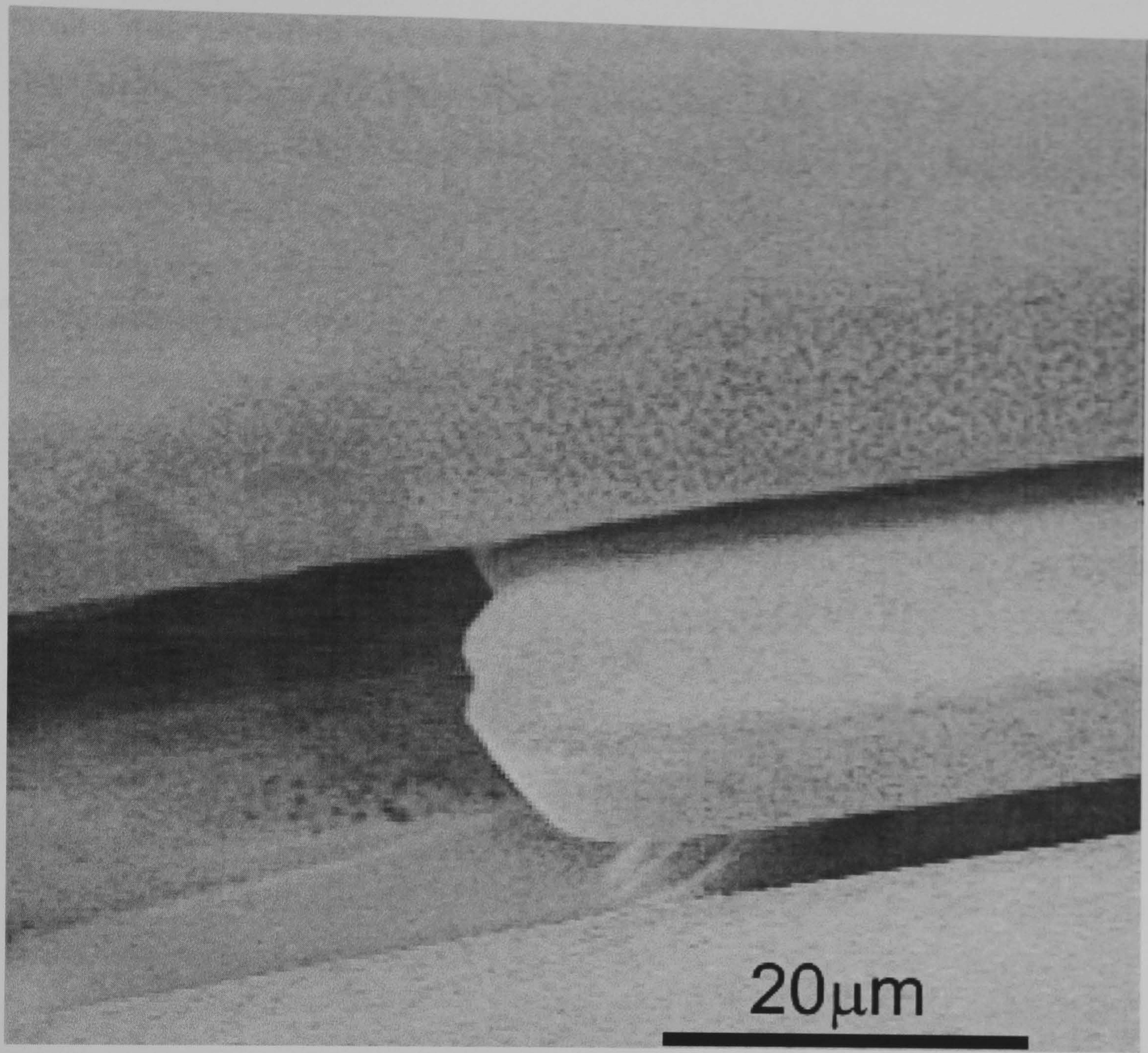


Fig. 7.12 Cleanly released thick interconnect capacitor showing the upper and lower gold electrodes.

7.5 Quality factor measurements for thick interconnect devices

The primary objective of the modified process flow presented in the previous section was to provide a demonstrable improvement in the quality factor of the capacitor structure. Thin interconnect acts as a resistive bottleneck for RF in the low GHz regime.

The use of thick interconnect should eliminate these skin depth related resistive losses and, consequently, the peak Q should be observed at a lower frequency and be higher in magnitude than in section 7.2.

Ideally in an RF MEMS structure there should be either an infinitely thin or resistive substrate to minimise RF losses. This is particularly valid for operation in the low GHz range. At high GHz this becomes less important since the skin depth of the RF is significantly reduced and less penetration occurs into the substrate.

Three substrates were used to produce thick interconnect devices; low resistivity silicon, mechanical grade gallium arsenide (GaAs) and optical grade glass. These are listed in order of decreasing conductivity and consequently anticipated RF loss.

All subsequently documented RF measurements were taken on a HP8753C vector network analyser (VNA) with a Picoprobe GS-150 Model 12 microwave probe. A 50Ω calibration (open-short-load) substrate for 100μm square pads with a 150μm spacing was used. Although, the VNA can achieve 6 GHz operation, the relatively inexpensive GS microwave probe cannot be effectively calibrated on a manual probe station (when compared to the Cascade automatic approach) at these frequencies. Therefore, 3 GHz was found to be the optimum peak frequency before calibration errors became significant.

Fig. 7.13 shows quality factor response of thick interconnect capacitor on silicon, GaAs and glass. As expected the peak Q is highest on the most insulating substrate which is glass. A peak Q of 243 at 0.9 GHz for 0.26pF is achieved. For GaAs this is lower at 19 at 0.9 GHz for 0.42pF and for silicon, this is lower again at 0.53 at 0.9 GHz for 0.57pF. As in section 7.3, the low resistivity silicon is heavily suppressing the Q.

Glass, as expected, provides the highest Q and therefore is the best approximation to a capacitor floating in free space. It is not unreasonable to quote the performance on glass considering the relative immaturity of the packaging solutions for RF MEMS. Flip-chip transfer of a glass substrate onto a GaAs MMIC substrate is a feasible integration process.

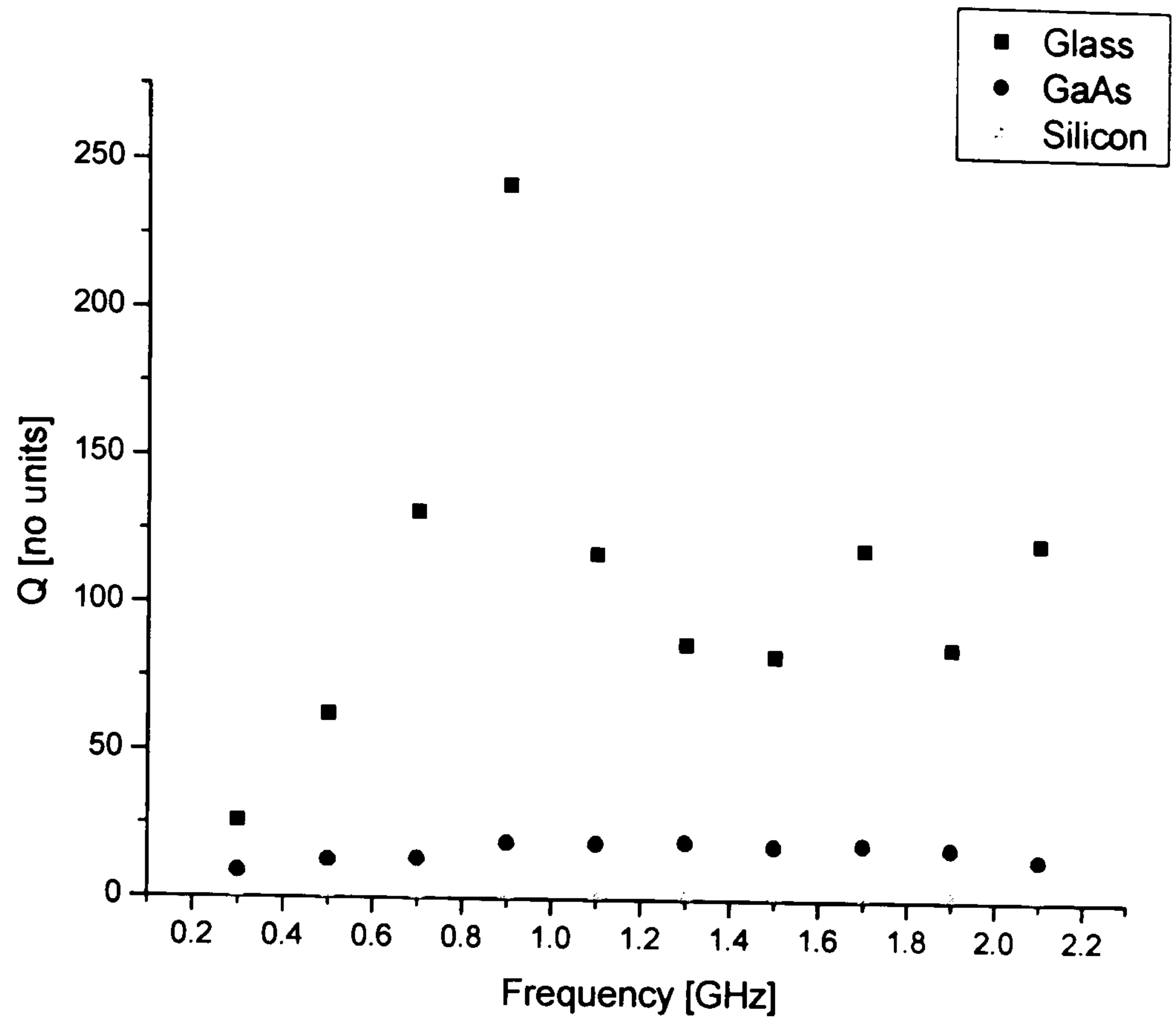


Fig. 7.13 The quality factor response of thick interconnect devices on glass, silicon and gallium arsenide substrates.

The process flow enables very thick interconnect to be accommodated alongside relatively small sub-micron gaps forming very high Q capacitor structures. However, the tuning range of these devices was found to be very low due to a latching phenomenon shown in fig. 7.14.

The peak under the upper electrode is evidence of partially incomplete electroplating bridging to the thick photoresist. This acts as a bump stop which impairs motion of the upper electrode. In order to solve this problem a better photoresist will need to be employed. In this case, better is defined as having good temperature resistance whilst also producing near vertical sidewalls.

As was evident in fig. 7.8, the photoemulsion masks used for the fabrication of these devices introduce a lateral wobble into the photoresist pattern. This effectively means that in some regions the electrodeposit can be fully bridged. However, in other regions a critical gap can occur producing the phenomena seen in fig. 7.14.

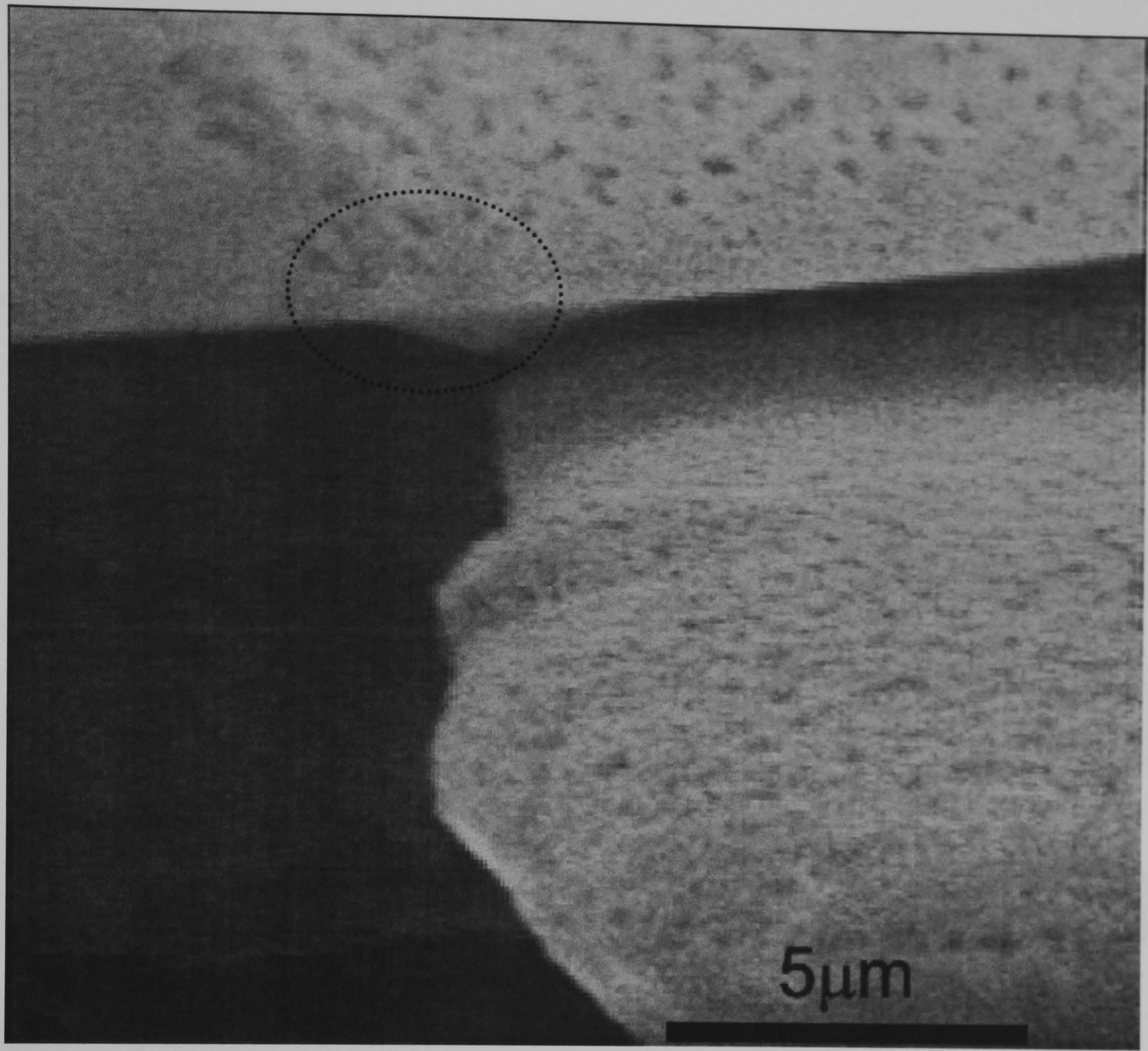


Fig. 7.14 A thick gold electrode capacitor. Evidence of an upper electrode bump stop has been circled.

New photoresists are under development which address this shortfall for electroplated structures. When these are fully brought to market the technical issues with this part of the process can be remedied.

7.6 Demonstration of an all photoresist sacrificial layer device

The use of photoresist as a single sacrificial layer was detailed in chapter 5. The chapter concluded that photoresist was unsuitable for use in small gaps for tunable capacitors due to organic scum. This section addresses this scum issue and presents tuning results from a tunable capacitor using only a photoresist sacrificial layer.

Fig. 7.15 illustrates the device process flow. A single-gap structure was utilised to identify pull-in conditions. The primary purpose of this device is to identify the effect on Q of using thinner interconnect on a glass substrate compared to the very thick interconnect devices.

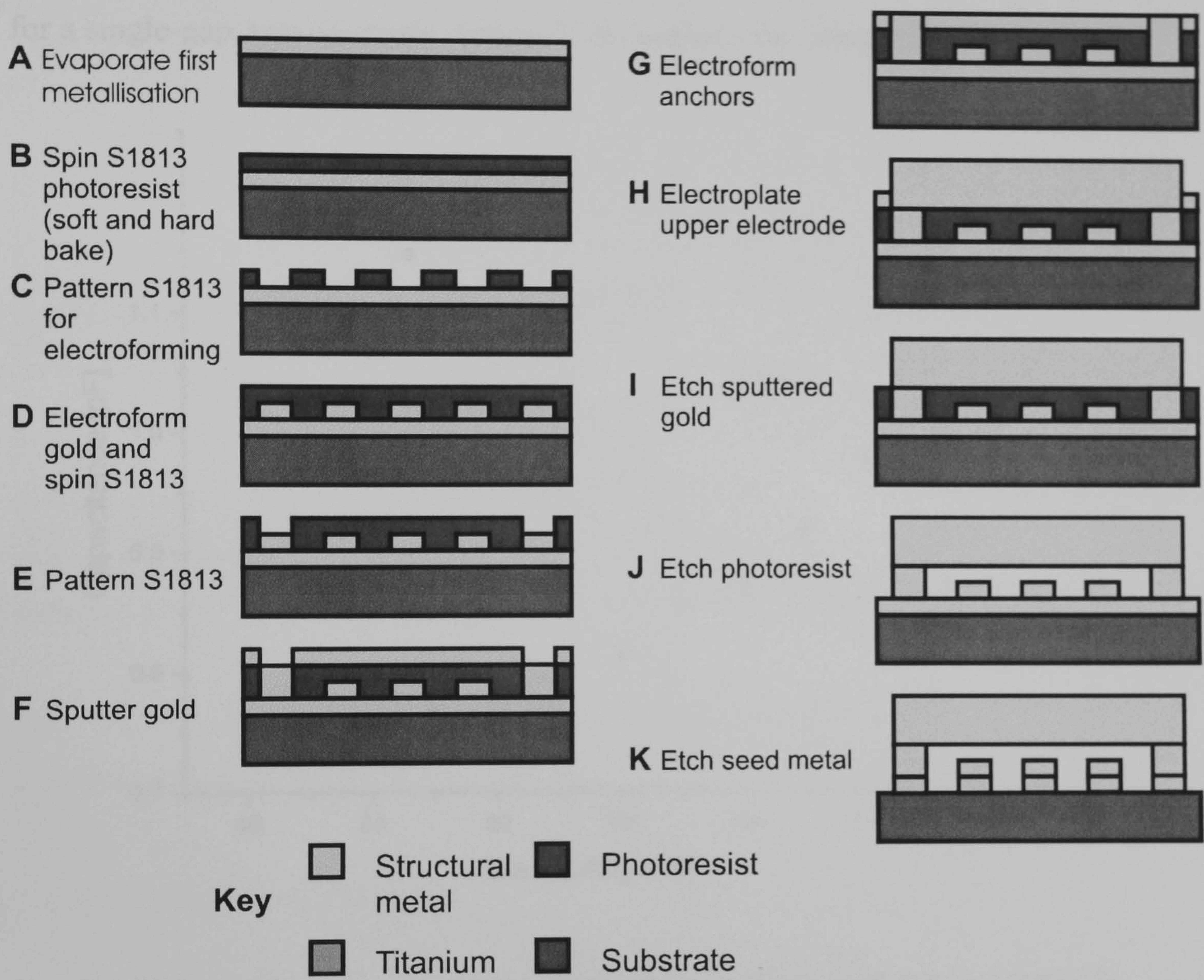


Fig. 7.15 Process flow for a photoresist sacrificial layer gold capacitor.

Each interconnect stage consists of a single layer of S1813 photoresist which is both soft baked at 90°C and hard baked at 120°C. The central gap was formed again by S1813. A gold seed layer (500Å) was sputtered onto the photoresist to enable plating for the upper electrode. Release is performed in acetone and an ultrasonic bath. A 1:1 solution of H_2O_2 and conc. H_2SO_4 was used to remove any organic residue prior to a further treatment in acetone/IPA and a high temperature bake.

The tuning characteristic of the fabricated device is shown in fig. 7.16. It can be seen that a very high tuning voltage of 150V is required. A 10μm thick upper electrode in combination with the large bias electrode gap causes this. However, only tuning range of 1.52:1 can be achieved from an unbiased capacitance of 0.75pF measured on the VNA at 1.66 GHz.

After this voltage is applied pull-in occurs causing the upper electrode to contact the lower. This tuning range is an improvement on the maximum theoretical achievable for a single-gap, two electrode device. This confirms the simulations in chapter 3.

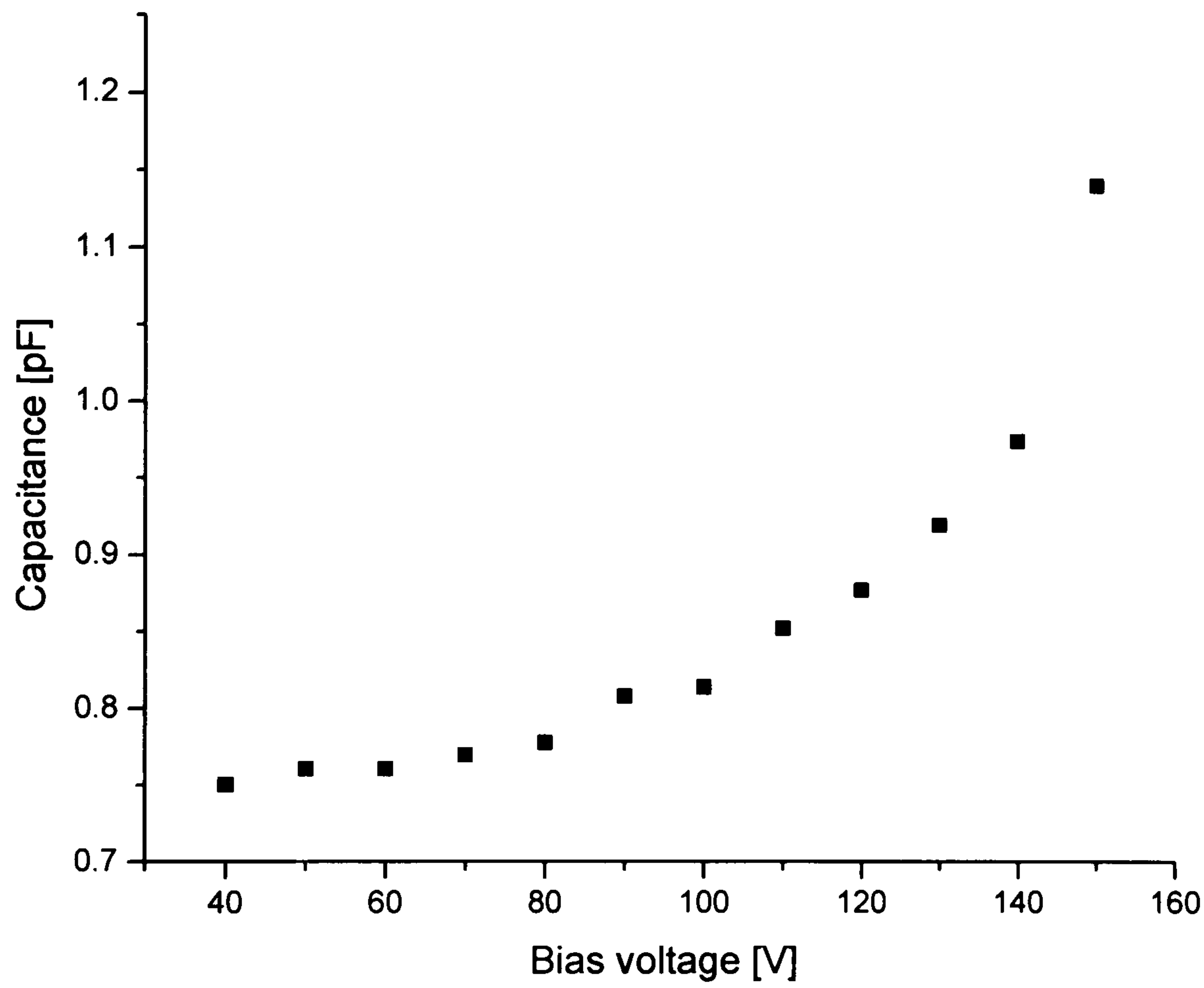


Fig. 7.16 The tuning characteristic of the photoresist sacrificial layer device.

Fig. 7.17 shows a SEM image of the device gap region showing it to be clear of organic residue. The peak quality factor of this device was determined to be 4 at 0.9GHz. These results confirm the added value of the thick interconnect achievable through the two-gap, dual sacrificial approach for improved performance characteristics. The use of thinner interconnect does reduce the quality factor when compared to fig. 7.13.

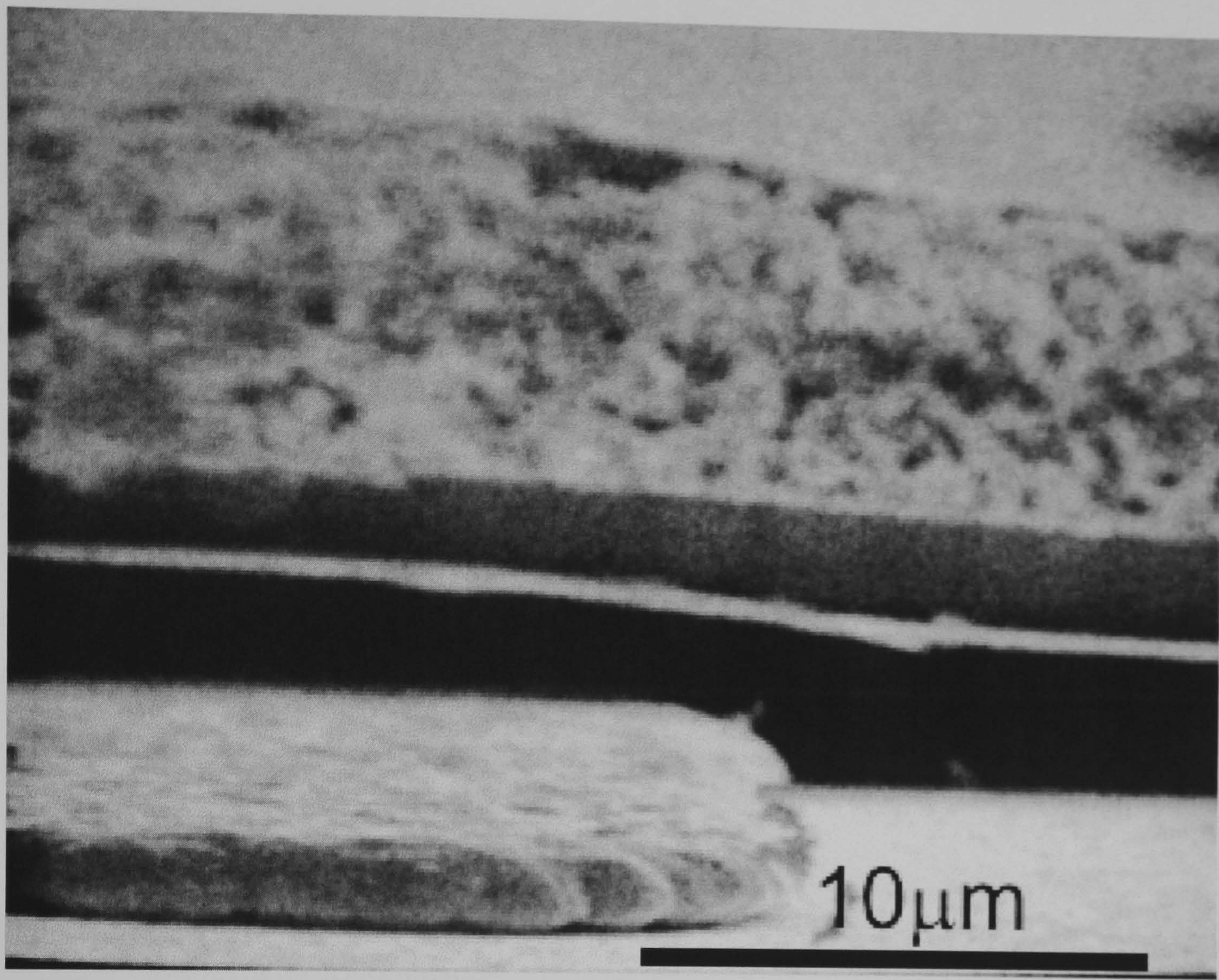


Fig. 7.17 An electron micrograph of the capacitive gap region of a photoresist sacrificial layer tunable capacitor.

7.7 Micromachined inductors

The effective development of micromachined inductors is integral to the final implementation of *LC* tanks oscillators in RF MEMS circuits. The thick electroforming process used for the dual sacrificial layer devices is adaptable to readily accommodate the inclusion of micromachined inductors.

In the simplest form a meander inductor can be formed which essentially is a long length of metal meandered to reduce substrate consumption. A fabricated gold device on a glass substrate is shown in fig. 7.18. A metallisation thickness of 20 μm was used. The peak *Q* measured on the VNA was 9.3 at 1.1 GHz for an inductance of 3.20nH.

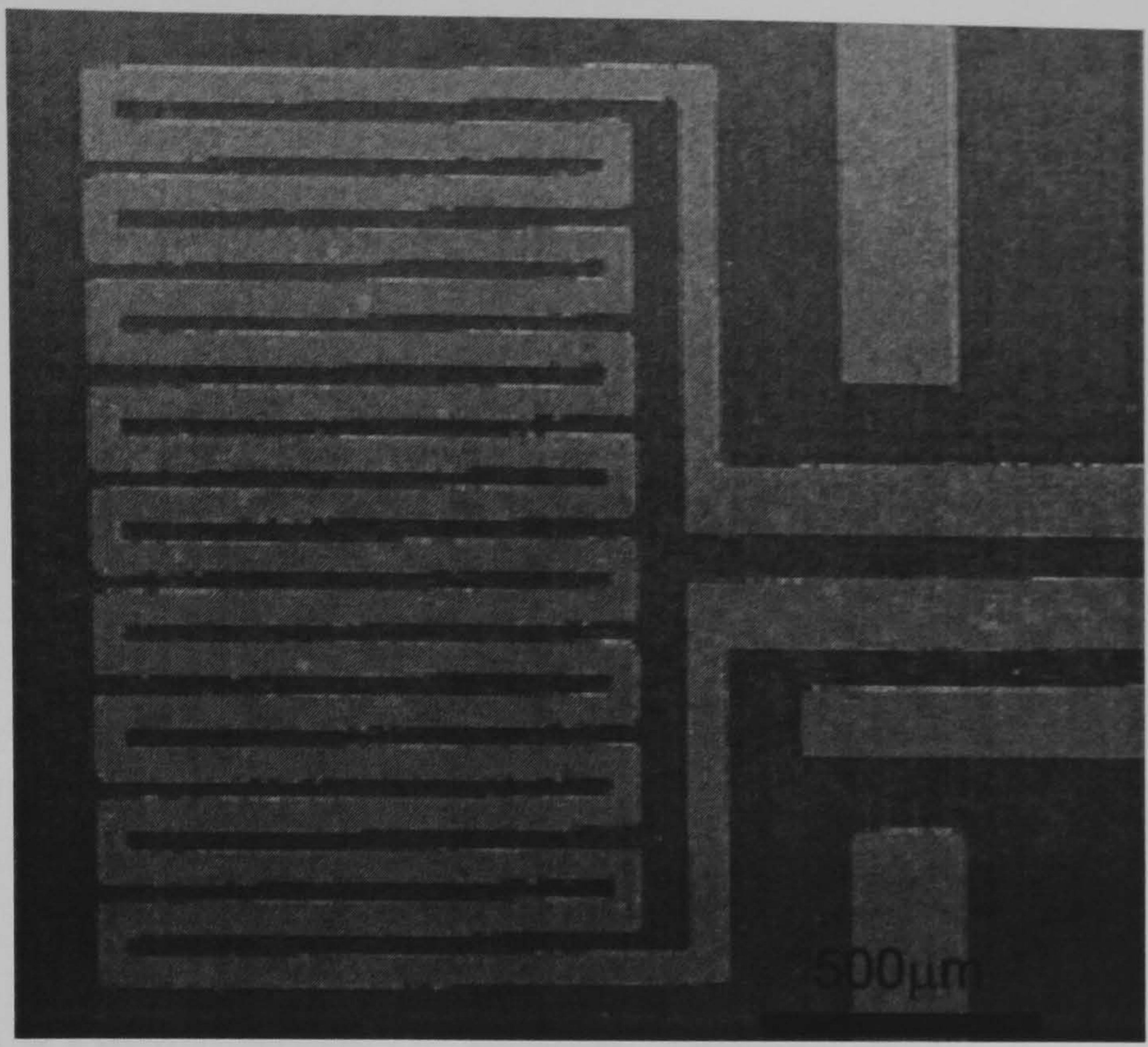


Fig. 7.18 Gold meander inductor on a glass substrate.

Meander inductors are effective for low inductances: however, they have drawbacks. This primarily includes a large consumption of substrate area per unit inductance relative to a coil. Second, when mounted directly onto a substrate other than glass substrate losses and capacitance to ground can become high therefore limiting the quality factor.

An alternative approach is to use a coil inductor and suspend it above a substrate. Fig. 7.19 shows a model of an example approach. There are essentially two structural metallisations required to fabricated such a structure. The first metallisation defines lower pads and interconnect from the centre of the coil. The second metallisation defines the inductor coil.

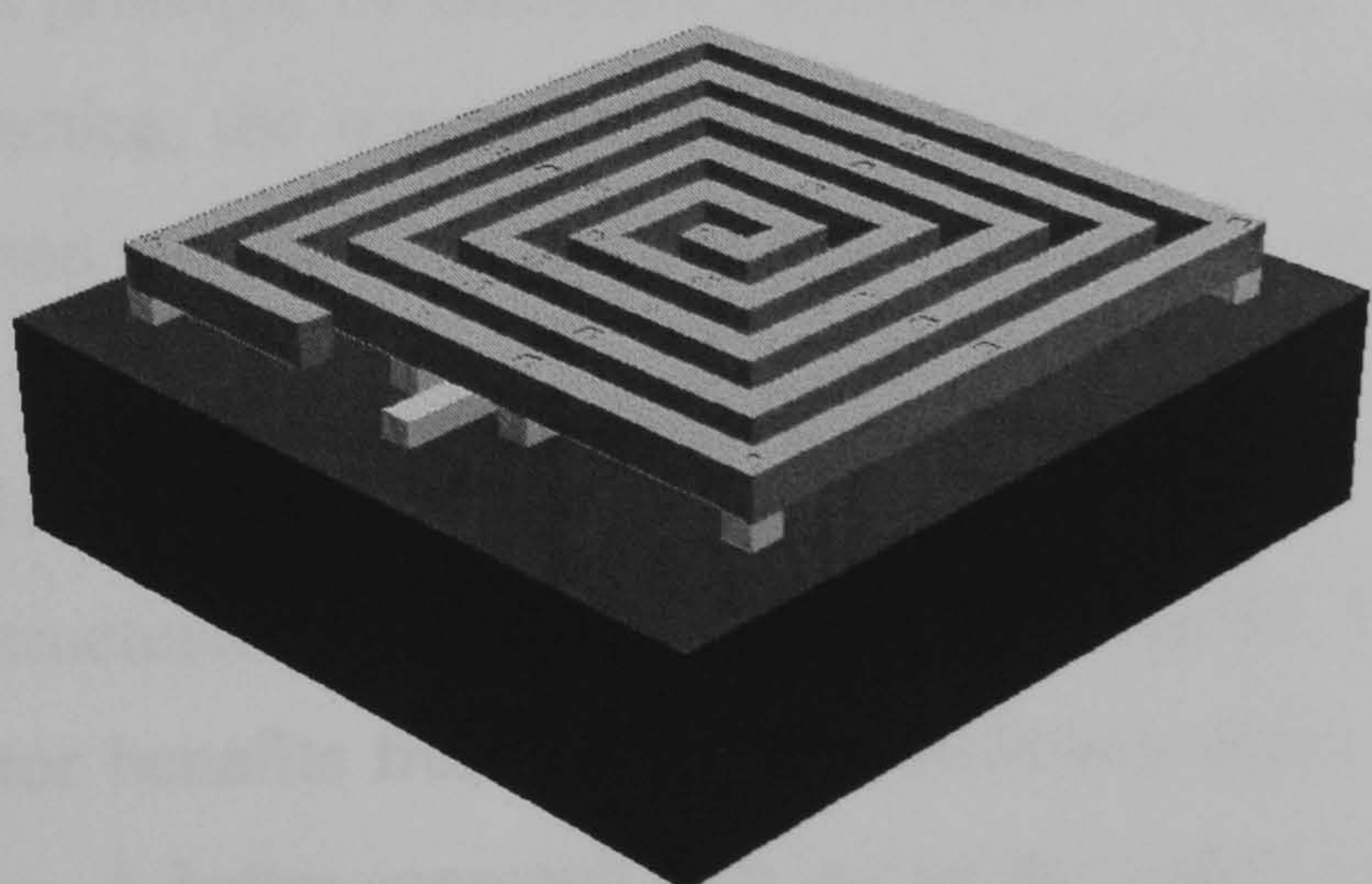


Fig. 7.19 Inductor model indicating metallisations

The dual sacrificial layer approach with AZ4562 lends itself to this, as illustrated in fig. 7.20. This is using the metallisation which defined the interconnect for the capacitors to provide the centre coil interconnect and pad structures for the inductor. The AZ4562 spacer provides primary spacing from the substrate for the inductor coil. The coil is isolated from the output interconnect through the use of the titanium sacrificial layer.

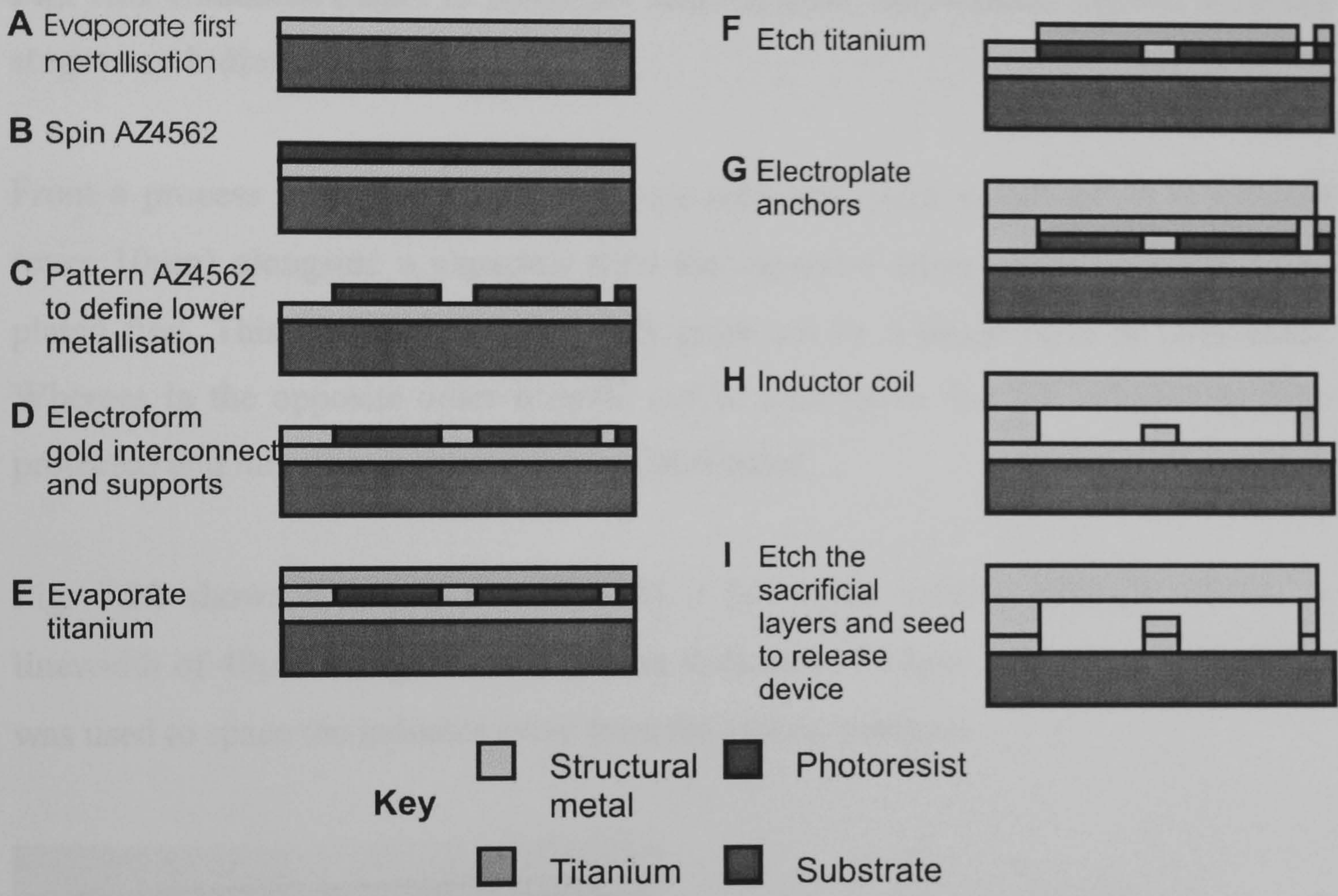


Fig. 7.20 Process flow for a suspended inductor.

The release process is therefore identical to that used for the dual layer capacitors and can in principle be combined as illustrated in fig. 7.21 which shows common stages. In practice, the number of photolithographic stages can be minimised by sharing a common metallisation between the inductor coil and the capacitor.

This is not an attractive option though because of the differing requirements for the two structures. The capacitor needs to retain the flexibility for motion however, the inductor benefits from a thick metallisation which is rigid to accommodate any coil stresses. A better approach is to isolate the metallisations as indicated.

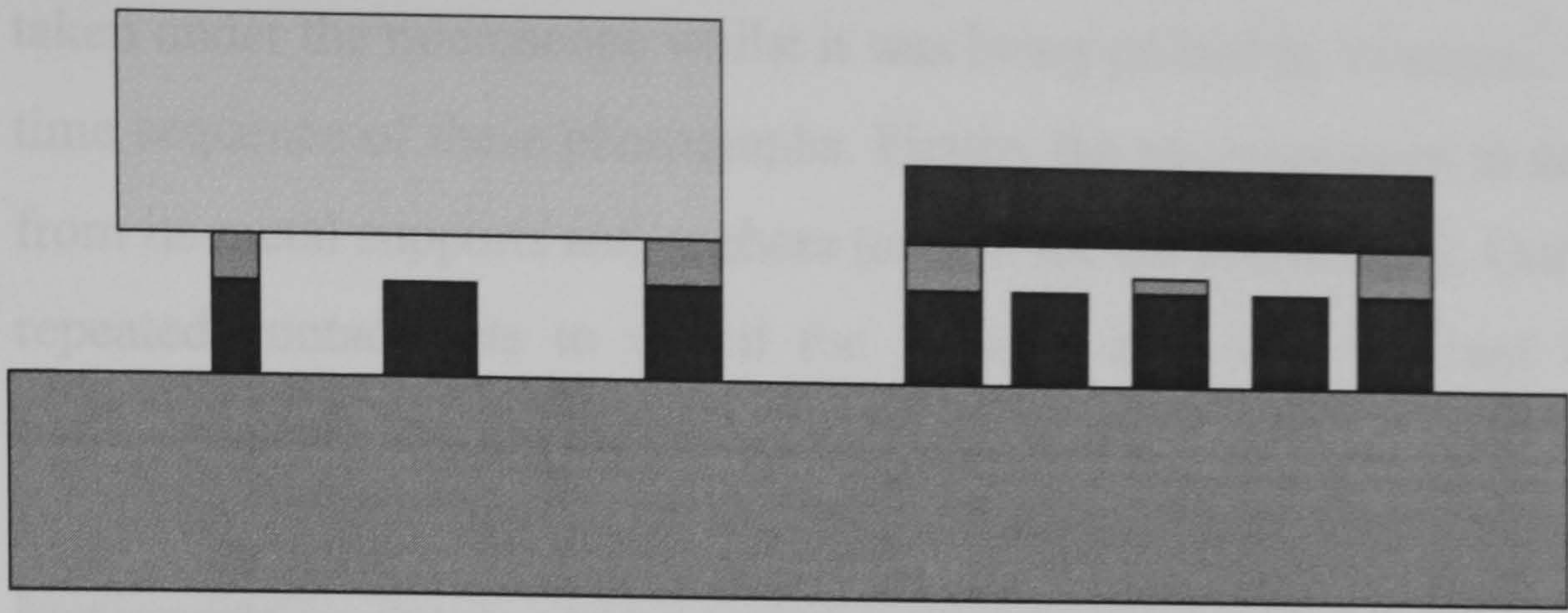


Fig. 7.21 Common stages in capacitor and inductor fabrication. Shared masking stages are indicated by colour.

From a process perspective, if an inductor with very thick metallisation is required (over 10μm) alongside a capacitor then the capacitor upper electrode needs to be plated first. This can then be effectively protected by a single layer of photoresist. Whereas in the opposite order it could not be guaranteed that the inductor be fully protected and therefore insulated during fabrication.

Fig. 7.22 shows a microscope view of a fabricated inductor coil on silicon. A linewidth of 40μm and gold metallisation thickness of 30μm was used. The AZ4562 was used to space the inductor away from the silicon substrate.

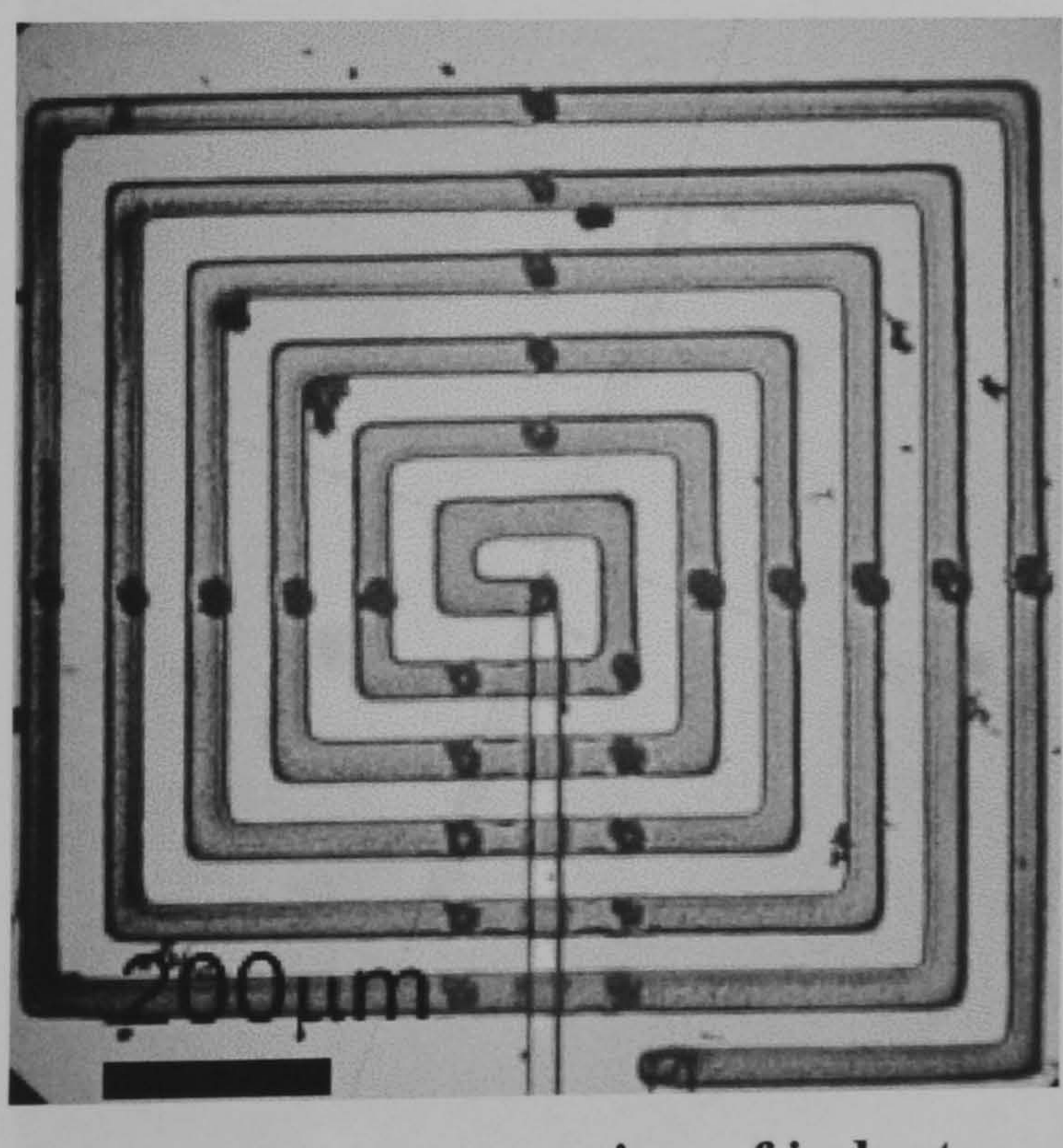


Fig. 7.22 Microscope view of inductor

This device is a clamped spring. Metal supports have been included to support the coil in isolated critical regions. These act to enhance the rigidity of the structure. In order to demonstrate the spring like characteristics of the coil, a series of photographs were taken under the microscope whilst it was being probed by tweezers. Fig. 7.23 shows a time sequence of these photographs. Firstly, the tweezers need to detach the inductor from its metal supports and anchors (except for the central one). Once this is achieved repeated contact acts to uncoil the inductor and once released it recoils until it partially shears leaving the central coil (frame 46).

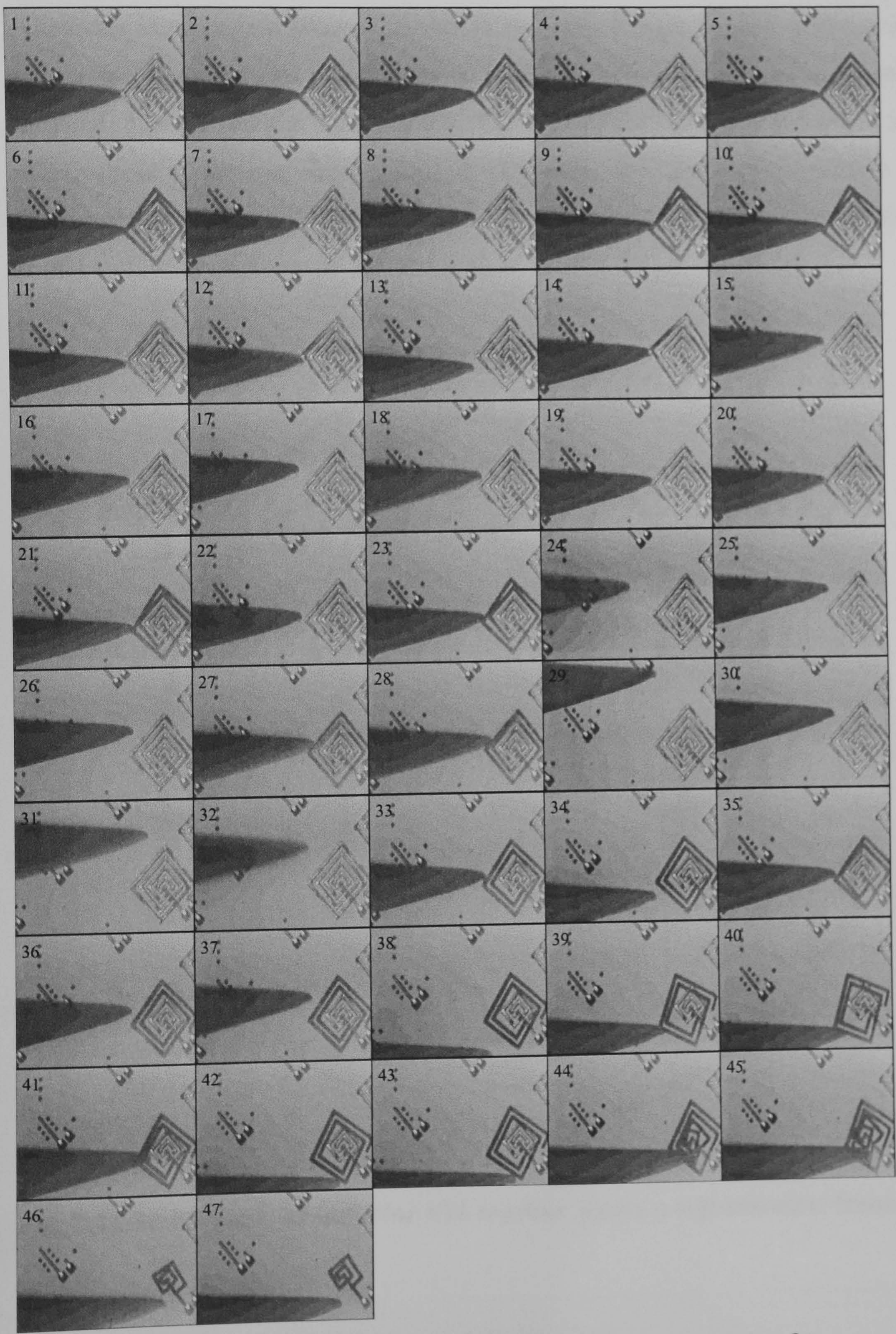


Fig. 7.23 Series of inductor stills during displacement by a pair of tweezers.

The RF performance of the suspended inductor can be seen in fig. 7.24, which shows the S_{11} response. The marker is at the self-resonant frequency of 3.06 GHz. A peak *Q* of 4.5 at 0.9 GHz is observed for an inductance of 9nH. This is a considerable improvement on the meander inductor in terms of inductance. However, the peak *Q* is approximately half that of the meander device. This is to be expected when the higher inductance is taken into account. It should be noted though that the *Q* factor is very respectable when the fact that the device is mounted on lossy silicon is allowed for. Although glass introduces demonstrably lower RF losses, silicon was used to test the effectiveness of the suspended structure. However, only a marginal increase in the performance was found when the structures were transferred onto a glass substrate. Routes to further improve the performance are still under investigation.

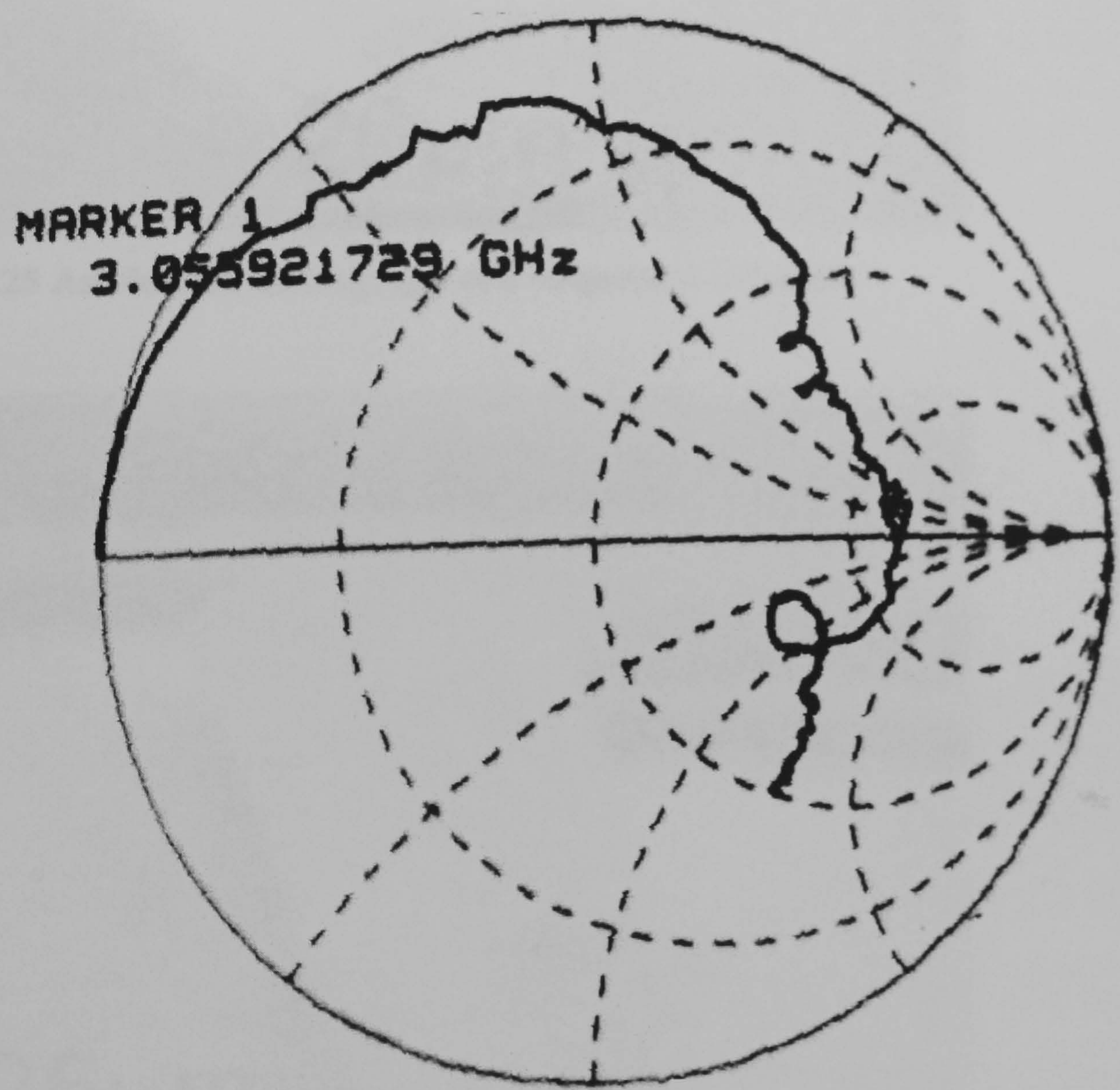


Fig. 7.24 Smith chart of inductor S11 marker shows a self-resonant frequency of 3 GHz.

The mechanical effectiveness of the suspension can be seen in figs. 7.25, 7.26. These are electron micrographs of a gold suspended inductor. In each figure, good isolation from the substrate can be observed.

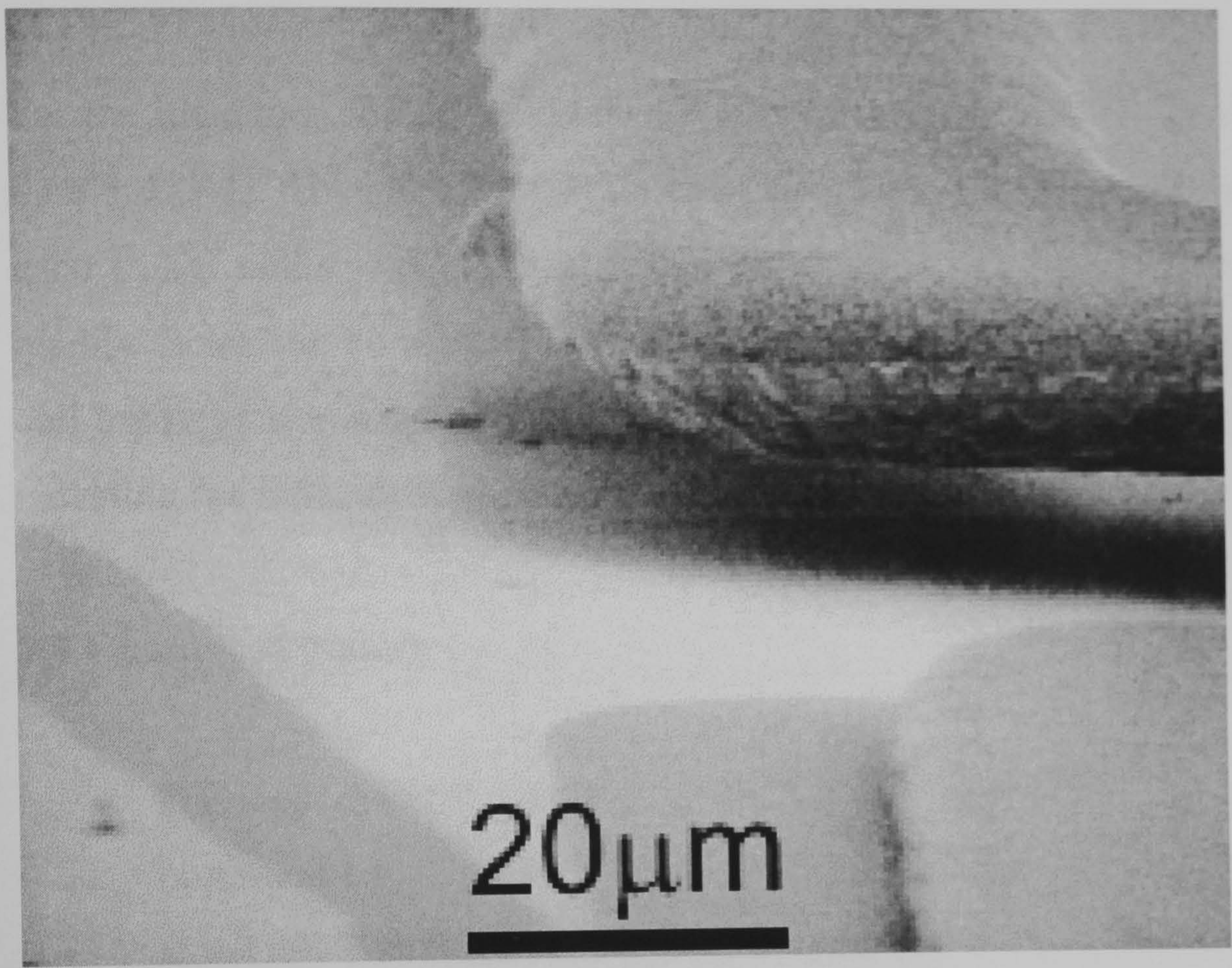


Fig. 7.25 An electron micrograph of a suspended inductor.

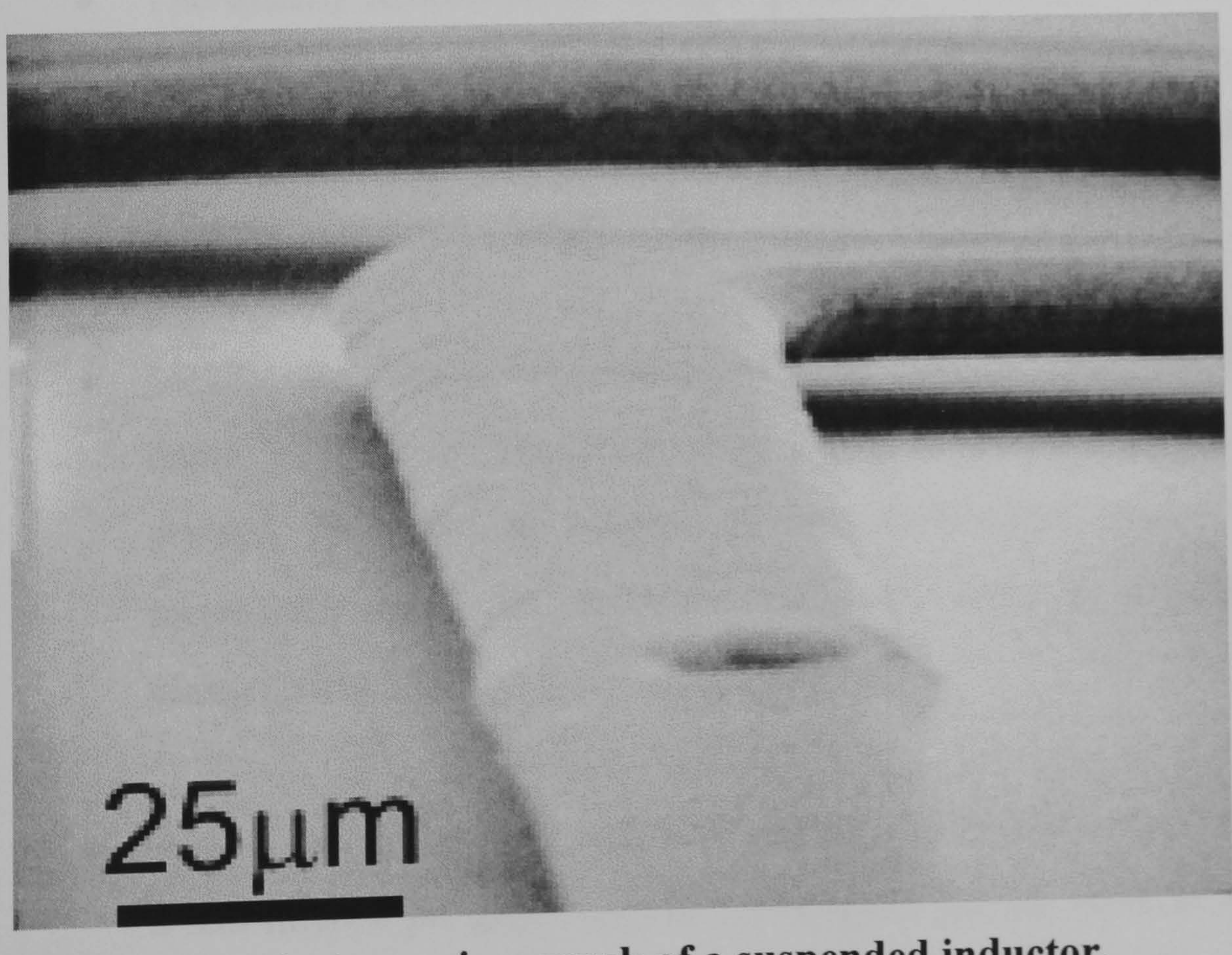


Fig. 7.26 An electron micrograph of a suspended inductor.

The inductors are fixed and consequently the photoresist bridging issues highlighted in the previous section are less important for the implementation of this technology. If a 9nH inductor is achievable a key question is how does this equate to a tuning frequency when coupled with the capacitor structures. If a worst case capacitance of 0.25 pF is allowed for then this equates to an expected resonant frequency for the *LC* tank of 3.4GHz in an unbiased state.

For the inductors, the self-resonant frequency observed in fig. 7.24 is seen to be less than 3.4 GHz. Therefore in their existing form, these inductors cannot be effectively used in *LC* tanks with resonant frequencies above this value. Improvements to the quality factor can be achieved through further reducing RF losses by using improved coil topology (i.e. a spiral) and lower resistivity metallisations, such as copper, or by elevating the inductor further away from the substrate.

7.8 Chapter summary

- Previous chapters focused on the tuning range of the two-gap design. The important figure of merit for RF MEMS capacitors and inductors is the quality factor, *Q*. This leads to sharper tuning peaks.

- The quality factors of the designs presented in chapter 6, had a peak quality factor is 3.4 at 11.4 GHz for a capacitance of 0.24pF. The peak *Q* was in the 11 to 12 GHz regime. This has been attributed to skin depth losses associated with the thin interconnect.

- Ideally, the interconnect and metallisation thicknesses should exceed the skin depth at the low frequency. Due to the limitations of the self-planarising process presented in chapter 6, the interconnect cannot be significantly increased above its 0.04μm thickness without impeding the device planarisation.

- A dual sacrificial layer approach enabled thick interconnect to combined with a sub-micron air gap. AZ4562 photoresist can be used as an electroforming mould for thick interconnect. Titanium was retained for the air gap because of its clean etching characteristics.

- The key advantage of this process flow is the ability to be readily transferred to a range of substrates and the flexibility to produce thick, low loss, interconnect feeds. In the chapter 6 process flow, the long exposure to HF:ethanol could cause delamination on a substrate such as glass.

- For thick interconnect devices on glass, a peak Q of 243 at 0.9 GHz for 0.26pF was achieved. For GaAs this was lower at 19 at 0.9 GHz for 0.42pF and for silicon, this was lower again at 0.53 at 0.9 GHz for 0.57pF.

- Tuning limitations associated with latching of the upper electrode have been identified. These are caused by the use of photoemulsion masks and the temperature instability of the AZ4562 photoresist. Alternative thick resist technology in combination with chrome masks have been identified as a solution to this.

- A single-gap split lower electrode structure was implemented to compare against the two-gap approaches presented. A tuning ratio of 1.52:1 was achieved from an unbiased capacitance of 0.75pF measured on the VNA at 1.66 GHz. This confirms the simulated predicted improvements for this design presented in chapter 3.

- The effective development of micromachined inductors is integral to the final implementation of *LC* tanks oscillators in RF MEMS circuits.

- The dual sacrificial layer approach with AZ4562 enables inductor coils to be suspended above a substrate in parallel with the capacitors. These have a peak Q of 4.5 at 0.9 GHz and a self-resonant frequency of 3.05 GHz on silicon substrates.

Chapter 8

Conclusions and suggestions for future work

This thesis has presented comprehensive coverage of the development of a micromachined tunable capacitor which represents the first RF MEMS research work at this University. The device has been designed and modelled using Coventorware. All the fabrication details have been developed to enable structures to be released successfully. RF testing has realised state-of-the-art performance. Finally, suspended inductors have been developed using a process flow which is compatible with the capacitors.

Key results from this thesis are:

- State-of-the-art tuning ratio demonstrated using the two-gap tunable capacitor.
- State-of-the-art Q factors using thick gold electroplated interconnect on glass.
- The first RF MEMS research work conducted at the University of Durham.
- The development and delivery of all cleanroom fabrication and testing techniques.
- The first simulations published using Coventorware on the two-gap structure.
- Topological studies on the electrode surfaces and influence of the titanium sacrificial layer on high aspect ratio devices.

- Demonstration of suspended micromachined inductors using a minor modification to the capacitor process flow.
- The development of substrate independent process flows which are readily transferable to the Filtronic production line.
- 8 papers generated and a patent.

8.1 Conclusions

This thesis has detailed the development process for widely tunable micromachined capacitors. In recent years, as demonstrated by the references in chapter 2, research has been extremely active worldwide in the field of RF MEMS.

At the time of development, the tuning ratios exhibited by the devices in chapter 6 were the highest reported in the literature. Recent advances to the tuning ratio of the two-gap design have been achieved [69] through the use of aluminium electrodes. The native oxide enables the electrodes to achieve total contact without shorting the capacitor. This essentially provides an additional tuning range which cannot be achieved through the gold or nickel devices presented here. As discussed, however, a key benefit of RF MEMS is the use of air dielectrics. The inclusion of a native oxide as part of the capacitive tuning state is therefore removing the air and will have an impact on the quality factor of the device at high capacitances.

The two-gap design has been demonstrated through simulation and testing to provide significant tuning benefits over the single-gap designs. A tuning ratio of up to 7.3:1 has been demonstrated. The downside is that the inclusion of separate biasing and capacitive electrodes has an impact on total device area.

The self-planarising approach using titanium as a sacrificial layer limited interconnect feed thickness and therefore inhibited the RF performance, in terms of the quality factor. A dual sacrificial layer approach was developed to demonstrate quality factor gains achievable through thick electrodes. Interconnect up to 6.2μm thick was demonstrated by using AZ4562 photoresist in conjunction with titanium as a dual sacrificial layer. Capacitors fabricated using the thick interconnect approach on glass exhibited a state-of-the-art peak quality factor of 243 at 0.9 GHz.

Limitations with the temperature resistance of standard thick positive photoresist combined with photoemulsion masks introduced effective bump stops into the upper electrode, which restricted the tuning range of these devices. In future developments this can be remedied through improved photoresist and mask technology.

The dual sacrificial layer approach lends itself to the development of suspended inductor coils. These have exhibited an inductance of 9 nH and a Q of 4.5 at 0.9 GHz on low resistivity silicon. The self-resonant frequency of 3 GHz needs to be increased to form an effective LC tank with the capacitor structure. This can be achieved by improved electrode design or improved isolation from the substrate.

Micromachining simulation software is still in its infancy compared to CMOS design software. Coventorware proved successful in identifying key design parameters and creating suitable designs for implementation. The resulting simulations were in the correct regime when compared to experimental results.

The capacitors use a high aspect ratio approach with a small gap to reduce the effect of electrode curvature on the tuning ratio. Therefore, the ideal parallel plate situation for achieving a high tuning ratio is better achieved. Filtronic has purchased the patent for the key processes required to achieve this.

Finite element analysis tools such as Coventorware are limited in their true representation of the surface topology which can be a significant factor in real device performance. Simulation assumptions are made with respect to planar electrodes and at a distance this can be valid. However, the AFM results in chapter 6 show that the surface topology at close spacing is a consideration with respect to surface meshing and sacrificial layer pattern transfer.

Device specific models and algorithms would need to be developed to improve the simulation of surface topology on device performance. Furthermore, Coventorware is very limited with respect to RF simulation and the inclusion of the feature would greatly benefit its applicability to RF MEMS. The original aim of this work was to use the commercially available MEMS simulation tools as a guide to a design rather than an absolute result.

8.2 Future work

As discussed in chapter 1, the ultimate aim of this work is to transfer the RF MEMS components to existing microwave monolithic integrated circuits (MMICs). The original impetus behind RF MEMS was to provide high performance on-chip components. Therefore to produce a RF MEMS tank packaged as a discrete negates many of the performance advantages. Even wire bonding between a MMIC die and MEMS die introduces inductive parasitics, which impair performance.

There are three distinct approaches available to integrate RF MEMS components with MMICs. These are simultaneous fabrication, sequential fabrication and separate fabrication with flip-chip integration.

The aim of the simultaneous fabrication approach is to minimise masking and fabrication steps by sharing masks and depositions as much as possible with a MMIC process flow. This is feasible if there are common metallisations, for example thick electroplated gold.

However, for a MMIC fab with little or no micromachining experience this is a significant stage. Existing, and well refined, process stages need to be fully integrated whilst maintaining yield. This requires a redesign of every fabrication stage and a consideration of compatibility with the micromachined devices. If this can be achieved then simultaneous fabrication could be a low cost technique for high volume production because process steps are minimised.

From a performance perspective, interconnects can be minimised and the MMIC and RF MEMS closely integrated. Importantly for practical simultaneous integration, the fabrication should all be performed in the same cleanroom facility.

Sequential fabrication requires the MMIC to be fabricated first followed by the RF MEMS component or vice versa. This essentially combines the number of MMIC process steps and masks with the RF MEMS steps and masks. This makes less efficient use of materials and process flows and is therefore more expensive than the simultaneous integration approach.

However, the sequential technique does have a viable advantage. For example, an established MMIC process flow could be performed in a MMIC fab. The device could be protected and then transferred to a specialist MEMS fab. Providing the MEMS process flow does not damage the MMIC then the micromachined device could be fabricated on top of the MMIC. This enables a well-established MEMS process flow to be closely integrated with a well established MMIC process flow without radical process redesign. Performance could be comparable to the simultaneous technique but fabrication time and therefore cost is increased.

Sequential fabrication opens up the possibility of using the thin electrode design without impairing performance. Interconnect to the capacitor could be fed from below. This would remove the requirement for thick interconnect feed to sustain high quality factors.

A third integration technique is to fabricate the MEMS and MMIC devices on separate substrates. The MEMS device can then be transferred to the MMIC substrate using flip-chip. This enables chemically incompatible process flows or even different substrates to be used. However care needs to be taken to ensure interconnect parasitics are minimised since the device is not as closely integrated as in the other techniques. This is the simplest technique from a technical perspective because it enables RF MEMS components to be bulk manufactured and shipped to a MMIC fab for integration onto their devices.

Surface micromachining shares many process methodologies with traditional integrated circuit (IC) fabrication. However, the crucial difference is that IC encapsulation and packaging does not allow for the movable or delicate parts of micromachined structures.

Prior to wafer dicing, ICs are encapsulated in thick protective polymers. This provides protection against debris and moisture. If this basic encapsulation is eliminated then the dicing and packaging processes need to be much cleaner and mechanically delicate. In this situation, the chip header becomes the primary protection for the microsystems device.

Wafer level packaging uses caps to protect the micromachined devices. These caps have been demonstrated using bulk micromachining. The individual caps have to be flip-chip bonded over the device to be protected. This approach relies upon a low thermal mismatch between the cap and the host wafer. Flip chip bump stops need to be included on the host wafer.

A better route for the widely tunable capacitor is to use a surface micromachined cap. Stark et al [122] demonstrated surface micromachined caps using nickel electroplating and solder sealing. These were fabricated over the micromachined devices. This additional processing stage is a feasible route for the capacitors in this thesis because it could be included in the surface micromachining approach already present.

Finally, before this and other RF MEMS devices enter the market place much more work with respect to lifetime and environmental testing needs to be undertaken. This would test both the device and its packaging solution. Ultimately though, the RF industry needs to invest heavily in the technology if it is to succeed.

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