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A Non-Isolated DC-DC Converter With An Ultra-High Voltage Ratio for Offshore Power Applications

Dax Blackhorse-Hull

A Thesis presented for the degree of

Doctor of Philosophy

Department of Engineering
Durham University
United Kingdom
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Abstract

To maximise renewable energy generation, different forms of renewable power systems will need to be utilised. With this comes the opportunity to minimise capital expenditure and spatial usage via co-location. A promising co-location opportunity comes from the integration of the offshore wind farms with wave energy converters. Where floating or submerged wave energy converters are placed within the space between offshore wind turbines, to optimise marine spatial usage and utilise the same electrical infrastructure. To achieve this integration, the low output voltage of the wave energy converters would need to be stepped up to a medium voltage compatible with the inter-array voltage of an offshore wind farm. Conventionally, power converters which utilise step-up transformers have been adopted to produce similar forms of voltage conversion. While effective for offshore wind applications, complications arise from the mechanical constraints and environmental hazards associated with the use of a transformer on a floating or submerged platform. To study this issue, the work presented explored a strategy to achieve low to medium voltage conversion without the need for a step-up transformer. This strategy involved the exploration and development of transformerless DC-DC converters capable of high and ultra-high voltage conversion ratios, which produced an output voltage multiple times greater than the given input voltage.

Conventionally, to achieve a high voltage conversion ratio (> 10) in generic DC-DC converters, designs either require the use of excessive duty ratios (> 0.75) or the integration of voltage multiplying sub-circuits. Excessive duty ratios are often associated with reduced operational power efficiency, which limits the maximum amount of energy that may be extracted from a power system. Conversely, voltage multiplying sub-circuits increase circuit complexity while maintaining high operational efficiency. Therefore, voltage multiplication sub-circuits are often the chosen strategy to achieve high voltage conversion ratios when the maximisation of energy extraction is of high priority. To electrically integrate low-voltage wave generation technologies into medium-voltage offshore wind farm infrastructure, ultra-high voltage conversions (> 40) would be required. To achieve this, combinations of voltage multiplication techniques demonstrated within the literature were explored and evaluated for suitability.

Three transformerless DC-DC converters were sequentially conceptualised and devel-

oped. The operational analysis of all designs was presented and then subsequently validated via simulated and experimental demonstration. The novel continuous operation of a 1 kW scalable bipolar switched capacitor-based boost converter capable of a high voltage conversion ratio at a 98.2 % power efficiency was initially proposed. The experimental converter demonstrated a gain of ±10 via the step up of a 100 V input into a ±1 kV output. Following this, a scalable unipolar switch capacitor boost submodule was combined with a new method of scaling the voltage lift switched inductor topology to achieve ultra-high voltage conversion. The device demonstrated a voltage conversion ratio of 41 with a 100 V input and 4.1 kV output, at 97.5 % efficiency when operating at 1 kW. Finally, the bipolarity was reintegrated into the design to demonstrate an innovative DC-DC converter capable of a greater voltage conversion ratio than the previously demonstrated converters and those reported in the literature for continuous, not isolated, operation. The peak operating efficiency was recorded during a 2 kW test with an input of 100 V and output of ±4 kV where the converter achieved an efficiency of 95.7 %. To demonstrate the ability of the converter to achieve a continuous medium voltage output from a range of low voltage inputs, two DC sweeps were conducted at 1 kW. During the unipolar DC sweep, the positive output of the converter was referenced to the negative output. From this operation, the converter produced a single 4.7 kV output for an input voltage range of 40 - 125 V. During the bipolar DC sweep, the two outputs of the converter were referenced to a common ground. From this operation, the converter produced a positive and negative output of ±4.7 kV output for an input voltage range of 70 - 200 V. When considering both unipolar and bipolar operation, the converter demonstrated a voltage conversion ratio range of 24 - 118.

Opportunities for power efficiency optimisation were identified based on the simulated and experimental findings. A particular focus was on the reduction of power and voltage losses in switched capacitor voltage multipliers. From this, key trade-offs were identified between both types of losses and capacitor sizes. The greatest unrealised pathway for power loss reduction originated from the active switching devices. A focus on the reduction of conduction-based losses led to the selection of devices with low on-state resistances. Due to this, the greatest proportion of power dissipation originated from switching-based losses. From this, strategies for the reduction of switching losses were identified as a key area for future research. Further opportunities for development were identified based on the experimental findings, strategies for integration into a solid-state transformer, allowing for bidirectional power flow, upscaling operation power and potential alternative applications were outlined and discussed.

Declaration

The work in this thesis is based on research carried out at the Department of Engineering, Durham University, United Kingdom. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

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Firstly, my thanks to Professor Alton Horsfall for his guidance and support throughout this process and for ensuring we did not 'kill each other in the 3 years of the project'; And to Dr Nur Sarma for her thorough feedback on the project, including when to utilise semi-colons appropriately.

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Finally, I would like to thank Dr Oliver Morgan Clague for playing a significant role in my decision to undertake this PhD... I will never forgive you.

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Nomenclature

Symbols

η	Efficiency
C	Capacitance
D	Duty Ratio
f	Switching Frequency
I	Current
L	Inductance
N	Number of
P	Power
R	Resistance
V	Voltage

List of Acronyms

AC	Alternating Current
ADC	Analogue to Digital Converter
BCM	Boundary Conduction Mode
CBC	Conventional Boost Converter
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DC	Direct Current
FWBVLSIMBC	Full-Wave Bipolar Voltage Lift Switched Inductor Multi-level Boost Converter
FWCW	Full-Wave Cockcroft-Walton
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
MBC	Multi-level Boost Converter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor

MVAC Medium Voltage Alternating Current

MVDC Medium Voltage Direct Current

PV Photovoltaic

PWM Pulse Width Modulation

SiC Silicon Carbide

SI Switched Inductor

SST Solid-State Transformer

VLSIMBC-HCL Voltage Lift Switched Inductor Multi-level Boost Converter High Capacitance Series Inductor

VLSIMBC-HC Voltage Lift Switched Inductor Multi-level Boost Converter High Capacitance

VLSIMBC-LCL Voltage Lift Switched Inductor Multi-level Boost Converter Low Capacitance Series Inductor

VLSIMBC-LC Voltage Lift Switched Inductor Multi-level Boost Converter Low Capacitance

VLSIMBC Voltage Lift Switched Inductor Multi-level Boost Converter

VLSI Voltage Lift Switched Inductor

WEC Wave Energy Converter

Dedication

Dedicated to my wonderful partner Amy... and living the PhDream

CHAPTER 1

Introduction

Innovations in the renewable energy sectors have led to a surge in the development of DC-DC converter topologies to accommodate new generator designs with the aim to maximise power extraction [1]. To minimise transmission-based power losses, high-gain, high-efficiency power converters have been a key component for the integration of renewable energy systems into distribution networks [2–4].

With the expansion of the offshore wind sector has led to larger capacity wind farms. With this comes the opportunity to exploit the existing electrical infrastructure for use in alternative renewable generation [5]. Wave energy converters (WEC) transform the kinetic energy of waves into electrical energy [6, 7]. The technology has yet to reach maturity due to a diverse set of challenges, including: development of power-efficient designs, optimising power extraction from high peak, low average power of waves and large initial costs [6–8]. While many WEC projects focus on efficient and scalable designs [9–12], work to explore generalised integration solutions of WECs into the distribution grid has

been limited. One potential solution is to integrate WECs with offshore wind farms, utilising the space between wind turbines for placement and electrically connecting to established infrastructure [5]. This approach would optimise marine spatial use and reduce capital expenditure in comparison to the development of 2 separate renewable energy installations.

1.1 Wave and Wind Energy Integration

As the offshore wind sector is reaching maturity and the wave energy sector is still emerging, any integration between the technologies would require wave technology to adapt to the established requirements of wind technology. Therefore, to integrate WEC platforms into offshore wind farms, the WEC power take-off system must be compatible with the current and ideally future infrastructure of offshore wind farms.

Within the UK offshore wind farm arrays primarily operate at 33 kV_{AC}, with discussion of future wind farms operating at 66 kV_{AC} [13]. Additionally, due to their increased efficiency and safety, DC collection networks are becoming an appealing future alternative for offshore wind farm infrastructure [14]. Due to the relative immaturity of the sector, there has been no convergence on operating voltages for WEC platforms. Current discussion within the literature outlines a range of low voltage operating points ranging from 40 V_{AC} to 1 kV_{AC} [15–17]. Of these, the WEC platforms may be divided into medium voltage platforms, which operate around 1 kV_{AC} [17] and low voltage platforms, which operate in the range of 40 V_{AC} - 240 V_{AC} [15,16]. To achieve effective wind-wave integration, the WEC output must be stepped up into a voltage comparable to a given offshore wind farm array voltage.

For high voltage step-up applications, including both AC & DC networks, designs commonly rely on transformers with large voltage step-up ratios. While demonstrably

effective in offshore wind applications, and useful for both galvanic isolation, offering circuit protection; and simple voltage conversion method, only requiring an AC or pseudo-AC input. Transformer-based designs are often subject to leakage inductance, which generates overvoltage spikes that reduce component reliability and lifespan [18]. The mechanical stress of the transformer, related to the size and mass of the component, can introduce further design constraints [19]. For WECs, mechanical stress may impede technological development as designs would be required to ensure both enough buoyancy in floating platforms and adequate shielding in the event of device failure to prevent transformer oil leakage. A simple solution would be to utilise a separate platform for power conversion, relieving the WEC of the constraints of the transformer, while also allowing the use of pre-existing, transformer-based technology. However, such a design would be subject to transmission based power losses from the low-voltage, high-current output of WECs, leading to conduction losses through connecting cables, reducing the power extracted and overall system efficiency. Therefore, to aid in the maximisation of power extraction, some form of voltage conversion is required within the WEC platform. With this, transformerless high-gain DC-DC converters offer a potential, physically small, lightweight solution.

While transformers within a WEC platform are not ideal, the galvanic isolation and associated circuit protections are paramount in offshore wind farms. This issue may partially be solved with the use of currently utilised transformer based power converters. Galvanically isolated designs, capable of stepping up the MVAC output of wind turbines, may be used as an integration point for multiple WEC platforms into the electrical network of offshore wind farms. This strategy would be effective for a medium voltage WEC platform, because the output voltage is similar to an offshore wind turbine. Low voltage WEC platforms would require an additional voltage conversion stage to achieve an inte-

grable voltage. Figure 1.1 outlines a block diagram of how low voltage WEC platforms may be integrated into offshore wind farm infrastructure, utilising an in situ converter to achieve a medium voltage, and an isolated converter to step up into a compatible inter array voltage.

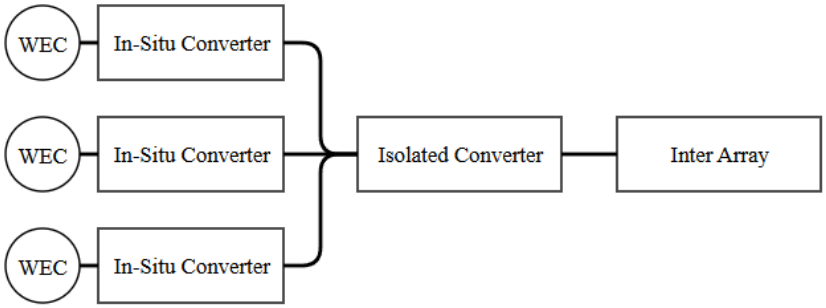

Figure 1.1: Wind-wave electrical integration outline

In this paradigm, the power converter within the WEC would only be required to step up the WEC output voltage to the output voltage of an offshore wind turbine rather than the inter-array voltage. Additionally, the transformer based power converter would not physically impede the connected WEC platforms, mitigating design constraints.

To realise the highlighted in-situ LVAC-MVAC converter, power electronic circuits may be utilised as shown in Figure 1.2

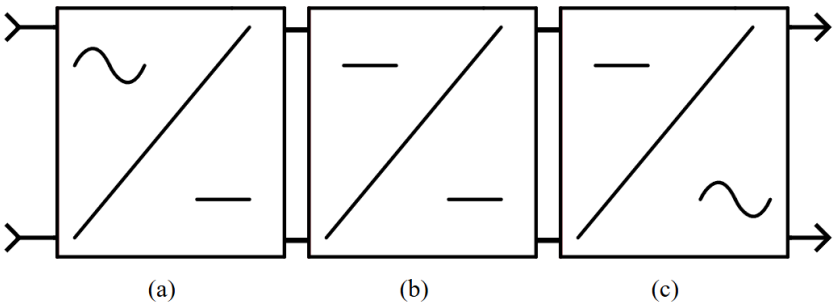

Figure 1.2: Block diagram of a proposed in situ converter where: (a) is a low voltage rectifier (b) a transformerless DC-DC converter, and (c) is a medium voltage inverter.

Of the 3 stages low voltage rectification and medium voltage inversion are relatively well understood [20–22], whereas transformerless LVDC-MVDC are less well researched.

With this comes the opportunity to explore the potential of ultra-high-gain DC-DC to achieve low to medium voltage conversion.

1.2 Research Aim

This project sought to explore the potential of transformerless DC-DC converters for LVDC to MVDC conversion as an alternative to conventional step-up transformers. The project objective was the development of a DC-DC converter that could step-up a range of low voltage inputs similar to reported WEC outputs, into an output voltage that could be inverted into an MVAC comparable to that generated in offshore wind turbines. With this, a specific target output of 4.7 kV_{DC} was identified, as this is the required voltage to achieve 3.3 kV_{AC} inversion, assuming the utilisation of a standard 3-phase inverter circuit. This voltage would be compatible with the power converters proposed as a WEC integration point. As identified, different low-voltage WEC platforms have reported operation in the range of 40 V to 240 V. After rectification, this voltage range would be approximately 38 V to 230 V, when assuming a full wave 3-phase rectifier. This translates to a voltage conversion ratio range of 20 - 124 to achieve an output of 4.7 kV_{DC}. When discussing high-gain transformerless DC-DC converters, a voltage conversion ratio of 10 [23–26] is considered high, with little research present exploring voltage conversion ratios above 20, which has been termed ultra-high [12]. Therefore, this project aimed to demonstrate a proof of concept device, with a voltage conversion ratio range equal to the ratios required for low voltage WEC platforms to achieve 4.7 kV_{DC}.

1.3 Thesis Structure

The thesis is organised into the following:

Chapter 2 explores innovative DC-DC converter voltage multiplication techniques capable of high step-up voltage conversion described in the literature. These techniques are discussed based on key characteristics, including isolation, output polarity, directionality of power flow and scalability. The techniques are evaluated to determine suitable designs to achieve the project objective.

Chapter 3 explores the potential of a high-gain single switch, bipolar converter operating with a continuous output. The design and analysis of a scalable, non-isolated, bipolar, switched capacitor-based topology, capable of producing a voltage conversion ratio of $\pm$ 10 with inherent voltage balancing within both the positive and negative output, are presented. The experimental characterisation of a 1 kW laboratory demonstrator is presented to experimentally validate simulated results and theoretical analysis.

Chapter 4 primarily explores the scalability of a unipolar variant of the switched capacitor design presented in Chapter 3. Additionally, a voltage lift switched inductor-based topology is identified and examined based on scalability and ability to achieve high voltage conversion ratios. A 4 kV voltage lift switched inductor multi-level boost converter capable of a voltage conversion greater than 40 is presented and analysed with a particular focus on non-idealities, including inductor imbalances, scalable voltage losses from the switched inductor topology and the trade-off between increased capacitance and voltage spikes. A secondary set of tests, which explores transient mitigation through variations of the capacitance within the switched capacitor network and the introduction of a small series inductor within the first stage of the network, is also presented. Findings from the secondary test demonstrate a trade-off between transient mitigation and operating efficiency.

Chapter 5 combines the bipolar design of Chapter 3 and the scalable topologies of Chapter 4 to realise an ultra high-gain bipolar DC-DC converter. With this, a ± 4.7 kV_{DC} laboratory demonstrator was developed and presented. Experimental results from the demonstrator are utilised alongside simulated findings to validate theoretical analysis. Results from additional tests, which demonstrate the ability of the proposed converter to maintain a stable output voltage of 4.7 kV_{DC} across an input voltage range of 48-200 V_{DC} are also shown. Factors that limited the voltage conversion range are identified, and solutions to achieve the voltage conversion ratio range specified in Section 1.2 are discussed.

Chapter 6 offers a summary of the findings of this thesis and identifies areas for future research, including strategies for upscaling operating power, without sacrificing voltage conversion; achieving bidirectional power flow, to allow for energy storage applications; and strategies of how the proposed converter, demonstrated in Chapter 5, may be integrated into a solid state transformer to achieve LVAC to MVAC conversion to facilitate wind-wave integration.

CHAPTER 2

Literature Review

2.1 Introduction

This chapter explores DC-DC converter designs, which may be used to achieve high voltage conversion ratios. The second section of this chapter describes the fundamental boost converter design and how it achieves voltage conversion. The third section considers key characteristics of DC-DC converters, which define their functionality as well as how these characteristics may contribute to the design specifications. This includes aspects related to galvanic isolation, unipolar and bipolar outputs, direction of power flow and the ability to scale up designs to achieve greater voltage conversion ratios. The fourth section in this chapter explores high-gain voltage multiplication techniques reported within the literature and compares them to these key characteristics. Finally, a comparison between these techniques is presented and evaluated to identify suitable designs to achieve the project objective.

2.2 DC-DC Converter Theory

DC-DC converters are utilised to change a given input voltage into a specified output voltage. Converters which produce a lower output voltage than the input are designated as buck converters, whereas designs which produce a higher output voltage in comparison to the input are boost converters [20]. As the aim of this project is to produce high output voltages with low voltage inputs, only boost converters were considered.

2.2.1 Conventional Boost Converter

The most understood and arguably simplest type of boost converter is the conventional boost converter (CBC) [20] shown in Figure 2.1.

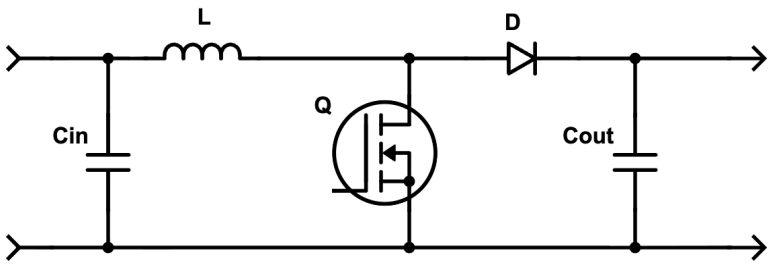

Figure 2.1: Circuit diagram of a CBC

The operation of the CBC may be observed by considering two working states, or modes of operation. In the first state, or Mode 1, the switching device conducts which creates a short pathway to ground. This pathway leads to the parallelisation of the input supply and inductor, allowing a relatively large amount of current to flow in the inductor, which in turn generates a magnetic field. In the second state, or Mode 2, the switching device blocks, removing the short pathway. In this configuration, the input supply and inductor are in series with the output capacitor; the magnetic field generated by the inductor collapses, generating a voltage spike. This inductive voltage spike combines with the input supply voltage, resulting in a higher voltage across the output capacitor. After

the next transition to Mode 1, while the magnetic field in the inductor regenerates, the output capacitor discharges into the output, allowing for a constant output voltage and current between switching modes.

This operation may be quantitatively described with relatively simple equations. During Mode 1, the voltage across the inductor and input stage are equal, giving:

$$V_{Lm1} = V_{in}D \tag{2.1}$$

where V_{Lm1} is the voltage across the inductor during Mode 1, V_{in} the input voltage, and D the duty ratio used to describe the ratio of Mode 1 operation over a complete switching period. The voltage across the inductor during Mode 2 may be described using Kirchhoff's second law:

$$V_{Lm2} = (V_{in} - V_C)(1 - D) \tag{2.2}$$

where V_{Lm2} is the voltage across the inductor during Mode 2 and V_C the voltage across the output capacitor. During steady state operation, when the charge of the inductor during Mode 1 is equal to the discharge of the inductor during Mode 2, $V_{Lm1} + V_{Lm2} = 0$. This allows the voltage conversion ratio, or gain of the CBC to be calculated with

$$\frac{V_C}{V_{in}} = \frac{1}{(1 - D)} \tag{2.3}$$

as the capacitor and output are in parallel, this equation may be expressed with

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)} \tag{2.4}$$

where V_{out} is the output voltage. Therefore, by varying the duty ratio, the magnitude of the output voltage compared to the input voltage may be controlled. Theoretically, as

D approaches 1, the voltage gain of a boost converter will tend towards infinity, offering infinite voltage gain. Practically, when the duty ratio surpasses 0.8, losses within the CBC reduce the output voltage substantially. This limits the practical voltage gain of a CBC to a maximum of 5 times the input value. To overcome this limitation, research has explored alternative designs to the CBC to achieve greater voltage conversion ratios in addition to offering additional capabilities to improve the functionality of a given DC-DC converter.

2.3 DC-DC Converter Characteristics

When discussing alternate DC-DC converters designs, key distinctions are required to accurately describe operation and capability.

2.3.1 Isolation

Isolation is a characteristic primarily associated with circuit protection. Isolated devices utilise magnetic coupling, often a transformer, to physically separate 2 sections of a circuit while maintaining an electrical connection. This is often used to reduce electrical noise between sections of a circuit and protect low voltage connections from high voltage operating points. [27].

A by-product of isolated topologies is the ability to achieve high voltage conversion ratios by configuring the turns ratio of the magnetic coupling. However, this comes at the expense of the previously identified transformer shortcomings. To outline the characteristic, Figure 2.2 provides a diagram demonstrating the difference between Isolated and non-isolated designs

Due to the separation, if a large voltage increase were to instantaneously occur in Figure 2.2(b), the coupling would limit the potential damage to the devices connected to the output. Conversely if the same increase were to occur in Figure 2.2(a), the increase

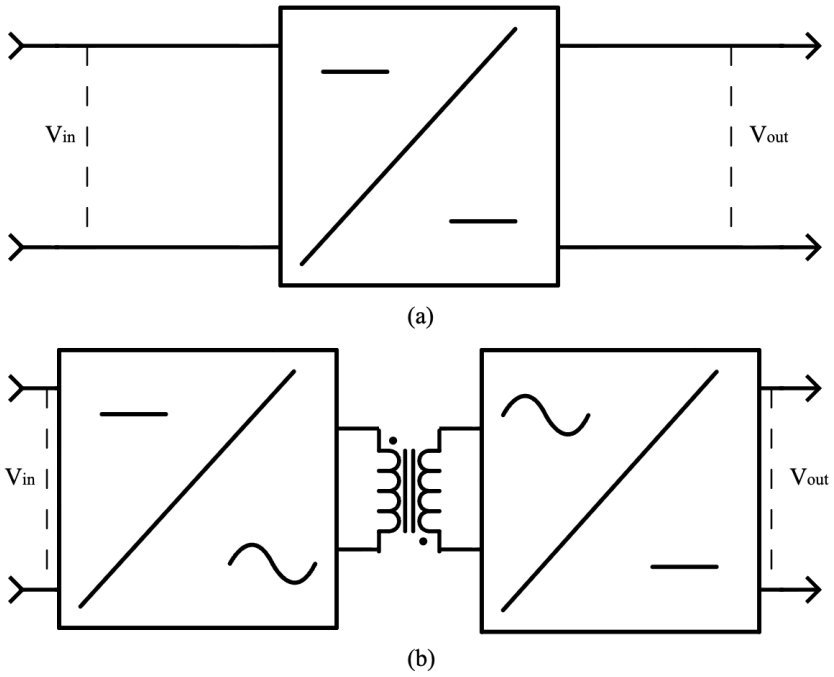

Figure 2.2: Block diagram of (a) Non-Isolated converter, (b) Isolated converter

would propagate through the converter, potentially damaging connected devices.

The implications of isolated technologies, which include increased instillation costs and mechanical fatigue associated with transformers, commonly utilised in isolated converters, have already been identified for wind energy applications [28]. These concerns are compounded for wave energy applications when considering many designs are more sensitive to mechanical and environmental constraints due to this, non-isolated topologies were identified as preferable for DC-DC converter designs in WEC platforms.

2.3.2 Polarity

Polarity outlines whether a given converter is capable of producing a single, unipolar, output or two, bipolar, outputs of equal and opposite magnitude. Bipolarity offers both the potential of integration into bipolar collection networks and devices as well as the ability to double a converters voltage conversion ratio by referencing the outputs to each

other rather than a common ground.

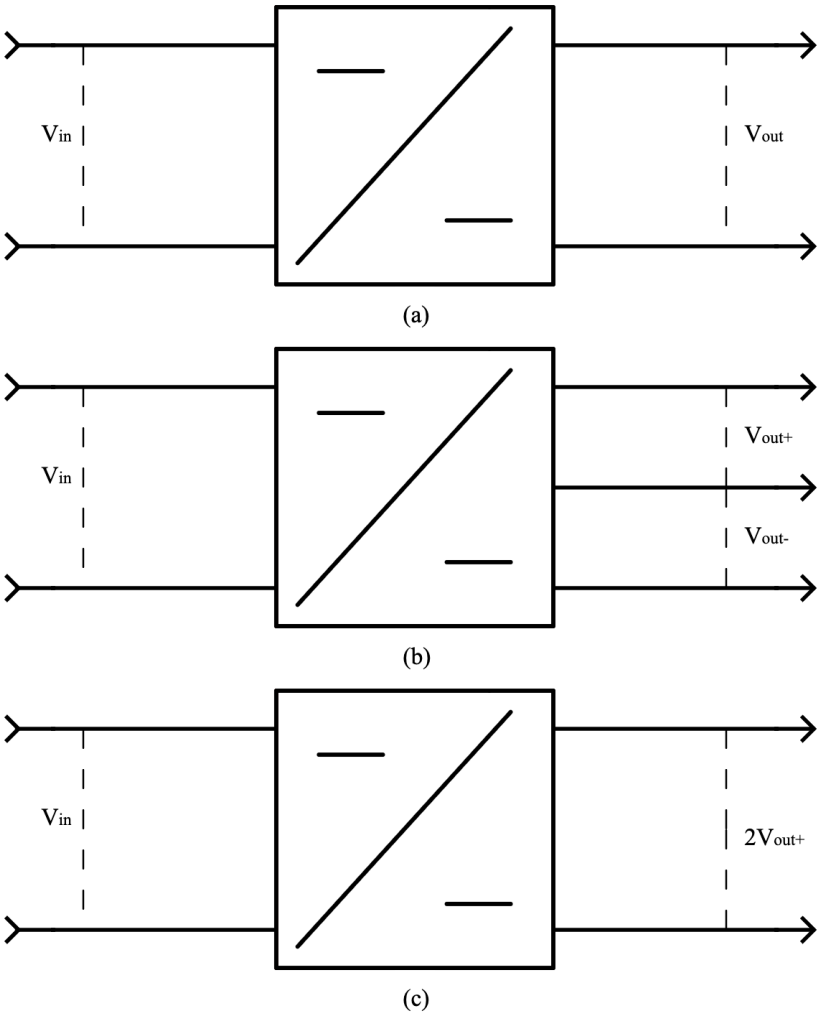

Figure 2.3: Block diagram of (a) Unipolar converter, (b) Bipolar converter with 2 outputs referenced to a common ground (c) Bipolar converter with positive output referenced to the negative output.

Unipolar converters, shown in Figure 2.3(a), utilise a single referenced output offering reduced circuit complexity compared to bipolar designs. Bipolar converters with 2 equal and opposite outputs, shown in Figure 2.3(b), have been discussed in the literature as part of a potential solution to cable failure in offshore wind farms. Such designs allow for continued power extraction in the event of a single cable failure, reducing unexpected costs at the expense of increased capital investment. However, the operating voltages of such designs are at least an order of magnitude greater than the project objective

[29, 30]. Bipolar converters operating with a single, combined voltage output, shown in Figure 2.3(c), increase the voltage conversion ratio given converter by a factor of 2, while offering the same integration potential as unipolar converters. This method of voltage multiplication may be compounded with other voltage multiplication techniques to achieve large voltage conversion ratios.

2.3.3 Directionality

The directionality of a DC-DC converter outlines how power may potentially flow through a given converter. Unidirectional converters, shown in Figure 2.4(a), allow power to flow in a single direction, extracting energy from a source and delivering energy into a single load. Bidirectional converters, shown in Figure 2.4(b), are capable of power flow in both directions. This allows devices connected to be treated as either a source or a load.

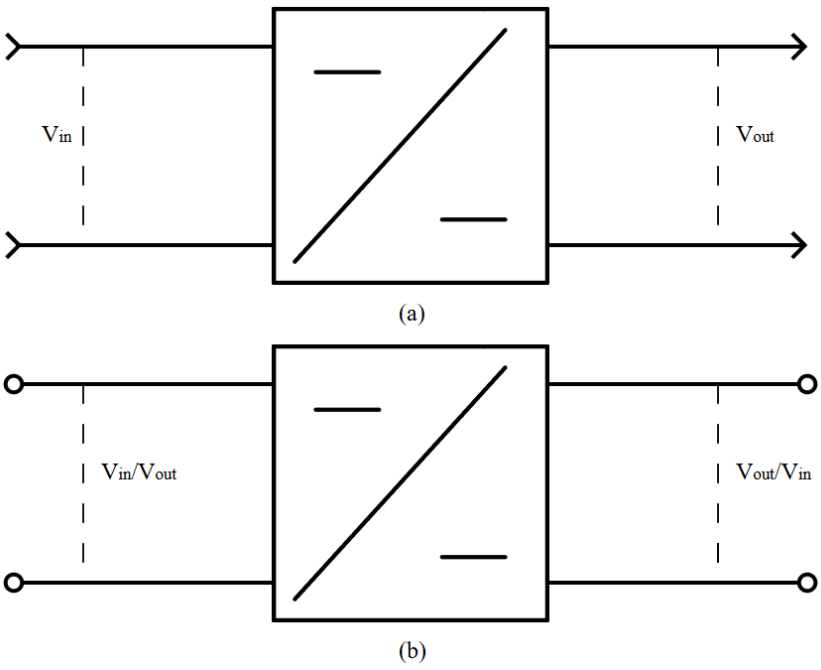

Figure 2.4: Block diagram of (a) Unidirectional converter, (b) Bidirectional converter

Bidirectional converters are capable of power extraction and injection, and as such have been identified for their ability to integrate energy storage systems in generator networks

[31–35]. Such designs may smooth out the large variation in power in renewable systems and as such may be highly benficial in providing a consistent power output for high peak, low average wave generation. Transformerless, high-gain bidirectional converters often require comparatively more switching devices than unidirectional devices, which often rely on diodes to limit power flow within the device [36, 37]. This requires bidirectional converters to utilise more complex control schemes during operation, as well as develop strategies to mitigate switching losses from the additional devices. Therefore, while a desirable trait, the use of bidirectionality must be considered based on its impact on operational complexity and efficiency.

2.3.4 Scalability

An intuitive method of achieving a high voltage conversion ratio is to use topologies that both produce a voltage gain and may stack upon themselves. Such designs may scale in series with another to achieve a cascading effect as shown in Figure 2.5(a) [32, 33, 38, 39]. Alternative designs may scale in parallel as shown in Figure 2.5(b) [37, 40–46]. These approaches may also be combined to achieve a form of cascaded parallelisation.

Series scaled designs are capable of quadratic voltage conversion ratios; however, this often comes at a trade off resulting from the increased voltages across individual components. which leads to increased power losses. Conversely, parallel scaled designs produce linear increases in voltage conversion ratio; however, the increased voltage may be shared across the parallel states to limit the voltage across of any singular device.

2.4 Analysis of Innovative High-Gain DC-DC Topologies

A range of voltage multiplication techniques presented in the literature were identified and compared, based on the outlined characteristics, to determine potential designs compatible

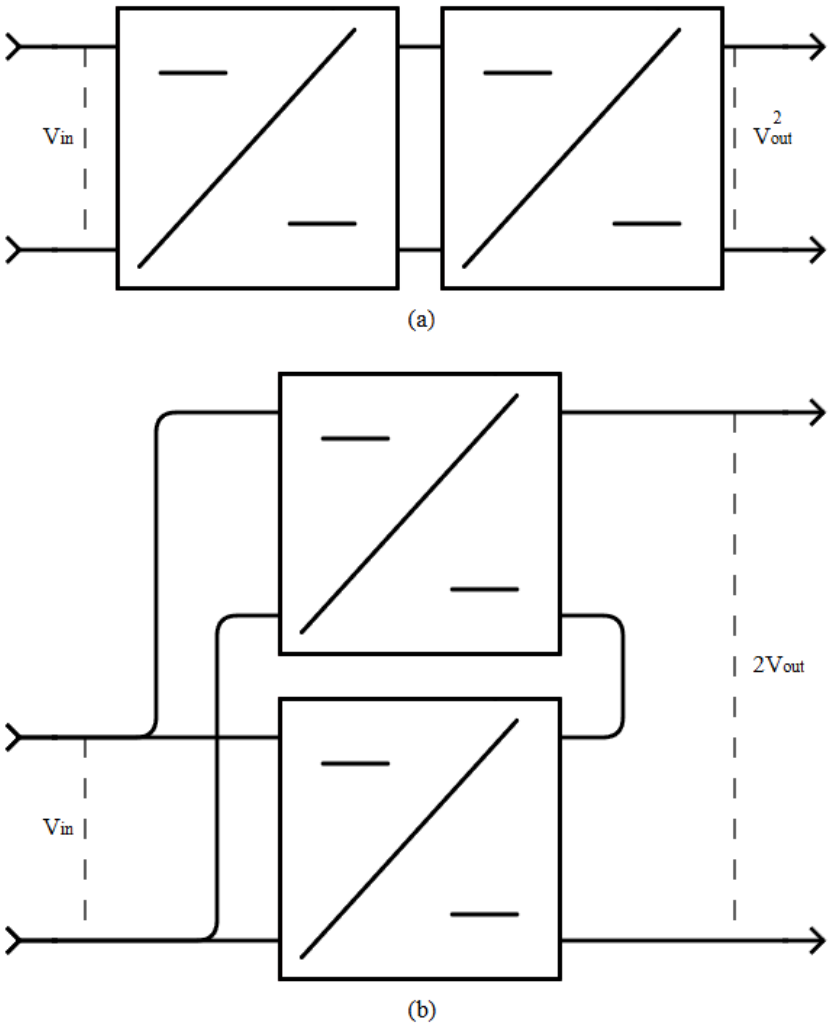

Figure 2.5: Block diagram of (a) Series scaled converter, (b) Parallel scaled converter.

with DC-DC boost converters.

2.4.1 Cascaded

Cascaded topologies may overcome the voltage gain limitation of a single CBC, by scaling multiple in series, combining the output of one CBC to the input of another [39]. These boost converters may be stacked to achieve a quadratic voltage conversion ratio, based on the number of CBCs utilised. The fundamental cascaded boost converter schematic is outlined in Figure 2.6.

For a 2 stage cascaded boost converter the voltage gain of the individual converters

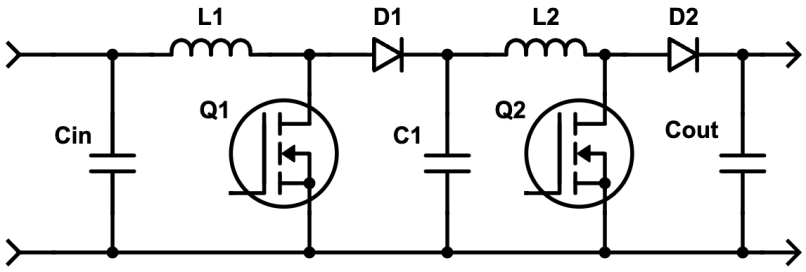

Figure 2.6: Circuit diagram of a cascaded boost converter

are multiplied to create a voltage conversion ratio of

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D_1)(1-D_2)} \tag{2.5}$$

where D_1 and D_2 are the duty ratios of the first (left) and second (right) switching devices with respect to Figure 2.6. When considering the scalable nature of the cascaded boost converter, this equation may be generalised, assuming all duty cycles are equal, to:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)^{N_{Cas}}} \tag{2.6}$$

where N_{Cas} is the number of converters cascaded. With the concept of cascaded boost converters, which involves connecting the output of one boost converter to the input of another, a range of cascaded boost converters, exploring different functionalities, have also been demonstrated. While non-isolated cascaded designs are more prevalent within the literature [32, 33, 38] isolated designs have also been reported [47]. With the use of a step up transformer, isolated designs can easily achieve high voltage conversion ratios at the isolation stage in addition to the cascaded boost stages [47].

The cascaded design is inherently scalable, as theoretically any number of boost converters may be cascaded together to achieve any target voltage converion ratio. However, as more stages are implemented, greater voltage stresses are observed by the subsequent

converters, leading to large power losses and reductions in power efficiency, mitigating the effective scalability of such topologies. Bidirectional cascaded designs utilise topologies capable of energy extraction and delivery have been demonstrated [32, 33, 48]. Due to the low component usage and relative simplicity, some bidirectional designs have reported power efficiencies in excess of 98 % [32, 48]. However, [32] achieved bidirectionally via the use of a buck and boost element, such designs have demonstrated voltage gains comparable to the practical limit of the CBC and [48] was only able to achieve greater than 98 % operation efficiency, with a high voltage gain when operating below 40 W. Boost based bipolar cascaded designs have been reported in low power applications (<5 W) where they demonstrate comparitively low power efficiencies and low voltage conversion ratios [49, 50]. This is likely due to the reported application of audio amplifiers. Further research would be required to determine the performance of bipolar cascaded designs at higher operating powers.

Due to the general definition of a cascaded design, a design capable of any of the key characteristics outlined is possible; the limiting factor originates from high voltage stress in addition to limited reported applicability at operating powers above 1 kW.

Quadratic Designs

To overcome the high voltage observed across the later stage switches in cascaded topologies, Quadratic converters exchange a switching device for a capacitor [24]. By definition, the quadratic boost converter is a design such that the duty cycle of a single switch has a quadratic relationship to the voltage gain, which may include a 2 stage cascaded design; however the commonly accepted fundamental quadratic topology is outlined in Figure 2.7. Such a design sacrifices the scalability of the cascaded boost topology to achieve lower voltage stress across switching components, reduce operation complexity and increase device

efficiency.

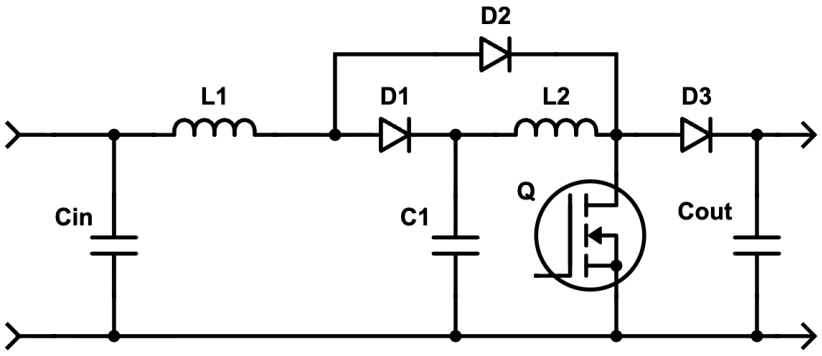

Figure 2.7: Circuit diagram of quadratic boost converter

The voltage conversion ratio of a basic quadratic boost converter is

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1-D)^2} \tag{2.7}$$

which offers a quadratic voltage conversion ratio when utilising large duty ratios. Similar to the cascaded boost designs, quadratic boost converters have been demonstrated to be capable of unipolar [51–53] or bipolar [54] operation as well as bidirectional power flow [55]. Quadratic topologies have also been demonstrated to achieve comparable operating efficiencies to cascaded designs; however, efficient operation has also only been demonstrated at operating powers below 1 kW [52, 53]

2.4.2 Coupled Inductor

Conceptually coupled inductors operate in the same manner as transformers, where 2 or more inductor windings are wound around the same magnetic core. With this, coupled inductor are subject to the same benefits and drawbacks as transformers. Including high efficiency, scalable voltage conversion, undesirable leakage inductances and comparatively greater weight to other components from the magnetic core [19].

The most well know example of a coupled inductor based boost converter is the flyback

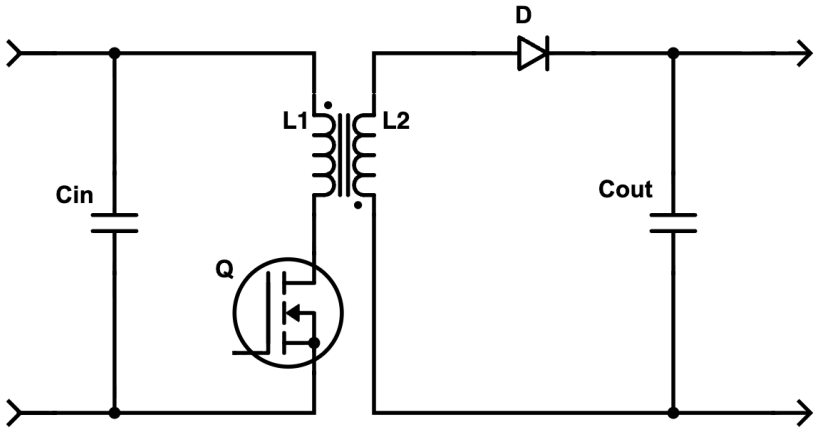

Figure 2.8: Circuit diagram of a flyback converter

converter [19]. Shown in Figure 2.8 flyback converters couple the primary inductor used in a CBC with a secondary inductor placed in parallel of the output capacitor. This design offers inherent isolation between the input and output, with a voltage conversion ratio of:

$$\frac{V_{out}}{V_{in}} = N_T \frac{1}{(1-D)} \tag{2.8}$$

where N_T is the turns ratio between the primary and secondary inductors.

As coupled inductor designs are based on a device with galvanic isolation, many isolated coupled inductor based topologies have been reported in the literature [23,25,34,56]. When isolation is not required, coupled inductor topologies may be reconfigured to allow a direct connection to the input and output [26, 57–60]. Bipolarity has also been achieved with coupled inductor designs, [26] reported a design capable of a balanced bipolar output with an operating efficiency of 93.3 % at 210 W, but demonstrated a voltage conversion ratio of ±4.4, which is comparable in magnitude to the CBC. [59] utilised a triple coupled inductor in a similar configuration to achieve bipolar outputs with a reported greater efficiency of 96.27 % at 200 W and a slightly increased voltage gain of ±5.9. As the voltage gain of these converters is proportional to the turns ratio of the coupled inductors, the gain is inherently scalable, without the need for additional circuitry. When considering

bidirectionality, coupled inductor designs possess an inherent advantage, as the direction of power flow dictates whether a coupled inductor with a given turns ratio will boost or buck [34]. However, as with other bidirectional designs, the ability to allow power to flow bidirectionally in a circuit required the use of comparably more active switching components than unidirectional designs. For example, the design proposed in [26] required 2 MOSFETs where as the bidirectioanl design outlined in [34] required 4.

When holistically considering coupled inductor topologies, designs capable of meeting all the ideal characteristics have been demonstrated within the literature. The voltage gain of coupled inductor topologies can be scaled relatively simply by adjusting the turns ratio. Furthermore, they may also be designed to limit the voltage stresses observed by active switching devices, offering an inherent advantage over cascaded and quadratic topologies. However, coupled inductor designs are subject to the same limitations of transformers, such as leakage inductance, which needs additional circuitry to mitigate [58]. Furthermore, as the aim of this project was to explore transformerless alternatives for high gain converters, the use of coupled inductors would undermine the initial goal of the project. Therefore, coupled inductor techniques were identified as unsuitable for the project design.

2.4.3 Switched Inductor

Switched inductor topologies offer an alternative use case for inductors in high gain applications [11, 61–63]. By charging inductors in parallel and then discharging in series, switched inductors offer a scalable form of voltage multiplication. Outlined in Figure 2.9, switched inductor topologies may replace single inductor stages in boost converter designs with a stacking inductor diode network.

When implemented into a CBC, and assuming no losses from the diodes, the voltage across an inductor during Mode 1 remains unchanged. During Mode 2 the voltage across

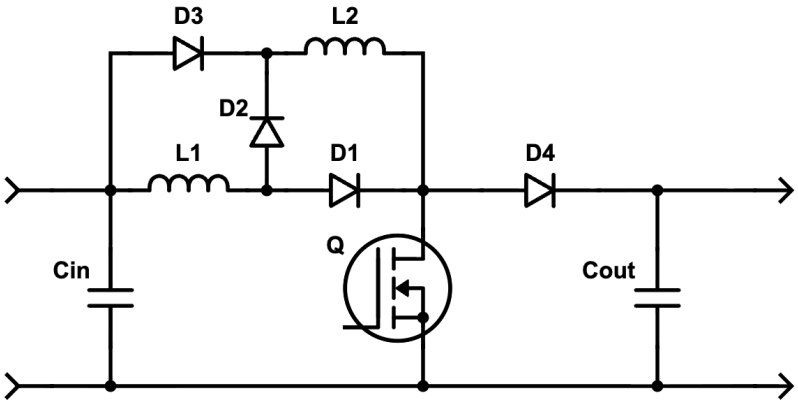

Figure 2.9: Circuit diagram of a modified CBC with a 2-stage switched inductor

a single inductor becomes:

$$V_{Lm2} = \frac{(V_{in} - V_C)(1 - D)}{N_L} \tag{2.9}$$

where N_L is the number of switched inductor stages. This leads to a voltage gain equation of

$$\frac{V_{out}}{V_{in}} = \frac{1 + (N_L - 1)D}{1 - D} \tag{2.10}$$

Due to the ability of the topology to be implemented at any point where there is a switching inductor, switched inductor topologies have been deomstrated with non-isolated converters [11, 61, 62], unipolar [11, 61, 62] and bipolar [63] as well as unidirectional [11, 61–63] and bidirectional [35, 36, 64] designs. No designs of isolated topologies utilising switched inductors were found within the literature. This was likely due to the lack of need for a scalable voltage multiplication switching network, when isolated topologies may simply change the winding ratios at the point of isolation to achieve the same effect.

Voltage Lift Switched Inductor

The voltage lift switched inductor (VLSI) topology is a variant of the switched inductor design, which exchanges the diodes forward biased during Mode 2 for a voltage lift

capacitor, illustrated in Figure 2.10 [12, 65].

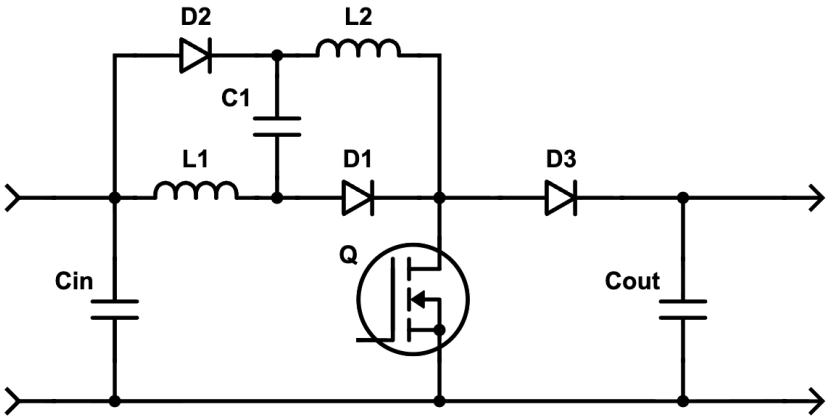

Figure 2.10: Circuit diagram of a modified CBC with a 2-stage voltage lift switched inductor

The voltage lift capacitor charges in Mode 1 and discharges in series with the switched inductors during Mode 2. Similar to the base switched inductor design, the voltage across an individual inductor remains unchanged during Mode 1. During Mode 2 the voltage across a single inductor becomes

$$V_{Lm2} = \frac{(V_{in} + (N_L - 1)V_{CVL} - V_C)(1 - D)}{N_L} \tag{2.11}$$

where V_{CVL} is the voltage across the voltage lift capacitor that, under ideal conditions, is assumed to equal V_{in}. This leads to a voltage gain equation of

$$\frac{V_{out}}{V_{in}} = \frac{N_L}{1 - D} \tag{2.12}$$

From this, it can be observed that a VLSI topology may achieve a greater voltage conversion ratio, for the same number of stages, compared to the switched inductor topology.

While from this analysis, voltage lift switched inductor designs are scalable [66], most literature which reported on the topology utilised a 2-stage design [12, 65]. Additionally, although voltage lift variants could be implemented into bipolar switched inductor

converters with relative simplicity, there has been limited demonstration of this.

Similar to switched inductor designs, the voltage lift variant has only been reported in non-isolated topologies, likely due to the redundancy of a high-gain sub-circuit operating with a step up transformer. Bidirectionality has also not been demonstrated in the literature; this is potentially due to difficulties appropriately charging and discharging the voltage lift capacitor during reverse power flow operation.

When considering the voltage lift variant of the switched inductor, initial research demonstrates that the topology can achieve a greater voltage conversion ratio than the CBC. However, research that explores key factors such as the scalability of the variant topology as well as the ability to operate in bidirectional and bipolar circuits was highly limited within the literature.

2.4.4 Switched Capacitor

Similar to switched inductor topologies, switched capacitor designs operate by charging capacitors either individually or in parallel and discharging in series to achieve an increased output voltage. As shown in Figure 2.11, switched capacitor topologies may create an output capacitor ladder, where in steady state all output capacitors (right-hand side) hold a potential difference equal to the voltage across the switching device. When utilised with a CBC, fundamental switched capacitor designs produce a voltage conversion ratio equation of:

$$\frac{V_{out}}{V_{in}} = \frac{N_C}{1-D} \tag{2.13}$$

where N_C is the number of stages within the switched capacitor topology. The topology possesses inherent scalability, with the gain of the sub-topology equal to the number of stages within the ladder. A bipolar switched capacitor boost converter has been realised

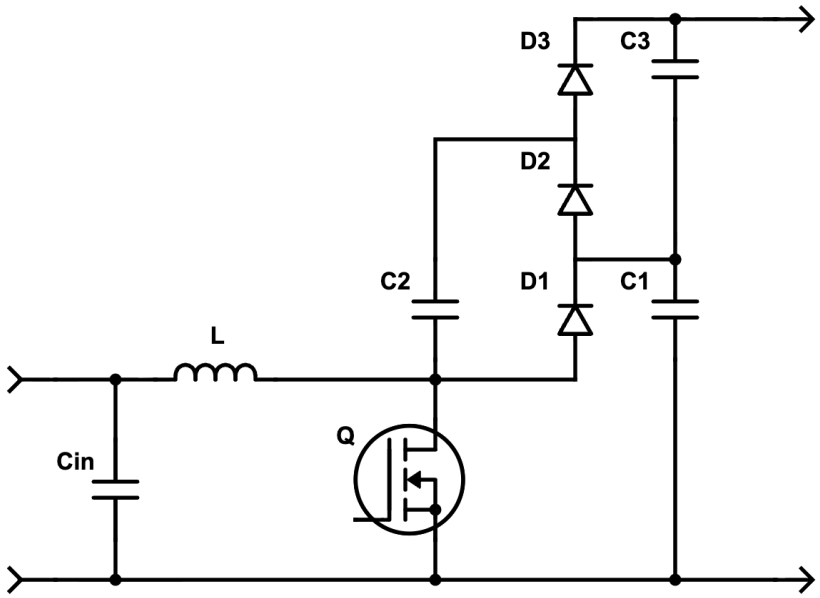

Figure 2.11: Circuit diagram of a modified CBC with a 2-stage Cockcroft-Walton switched capacitor

previously for pulsed power applications [67]. However, reports of continuous power designs have been limited to unipolar applications [37, 40–46]. Furthermore, reports which have experimentally demonstrated bidirectionality have utilised a variant of the switched capacitor that sacrifices scalability [45, 46].

2.4.5 Comparison of Discussed Topologies

Table 2.1 outlines the ability of the voltage multiplication techniques identified to achieve the characteristics highlighted in Section 2.3, based on the reviewed literature.

Cascaded designs have demonstrated the potential to achieve all characteristics at low power applications, whereas quadratic converters have demonstrated bipolarity, bidirectionality and non-isolated topologies at greater operating powers. However, the scalability of the topology is limited, making high power ultra high voltage conversion ratios difficult to achieve without excessive duty ratios. Coupled inductor designs have also demonstrated the potential to achieve all identified characteristics. However, due to the similarity of the

Table 2.1: Comparison of discussed voltage multiplication techniques based on identified key characteristics

Multiplication Technique	Non-Isolated Design	Bipolar Design	Bidirectional Design	Scalable
Cascaded	Yes	Demonstrated at <5 W	Demonstrated at gains ≈5	Via Number of Converters
Quadratic	Yes	Yes	Yes	No
Coupled Inductor	Yes	Yes	Yes	Via N_T
Switched Inductor	Yes	Yes	Trade off for Scalability	Via N_L
Voltage Lift Switched Inductor	Yes	Not Reported in Literature	Not Reported in Literature	Via N_L
Switched Capacitor	Yes	Pulsed-Power Application	Trade off for Scalability	Via N_C

voltage conversion technique to transformer based designs, coupled inductor topologies were deemed unsuitable for the project. Switched inductor designs presented a trade-off between scalability and bidirectionality. However, both non-isolated and bipolar designs have been demonstrated, which offered a potential technique to be utilised for the target ultra high gain converter. The voltage lift variant had not been reported in either bidirectional or bipolar designs; however, due to the similarity between the topologies, such designs are likely possible and have yet to be demonstrated. Furthermore, with the higher voltage conversion ratio, compared to the switched inductor topology, VLSI designs were considered a more attractive multiplication technique to achieve ultra high voltage conversion ratio. Similarly, switched capacitor designs have demonstrated key characteristics with the exception of bipolar operation for continuous power applications. As both inverting and non-inverting switched capacitor ladders had been presented in the literature,

it was highly likely that the design was possible but not yet reported.

When the identified voltage multiplication techniques were compared, it was prudent to consider how the discussed topologies operate as a submodule within the larger boost converter.

For medium and high voltage applications, the practical limitations of fast switching devices were also considered. In cascaded topologies, the switch parallel to the output would be required to tolerate the output voltage of the converter. This is often not an issue for low voltage applications; however, current commercially available SiC based MOSFETs are limited to 3.3 kV [68]. Higher blocking voltage IGBTs are available; however, these are undesirable due to their limited switching frequency, which in turn requires larger reactive elements within the converter. This leads to increased converter size and weight as well as increased switching losses compared to MOSFET devices [69]. This prevented the use of purely cascaded-based boost topologies in the project, as the switch parallel to the output stage would be required to operate at 4.7 kV. Similar to this, the switching device, used to create the short pathway to charge switched inductor topologies, must also be capable of withstanding the maximum output voltage of the stage. This prevented the use of purely switched inductor or VLSI based topologies. Switched capacitor topologies operate with an AC or pulse width modulated input, as such are located after switching devices, offering the potential of lower blocking voltage devices to be utilised as the voltage multiplication occurs after the switching device.

While discussed as individual topologies, many boost converter designs utilise a combination of voltage multiplication techniques to achieve large voltage conversion ratios [36, 44, 62, 70]. One common combination is to combine a switched capacitor ladder with the switched inductor topology, where the output of the switched inductor feeds the input of the switched capacitor module to achieve multiplicative voltage gains [36, 44, 62].

Alternatively, to reduce the voltage across the switching devices, a cascaded or quadratic converter could feed into the input of a switched capacitor ladder, reducing the required voltage across the device. To demonstrate how the different techniques may interact, Table 2.2 outlines the potential voltage conversion ratios of the proposed topologies, the maximum voltage of the switch stage, how the topology interacts within a given stage of a CBC and the component complexity of the circuit with an input capacitor.

Table 2.2: Voltage conversion ratio, point of interaction, maximum switch voltage and component complexity of the discussed relevant topologies

Multiplication Technique	Voltage Conversion Ratio	Stage Interaction	Maximum Switch Voltage	No. of elements: C	D	S	L
Conventional	$\frac{1}{(1-D)}$	-	V_{out}	2	1	1	1
Cascaded	$\frac{1}{(1-D)^{N_{Cas}}}$	Adds $N_{Cas}-1$ Stages to CBC	V_{out}	$N_{Cas}+1$	N_{Cas}	N_{Cas}	N_{Cas}
Quadratic	$\frac{1}{(1-D)^2}$	Adds 1 Stage to CBC	V_{out}	3	3	1	2
Switched Inductor	$\frac{1+N_L D}{1-D}$	Operates at Input	V_{out}	2	$2N_L$	1	N_L
Voltage Lift Switched Inductor	$\frac{N_L}{1-D}$	Operates at Input	V_{out}	N_L+1	$2N_L-1$	1	N_L
Switched Capacitor	$\frac{N_C}{1-D}$	Operates at Output	$\frac{V_{out}}{N_C}$	$2N_C$	$2N_C-1$	1	1

2.5 Consideration of High Gain Topologies for Wind Wave Integration

A non-isolated DC-DC converter that is capable of both high voltage gain and bipolar output may be utilised in a range of applications, including PV energy extraction and transmission [71], DC links for bipolar microgrids [72], and solid-state transformers [10,73], for applications in wind wave integration. A high voltage gain DC-DC converter may be realised by integrating input, switching or output stage voltage multiplication topologies with a conventional boost converter (CBC), as shown schematically in Figure 2.12 A CBC input stage utilises a single inductor to produce a voltage gain of up to 5 and a scalable voltage gain may be achieved by adopting a switched inductor-based topology [12]. By introducing additional switching stages to a CBC, a cascaded or quadratic topology, exponential voltage gains may be achieved at the expense of high component voltage stress [57]. Switched capacitor topologies are also capable of scalable voltage multiplication, at the output stage, with a linear scalability achieved based on the number of steps within the ladder [74]. Additionally, multiple switched capacitor ladders, connected to the same switch stage, may operate independently from one another, allowing for both inverting and non-inverting designs to be integrated simultaneously to support a continuous bipolar output [67, 75]. Voltage multiplication topologies from a given stage multiplicatively combine voltage conversion ratios with topologies from other stages, offering an opportunity for greater voltage conversion ratios. Similar characteristics may be achieved with the utilisation of isolated topologies, such as dual active bridges [76]. However, the use of a transformer incurs additional circuit weight, in turn reducing power density, higher component costs and increased leakage inductance. These adverse effects cause undesirable transient behaviour leading to such designs being less desirable for applications where

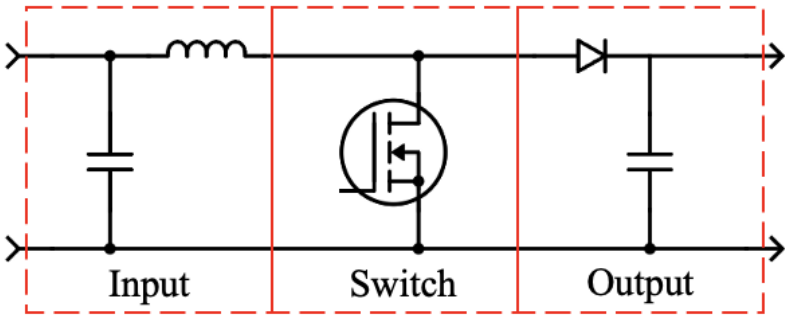

Figure 2.12: Circuit diagram of a CBC separated into 3 operating stages

galvanic isolation is not required [77].

A range of different non-isolated high-gain DC-DC converter topologies, which show evolution in different stages of the CBC, have been presented in the literature. Switched inductor designs have demonstrated high efficiency and voltage gain [11, 12, 57, 61, 65]; variations of this topology include voltage lift, which further increases voltage gain by swapping the series diode with a capacitor [12,65]. As well as coupled inductors, which offer reduced power losses at the cost of introducing increased leakage current and subsequent voltage spikes. These voltage spikes can be mitigated by additional filter circuits, but this can lead to either reductions in overall efficiency or increased circuit complexity [57, 70]. Cascaded and quadratic-based topologies have demonstrated high voltage conversion ratios above 10. However, due to their multiple switching stages, some reported designs have demonstrated comparably lower power efficiencies in relation to other high-gain DC-DC converter designs [71, 78, 79]. Similar to switched-inductor topologies, switched capacitor-based topologies possess scalable voltage gain, with multi-level and self-balancing outputs that present reduced voltage stress to the switching stage.

Cockcroft-Walton switched capacitor topologies utilise a series capacitor ladder to enable equal distribution of the output voltage between ladder elements. However, due to the series placements of the capacitors, the impedance of the topology increases rapidly, lead-

ing to a cubic relationship between voltage drop across the capacitors and the number of stages within the ladder, which negatively impacts the voltage gain of the topology [40–42]. In spite of this, experimental boost converter designs have demonstrated, via simulation, that the Cockcroft-Walton topology may produce voltage gains of 10 with up to 95.5% efficiency with an input power of 450 W [42]. The Dickinson multiplier, illustrated in Figure 2.13, utilises a parallel capacitor ladder to overcome the increased impedance observed in the Cockcroft-Walton topology. The parallel nature of the topology removes the voltage-sharing characteristic, leading to high voltage stress across components, and limits the topology functionality for high-voltage applications [43]. A hybrid topology, illustrated in Figure 2.14, mixing the series and parallel capacitors, to achieve reduced voltage drop in comparison to the Cockcroft Walton and increased voltage sharing compared to the Dickinson, was presented in [41]. This hybrid topology was capable of voltage ultra high gains greater than 10; however, the peak efficiency was less than that observed for cascaded and quadratic boost topologies at 90.9% for a 50 W device. Switched capacitor designs are often used in conjunction with switched inductor topologies due to multiplicative achievable voltage gain [44, 62, 67, 75], offering an alternative strategy for achieving voltage multiplication.

Both inverting and non-inverting switched capacitor topologies have been presented in the literature [9, 10, 43]. [43] demonstrates a bipolar Dickinson switched capacitor topology where the positive and negative outputs were connected to the same load, reducing the voltage stress on the output capacitor and doubling the effective voltage gain of the topology with the bipolar characteristic. A single switch DC-DC converter capable of a dual-polarity output with an inverting and non-inverting Cockcroft-Walton switched capacitor ladder has been identified in the existing literature [67]. This research has focused on pulsed power designs for water treatment applications rather than considering contin-

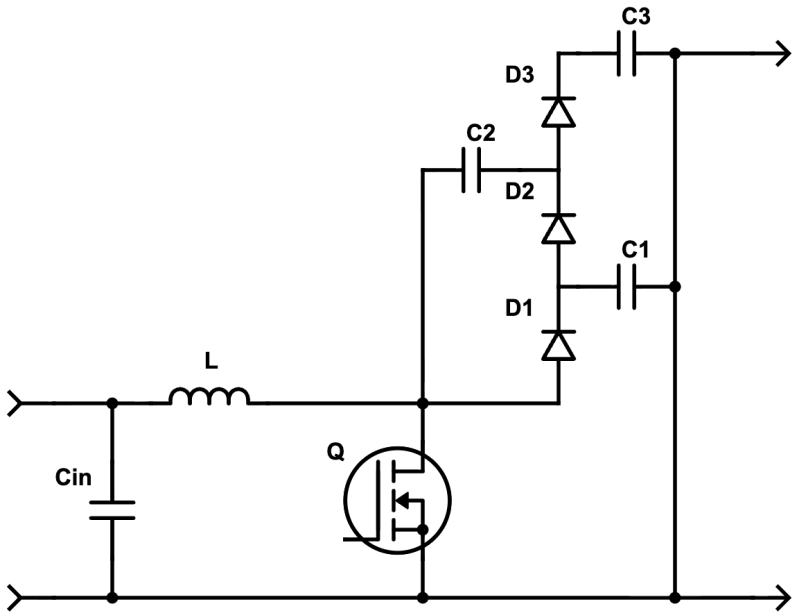

Figure 2.13: Circuit diagram of a 2-stage Dickinson switched capacitor

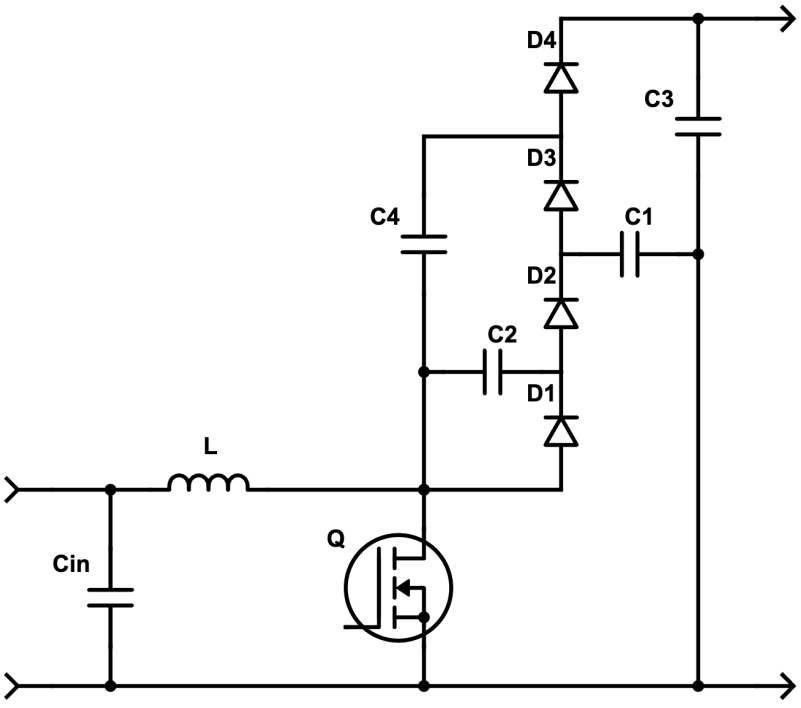

Figure 2.14: Circuit diagram of a 2-stage Hybrid Cockcroft-Walton Dickinson switched capacitor

uous operation for power extraction applications. Additionally, a full operational analysis of the circuit behaviour has not been fully explored. A converter that incorporates both types of switched capacitor ladder would be able to produce a balanced bipolar output

with a scalable gain while only requiring simple switch-driving techniques such as pulse width modulation (PWM).

This topological operation was identified as a suitable starting point for the exploration and development of novel DC-DC converters with high voltage conversion ratios for the integration of wind and wave generation technologies.

2.6 Chapter Summary

This chapter highlighted a set of key characteristics required for consideration for the selection of high-voltage gain DC-DC converter topologies. As this project sought to explore transformerless voltage conversion strategies, all topologies were required to be non-isolated. Bipolar and bidirectional designs offer an increased range of applications and functionality for a given converter. Bipolarity allows for integration into bipolar devices, as well as the potential to double the voltage gain of a converter when the outputs are referenced to each other. Bidirectionality allows for the consideration of energy storage solutions. However, this function is often granted at a trade off for either scalability or efficiency and may be solved with a separate dedicated circuitry. Hence, bidirectionality, while desirable, can be difficult to implement in high voltage conversion designs and was deemed non-essential based on the aim of the project. Scalability trades circuit complexity for an increased voltage conversion ratio and was considered an effective characteristic to achieve large output voltages.

Of the 6 proposed voltage multiplication techniques, coupled inductor designs confound the project aim, cascaded and Quadratic designs are limited to low ($<$ 1 kW) power applications. The 3 switched topologies were all capable of non-isolated operation, with switched inductor and switched capacitor designs providing the option of scalability to achieve large voltage conversion ratios. Furthermore, there were gaps in the literature

around bipolar switched capacitor and voltage lift switched inductor designs, allowing for novel applications of these voltage multiplication techniques in the development of an ultra high gain DC-DC converter.

CHAPTER 3

Design and Analysis of a High-Gain Bipolar DC-DC Converter

3.1 Introduction

This chapter presents a novel operation of a Cockcroft-Walton-based, non-isolated single-switch high-gain bipolar DC-DC converter. The design was realised by integrating the input and switch stage from a CBC with both an inverting and non-inverting Cockcroft-Walton voltage multiplier. The objective of the proposed topology was to produce a voltage gain of ± 10 to enable a direct comparison to that demonstrated by other topologies reported in the literature. The self-balancing characteristic of the chosen topology presented reduced voltage stress across the multiplier components and the switching device in comparison to cascaded and switch inductor-based topologies. The circuit consisted of a single SiC MOSFET, an inductor, 11 capacitors and 11 diodes. A fixed-width PWM signal to control the MOSFET was utilised to demonstrate open-loop functionality. To verify performance, an analysis of the converter's steady state operation was presented,

which was subsequently validated through both simulated and experimental data. A power efficiency analysis was lastly conducted to identify areas within the topology where optimisation may be used in the minimisation of power losses.

3.2 Converter Modes of Operation

To achieve a bipolar Cockcroft-Walton-based converter, 2 variations of the voltage multiplier are required. For non-inverting operation, a ladder consisting of $2N_C - 1$ diodes and capacitors was utilised, while for the inverting voltage multiplier, a ladder utilising $2N_C$ diodes and capacitors was selected. When describing the size of the voltage multipliers, N_C refers to the number of stages within the ladder. To maintain balance and simplicity N_C was treated as equal for both inverting and non-inverting topologies.

Figure 3.1 illustrates the proposed converter, which utilises a $2N_C - 1$ and inverting $2N_C$ topology, where $N_C = 3$ was selected, to achieve a high-gain bipolar output, and this configuration requires only a single active switch. The proposed design utilised 11 capacitors and diodes in addition to a single inductor and switch. This configuration produced a single input, multiple output design with a common ground.

During operation, the proposed converter switches between 2 states, based on the PWM input to the switching device. Mode 1 occurs when the PWM signal is high, the switching device conducts and shorts the inductor to ground. Mode 2 occurs when the PWM signal is low, the switch blocks and the input voltage and power supply are connected to the voltage multipliers. Steady-state is achieved when the capacitor ladders within the voltage multipliers achieve a net-zero change in charge during a complete switch cycle. The charging process creates a voltage rise across each capacitor, so that the potential difference across them is equal to the combination of the input voltage and voltage across the inductor. The capacitors are charged in stages, beginning with the lowest stage within

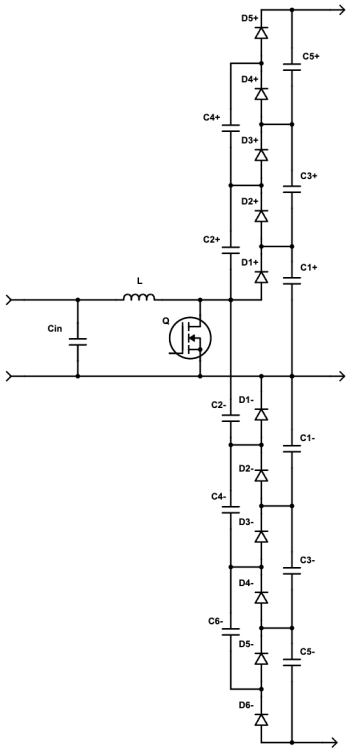

Figure 3.1: Circuit diragram of a modified CBC with a combined $2N_C - 1$ and inverting $2N_C$ topologies switched capacitor topology

the ladder. At this stage, charge is delivered to the capacitors in both ladders during Mode 2, which is then equalised within the stage during Mode 1. Once the voltage across the stage is equal to the combination of the input voltage and the voltage across the inductor, the next stage of the voltage multiplier ladder begins to charge.

Non-Inverting $2N_C - 1$ Ladder

The circuit diagram presented in Figure 3.2 demonstrates the current flow for the non-inverting, $2N_C - 1$, voltage multiplier topology. It may be observed that during Mode 2 operation, shown in Figure 3.2(b), the charge is delivered to the output capacitors (right side) via the equivalent output capacitor diodes. During Mode 1 operation, shown in Figure 3.2(a), the output capacitors equalise their charge with the smoothing (left side) capacitors via the equivalent smoothing capacitor diode. Once the voltage across a given

stage is equal to the input and inductor voltage, the output diode becomes reverse biased, allowing current to flow to the next stage of the voltage multiplier via the smoothing capacitors.

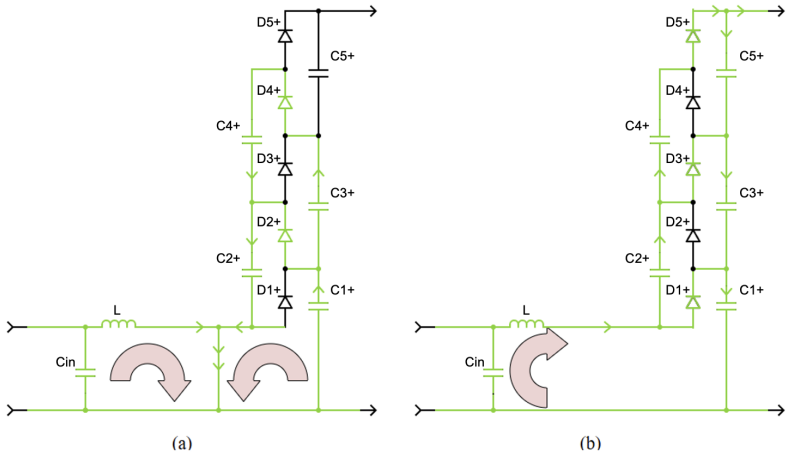

Figure 3.2: Equivalent non-inverting, $2N_C - 1$ Cockcroft-Walton circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

Inverting $2N_C$ Ladder

The circuit diagram presented in Figure 3.3 demonstrates the current flow for the inverting, $2N_C$, voltage multiplier topology. It may be observed that during Mode 2 operation, shown in Figure 3.3(b), the charge is delivered to the smoothing capacitors (left side) via the equivalent output capacitor diodes (right side). During Mode 1 operation, shown in Figure 3.3(a), the smoothing capacitors equalise their charge with the output capacitors via the equivalent smoothing capacitor diode. As with the non-inverting topology, once the voltage across a given stage is equal to the input and inductor voltage, the output diode is reverse-biased, allowing current to flow to the next stage of the voltage multiplier via the smoothing capacitors.

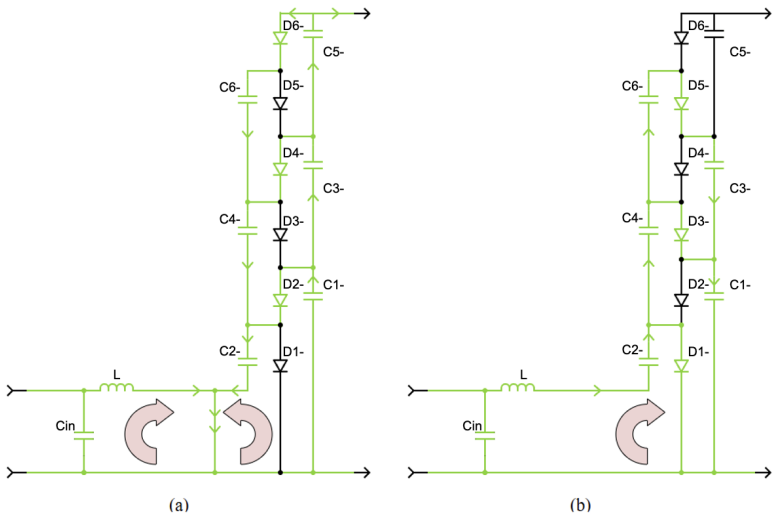

Figure 3.3: Equivalent inverting, $2N_C$, Cockcroft-Walton circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

Proposed Converter Operation

During operation, the $2N_C - 1$ and inverting $2N_C$ topologies build up charge in the capacitors independently during opposite modes. During Mode 1 operation, the inverting $2N_C$ topology discharges into the negative load while the non-inverting $2N_C - 1$ topology charges. Conversely, during Mode 1 operation, the inverting $2N_C$ topology charges and the non-inverting $2N_C - 1$ topology discharges into the positive load.

3.3 Proposed Converter Analysis

To establish principles of operation, a steady state analysis of the device was undertaken to identify the function of the converter and determine expected behaviours of the components within the converter.

3.3.1 Steady State Operation

Following a similar analysis used in [10], the ideal gain for the proposed converter design, assuming the inverting and non-inverting topologies are equal in magnitude, may be

expressed as:

$$\frac{V_{out\pm}}{V_{in}} = \pm\frac{N_C}{1-D} \tag{3.1}$$

where $V_{out\pm}$ is the non-inverting or inverting output voltage, V_{in} the input voltage, N_C the number of stages in the Cockroft-Walton multiplier, and D the duty ratio of the switching device.

Reductions in the output voltage arising from the voltage drops due to the output capacitor ladder and the equivalent series resistance of the inductor must be considered for practical applications [10, 80]. By initially assuming that the voltage losses associated with the forward voltage of the output diodes and the voltage drop due to the internal resistances of both the switching device and the inductor are insignificant in comparison to the magnitude of the output voltage. This can be supported with the knowledge that the diodes in the capacitor ladders are not constantly conducting and typically possess a forward voltage between 0.7 and 1.2 V. Additionally, appropriately selected inductors and switching MOSFETs possess an equivalent series resistance/on-state resistance less than 30 mΩ. With this, only voltage drops due to capacitive elements within the Cockcroft-Walton were initially considered in the analysis. Assuming all capacitors are identical, the general voltage drop equation presented in [80] may be used as a starting point to predict the non-inverting gain:

$$\frac{V_{out+}}{V_{in}} = \frac{N_C}{1-D} - \frac{I_{out+}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{3.2}$$

where V_{out+} is the non-inverting output voltage, I_{out+} the non-inverting output current, f the switching frequency and C the selected capacitor value used within the ladder.

For analytical purposes, the inverting $2N_C$ topology was considered identical to the $2N_C-1$ topology in terms of voltage gain and voltage drop. Therefore, the same analytical

method was utilised, resulting in the following expression for the inverting gain:

$$\frac{V_{out-}}{V_{in}} = -\frac{N_C}{1-D} + \frac{I_{out-}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{3.3}$$

where V_{out-} is the inverting output voltage and I_{out-} the inverting output current.

As the multiplier ladders operate independently and assuming equal output resistances for the inverting and non-inverting topologies, Equations 3.2 and 3.3 may be combined to express the proposed converter output gain considering capacitive voltage drops.

$$\frac{V_{out\pm}}{V_{in}} = \pm\frac{N_C}{1-D} \mp \frac{I_{out\pm}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{3.4}$$

Inductor Analysis

When both the inverting and non-inverting capacitor ladders operate at the same output voltage and load resistance, the utilisation of 2 voltage-multiplying topologies effectively doubles the inductor current, compared to the operation of the conventional single Cockcroft-Walton topology. With this and assuming ideal operation with no power losses, the average inductor current of the proposed topology may be given as:

$$< I_L >= \frac{2N_C^2 V_{in}}{(1-D)^2 R_{out}} \tag{3.5}$$

where $< I_L >$ is the average inductor current over a single switching period and R_{out} the load resistance of a single output capacitor ladder. From this, an ideal approximation of an average voltage across the input inductor, during steady state operation, may be represented as:

$$< V_L >= D(V_{in}) + (1-D)(V_{in} - V_{C1}) = 0 \tag{3.6}$$

where $< V_L >$ is the average inductor voltage over a single switching period, V_{C1} and the voltage across C_1. Although initially assumed to be insignificant, the equivalent series resistance, R_{esrL}, of the inductor can limit voltage gain at high duty ratios and should also be considered in the analysis. Equation 3.6 can be modified to include this non-ideal element, giving an average inductor voltage of:

$$< V_L >= D(V_{in} - < I_L > R_{esrL}) + (1 - D)(V_{in} - < I_L > R_{esrL} - V_{C1}) = 0 \tag{3.7}$$

Utilising a similar analysis and given that the voltage across C_1 is equal to the output maximum voltage observed from the inductive boost input stage, the input stage voltage gain may be deduced with consideration to R_{esrL} as:

$$\frac{V_{C1}}{V_{in}} = \frac{R_{out}(1 - D)}{R_{out}(1 - D)^2 + 2N_C^2 R_{esrL}} \tag{3.8}$$

This allows for the maximum input stage voltage to be determined based on the parasitic equivalent series resistance of the inductor.

Capacitor Analysis

For an ideal voltage multiplier, with no parasitic elements, operating at 100 % power efficiency, the expected voltage output at each stage may be determined by utilising a combination of Equation 3.1 and the voltage sharing characteristic of Cockcroft Walton multipliers, where $V_{C1} = V_{C2} = V_{C3}$, resulting in:

$$V_C = \pm \frac{V_{in}}{1 - D} \tag{3.9}$$

For practical applications, the impact of the capacitor voltage drop should be con-

sidered. At each intermediary output stage in the voltage multiplier, assuming equal capacitance, the voltage drop analysis, for a $2N_C$ Cockcroft-Walton ladder, based on [80], may be utilised for both inverting and non-inverting ladders. The voltage drops at each output stage of the voltage multiplier may be expressed using:

$$\Delta V_{Ck} = \mp \frac{I_{out}(N_C + k + 1)(N_C - k)}{2fC} \tag{3.10}$$

where k is the stage to be considered. With this, the voltage across the capacitor at any stage in the ladder may be calculated:

$$V_{Ck} = \pm \frac{V_{in}k}{1 - D} \mp \Delta V_{Ck+} \tag{3.11}$$

where V_{Ck} is the voltage across the output capacitor of the stage to be considered.

Diode Analysis

During the operation, Figures 3.2 and 3.3 outline the output diode switching operation for the non-inverting and inverting ladders, respectively. In Mode 1 operation, the odd-numbered diodes conduct, allowing a charge pathway for the smoothing capacitors in the non-inverting circuit and oscillating capacitors in the inverting topology. In Mode 2 operation, the even-numbered diodes conduct, creating charge pathways for the non-inverting oscillating capacitors and inverting smoothing capacitors. When blocking the maximum diode reverse-bias voltage, V_{Dk}, may be calculated as:

$$V_{Dk} = V_{Ck} \tag{3.12}$$

Assuming that the average capacitor current per switching cycle is zero and the equivalent series resistance of the capacitors are small enough to be insignificant, and thus it may be deduced that the average current flow through each diode can be expressed as:

$$< I_{D\pm} >= I_{out\pm} \tag{3.13}$$

Switch Analysis

As with the conventional boost converter, the maximum switch drain-source voltage, without considering transient voltage overshoots, may be expressed as:

$$V_{DSmax} = \frac{V_{in}}{1-D} = \frac{V_{out}}{N_C} \tag{3.14}$$

where V_{DS} is the maximum drain source voltage across the switch. The drain-source current can be calculated, using Kirchhoff's first law, with:

$$I_{DS} = I_L - I_{D1+} + I_{D1-} \tag{3.15}$$

where I_{DS} is the drain-source current, I_{D+} and I_{D-} the current in the positive and negative diodes, respectively.

3.4 Design Considerations

When considering the physical implementation of the proposed converter, practical factors should be considered, such as the impact of the input inductor on current ripple, the output voltage ripples, switch-based losses, and the determination of converter gain with consideration to component parameters.

3.4.1 Switching Device

An appropriate switching device may be determined by utilising Equations 3.14 and 3.15 to identify the maximum steady state voltage and currents. To obtain an optimal transistor, the switch conduction and switching losses must be considered. Conduction losses are defined as the power dissipated during the switch-on state due to the on-state resistance of the diode, and can be expressed as:

$$P_C = I_{DS}^2 R_{DSon} \tag{3.16}$$

where P_C is switch conduction loss and R_{DSon} the on state resistance of the switch. Switching loss outlines the power dissipated during turn-on and off transients as:

$$P_S = 0.5 I_{DS} V_{DS} f (t_{Rise} + t_{Fall}) \tag{3.17}$$

where P_S is the switching losses of the switching device, t_{Rise} the time for the switch to reach on state and t_{Fall} the time for the switch to reach off state.

MOSFETs were the primary choice for switching devices due to their higher switching frequency than IGBTs. With this, the trade-off between R_{DSon}, which dictates the maximum specification of the device as well as conduction losses as per Equation 3.16. And Q_C, which is proportional to t_{Rise} and t_{Fall} that impact switching losses as per Equation 3.17. Due to the need for a large current through the switching device, as the topology only utilised a single active switch, a bias was given to devices with low R_{DSon}, which in turn limited the maximum effective switching frequency of the device. During initial testing, it was found that for high voltage, low R_{DSon} silicon carbide MOSFETs, a switching frequency of 50 kHz was selected as a suitable operating point at which P_S did not

dominate converter losses.

3.4.2 Input Inductor

The inductance of the input inductor dictates both the current ripple and conduction mode of the topology. A low inductor current ripple is paramount in reducing the current stress observed by the switching device. Additionally, the mode of conduction operation influences the transients within the converter. The components within a device operating in discontinuous conduction mode (DCM) would experience higher voltage stresses than in continuous conduction mode (CCM); this would reduce both the power efficiency and lifespan of the device [81]. Conditions for operation modes of the proposed design may be determined via the identification of the boundary conduction mode, where the average inductor current $< I_L >$ is equal to half the inductor ripple current ΔI_L, which may be calculated using:

$$\Delta I_L = \frac{V_{in} D}{Lf} \tag{3.18}$$

Where L is the inductance of the input inductor. By combining Equations 3.5 and 3.18 an equation describing the conditions to achieve boundary conduction mode (BCM) operation may be realised:

$$\frac{R_{out}}{2Lf} = \frac{2N_C^2}{D(1-D)^2} \tag{3.19}$$

By making L the subject and plotting the equation against duty ratio, the minimum inductance to achieve CCM across the complete operating conditions of the proposed device may be determined.

The data in Figure 3.4 demonstrate how Equation 3.19 may be utilised to determine the inductance required to achieve CCM for the proposed converter across all duty ratios.

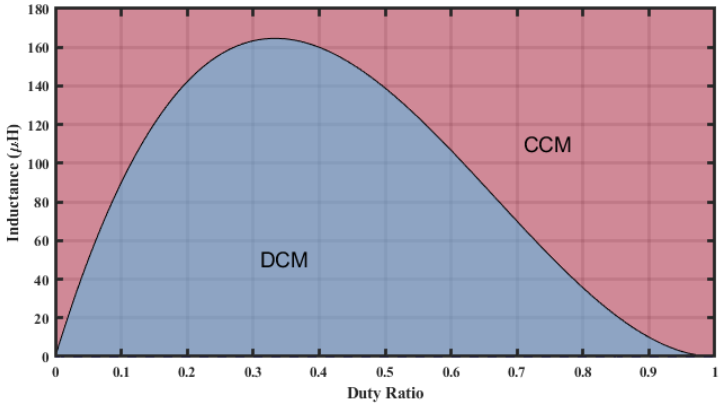

Figure 3.4: Conduction modes of proposed converter with a 50 kHz switching frequency and output load of 2 kΩ.

By selecting an inductance greater than the highest value presented in Figure 3.4, the converter will always operate within CCM at the specified frequency and load.

3.4.3 Output Capacitor Ladder

A key purpose of the output stage is to minimise voltage ripple. A common rule of thumb is for the ripple voltage of a DC source to be less than 5 %. However, the only standard found to cover ripple voltage was IEC 60050. This standard describes a voltage output as ripple-free, for low voltage equipment, when the voltage ripple is less than 10 % of the DC value [82]. In an attempt to maintain a stable voltage, the lower 5 % target was chosen as a target parameter when evaluating voltage ripple. An equation to determine the voltage ripple for Cockcroft-Walton multipliers can be defined as [74]:

$$\delta V = \frac{I_{out} N_c (N_c + 1)}{4fC} \tag{3.20}$$

where δV is the output ripple voltage. By making C the subject, a minimum capacitance required to achieve a 5 % voltage ripple may be determined with:

$$C = \frac{I_{out} N_c (N_c + 1)}{0.2 f V_{out}} \tag{3.21}$$

From this, suitable capacitors and switching frequency may be selected to maintain the specified voltage ripple.

3.4.4 Practical Estimated Gain and Maximum Duty Ratio

By utilising equations 3.4 and 3.8, a general equation for the voltage gain of the proposed topology may be realised as:

$$\frac{V_{out\pm}}{V_{in}} = \pm\frac{N_C R_{out\pm}(1-D)}{R_{out\pm}(1-D)^2 + N_C R_{esrL}} \mp \frac{I_{out\pm}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{3.22}$$

As I_{out} varies with the duty ratio, a secondary equation or duty ratio would be required to determine the practical gain. to eliminate this, Equation 3.1 may be modified to:

$$I_{out\pm} = \frac{N_C V_{in}}{(1-D)R_{out\pm}} \tag{3.23}$$

Which allows Equation 3.22 to be expressed as:

$$\frac{V_{out\pm}}{V_{in}} = \pm\frac{N_C R_{out\pm}(1-D)}{R_{out\pm}(1-D)^2 + N_C R_{esrL}} \mp \frac{N_C(4N_C^3 + 3N_C^2 - N_C)}{6fCR_{out\pm}(1-D)} \tag{3.24}$$

$-\infty$ Once the input voltage for the design is selected, the estimated voltage gain and maximum duty cycle, for a given capacitor and ladder size, may be determined using this equation. Figure 3.5 presents an example of how inductor equivalent series resistance may impact the voltage gain of the proposed topology.

It may be observed that the impact of increased inductor equivalent series resistance reduces the maximum voltage gain achievable for a given converter and reduces the greatest operable duty cycle before reductions in gain occur. It is rare to observe duty ratios above 80% within the literature due to high switch conduction losses associated with greater

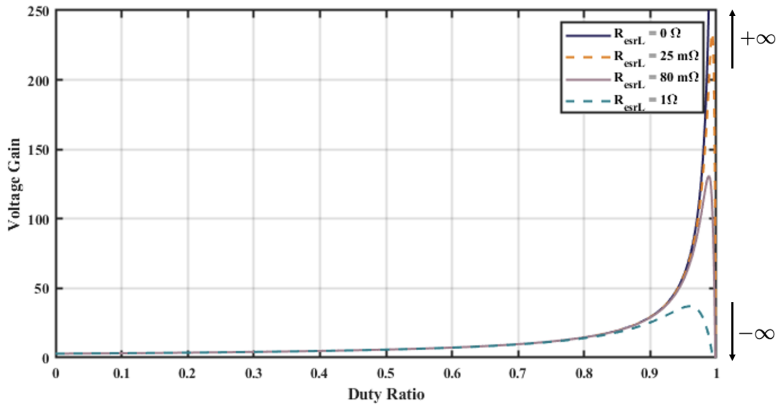

Figure 3.5: Voltage gain against duty cycle for a 3-stage multilevel boost converter with 10 μF capacitors and 50 kHz switching frequency.

currents within the transistor. Therefore, the key findings of this analysis show that if appropriate inductor, frequency and capacitor selections are made, the impact of inductor equivalent series resistance upon converter voltage gain will not be a detrimental factor for non-excessive (< 0.75) duty ratios. However, the equivalent series resistance of the inductor can negatively impact overall power efficiency via core and conduction losses, which is discussed in Section 3.6.1.

3.5 Simulation and Experimental Validation

A prototype of the proposed bipolar multilevel boost converter was developed (see Appendix A), experimentally characterised, compared against LTSpice-based simulations and the presented analytical equations to demonstrate the performance of the proposed topology. To demonstrate the high-gain potential of this converter, a target voltage gain of $\pm$ 10 was used as a benchmark during the experimental characterisation. The experimental parameters for the converter were outlined in Table 3.1.

To outline the switch mode of operation, at any point during simulated and experimental characterisation, the data in Figure 3.6 show the gate source voltage of the normally off MOSFET utilised in the proposed topology.

Table 3.1: Experimental parameters of the proposed multi level boost converter

Parameters	Value
V_{in}	100 V
$R_{out\pm}$	2 kΩ
L	500 μH
C	10 μF
f	50 kHz
D	0.71
R_{esrL}	25 mΩ
R_{esrC}	7 mΩ

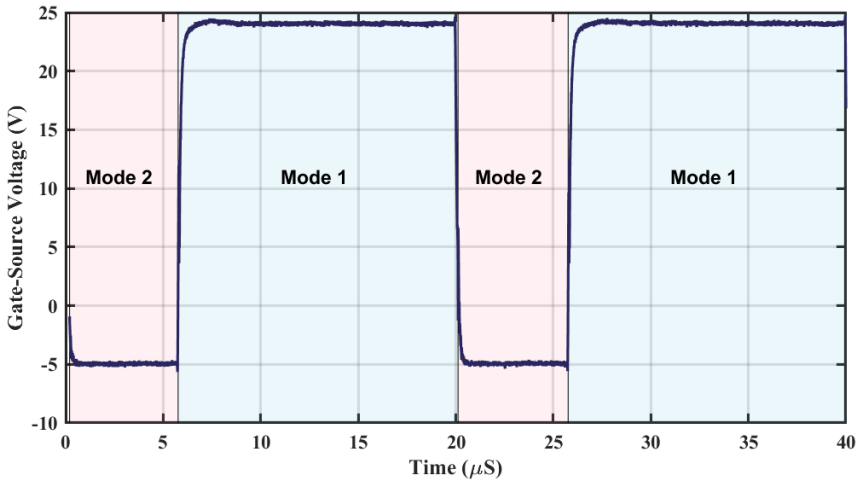

Figure 3.6: Experimental Gate-Source voltage waveform of the proposed bipolar converter.

3.5.1 Input Stage Operation

The data in Figure 3.7 show both the simulated and experimental input voltage and current waveforms. The average experimental values of 99.74 V and 10.85 A were complemented by simulated values of 100.0 V and 10.33 A. From this, the experimental input power was calculated to be 1082.2 W. It was also noted that an approximate 10 V input voltage transient was present during experimental characterisation. This was 8.5 V greater than the calculated ripple voltage of Equation 3.21. From this it was evident that the experimental voltage transients dominated the experimental and analytical voltage ripple. When observing the experimental transients in Figure 3.7, it was evident that the greatest change in voltage occurred during the transitions between operating modes. This behaviour was

expected to have originated from either the generation of low impedance loops, which is further discussed in Section 3.8.1 or due to the rapid change in input impedance when the device switched between operating modes. Additionally, as the input was connected directly to the inductor during simulation, the input current was characterised by the inductor current ripple waveform.

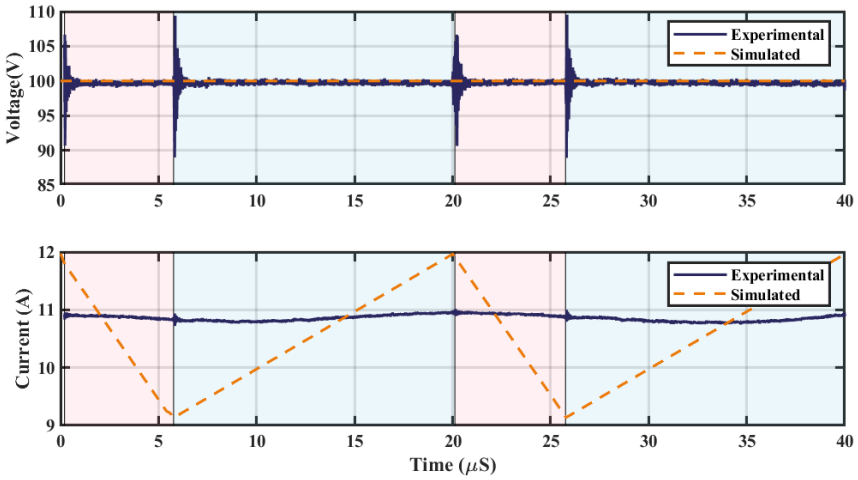

Figure 3.7: Input voltage and current waveforms of the proposed bipolar converter.

The experimental waveforms in Figure 3.8 show the converter operating in continuous conduction mode, as the input inductor current continuously exceeds 0 A. During Mode 1, the voltage across the inductor was 100 V and -251 V, and during Mode 2, with an average current of 10.85 A. This behaviour is consistent with both the simulated values of 100 V during Mode 1, -253 V during Mode 2 and an average current of 10.54 A. This was further validated with the steady-state analysis highlighted in Section 3.3.1, which predicted $< I_L >$ to be 10.67 A based on the experimental input voltage.

3.5.2 Output Stage Operation

The data in Figure 3.9 show the output waveforms of the non-inverting ladder with average experimental values of 1032 V and 520.0 mA. This was complemented by simulated values of 1022 V and 510.8 mA, which offered agreement to the analytical values of 1008 V and

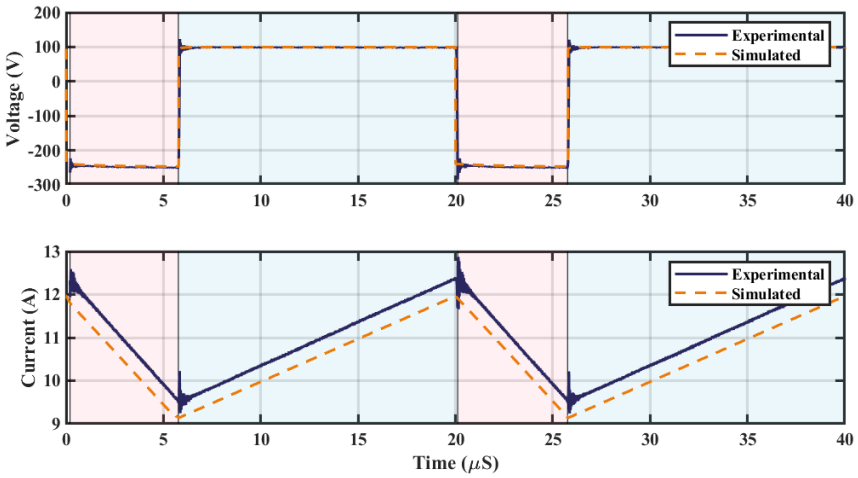

Figure 3.8: Input inductor voltage and current waveforms of the proposed bipolar converter.

516 mA, based on the analysis presented in Equations 3.23 and 3.24.

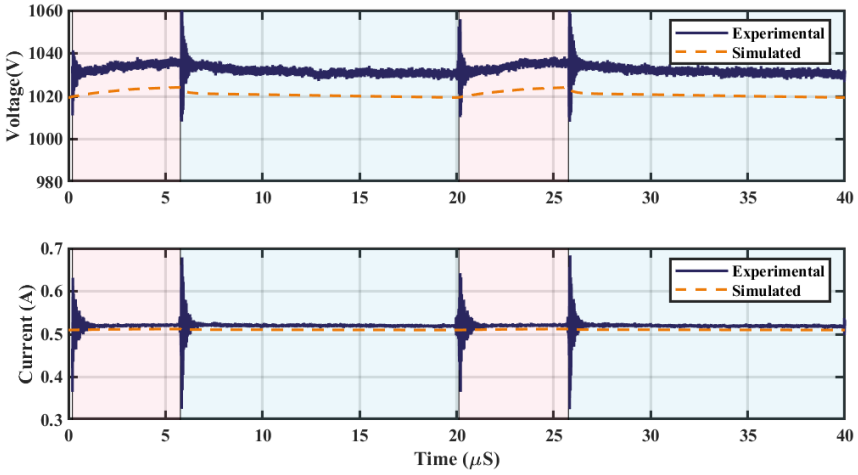

Figure 3.9: Non-inverting output ladder voltage and current waveforms of the proposed bipolar converter.

The data in Figure 3.10 show the output waveforms of the inverting ladder with average experimental values of -1020 V and -515.5 mA, which are complemented by simulated values of -1014 V and -506.8 mA, giving good agreement of -1008 V and -516 mA from the analysis presented in Equations 3.23 and 3.24. The effective experimental and simulated power output of the non-inverting ladder was 536.6 W and 522.0 W, respectively. The experimental and simulated output power for the non-inverting ladder was calculated as 525.8 W and 513.9 W, respectively. This resulted in the useful experimental output power

of the device to be 1062.4 W, which gave an experimental power efficiency of 98.2 %.

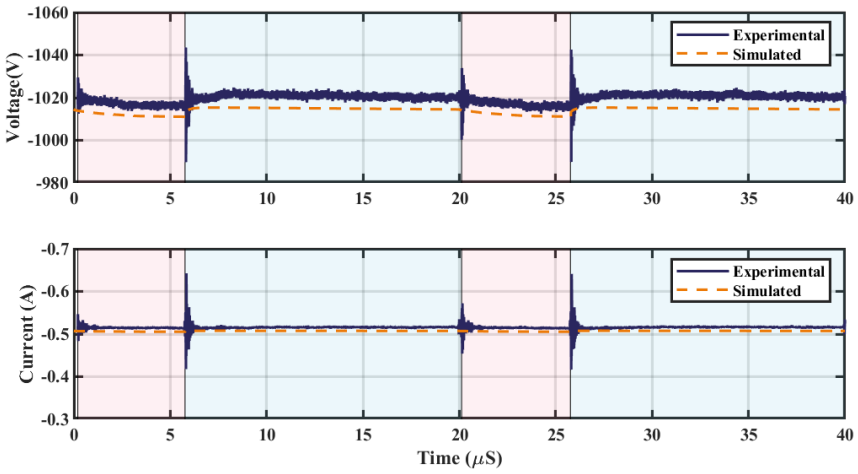

Figure 3.10: Inverting output ladder voltage and current waveforms of the proposed bipolar converter.

The average experimental voltages across C_{1+}, C_{3+} and C_{5+} were 349.7 V, 343.5 V and 343.0 V, respectively, showing voltage drops between the capacitors of 6.2 V from C_{1+} - C_{3+} and 0.5 V from C_{3+} - C_{5+} totalling 6.7 V. The experimental results deviated from the analytical voltage drop values of 4.7 V and 2.8 V, which totalled 7.5 V. While the magnitude was slightly reduced, the difference in the ratio of the voltage drop between C_{1+} - C_{3+} and C_{3+} - C_{5+} challenged the analytical method. This variation of the ratio was believed to be due to the assumption that the differences between the non-inverting $2N_C - 1$ and inverting $2N_C$ topologies were insignificant. This assumption allowed the use of the same analysis, based on an inverting $2N_C$ topology for both ladders. Since the non-inverting $2N_C - 1$ topology lacks the highest stage capacitor and diode compared to the inverting $2N_C$ topology, the components in the lower stages contribute more to the losses, which leads to an imbalance in voltage drops. As the difference in total magnitude between the analytical and total voltage drop is relatively low, the analysis utilised in Section 3.3.1 was determined to be suitable for total voltage drop in non-inverting $2N_C - 1$ topologies.

When observing the non-inverting voltage multiplier, the average experimental voltages

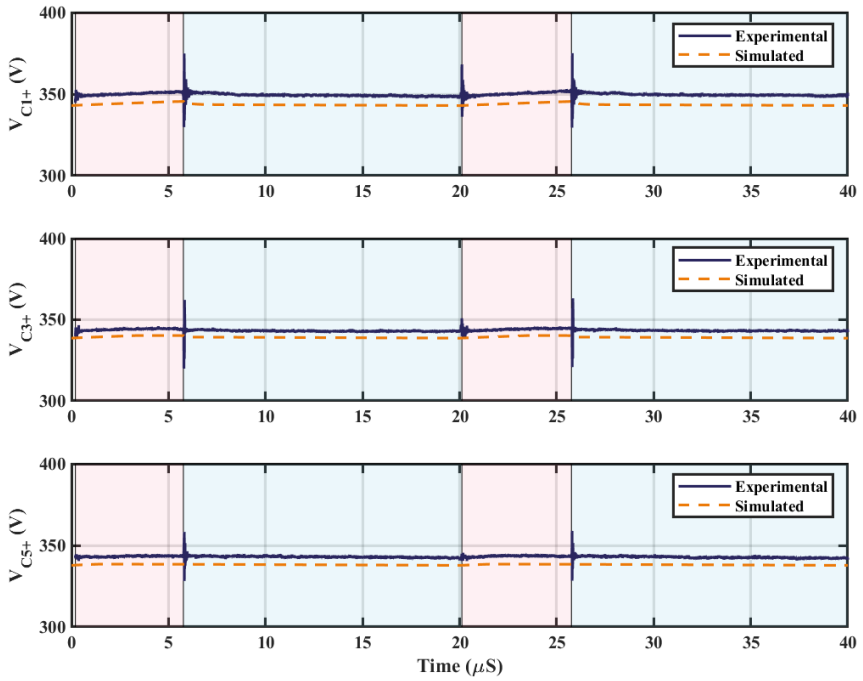

Figure 3.11: Voltage waveforms across each non-inverting output capacitor of the proposed bipolar converter.

across C1-, C3- and C5- were 346.0 V, 340.1 V and 338.8 V, respectively, with voltage drops between the capacitors of 5.9 V and 1.3 V, totalling 7.2 V. Again, these ratios of voltage values were inconsistent, albeit less than the 2N-1 topology, with the analytical voltage drop values of 4.7 V and 2.8 V, which totalled 7.5 V. The observed imbalance of voltages in the design of both topologies was also expected to be due to the analysis in Section 3.3.1 being derived from AC analysis. A significant variation in application between the analytical examples and proposed operation is the use of PWM. This operation scheme creates an instance of shorting during switch conduction, which leads to large cumulative current surges across all capacitors. This surge results in greater comparative losses for the lower-stage capacitors. This observation is further discussed in Section 3.8.1.

The data in Figures 3.11 and 3.12 presents the output capacitor voltages for both the inverting and non-inverting branches of the demonstrator unit. It can be seen that during Mode 1 operation, the positive output capacitors are charged. Conversely, during Mode 2 operation, the negative output capacitors are charged, which agrees with the

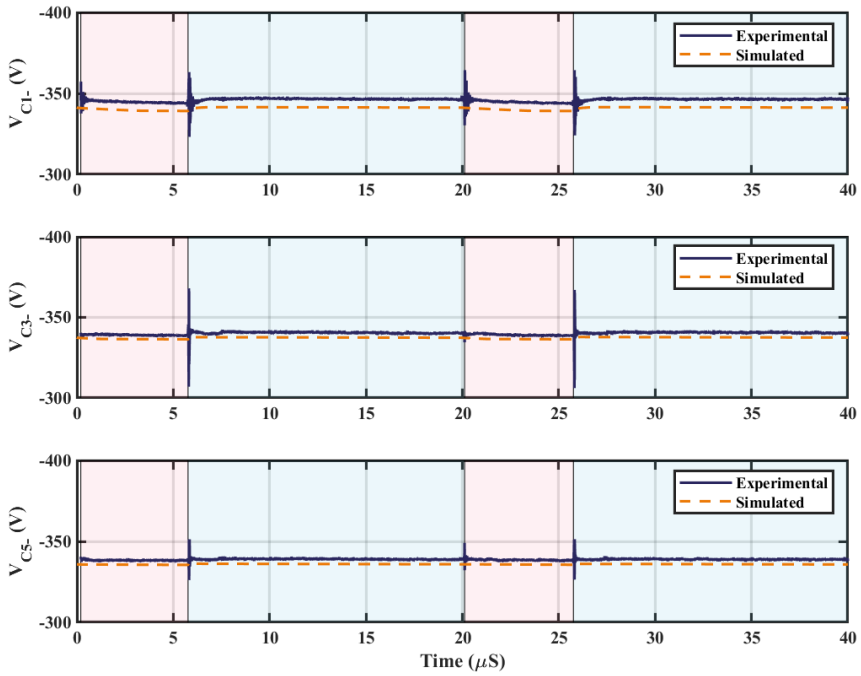

Figure 3.12: Voltage waveforms across each inverting output capacitor of the proposed bipolar converter.

operation description outlined in Section 3.2. The average observed voltage of V_{C1+} and V_{C1-} were 350 V and -346 V, respectively, highlighting a reduced voltage magnitude for the inverting topology due to the inclusion of the additional diode and capacitor. This was supported by the simulated voltage across the first stage capacitor of 344 V and -341 V, respectively. Additionally, as both experimental and simulated values were equal to the analytical value of 343 V within a 2 % margin of error, the difference between the inverting and non-inverting capacitors was deemed sufficiently small to justify utilising the analytical method outlined in [80] for both the inverting and non-inverting topologies.

Both the experimental and simulated data shown in Figure 3.13 supported the description of circuit operation outlined in Section 3.3.1 for the positive diodes, with D1+, D3+ and D5+ conducting during Mode 2, D2+ and D4+ conducting during Mode 1. Additionally, the maximum reverse bias for all diodes is equal to the average capacitor voltage for their given stage, demonstrating the voltage-sharing characteristic of the non-inverting switched capacitor topology.

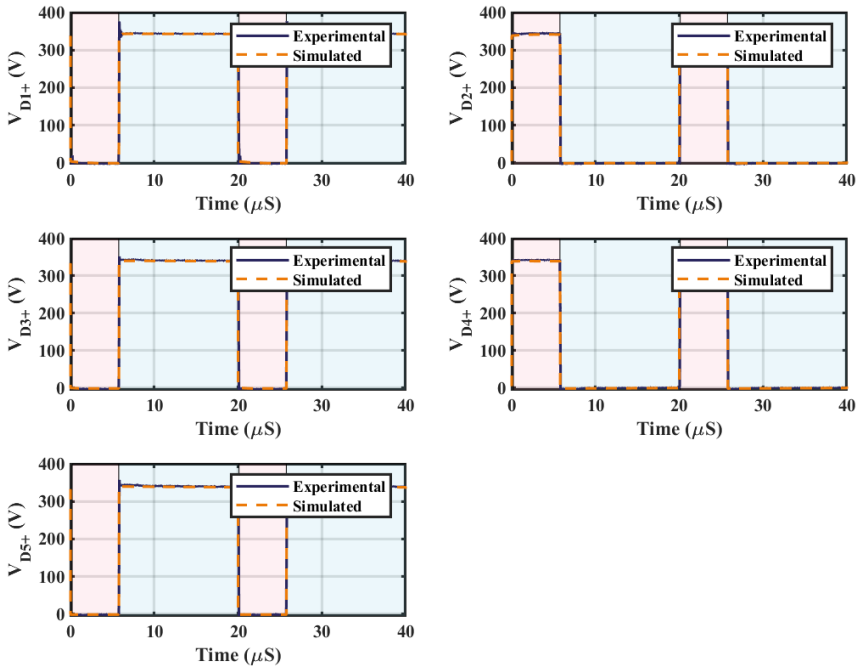

Figure 3.13: Non-inverting diode voltage waveforms of the proposed bipolar converter.

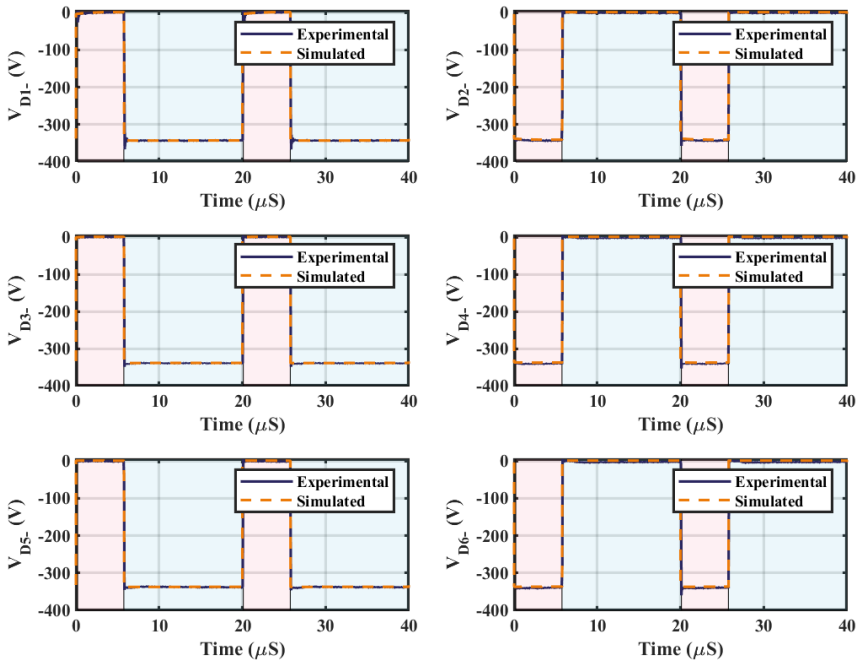

Figure 3.14: Inverting diode voltage waveforms of the proposed bipolar converter.

Similarly, the data in Figure 3.14 show that both simulated and experimental data support the analysis presented in Section 3.3.1, with D1-, D3- and D5- conducting during Mode 1, and D2-, D4- and D6- conducting during Mode 2 operation. Each diode also demonstrated voltage-sharing behaviour of the inverting switched capacitor topology of

$V_C = \frac{V_{out}}{N_C}$ with blocking voltages of ≈ 340 V.

The data in Figures 3.13 and 3.14 show the diode operating voltages for the non-inverting and inverting multipliers, respectively. Both sets of waveforms support the operation outlined in Section 3.3.1. V_{D+} exhibited 47 V overshoot during the switching transient, which reduced to 13 V in subsequent diode waveforms. A 30 V overshoot was also observed for V_{D-}, which reduced to 11 V in subsequent diode waveforms. These spikes were not observed in the simulated data, suggesting either ground bouncing or parasitic inductive elements within the switch or input stage of the topology may have caused the overshoots. The rapid decay in the overshoots was likely to be due to the smoothing capacitors absorbing the transient voltage spike before it was experienced by the subsequent diodes in the capacitor ladders.

3.5.3 Switching Operation

The data in Figure 3.15 show the voltage across the switching device. When blocking in Mode 2, the observed V_{DS} was 350 V, which was equal to V_{C1+} approximately $\frac{1}{N_C}$ of the average magnitude of the output voltages at 1026 V and in agreement with the simulated switch blocking value of 347 V. This demonstrates one of the key benefits of the Cockcroft-Walton voltage multiplier, which was the limiting of the voltage stress across the switching device. A lower blocking voltage switch may be used to generate an output voltage much greater than the rated voltage of the switch.

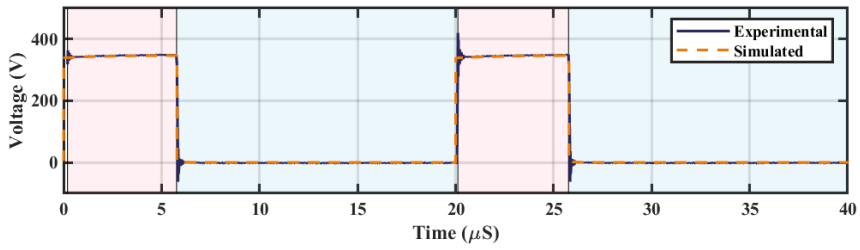

Figure 3.15: Switch Drain-Source voltage waveform of the proposed bipolar converter.

3.5.4 Efficiency at Different Power Operating Points

To demonstrate the converter efficiency operating within a range of operating powers, the load resistance for both inverting and non-inverting outputs was incrementally increased by 200 Ω, resulting in a change of input power from 1 kW to 520 W. For each incremental increase, the input and output voltage and current were measured to calculate the device efficiency with:

$$\eta = \frac{(V_{out+}I_{out+}) + (V_{out-}I_{out-})}{V_{in}I_{in}} \tag{3.25}$$

where η is the converter power efficiency.

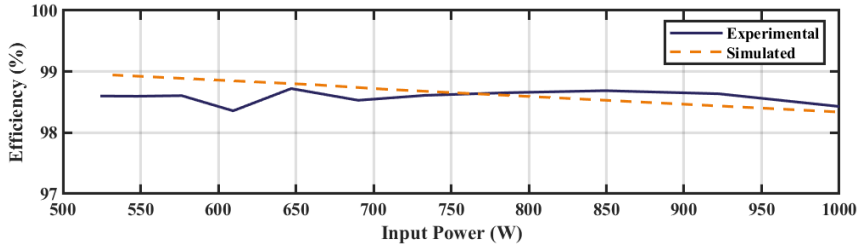

Figure 3.16: Power efficiency of the proposed 3-stage bipolar multilevel boost converter from 520 W to 1 kW

The data in Figure 3.16 show that below 900 W the experimental converter operated at approximately 98.6 % efficiency and decreased to 98.2 % efficiency between 900 W to 1 kW. A variation of ± 0.3 % was observed between 600 W to 650 W, which was determined to be likely due to experimental errors.

Consistent agreement between the simulated and experimental operation efficiencies was observed. While this agreement validates the simulated findings, the < 1 % error between the simulated and experimental results offers an argument for the use of simulation-based analysis for operational conditions beyond experimental boundaries. This allows for the initial validation of multi-kilowatt simulation models of the proposed topology with a high degree of confidence that any experimental design will operate in a manner consistent with the model.

3.6 Power Efficiency Analysis

Following the demonstration of open loop operation, a power analysis was conducted at the highest operating power of 1 kW to determine which topological factors had the greatest influence on power losses. The experimental power efficiency calculations in Section 3.5, were calculated using 3.25. With this, alongside experimental input and output powers calculated in Section 3.5, the power efficiency was calculated to be 98.2% with 19.8 W lost due to dissipation within the topology. To determine where the power losses were realised, a power analysis of each stage was undertaken.

3.6.1 Input Stage Power Losses

As the only component on the input stage is an inductor for this topology, the inductor is the only source of power loss for the input stage. Inductor power losses may be separated into core and DC conduction losses. By utilising the power loss analysis software provided by the inductor manufacturer [83] with the experimental findings, the core power loss was estimated at 1.1 W, and the DC conduction losses were calculated to be 3.0 W. To validate this approximation, the following equation was used:

$$P_{LDC} =< I_L^2 > R_{esrL} \tag{3.26}$$

where P_{LDC} is the DC condiction losses of the inductor, R_{Lesr} the equivalent series resistance of the inductor. The R_{esrL} of the utilised inductor was found to be 25 mΩ. With this and the average inductor current of 10.95 A, the input stage experimental inductor conduction losses were calculated as 3.0 W. This was in agreement with the manufacturer's analysis software [83]. From this, the total experimental power loss of the input stage was calculated as 4.1 W, which corresponds to 0.38 % of total input power.

3.6.2 Output Stage Power Losses

To determine power losses without measuring the current through each capacitor, it was assumed that the net change in charge of a capacitor during a complete switching cycle is 0 C during steady state. With this, the current can be estimated using basic capacitor charge equations to give:

$$I_C = CfV_{p-p} \tag{3.27}$$

where I_C is the magnitude of current through the capacitor ladders. By using Equation 3.20, I_C may be expressed as:

$$I_C = \frac{I_{out}N_C(N_C+1)}{2} \tag{3.28}$$

which may be implemented into a generic $P = I^2R$ conductive power loss equation to determine the capacitor power losses within the voltage multipliers:

$$P_{Cap+} = (2N_C - 1)\left(\frac{I_{out+}N_C(N_C+1)}{2}\right)^2 R_{esrC} \tag{3.29}$$

$$P_{Cap-} = 2N_C\left(\frac{I_{out+}N_C(N_C+1)}{2}\right)^2 R_{esrC} \tag{3.30}$$

where P_{Cap+} is the power dissipation of all capacitors within the non-inverting topology, P_{Cap-} the power dissipation of all capacitors within the inverting topology and R_{esrC} the equivalent series resistance of a capacitor. Using the values identified, the capacitive power dissipation was calculated to be 0.34 W and 0.39 W for the non-inverting and inverting ladder, respectively, totalling 0.73 W, which corresponded to 0.07 % of the total input

power. The power dissipation arising from the diodes was calculated using

$$P_{D+} = (2N_C - 1)V_f I_{out+} \tag{3.31}$$

$$P_{D-} = 2N_C V_f I_{out-} \tag{3.32}$$

where P_{D+} is the total diode dissipation in the non-inverting topology, P_{D-} the total diode dissipation in the inverting topology, and V_f is the forward voltage of the diodes. Due to the low current of the capacitor ladders, V_f was estimated to be 0.7 V, based on the device's datasheet [84]. With this, the power dissipation due to the output diodes was calculated to be 1.82 W and 2.14 W for the non-inverting and inverting ladder, respectively. Hence, the total power dissipation due to diodes present within the output stage was calculated to be 3.96 W, approximately 0.37 % of the total input power.

3.6.3 Switch Power Losses

Based on the analysis conducted in Section 3.4.1, the total switch power losses may be expressed as:

$$P_{Switch} = P_S + P_C \tag{3.33}$$

By utilising experimental results, alongside the switching device characteristic data, the experimental switch power dissipation was determined. Utilising Equation 3.16 with an experimental switch current of 9.6 A and on resistance of 30 mΩ, the conduction losses were 2.7 W. Equation 3.17 was used to determine switching losses; the rise and fall times were observed to be 0.47 ns and 0.64 ns, respectively, and the experimental switching loss of 9.06 W. With this, the total calculated experimental switch power dissipation was 11.77 W, which corresponds to 1.1 % of total input power.

3.6.4 Converter Efficiency

Based on input and useful output power, the total estimated power loss was 19.8 W. The individual sectional analysis was in agreement with this estimate, with a calculated total power dissipation of 20.56 W. The data in Figure 3.17 show the power dissipation ratio for each component group within the topology used in the experimental observations outlined in Section 3.5. From this, it can be observed that the greatest dissipation was caused by switching device losses, which may be optimised in future designs with either higher quality switches with lower on-state resistances or soft switching techniques. Due to the greatest diode dissipation losses being relatively fixed, as it is based on V_f, the proportion of its dissipation will reduce when larger voltage systems are introduced. To effectively minimise capacitor losses, devices with reduced equivalent series resistance should be carefully selected.

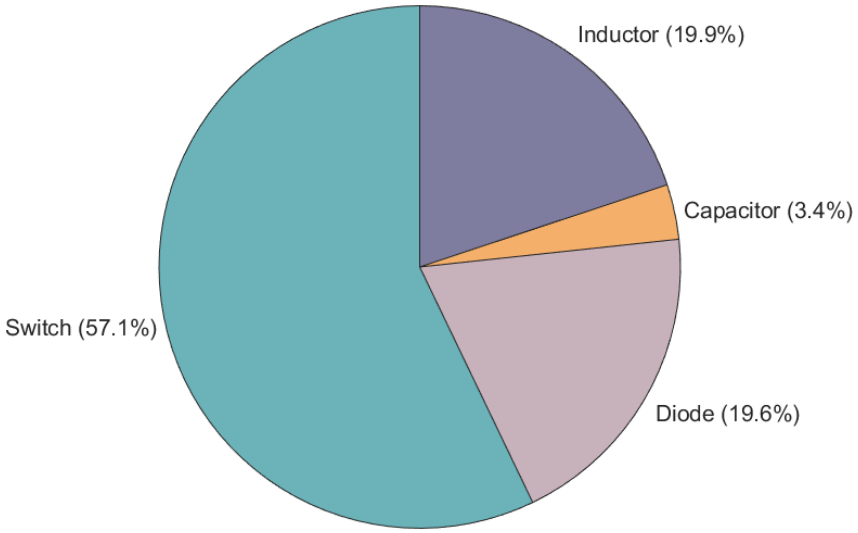

Figure 3.17: Distribution of 20 W power dissipation within experimental 1 kW bipolar multi-level boost converter.

3.7 Comparison to other converters

The data in Table 3.2 compares the operating characteristics of the proposed design against similar topologies reported within the literature.

The comparisons show that the proposed topology may produce voltage gains similar to those previously reported within the literature, focusing on achieving a high voltage gain [42, 43]. Additionally, the proposed topology produces a continuous bipolar output with greater efficiency than other reported designs [85, 86]. These advantages demonstrate a potential application of the proposed technology to operate a DC-link for unipolar LVDC to bipolar MVDC networks in addition to its original application operating as part of a converter to step up low-voltage generation sources to medium voltage transmission networks.

Table 3.2: Comparison of the proposed multi level boost converter with other topologies

Topology	Voltage Gain	Capacitor Voltage	Switch Voltage	Efficiency %	No. of elements: C	D	S	L
Bipolar Cuk-SEPIC Coupled-Inductor [85]	$\pm\frac{D}{1-D}$	V_{out}	$2V_{out}$	92	4	2	1	3
Bipolar SEPIC-Cuk [86]	$\pm\frac{D}{1-D}$	$V_{out}+V_{in}$	$V_{out}+V_{in}$	88	4	2	1	4
Interleaved Bipolar Boost-SEPIC [87]	$\pm\frac{1}{1-D}$	-	V_{out}	92	3	0	4	3
Hybrid Dickinson/ Cockcroft-Walton [41]	$\frac{N}{1-D}$	$\frac{V_{out}}{4}$	$\frac{Vin}{1-d}$	90.9	16	16	1	1
Cockcroft-Walton [42]	$\frac{2N_C+1}{1-d}$	$\frac{V_{out}}{N_C}$	$\frac{Vin}{1-d}$	96	4	4	2	2
Interleaved Dickinson [43]	$*$	$\frac{V_{out}}{2-2D}$	$\frac{V_{out}}{N_C}$	97.9	9	7	4	6
Proposed Design	$\pm\frac{N}{1-D}$	$\frac{V_{out}}{N_C}$	$\frac{V_{out}}{N_C}$	98	11	11	1	1

$$*\sqrt{\left(\frac{1}{D'}-\frac{D'Q}{4}\right)^2+\frac{5Q}{2}}+\left(\frac{1}{D'}-\frac{D'Q}{4}\right)$$

3.8 Chapter Summary of High-Gain Bipolar DC-DC Converter

3.8.1 Capacitor Size Converter Efficiency and Transient Spikes

A key inference from Equation 3.29 is that the power dissipation in the capacitors is independent of their capacitance. This would suggest that varying the size of the capacitors would have no impact on overall efficiency; however, subsequent experimental work discovered that reducing the capacitance within the ladder from 10 μF to 2.2 μF resulted in a reduced power efficiency of 92 % (See appendix B) in comparison to the 98.2 % efficiency presented in Section 3.5. An explanation for this was sourced from the impedance formula for capacitance. The formula shows an inverse relationship between capacitor reactance and switching frequency. This relationship may lead to an increased current at the start of the switching period, which is delivered to the switching device, resulting in high conduction losses. To demonstrate this, Figure 3.18 shows a comparison between the simulated drain-source current for the proposed topology with 10 μF and 2 μF capacitors.

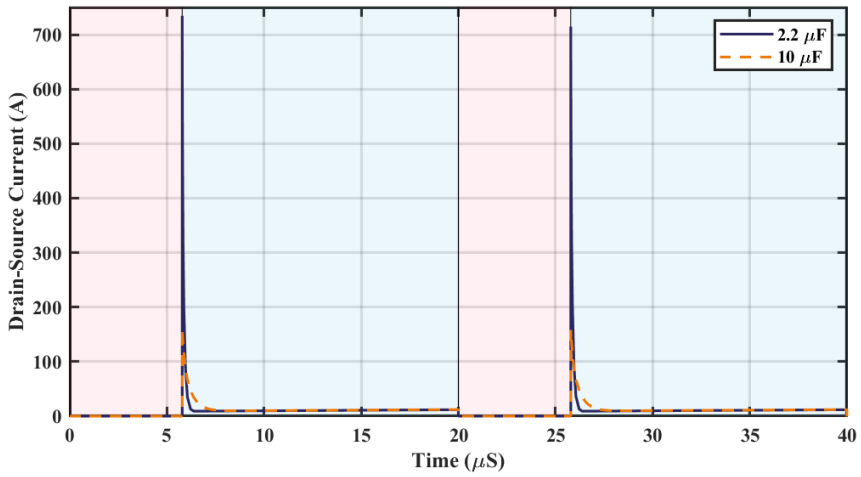

Figure 3.18: Simulated switch current for proposed design with 2.2 μF and 10 μF capacitors.

Additionally, current and voltage spikes were observed throughout the switch turn-on

and turn-off stages. These spikes are particularly evident in Figures 3.7 and 3.9, and were observed to be lower in the converter based on 2 μF components. With this observation, it was evident that the tuning of output stage capacitor values would be required to optimise power efficiency, as per Equations 3.29 and 3.30, and minimise the transient spikes observed in the laboratory demonstrator unit. This issue has not been highlighted in the literature, likely due to reported capacitor ladder designs which utilised a filter capacitor in parallel to the load. This aids in the reduction of transient mitigation with the trade off of increased voltage across the filter capacitor [41–43].

Figure 3.19 visualises how PWM input leads to a state immediately after the switch turn-on, where there are 2 stacks of capacitors, 1 partially discharged and the other fully charged. These 2 stacks are in a loop where the only opposing reactive and passive elements are parasitics from the capacitors and switching device.

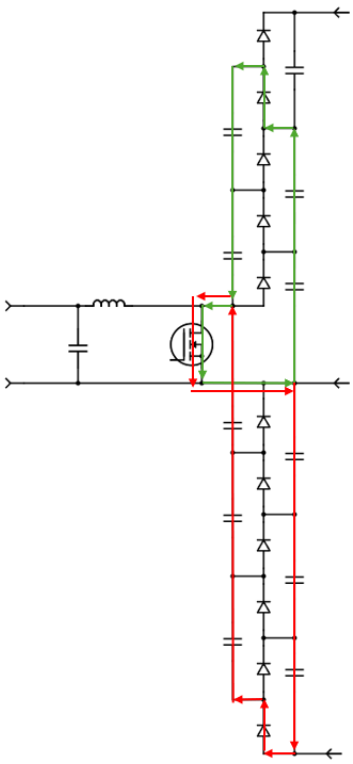

Figure 3.19: Circuit diagram of the proposed bipolar converter with highlighted capacitor ladder current pathways during mode 1 operation.

These shorts lead to periods of high $\frac{dI}{dt}$ and subsequently unanticipated power losses in addition to large voltage and current transients. To minimise the impact of these spikes, additional resistive or inductive elements may be introduced to limit the current at the potential trade off increased resistive conduction losses and thus reduce the efficiency of the device. An AC input would mitigate the issue by reducing $\frac{dV}{dt}$; however, this would require either additional switching devices, increasing switch-based power losses or a transformer, undermining the overall aim of the project to achieve high gain without the utilisation of a transformer. An alternative strategy to reduce $\frac{dI}{dt}$ during Mode 1 transition would be the implementation of small inductors that limit $\frac{dI}{dt}$ during initial transition between switch modes without impacting voltage gain.

3.8.2 Total Capacitive Voltage Against Output Voltage

Due to the self-balancing nature of the capacitive ladder, it is expected that for a 3-stage Cockcroft-Walton, the output voltage to be:

$$V_{out} = V_{C1} + V_{C2} + V_{C3} \tag{3.34}$$

This was corroborated by experimental data. A 4 V discrepancy between the combined capacitor voltages and output voltage was observed for both the inverting and non-inverting voltage multiplier. This discrepancy was determined to be a reading error, as the output voltages were taken with a single probe measuring 1012 V, whereas the capacitor voltages were taken with 3 probes measuring at a range of 360 V, allowing for more precise readings. An outline of the scale accuracy of the utilised voltage and current probes is outlined in Appendix A.

3.8.3 Conclusion

This chapter demonstrated the novel operation of a high-gain single-switch, bipolar-output, multi-level boost converter. An analysis of an inverting and non-inverting Cockcroft-Walton switched capacitor operating simultaneously in parallel was presented. A demonstrator unit of the design was developed and experimentally validated, both operationally and analytically. For 1 kW continuous operation, the demonstrator achieved a 98% experimental power efficiency. The converter topology was able to achieve a high bipolar voltage conversion ratio while only requiring a single active switching device, limiting potential failure points and allowing the opportunity to explore the use of simplistic control schemes.

For steady-state operation, the simulated and experimental results both support the analysis presented in Sections 3.3.1 and 3.4. The presented results demonstrated the proposed design to operate at comparatively high-efficiency while requiring components with voltage tolerances lower than the operational voltages for the converter.

When considering this design in relation to the project aim of designing a DC-DC converter capable of stepping up a range of low voltage DC inputs into a stable DC output capable of inversion to 3.3 kV_{AC}. This chapter explored a device with a voltage conversion ratio greater than what is often reported in the literature at a higher operating power and efficiency. This provided a foundation for further exploring techniques to increase the voltage conversion ratio. However, the voltage spikes discussed in Section 3.8.1 imposed concerns regarding reliable long-term operation. With this, further work that explores additional scalable voltage multiplication topologies was required to achieve the target voltage conversion ratios, and methods that minimise the transient voltage spikes were required to achieve the target converter.

CHAPTER 4

Design and Comparison of Ultra-High Gain DC-DC Boost Converter

4.1 Introduction

While the data reported in Chapter 3 demonstrated a successful prototype of a high-gain Bipolar DC-DC converter, the scalability of the topology is limited due to the increased voltage drop when more capacitor stages are introduced, as outlined by Equation 3.24. As a result, to achieve further enhancement in the voltage conversion ratio, other voltage multiplication topologies must be implemented. Switched inductor (SI) based topologies have been demonstrated to operate with Cockcroft-Walton-based designs to achieve voltage gains > 10 [11, 42]. The integration of an SI stage may occur at the input stage of a conventional boost converter to operate with an associated output stage voltage multiplier. An input stage SI voltage multiplier is capable of increasing the voltage observed by the output stage Cockcroft-Walton, which functionally multiplies the gain of the two topologies together, offering two scalable voltage multiplication sources. As the voltage

multiplication achieved by the input stage is observed at the switching stage, any voltage multiplication designs integrated at the input stage have the potential to realise high voltage stress, increased power losses of devices within the switch stage, and are limited by the capabilities of the switching devices. A promising variant of the SI design is the voltage lift switched inductor (VLSI), which is capable of achieving higher voltage multiplication in comparison to the SI in exchange for additional capacitive elements. As of writing, only 1 report has documented the use of a scalable VLSI topology [66]. The report presented a topology designed for high voltage gain with reduced voltage stress across the switching device by utilising a modified VLSI topology designed to operate after the switching device, with a non-scalable switched capacitor design. To demonstrate the ultra-high voltage multiplication potential of DC-DC boost converters, the main objective of this chapter was to analyse and demonstrate the scalability of a VLSI input stage compatible with the scalable, switched capacitor Cockcroft-Walton multiplier shown in Chapter 3. The aim of this was to achieve a converter capable of low to medium voltage conversion.

One of the key findings of the previous chapter was the presence of high current transients through the capacitor ladder during switch conduction (Mode 1) operation due to the formation of a low impedance loop within the Cockcroft-Walton. This high current contributes to increased conduction losses within the switching device and reduces the lifespan of both the switching device and the capacitors via thermal degradation. To overcome this, the inclusion of a current limiting inductor was proposed. This inductor operated in series with the first stage Cockcroft-Walton smoothing capacitor to limit the $\frac{dI}{dt}$ within all Cockcroft-Walton capacitors and the switching device. Previous literature has explored the utilisation of a series inductor under the lens of resonance and increased output voltage at the expense of efficiency [88, 89], and as a way to limit inrush current at the switching stage [11]. However, the reduction in switching transients within a boost

converter has not been explored. As a result, to evaluate this solution, four designs were proposed: two designs with no series inductor, which were used to demonstrate the combined voltage multiplication capabilities of VLSI and Cockcroft-Walton topologies, and two series inductor designs, each with a high and low capacitance variant. The objective of these designs was to explore the current reduction capabilities and evaluate the effectiveness of the series inductor for reducing current ripples across capacitor ladders with different capacitors.

The operational parameters and key features of the proposed design were presented through circuit analysis, which was then demonstrated via simulation and experimental characterisation. Each design was then compared to examine the impact of capacitance values upon the Cockcroft-Walton multiplier and the function of the series inductor design.

4.2 Proposed Topology Specifications

The 4 specifications of the proposed topology were based on a 3-level voltage lift switched inductor topology on the input stage, which utilised 3 inductors, 2 capacitors and 4 diodes. All switch stages consisted of a single MOSFET switching device. The output stage capacitor ladder consisted of a 7-stage non-inverting $2N_C - 1$ Cockcroft-Walton multiplier, which included 13 capacitors and 13 diodes. In total, all designs presented were comprised of at least 3 inductors, 15 capacitors, 17 diodes and 1 MOSFET.

The variations between the presented specifications were constrained to the output stage; the first design specification is an extension of the capacitor design principles adopted in Chapter 3, utilising comparatively higher value capacitors to reduce voltage drop and maximise voltage gain. The second design specification utilised the same capacitance capacitors with an inductor in series with the first stage smoothing capacitor to reduce the maximum transient current outlined in Section 3.8.1. The third specification

utilised the same-value capacitors as the first and second designs for the first smoothing capacitor and significantly smaller capacitors for all other elements within the ladder. The final specification utilised the same capacitor layout as the third specification, in addition to the series inductor, to assess the impact of the inductor on voltage drop. As all design specifications were classified as voltage lift switch inductor multi-level boost converters (VLSIMBC), to differentiate them, additional suffixes were given. The VLSIMBC high capacitor design was referred to as VLSIMBC-HC, the high capacitor series inductor was the VLSIMBC-HCL, the VLSIMBC low capacitor design was referred to as VLSIMBC-LC, and the low capacitor series inductor design was referred to as VLSIMBC-LCL. Figure 4.1 illustrates the circuit diagram for these proposed designs.

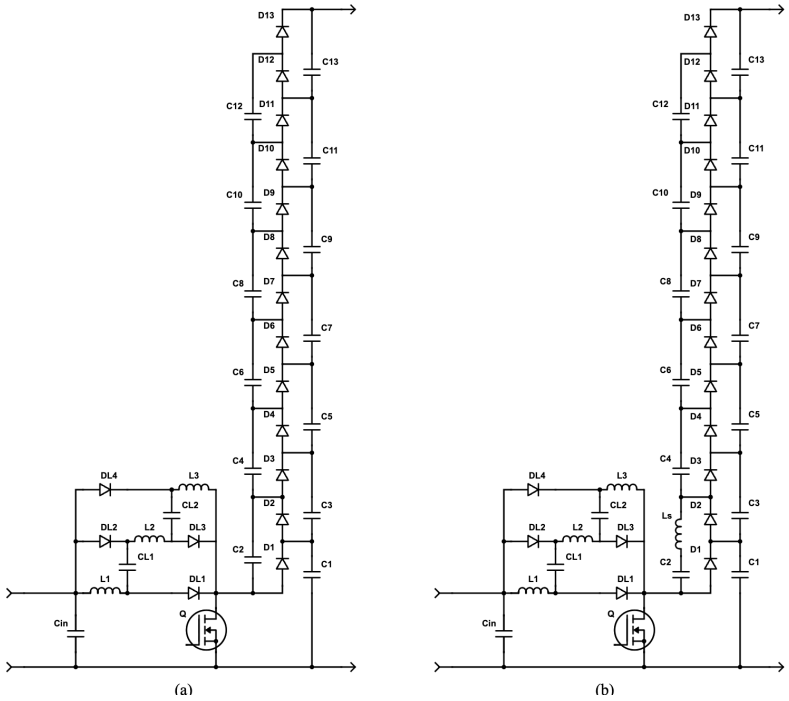

Figure 4.1: Circuit diagram of VLSIMBC designs, (a) The capacitor ladder presented in Chapter 3 and (b) The capacitor ladder with a series inductor.

As previously stated, the primary role of the series inductor was the mitigation of the impact of the current spikes caused by PWM operation with the Cockcroft-Walton topology [11]. The inspiration for exploring the use of a series inductor was based on the

simulated observation of current transients shown in Figure 4.2. This figure illustrates the difference in current transients in the first stage smoothing capacitor of the VLSIMBC-HC and VLSIMBC-HCL with a 5 nH inductor. This demonstrated that adding a 5 nH inductor

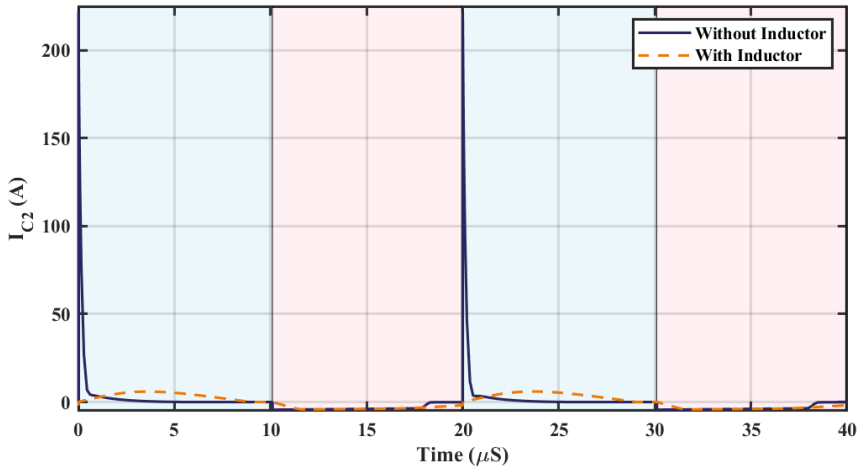

Figure 4.2: Simulated current through the first stage smoothing capacitor, C_2, for a VLSIMBC with and without a 5 μF series inductor.

in series with the first-stage smoothing capacitor caused an approximate 97.5 % reduction in the simulated current spike immediately after the transition from switch blocking (pink) to switch conduction (blue). The reduction in simulated current spike also resulted in a 0.8% increase in power efficiency due to reduced conduction losses in components present within the output and switch stages. These initial simulations provided an argument for the exploration of an inductor in series with the first stage smoothing capacitor as a potential option for converter optimisation.

To mitigate performance losses associated with the lower capacitance designs, such as voltage drop outlined in Equation 3.10 and reduced efficiency described in Section 3.8.1, a mixed capacitor design was utilised for the VLSIMBC-LC and VLSIMBC-LCL designs. By utilising a single high-value capacitor within the first stage smoothing capacitor of the Cockcroft Walton multiplier, both the voltage drop and ripple may be reduced in comparison to homogenous low capacitance designs [74].

4.2.1 Steady State Operation

Figure 4.3 outlines the labelled circuit diagram of the proposed VLSIMBC topology utilised for steady-state circuit analysis. By utilising an expanded analysis of Section 3.3.1, the ideal voltage conversion ratio of the proposed designs may be given as:

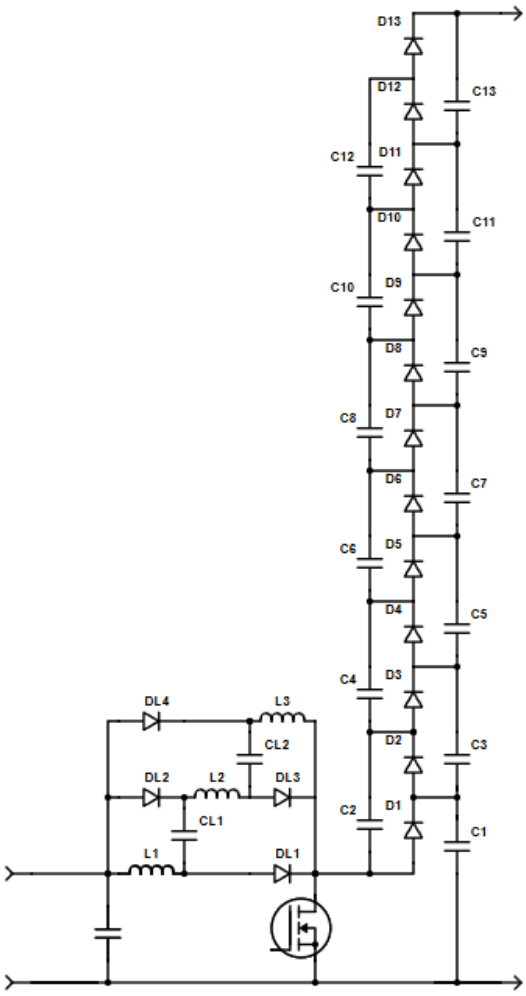

Figure 4.3: Circuit diagram of the proposed VLSIMBC topology.

$$\frac{V_{out}}{V_{in}} = \frac{N_L N_C}{1 - D} \tag{4.1}$$

where V_{out} is the output voltage, V_{in} the input voltage, N_C the number of stages within the switched-capacitor ladder, N_L the number of stages within the voltage lift switched inductor stage and D the duty ratio. By utilising the voltage drop analysis presented

in [80] and utilised in Chapter 3, a voltage gain that considers the impact of the voltage drop from the capacitor ladder may be realised:

$$\frac{V_{out}}{V_{in}} = \frac{N_L N_C}{1-D} - \frac{I_{out}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{4.2}$$

where f is the switching frequency, I_{out} the output current and C the selected capacitor value used within the ladder. Additional reductions in output voltage are caused by the parasitics present in the switched-inductor voltage lift stage.

Input Inductor Analysis

Based on Equation 4.1 describing the ideal gain, for a generic VLSIMBC topology and assuming 100 % power efficiency, the average input current, $< I_{in} >$, may be given as:

$$< I_{in} >= \frac{N_L N_C V_{out}}{(1-D)R_{out}} \tag{4.3}$$

where R_{out} is the load resistance. This equation may be used to describe the average current through each inductor in the input stage. When given equal inductances, it may be assumed that $< I_{in} >= N_L < I_L >$ and that $V_{out} = N_C V_{c1}$. The average current through an inductor may be given as:

$$< I_L >= \frac{N_C^2 V_{C1}}{(1-D)R_{out}} \tag{4.4}$$

where $< I_L >$ is the average current through a single inductor. When considering inductor-based losses, the voltage across any inductor in an N_L stage VLSI topology during Mode

1 operation, V_{Lm1}, may be given as:

$$V_{Lm1} = D\frac{(V_{in} - (N_L - 1)V_{CL}) - N_L < I_L > R_{esrL}}{N_L} \tag{4.5}$$

Where R_{esrL} is the equivalent series resistance of the inductor and V_{CL} the voltage across the assumed identical capacitors within the VLSI. Assuming the input stage capacitors are sufficiently large so that over a complete switching period in steady state $V_{CL} = V_{in}$, and thus Equation 4.5 may be simplified to:

$$V_{Lm1} = (V_{in} - I_L R_{esrL}) \tag{4.6}$$

By making the same assumptions used in the analysis of Mode 1, the voltage across an inductor during Mode 2 is:

$$V_{Lm2} = \left(V_{in} - I_L R_{esrL} - \frac{V_{C1}}{N_L}\right) \tag{4.7}$$

with the total average voltage across a single inductor during a switching period, $< V_{Lx} >$, expressed as:

$$< V_{Lx} >= (V_{in} - I_L R_{esrL})D + \left(V_{in} - I_L R_{esrL} - \frac{V_{C1}}{N_L}\right)(1 - D) \tag{4.8}$$

and by extension, the voltage across the entire input stage can be expressed as:

$$< V_L >= (V_{in} - I_L R_{esrL})\, D + (V_{in} - I_L R_{esrL} - V_{C1})(1 - D) \tag{4.9}$$

Equation 4.8 also allows for the voltage gain of the input stage, considering the equiv-

alent series resistance of the individual inductors, to be realised:

$$\frac{V_{C1}}{V_{in}} = \frac{N_L(1-D)R_{out}}{(1-D)^2R_{out} + R_{esrL}N_LN_C^2} \tag{4.10}$$

Similar to the voltage losses identified in Equation 3.8, the reduction in voltage gain due to the equivalent series resistance of the inductor has a quadratic relationship with the number of capacitor stages, in addition to a proportional increase between the number of inductor stages.

Capacitor Analysis

Utilising the same analysis proposed in Section 3.3.1, the voltage drop at any intermediary capacitor stage may be given by Equation 3.10. By utilising Equations 4.10 and 3.10, the voltage across the capacitor at any intermediary stage in the ladder may be calculated:

$$V_{Ck} = \frac{V_{in}kN_L(1-D)R_{out}}{(1-D)^2R_{out} + R_{esrL}N_LN_C^2} - \frac{I_{out}(N_C+k+1)(N_C-k)}{2fC} \tag{4.11}$$

where V_{Ck} is the voltage of a given capacitor stage referenced to ground and k the stage to be observed.

Diode Analysis

The diodes operating within the output stage Cockcroft-Walton may be described in the same manner as outlined in Section 3.3.1. With reference to Figure 4.3, during operation, the odd-numbered diodes conduct during Mode 1. During Mode 2, the even-numbered diodes conduct. Following these charge patterns the maximum diode reverse voltages, V_{Dk} , may be determined using:

$$V_{Dk} = V_{Ck} = \frac{V_{out}}{N_C} \tag{4.12}$$

Assuming that the average capacitor current per switching cycle is zero and the capacitors have negligible equivalent series resistance. It may be deduced that the average current flow through each diode can be expressed as:

$$< I_D >= I_{out} \tag{4.13}$$

When considering the operating characteristics of the input VLSI diodes, the blocking voltage across the first-stage VLSI diode, V_{DL1}, may be expressed as:

$$V_{DL1} = V_{C1} - V_{L1} - V_{in} \tag{4.14}$$

Likewise, blocking voltage across the highest stage voltage lift diode, V_{DL4}, may be expressed as:

$$V_{DL4} = V_{C1} - V_{L3} - V_{in} \tag{4.15}$$

By assuming inductors L_1 and L_3 are equal, V_{DL1} and V_{DL4} may be represented with:

$$V_{DL1} = V_{DL4} = V_{C1} - V_{Lm2} - V_{in} \tag{4.16}$$

This may be simplified to:

$$V_{DL1} = V_{DL4} = \frac{V_{in}(N_L - 1)}{(1 - D)} \tag{4.17}$$

By utilising the same analysis, the blocking voltage of the intermediate voltage lift diodes may be calculated with:

$$V_{DL2} = V_{DL3} = \frac{V_{in}(N_L - 1)}{2(1 - D)} \tag{4.18}$$

From this analysis, it can be concluded that intermediate stage input diodes were required to block half the voltage, compared to the first and final stage diodes. This offers the potential to use lower voltage, lower power dissipation diodes within the intermediate stages. However, for simplicity, all VLSI diodes should be based on the requirements of the first and last stage diodes.

When considering the current through the VLSI diodes, during Mode 1 operation, the diodes must conduct sufficient current to maintain the average inductor voltage across the complete switching period and block during Mode 2 operation. With this, the average current of a voltage lift stage diode, $< I_{DL} >$, may be expressed as:

$$< I_{DL} >= \frac{< I_{in} >}{N_L} \tag{4.19}$$

Therefore, it may be deduced that during steady state operation, to maintain a net-zero change in charge over a complete switching period, the average current during Mode 1 operation, $< I_{DLm1} >$ may be determined with:

$$< I_{DLm1} >= \frac{< I_{in} >}{DN_L} \tag{4.20}$$

This allows for the identification of the maximum current flow through the input diodes during steady-state operation.

Switch Analysis

When considering the integration of the input VLSI stage, the maximum drain-source voltage of the switch, without considering transient voltage overshoots of all the proposed designs, was calculated as:

$$V_{DSm2} = \frac{V_{in}N_L}{1-D} = \frac{V_{out}}{N_C} \tag{4.21}$$

where V_{DSm2} is the voltage across the switching device during Mode 2 operation. The drain-source current during switch conduction may be calculated as:

$$I_{DSm2} = I_L - I_{out} \tag{4.22}$$

where I_{DSm2} is the drain-source current during Mode 2 operation. When comparing Equation 4.21 with the equivalent switch voltage analysis in Section 3.3.1, it is apparent that, under the same operating conditions, the switch utilised within the VLSIMBC designs experiences a greater drain source voltage by a factor of N_L; therefore, devices capable of greater blocking voltages would be required.

Series Inductor Analysis

The main function of the series inductor was to limit current surges during Mode 1 operation, originating from the shorting of the capacitor ladder to the ground. This initial current surge, I_{Cinit}, may be described using:

$$I_{C,init} = \frac{2\delta V}{Z_{Mode1,init}} \tag{4.23}$$

where $Z_{Mode1,init}$ is the circuit impedance of the capacitor ladder during Mode 1 operation and δV the ripple voltage. When ignoring parasitic inductances, the impedance of the capacitor ladder, without a series inductor, immediately following the transition from Mode 2 to Mode 1 operation may be assumed as 0 Ω. From this, a current loop is created between the switch and the output stage. This loop is wholly resistive and dependent on the equivalent series resistance of the output stage capacitors and the on-state resistance

of the switching device. This results in an initial impedance which was calculated using:

$$Z_{Mode1,init} = 2(N_C - 1)R_{esrC} + R_{DSon} + R_{Don} \tag{4.24}$$

where R_{esrC} is the equivalent series resistance of an individual capacitor, R_{DSon} the on-state resistance of the switching device and R_{Don} the on-state resistance of the diode. By introducing an inductor in series with the first stage smoothing capacitor, the impedance at t = 0 is theoretically infinite, resulting in $I_{C,init} = 0$ A. Following this, the change in capacitor current is limited by:

$$di_C = \frac{dt\delta V}{2L_S} \tag{4.25}$$

where L_S is the inductance of the series inductor. With this, the transient current flowing through the capacitors during the short caused by Mode 1 operation is limited. This leads to a reduction in transient conduction losses within the Cockcroft-Walton ladder and switching device.

4.3 Design Considerations

The proposed topology presented utilises a similar circuit design to the bipolar multilevel boost converter discussed in Chapter 3, which allowed for similar equations to identify Boundary conduction mode (BCM), the capacitive voltage drops and estimated voltage gain of the VLSIMBC topology. Moreover, the addition of the voltage lift stage poses new considerations for the operation of the topological design. The increased circuit complexity leads to new considerations, such as the impact of imbalances between the input VLSI inductors. To minimise losses in voltage gain and reductions in efficiency observed in low capacitance Cockcroft-Walton, the possibility of non-homogeneous capacitor selections, such as those highlighted in [74], was also considered.

4.3.1 Input Inductor

With the utilisation of multiple input inductors, further analysis was required to determine the criteria for changes in conduction operation mode. Additionally, the impact of manufacturing tolerances of the inductors within the VLSI topology also required consideration.

BCM Operation

The conditions for the conduction modes of the proposed design may be determined by the identification of the operating conditions that give rise to BCM. Assuming all inductors in the input stage are equal, BCM occurs when the average inductor current $< I_L >$ is equal to half the inductor ripple current, ΔI_L, and may be calculated using:

$$\Delta I_L = \frac{V_{in} D}{Lf} \tag{4.26}$$

Combining Equations 4.4 and 4.26 the operating conditions required to achieve BCM operation may be determined:

$$\frac{R}{Lf} = \frac{2N_L N_C^2}{D(1-D)^2} \tag{4.27}$$

Hence, the minimum inductance to achieve CCM across the complete operating conditions of the proposed converter topology may be determined. The data in Figure 4.4 demonstrates how Equation 4.27 may be utilised to determine the minimum inductance required to achieve CCM for the proposed converter for all duty ratios. By selecting an inductance greater than the highest value presented in Figure 4.4, the converter will always operate within CCM at the specified frequency and load.

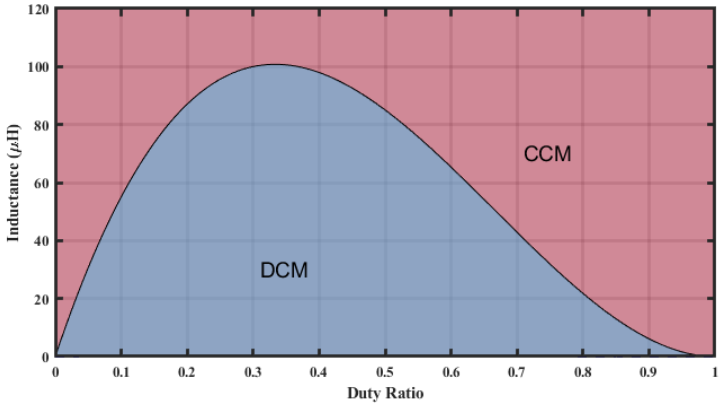

Figure 4.4: Operating modes of the proposed VLSIMBC converter with a 50 kHz switching frequency and output load of 15 kΩ.

Inductor Imbalance

With multiple inductors utilised in the input stage of the VLSI topology, differing values will have an adverse effect upon device operation. For a 3-stage voltage-lift switched inductor, let

$$L_1 = N_{I2}L_2 = N_{I3}L_3 \tag{4.28}$$

where L_1, L_2 and L_3 are the inductances of the inductors within the input VLSI stage and N_{I2} and N_{I3} are the imbalance ratio, where $N_{I3} > N_{I2}$. The data in Figure 4.5 outlines the inductor current and voltage behaviour resulting from the imbalance.

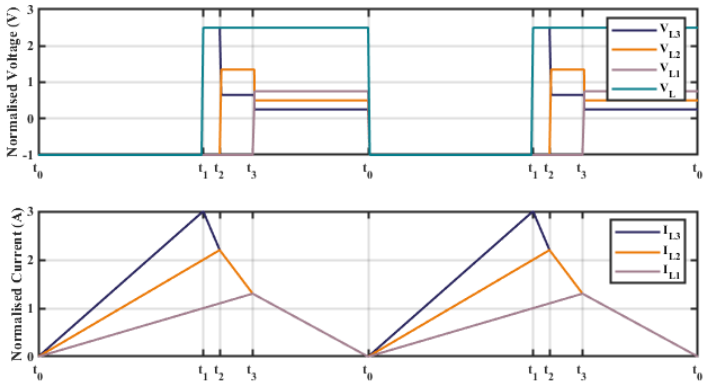

Figure 4.5: Current and voltage waveforms of inductors with imbalance ratios of $N_{I2} = 2$ and $N_{I3} = 3$.

During Mode 1 from $(t_0 > t > t_1)$,

$$V_{L1} = V_{L2} = V_{L3} = -V_{in} \tag{4.29}$$

therefore,

$$N_{I3}\frac{di_{L1}}{dt} = \frac{N_{I3}}{N_{I2}}\frac{di_{L2}}{dt} = \frac{di_{L3}}{dt} \tag{4.30}$$

During Mode 2 from $(t_1 > t > t_2)$, L_3 will discharge to match the current of L_2. The voltages across the charging inductors may be given as:

$$V_{L1} = V_{L2} = -V_{in} \tag{4.31}$$

As L_3 is the only discharging inductor to satisfy Equation 4.1

$$V_{L3} = (V_{DS} - V_{in}) \tag{4.32}$$

for a duration of

$$dt_{L3} = \frac{L_3 di_{L3}}{V_{L3}} \tag{4.33}$$

From $t_2 > t > t_3$, $I_{L2} = I_{L3}$, L_2 and L_3 discharge. The voltages across L_1 remains equal to $-V_{in}$, the voltages across L_2 and L_3 are calculated as:

$$V_{L2} = \frac{V_{DS} - V_{in} - V_{CL2}}{N_{I2}} = \frac{V_{DS} - 2V_{in}}{N_{I2}} \tag{4.34}$$

$$V_{L3} = \frac{V_{DS} - V_{in} - V_{CL2}}{N_{I3}} = \frac{V_{DS} - 2V_{in}}{N_{I3}} \tag{4.35}$$

for a duration of

$$dt_{L2} = \frac{L_2 di_{L2}}{V_{L2}} \tag{4.36}$$

From $t_3 > t > t_0$,

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{di_{L3}}{dt} \tag{4.37}$$

With this, the imbalance in voltages across the inductors may be expressed as:

$$V_{L1} = N_{I2}V_{L2} = V_{L3}N_{I3} \tag{4.38}$$

By considering the voltage lift capacitors, the inductor voltages may be determined with respect to the peak switch voltage, with,

$$V_{L1} + N_{I2}V_{L2} + V_{L3}N_{I3} = V_{DS} - 2V_{in} \tag{4.39}$$

From this, it can be observed that imbalanced inductor sizes lead to variations in current ripples between the input VLSI inductors. Additionally, increased voltages across the smaller inductance inductors stress was proportional to the VLSI output voltage, reducing device reliability and increased conduction losses.

4.3.2 Output Capacitor Ladder

As there have been no changes to the Cockcroft-Walton design proposed in Chapter 3, Equation 3.20 may be utilised to describe the ripple voltage, δV, for the VLSIMBC-HC designs. This may also be used to describe δV for the VLSIMBC-HCL design, as the function of the inductor was to facilitate pseudo AC operation within the Cockcroft-Walton. This creates an operation closer to that utilised in the derivation of Equation 3.20 [74].

Due to the mix of capacitors in the VLSIMBC-LC and VLSIMBC-LCL designs, an analysis without the assumption of all capacitors being equal was required. The funda-

mental ripple voltage equation for a 7-stage Cockcroft-Walton multiplier may be expressed as [74]:

$$\delta V = \frac{1}{f}\left(\frac{1}{C_{13}} + \frac{2}{C_{11}} + \frac{3}{C_9} + \frac{4}{C_7} + \frac{5}{C_5} + \frac{6}{C_3} + \frac{7}{C_1}\right) \tag{4.40}$$

From Equation 4.40 it may be observed that the lower stages contribute more to δV, with C_1 a 7 times greater contribution to the ripple voltage, compared to C_{13}. It is evident that the first stage has the greatest influence on ripple voltage on capacitors within a Cockcroft-Walton. Hence, an increase in the first-stage capacitors would lead to the greatest ripple reduction when changing a single component. Additionally, as the first stage smoothing capacitor, C_2, is the first capacitor connected to the switch in the zero impedance loop, formed following the transition from Mode 2 to Mode 1 operation, there was an argument, highlighted in Section 3.8.1, to increase its size in an attempt to reduce the transient voltage spikes. Based on Equation 4.40, this change should not have an impact on ripple voltage. Previous works have recommended doubling the 1st stage capacitor to reduce ripple. For example, one of the key arguments for simply doubling the capacitance is simplicity in component usage [74]. As two different capacitors were already in use to compare low and high capacitance designs, there was an opportunity to explore the impacts of a greater ratio of first-stage capacitance to later stages. Hence, an increase in C_2 by a factor of 11 would transform the capacitive voltage drop function in Equation 3.2 into

$$\Delta V_{out} = \frac{I_{out}}{f}\left(\frac{197}{C_{3-11}} + \frac{55}{C_2}\right) \tag{4.41}$$

which would result in an approximate 25 % reduction in voltage drop in comparison to a homogenous capacitor design.

4.3.3 Practical Estimated Gain and Maximum Duty Ratio

Due to the difference in capacitances between the topological variants, as well as the inclusion of the series inductors, additional analysis was required to describe the voltage gain equations for the different designs.

VLSIMBC-HC Design

By following the same analysis outlined in Section 3.4.4, Equations 4.2 and 4.10 may be combined to achieve a general equation for the voltage gain of the VLSIMBC:

$$\frac{V_{out}}{V_{in}} = \frac{N_L N_C (1-D) R_{out}}{(1-D)^2 R_{out} + R_{esrL} N_L N_C^2} - \frac{I_{out}(4N_C^3 + 3N_C^2 - N_C)}{6fCV_{in}} \tag{4.42}$$

To remove the dependence on I_{out}, and eliminate the variation with duty ratio, it may be substituted with:

$$I_{out} = \frac{N_L N_C V_{in}}{(1-D) R_{out}} \tag{4.43}$$

which can be used to provide a suitable estimate without the need to measure I_{out} at each duty ratio when testing. This allows Equation 4.42 to be expressed as:

$$\frac{V_{out}}{V_{in}} = N_L N_C \left(\frac{(1-D) R_{out}}{(1-D)^2 R_{out} + R_{esrL} N_L N_C^2} - \frac{(4N_C^3 + 3N_C^2 - N_C)}{(1-D) R_{out} 6fC} \right) \tag{4.44}$$

Once the input voltage for the design is selected, the estimated voltage gain and maximum duty cycle for a given capacitor and ladder size may be determined. The data in Figure 4.6 offers an example of the impact of inductor equivalent series resistance for the proposed topology.

Similar to the analysis presented in Section 3.4.4, it may be observed from the data in

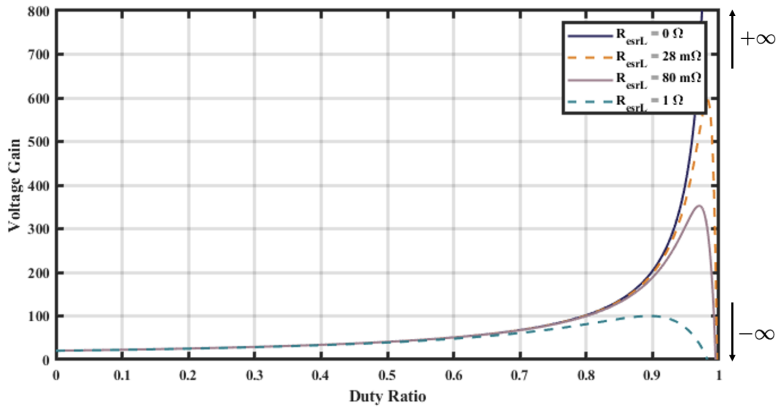

Figure 4.6: Gain against high duty cycle for a 3 inductor stage, 7 capacitor stage, voltage lift multilevel boost converter with 11 μF capacitors and 50 kHz switching frequency.

Figure 4.6 that an increase in inductor equivalent series resistance reduces the maximum voltage gain achievable for a given converter and reduces the greatest operable duty cycle before reductions in gain occur.

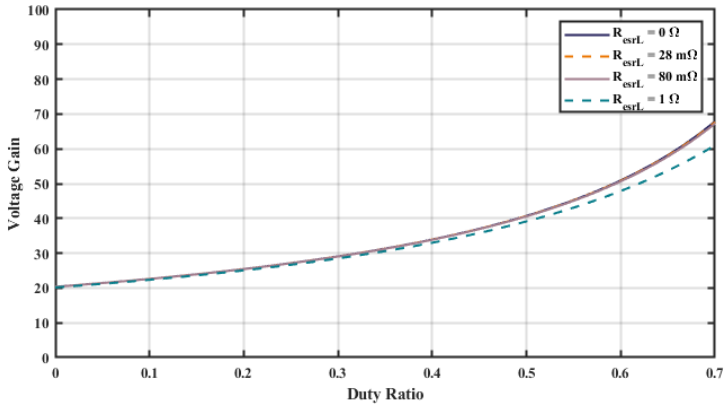

Figure 4.7: Gain against duty cycle from 0 to 0.7 for a 3 inductor stage, 7 capacitor stage, voltage lift multilevel boost converter with 11 μF capacitors and 50 kHz switching frequency.

The data in 4.7 also show that the impact of inductor equivalent series resistance upon converter voltage gain was insubstantial, with observable deviations from the excessively high equivalent series resistance of 1 Ω occuring 45 % duty ratio. However, it should be noted that increased equivalent series resistance would lead to losses from increased conduction losses. When compared to similar conditions to the bipolar multi-level boost

converter proposed in Section 3.4.4, it was apparent that due to the increased number of inductors present in the VLSI design, the equivalent series resistance of the inductor had a greater impact on voltage gain. For the proposed VLSIMBC converter, deviations in gain began to be observed between $D = 0.4 - 0.5$ compared to $D > 0.75$ for the topology proposed in Chapter 3. With this, it was highlighted that appropriate inductor selection based on the equivalent series resistance of the component was required to achieve optimal power efficiency for high-duty cycle operation.

VLSIMBC-LC Design

By utilising Equations 4.10 and 4.41, an equation which may describe the voltage drop across the capacitor ladder of the VLSIMBC-LC may be realised with:

$$\frac{V_{out}}{V_{in}} = \frac{N_L(1-D)R_{out}}{(1-D)^2R_{out} + R_{esrL}N_LN_C^2} - \frac{I_{out}}{f}\left(\frac{197}{C_{3-11}} + \frac{55}{C_2}\right) \tag{4.45}$$

VLSIMBC-LCL/HCL Designs

The introduction of the series inductor leads to 2 key gain considerations: the limitation of change of current described in Equation 4.25, and the change in topology impedance. An implicit assumption of all voltage gain equations of the Cockcroft-Walton multiplier is that $\frac{dI_C}{dt}$ is large enough to ensure the capacitors within the topology are sufficiently charged to achieve voltage multiplication. To reduce the complexity of analysis. It was assumed that the series inductance is of a value which allows this assumption to be true; hence, for series inductors with inductances are small enough such that $\frac{dI_C}{dt}$ is sufficiently large, and Equations 4.44 and 4.45 may be used to calculate the output voltages of the VLSIMBC-HCL and VLSIMBC-LCL designs, respectively.

4.4 Simulated and Experimental Validation

To demonstrate the potential of the proposed VLSIMBC designs, the VLSIMBC-HL design was experimentally characterised at $\tilde{1}$ kW operating power, and compared against LTSpice-based simulations and the presented analysis. The operating parameters for the converter were outlined in Table 4.1. The 1 kW operation was selected in part to allow for comparison with the topology presented in Chapter 3, and also due to experimental design limitations. As a consequence, a 15 kΩ load was required, which resulted in I_{out} operating at 200-300 mA. This was identified as an experimental limitation, as the impact of the capacitive-based voltage loss outlined in Equation 4.44 could not be fully explored. However, the experimental results were used to validate equivalent simulated designs; agreement of results at low operating powers could justify the use of simulated characterisations for designs beyond the remit of experimental prototyping.

Table 4.1: Experimental parameters of the proposed VLSIMBC high capacitance designs

Parameters	Value
V_{in}	100 V
R_{out}	15 kΩ
L	1 mH
C	11 μF
f	50 kHz
D	0.50
R_{esrL}	28 mΩ
R_{esrC}	7.2 mΩ

To outline the mode of switching of operation, the data in Figure 4.8 show the gate source voltage of the normally off MOSFET utilised in the proposed topology.

4.4.1 Input Stage Operation

The data in Figure 4.9 show both the experimental and simulated input voltage and current waveforms. The average experimental input voltage and current values of 99.56 V and

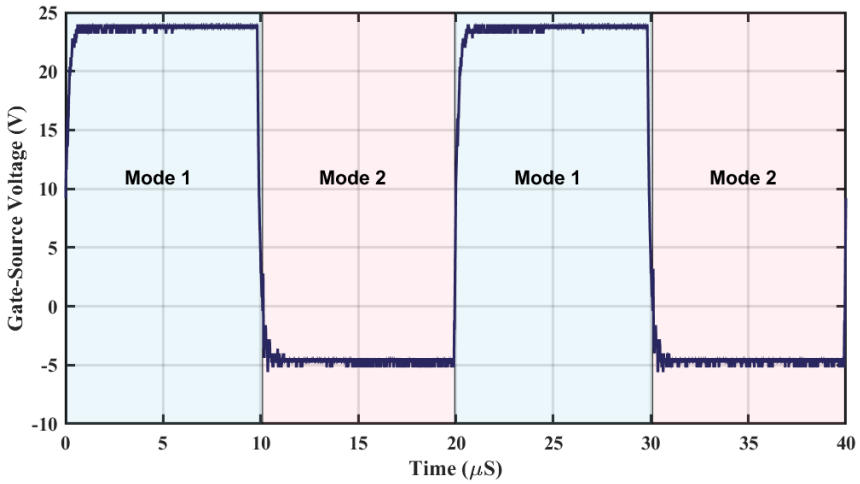

Figure 4.8: Experimental Gate-Source voltage waveform of the proposed VLSIMBC.

11.88 A were complemented by simulated values of 100.0 V and 11.61 A. From this, the experimental input power was calculated to be 1183 W. It was noted that an approximate 20 % input voltage ripple was observed during experimental characterisation, which was not present in the simulated results. Unlike the input ripple observed in the bipolar converter shown in Section 3.5.1, the transient voltage which occurred when transitioning from Mode 1 into Mode 2 was over double that observed during the transition from Mode 2 to Mode 1. This behaviour did not coincide with the generation of the zero impedance loops outlined in Section 3.8.1. A more likely explanation would be the rapid change in impedance when the device changed from the short condition of Mode 1 to the switch capacitor charging state of Mode 2. This state change would lead to a rapid change in current demand, which in turn would require a rapid response from the power supply to accommodate. Limitations in the ability of the power supply would lead to large variations in voltage delivery and potentially explain the large ripple observed in Figure 4.9. This limitation is further discussed in Section 4.6.1.

Large current transients were observed at the simulated input. This was expected to be due to the simulation prioritising the dissipation of the capacitors in the input stage during Mode 2 operation, which created the 6.7 A difference between the experimental

and simulated input current during Mode 2. This, in turn, would require the simulated input supply to compensate for the discharged capacitors during Mode 1 operation. As the average simulated and experimental values were in agreement, this suspected artefact of the simulation was determined to be non-confounding.

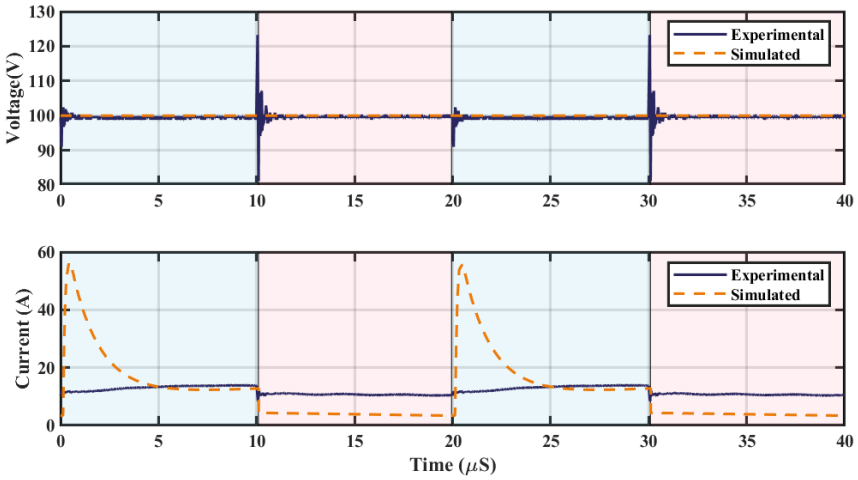

Figure 4.9: Experimental and simulated input voltage and current waveforms of the VLSIMBC-HC design.

To demonstrate the input stage operation, the data in Figure 4.10 show the total experimental voltage across the input stage and each input inductor. When ignoring initial transients, the peak and minimum input stage voltage V_L were observed to be 495 V and -105 V, respectively, which supports the operation of the VLSI stage described by Equation 4.9. The individual inductors were observed to oscillate around 100 V during Mode 2 and maintain -100 V during Mode 1 operation, which supported the operation of a single inductor outlined in Equation 4.8.

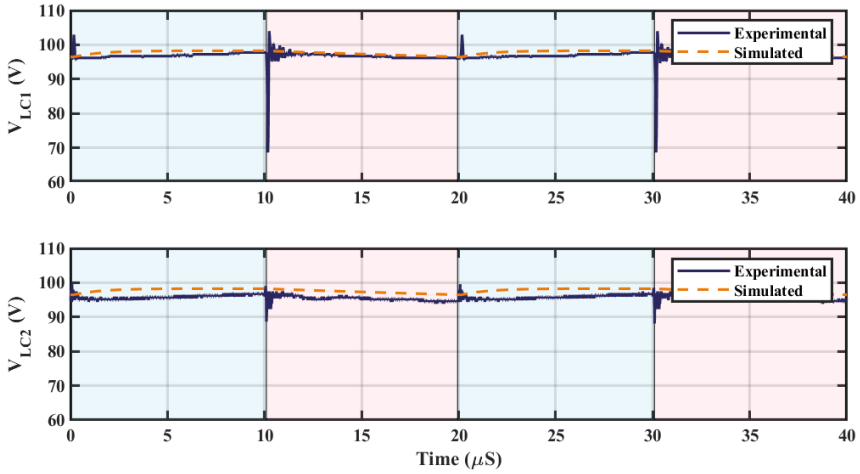

Figure 4.11: Experimental and simulated voltage waveforms of voltage lift capacitors of the VLSIMBC-HC design.

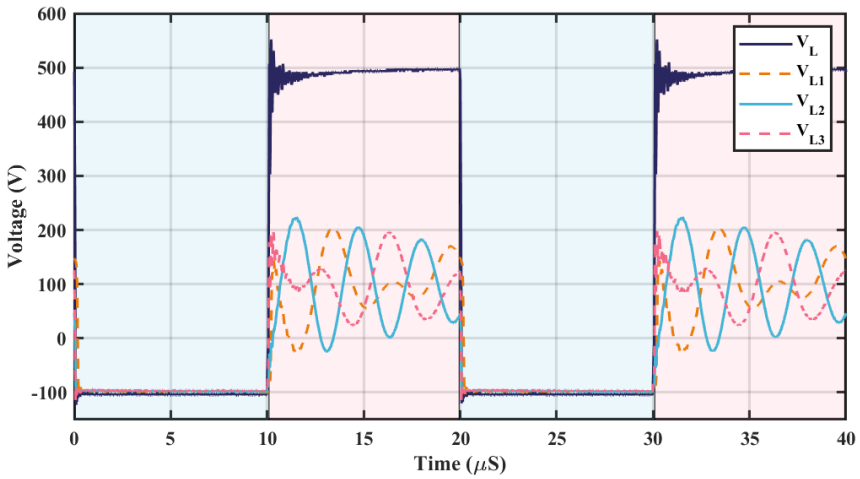

Figure 4.10: Experimental voltage waveforms across input inductors and converter input stage for the VLSIMBC-HC design.

The combined voltage across the three inductors was observed to be -102 V during Mode 1, where the inductors charged in parallel and 300 V during Mode 2, where the inductors discharged in series. Additionally, the data in Figure 4.11 show the voltage across V_{LC1} and V_{LC2} to be 97 V and 96 V, respectively. The combined voltage across the VLSI inductors and capacitors was found to be 491 V. This was in agreement, within a 1 % error, with the Mode 2 description Equation 4.9, which calculated a voltage across the input stage of -99.4V during Mode 1 and 495 V during Mode 2, respectively.

To demonstrate consistency between simulation and experimental findings, the data in

Figures 4.12 and 4.13 compared the voltages across the input VLSI stage and individual inductors, respectively. Except for the switching transients previously highlighted in Section 3.8.1, the data in Figure 4.12 show agreement between experimental and simulated data for the voltage across the input stage, as well as the previously highlighted calculated values of -99.4 V during Mode 1 operation and 495 V during Mode 2 operation, respectively.

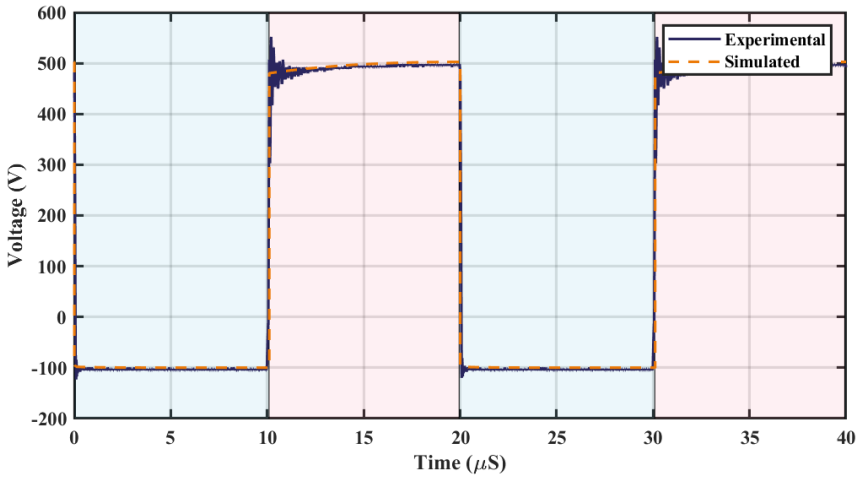

Figure 4.12: Experimental and simulated voltage across the input stage of VLSIMBC-HL design.

The data in Figure 4.13 demonstrates consistency in Mode 2 operation between experimental and simulated data. However, the simulated data did not predict the oscillations observed across the individual inductors during Mode 1 operation. The resonant frequency of the VLSI sub-circuit was approximately 175 kHz. During Mode 1 operation, the combined inductance was 333 μH. To achieve the observed resonant frequency, the equivalent capacitance would have been 2.5 nF. Conversely, as there were no oscillations observed in the data shown in Figure 4.11, it was highly unlikely that the voltage lift capacitors contributed to the observed resonance. Therefore, these oscillations were suspected to be due to a combination of capacitive parasitics, generated during the manufacture of the VLSI stage, operating in series with the inductors within the VLSI. Because the oscillations

destructively interfered with each other and were not observed across the input stage, as shown in Figure 4.10, this operation was deemed non-adverse to the function or general analysis of the topology.

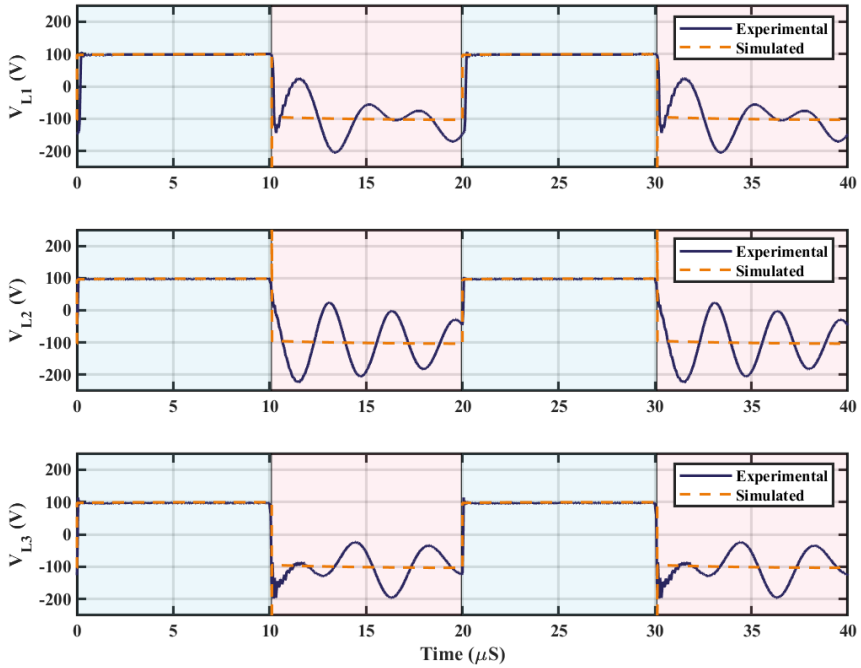

Figure 4.13: Input inductor voltage waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs

From the data in Figure 4.14, the average experimental currents through $L1$, $L2$, and $L3$ were 3.95 A, 3.95 A and 3.9 A over a complete switching period. With a measured experimental input current of 11.9 A. From this, the assumption of $I_{in} = N_L < I_L >$ in Section 4.2.1 was validated with $< 1\%$ error between the combined currents and the assumed total current. This assertion is also supported by the average simulated inductor of 3.88 A for all input VLSI stage inductors. During Mode 2 operation, a similar oscillatory pattern to that observed on the inductor voltage waveforms in Figure 4.13 were also observed. As the shape of current oscillations of the individual inductor matched that observed in the voltage waveforms, the current oscillations were determined to be due to the same parasitic capacitance. Furthermore, with the current oscillations following the same shape as the voltage oscillations. It was determined that the oscillatory behaviour

of the currents of the individual inductors also destructively interfered with one another and were non-confounding to device operation.

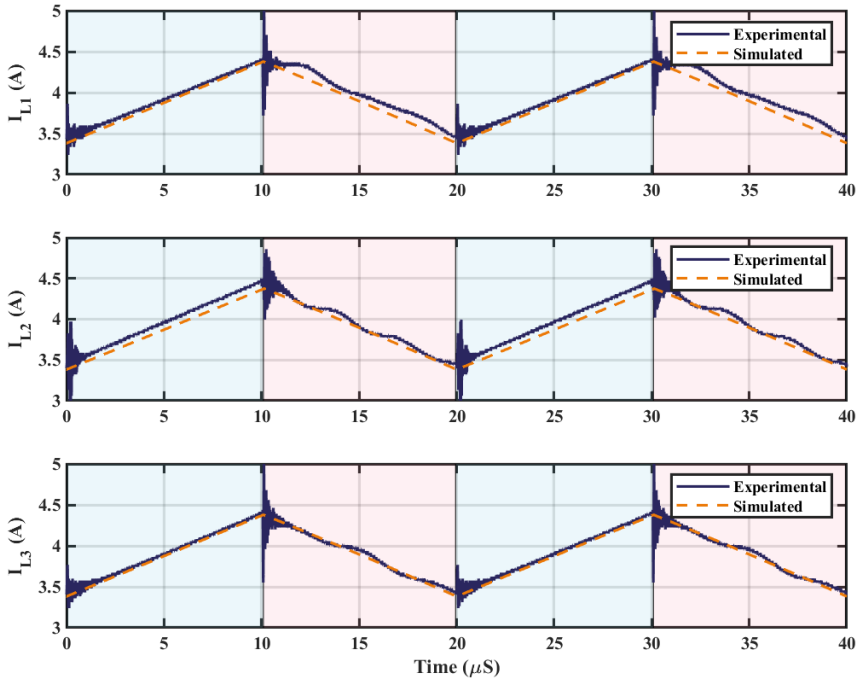

Figure 4.14: Input inductor current waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs.

4.4.2 Output Stage Operation

The data in Figure 4.15 show the output waveforms of the non-inverting ladder with average experimental values of 4146 V with a maximum ripple of 126 V and 278.0 mA. This was complemented by the simulated values of 4108 V and 273.9 mA. Additionally, both output voltages were found to agree with the analytical value of the output voltage, based on Equation 4.44, of 4086 V within a 2 % error. The experimental and simulated output powers were then calculated to be 1153 W and 1125 W, respectively, leading to calculated power efficiencies of 97.5 % and 96.9 %. This demonstrated further agreement between simulated and experimental data.

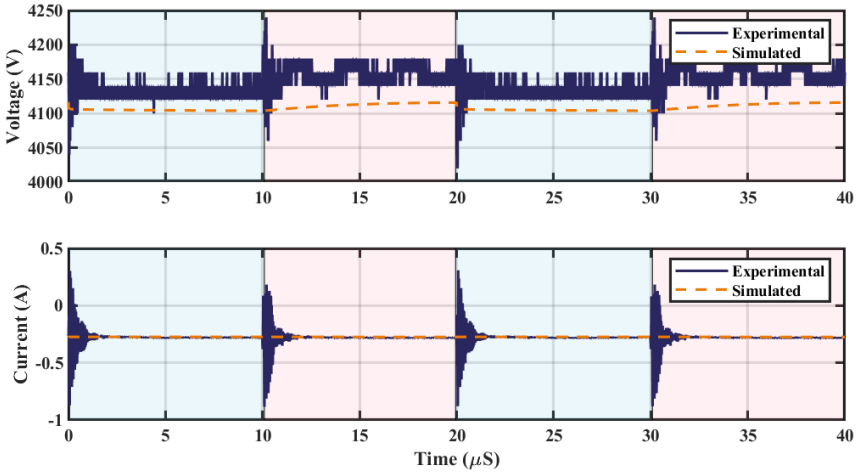

Figure 4.15: Output voltage and current waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs.

To observe the impact of voltage drop due to the use of multiple stages, the data in Figure 4.16 show the voltage across the first and last stage output capacitors. The experimental voltage drop between C_1 and C_{13} was observed to be 24.3 V with V_{C1} operating at 595 V. This was in agreement with the simulated voltage drop of 19.8 V with V_{C1} operating at 600 V and the expected analytical value of 588 V based on Equation 4.11.

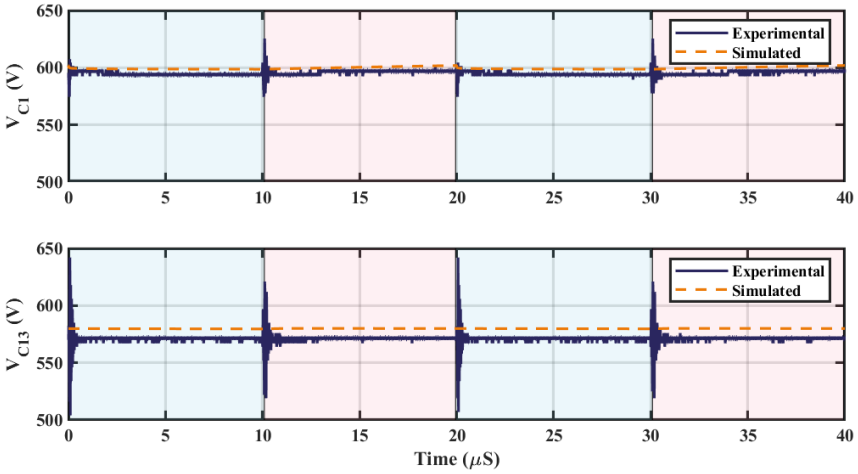

Figure 4.16: Experimental and simulated voltage across the first and final stage output capacitors of the VLSIMBC-HC design.

To observe the converter switching operation and validate the analysis proposed in Section 4.2.1, the voltages across D_1 and D_2 were presented in Figure 4.17. It was observed

that during Mode 1, D_1 was reverse biased at 598 V, which was approximately equal to V_{C1} and D_2 was forward biased. Conversely, during Mode 2, D_1 was forward biased and D_2 was reverse biased at 595 V, which was equal to V_{C1} . This experimental data demonstrated agreement with the operational analysis outlined in Section 4.2.1.

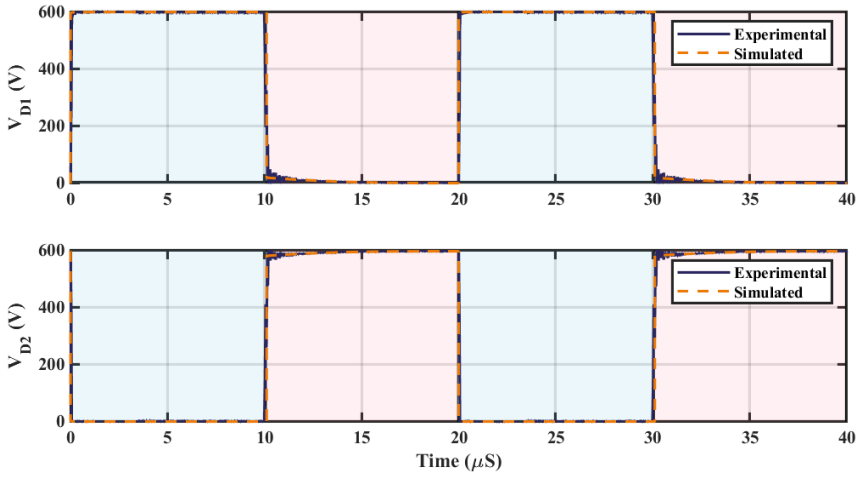

Figure 4.17: Experimental and simulated voltage waveforms across D_1 and D_2.

4.4.3 Switching Operation

The data in Figure 4.18 show the voltage across the switching device. When blocking in Mode 2, the observed V_{DS} was 595 V which was equal to V_{C1}, and approximately $\frac{1}{N_c}$ of the experimental output voltage of 4146 V. The average drain-source current was observed to be 11.47 A, offering agreement with the simulated value of 11.40 A. A discrepancy was observed during the switch turn-on transient, from Mode 2 to Mode 1, with the simulated drain-source current overshooting 948 %. This was suspected to be due to the simulation not considering current limiting parasitic inductances within the loops described in Section 3.8.1, creating a zero impedance loop, which resulted in the overshoot. Inductive elements within the device packaging were expected to have limited this observed overshoot during experimental characterisation.

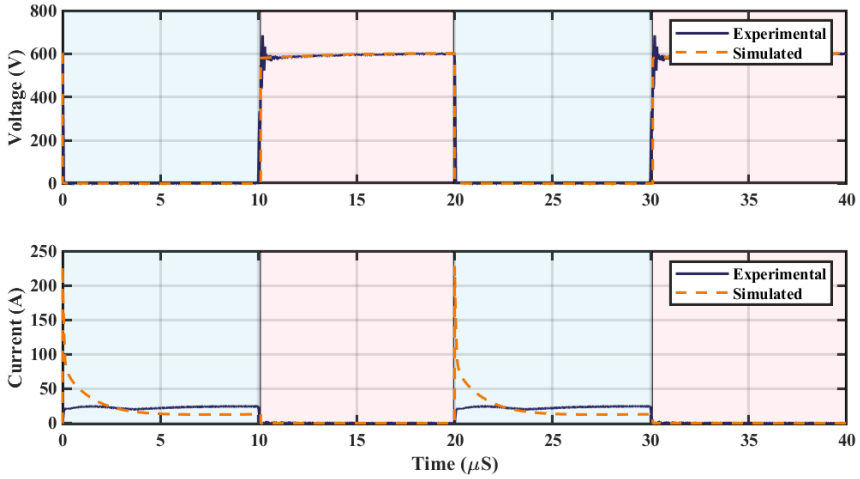

Figure 4.18: Experimental and simulated drain-source voltage and current waveforms of the VLSIMBC-HC design.

4.5 Experimental Designs Comparison

To investigate the use of the series inductor designs, explore the effect of capacitance on the designs and identify areas of optimisation. The proposed designs were experimentally characterised and compared. The parameters summarised in Table 4.2 describe the operating characteristics of the low capacitance designs, as well as the value for the series inductor. The main difference was the reduced capacitances for all capacitors aside from the lowest stage smoothing capacitor, C_2, and the reduced R_{esrC} associated with the smaller capacitors.

To maintain consistency between experiments, the VLSIMBC variants were characterised with the same 1 kW experimental set-up, which was utilised in the initial experimental characterisation test outlined in Section 4.4.

4.5.1 Input Stage Operation

The data in Figure 4.19 show the experimental input voltage and current waveforms for the VLSIMBC-HC and VLSIMBC-HCL designs. The average experimental values were

Table 4.2: Experimental parameters of the proposed VLSIMBC low capacitance designs

Parameters	Value
V_{in}	100 V
R_{out}	15 kΩ
L	1 mH
C_1	1 μF
C_2	11 μF
C_{3-13}	1 μF
f	50 kHz
D	0.50
R_{esrL}	28 mΩ
$R_{esrC1,\ 3-13}$	3.3 mΩ
R_{esrC2}	7.2 mΩ
L_S	5 nH

99.56 V at 11.88 A, which resulted in an input power of 1183 W for the VLSIMBC-HC design, and 100.45 V at 11.91 A, which resulted in an input power of 1196 W for the VLSIMBC-HCL design. A 24.8 % reduction in the transient voltage ripple from 42.1 V for the VLSIMBC-HC design to 31.7 V for the VLSIMBC-HCL design was also observed. These reductions demonstrated the potential of the series inductors to reduce noise at the input of the converter.

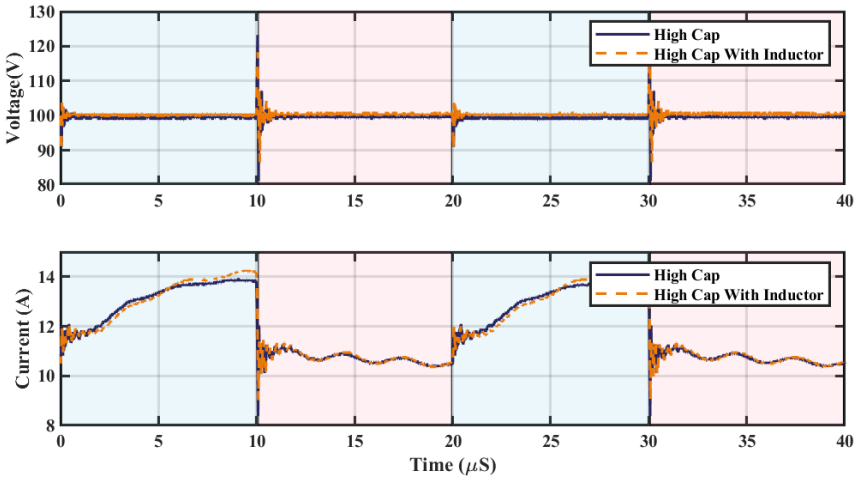

Figure 4.19: Input voltage and current waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs.

The data in Figure 4.20 show the experimental input voltage and current waveforms

for the VLSIMBC-LC and VLSIMBC-LCL designs. The average experimental values were 99.75 V at 11.56 A, which resulted in an input power of 1153 W for the VLSIMBC-LC design. These values were identified as 99.95 V at 11.67 A, which resulted in an input power of 1166 W for the VLSIMBC-LCL design. The inclusion of the series inductor for the low capacitor designs led to a 10.5 % voltage ripple reduction from 17.2 V to 15.4 V. This was less than half of the reduction observed in the high capacitor design. However, the ripple voltage between the series inductor designs differed by 0.5 V, which suggests that the inductor only limits the input voltage ripple to a certain point.

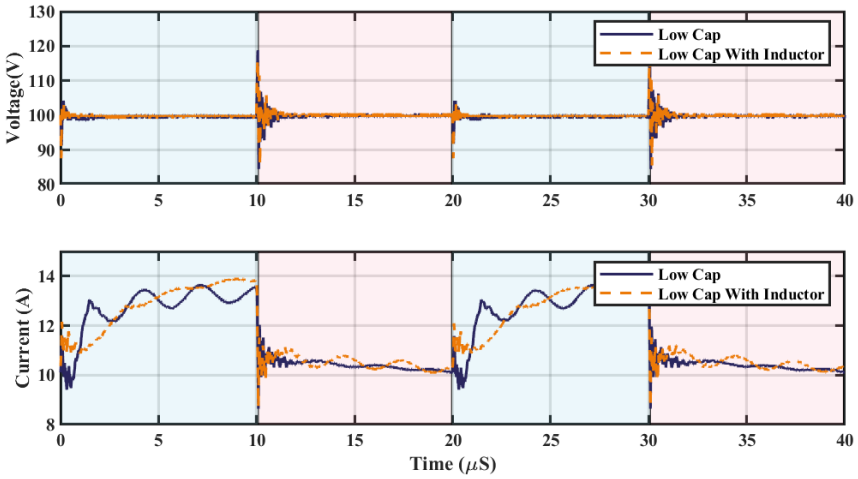

Figure 4.20: Input voltage and current waveforms of the VLSIMBC-LC and VLSIMBC-LCL designs.

When input waveforms were compared, the most significant observed difference between the HC and LC designs was the input voltage transients present during the transition from Mode 1 to Mode 2 operation. This was expected to be due to the limitations of the power supply, which failed to respond to the instantaneous demand of the larger capacitive load, and is discussed further in Section 4.6.1

4.5.2 Output Stage Operation

The data in Figure 4.21 show the experimental input voltage and current waveforms for the VLSIMBC-HC and VLSIMBC-HCL designs. The average experimental values were

4146 V at 278 mA, which produced 1135 W output and 4178 V at 278 mA, which produced 1161 W output for the VLSIMBC-HC and VLSIMBC-HCL designs, respectively.

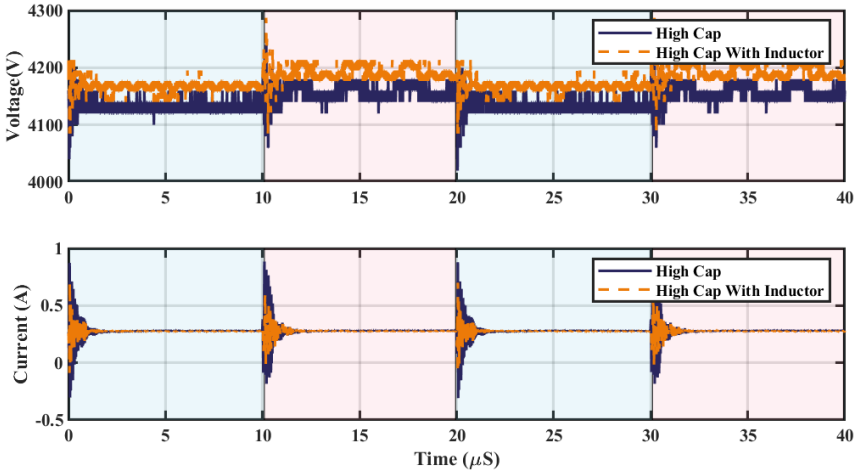

Figure 4.21: Output voltage and current waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs.

With the data from Figures 4.19 & 4.21 the experimental voltage gain of the VLSIMBC-HC and VLSIMBC-HCL designs were both 41.6, with power efficiencies of 97.5 % and 97.0 %, respectively. This showed that the addition of the series inductor has no observable impact on voltage gain, and led to a reduction in system level power efficiency of 0.5%.

The implementation of the series inductor for the high capacitor designs resulted in a 32 V increase in output voltage, while also improving switching transients by reducing the current ripple by 33.3 % and the voltage ripple by 8 %. However, the increased output voltage was almost certainly due to the approximately 1 V higher input voltage observed for the VLSIMBC-HCL design compared to the VLSIMBC-HC design. With a voltage gain of 41.6, the increased output voltage of 32 V falls within the expected range for a 1 V increase in input voltage. Hence, for the high capacitance design, the main benefit of the series induction was transient mitigation. However, this came at the trade-off of reduced power efficiency.

The data in Figure 4.22 show the experimental input voltage and current waveforms

for the VLSIMBC-LC and VLSIMBC-LCL designs. The average experimental values were 4100 V at 272 mA, which produced 1115 W and 4115 V at 272 mA, which produced 1119 W, for the VLSIMBC-LC and VLSIMBC-LCL designs, respectively.

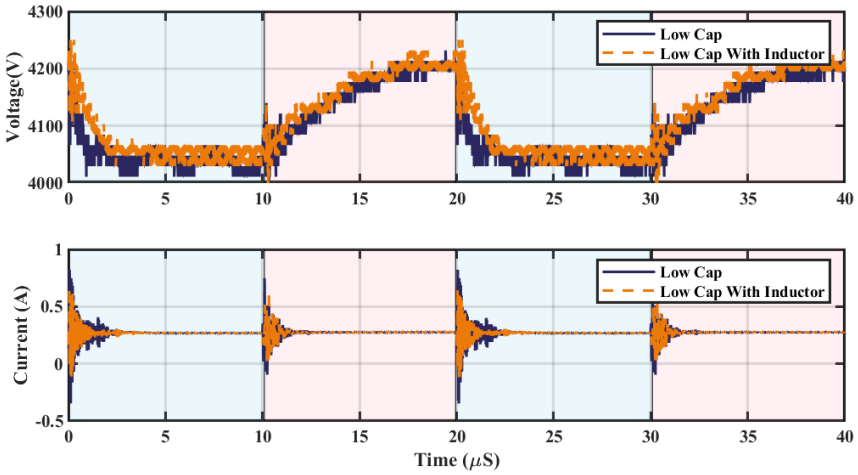

Figure 4.22: Output voltage and current waveforms of the VLSIMBC-LC and VLSIMBC-LCL designs.

With the data from Figures 4.20 and 4.22, the observed voltage gain of the VLSIMBC-LC and VLSIMBC-LCL designs were both 41.1 and 41.2, with power efficiencies of 96.6 % and 96.0 %, respectively. This reinforced the assertion that the introduction of a series inductor within the smoothing stage of the Cockcroft-Walton ladder has no impact on voltage gain, and slightly reduces overall power efficiency as a trade-off for improved output voltage quality via reduced transient overshoot.

When the high and low capacitance designs were compared, it was evident that higher capacitance designs were capable of achieving higher power efficiencies at 97.5 % compared to equivalent design lower capacitance designs at 96.6 %. Conversely, the lower capacitance designs operate with a voltage ripple of approximately 150 V, which peaked during Mode 2. This is in agreement with Equation 3.20, which resulted in a δV to be less than 2.5 % of the output voltage. In contrast, the high capacitance design maintained a ripple voltage of 300 V, which peaks during the transition between switching modes, and was expected

to be related to the limitations of the power supply.

4.5.3 Capacitor Operation

The data in Figure 4.23 outline the voltage across the first and highest-stage capacitors for the high capacitance capacitor designs. The average voltage of the first-stage output capacitor was observed to be 595 V for VLSIMBC-HC and 593 V for VLSIMBC-HCL. The average voltage of the highest stage output capacitor was observed to be 570 V for VLSIMBC-HC and 572 V for VLSIMBC-HCL, respectively. These minor voltage shifts suggested that the implementation of the series inductor had no significant impact on the voltage drop across the capacitor stages. However, the inclusion of a series inductor resulted in a 169 % increase in ripple voltage for the first stage and a 44 % reduction for the highest stage. This presented a trade-off between output voltage quality and increased voltage stress for lower-stage capacitors for high-capitance designs.

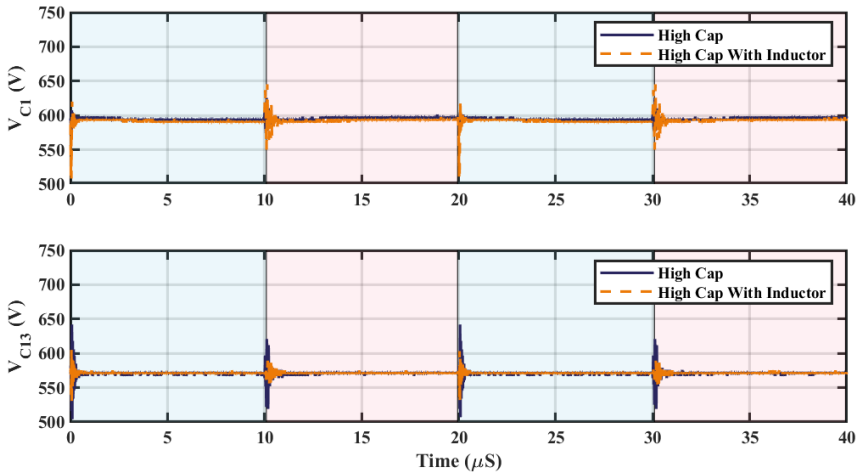

Figure 4.23: Output voltage waveforms from the first and last stage output capacitors of the VLSIMBC-HC and VLSIMBC-HCL designs.

Figure 4.24 outlined the voltage across the first and highest stage capacitors for the low capacitance capacitor designs. The average voltage of the first-stage output capacitor was observed to be 633 V for VLSIMBC-LC and 628 V for VLSIMBC-LCL. Additionally, the average voltage of the highest-stage output capacitor was observed to be 534 V

for VLSIMBC-LC and 523 V for VLSIMBC-LCL. As with the high-capacitance designs, the similar voltages between the inductor and no-inductor designs suggest that the implementation of the series inductor had no significant impact on the voltage drop across the capacitor stages. Furthermore, the data show a 36 % decrease in ripple voltage for the first stage and a 47 % reduction for the highest stage. This demonstrates how the implementation of a series inductor may reduce voltage ripple for the low capacitance VLSIMBC designs.

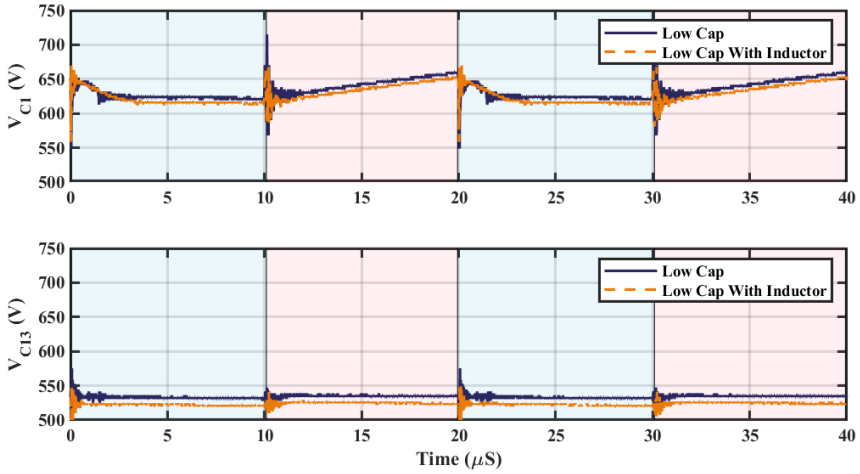

Figure 4.24: Output voltage waveforms from the first and last stage output capacitors of the VLSIMBC-LC and VLSIMBC-LCL designs.

4.5.4 Switching Operation

The data in Figure 4.25 show the current and voltage waveforms for the high capacitor designs. It was observed that the introduction of the series inductor reduced voltage overshoot by 6 %, and eliminated current overshoot during turn-on, whilst having a minimal impact on the current transients observed during turn-off. This showed that the introduction of a series impact inductor had a relatively low effect upon switching device operation for the high capacitance designs.

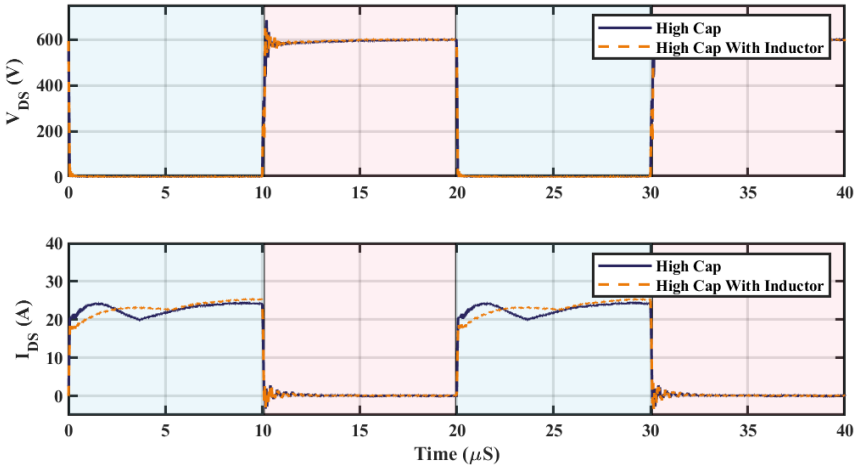

Figure 4.25: Drain-Source voltage and current waveforms of the VLSIMBC-HC and VLSIMBC-HCL designs.

The data in Figure 4.26 shows that the introduction of the series inductor in low capacitance designs increased transient voltage overshoot by 27 %. However, this voltage overshoot was lower than the final peak voltage. Conversely, the current overshoot was reduced by 38.5 % when the series inductor was introduced, demonstrating the potential of the series inductor to be utilised in the mitigation of large current overshoots present in low capacitance VLSIMBC designs.

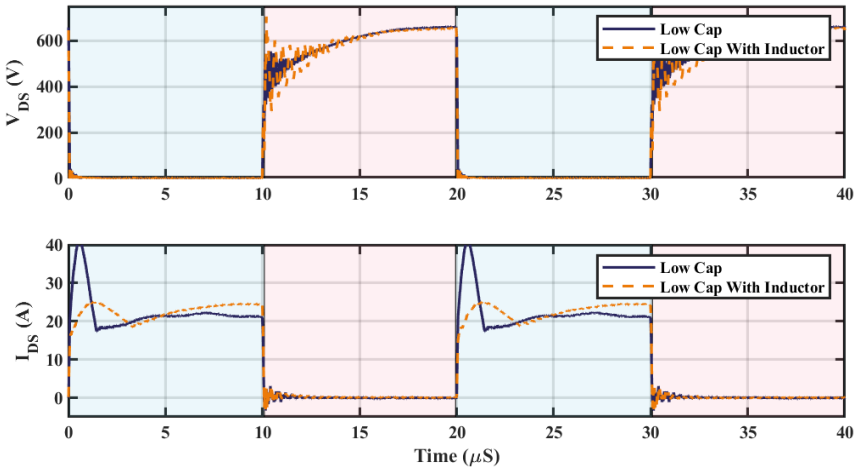

Figure 4.26: Drain-Source voltage and current waveforms of the VLSIMBC-LC and VLSIMBC-LCL designs.

The greatest variation in switch operation between the low and high capacitance designs was observed to be the increased transient overshoot in the low capacitance design.

This may be analytically explained by Equation 3.20, defining the inverse relation between capacitance and output voltage ripple, along with Equation 3.27, which defined the proportional relationship between voltage ripple and the magnitude of current through the capacitors that flows through the switching device during Mode 1. The increased transient current observed in the low capacitor design leads to increased conduction losses, partially accounting for the 1.5% power efficiency difference between the high and low capacitance designs.

4.6 Chapter Summary of Ultra-High Gain DC-DC Boost Converter

4.6.1 Power Supply Limitations and Input Current

During initial testing of the VLSIMBC-HC design, during 1 kW operation, a periodic low-frequency voltage instability was observed. This instability produced instantaneous input voltages 100 % greater than the normal working voltage. This instability, illustrated in the data in Figure 4.27, resulted in switching-stage device failures and limited the operational range of the device.

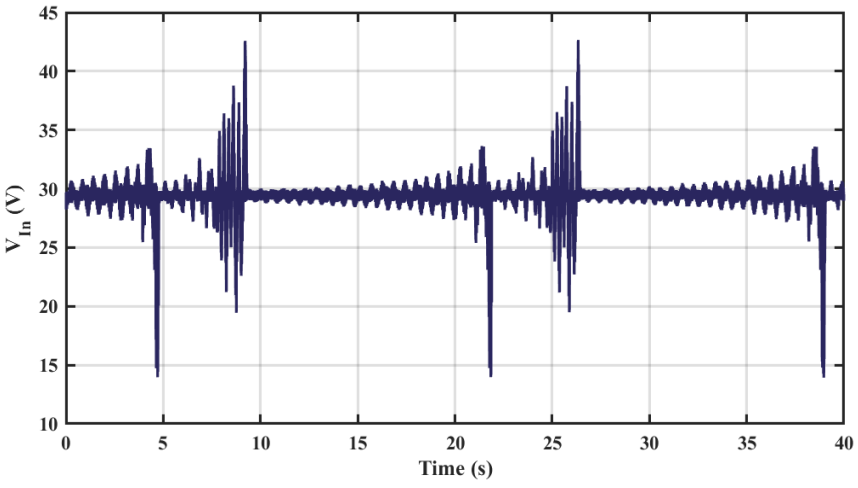

Figure 4.27: Input voltage waveform of the proposed VLSIMBC converter without decoupling capacitors.

It was determined that the current instability was due to limitations in the responsiveness of the power supply, being unable to transition between charging a large capacitive load in Mode 2 and shorting through the switch stage in Mode 1. To account for this, a 39 mF capacitive bank was implemented to allow for rapid input responses during transition from Mode 2 to Mode 1, which allowed for testing of the converter at a similar power to the converter in Chapter 3. A second effect of the introduction of this input capacitor bank was the reduction in transient voltage ripple through the converter and input voltage transient from Mode 2 to Mode 1, which was less than 25 % than that observed from Mode 1 to Mode 2. This suggests that the high transient voltage observed for the HC designs may not be entirely due to the configuration of the converter and at least partially due to the limitations of the power supply utilised during experimental characterisations and comparisons.

4.6.2 Series Inductor Design Implementation

After analysing the implementation of the series inductor across both high and low-capacitance designs, it became apparent that the component presents a trade-off between transient reduction and power efficiency. Reductions in overshoot were observed across the transient voltage waveforms, ranging from 6 % to 44 % for the high capacitance design and from 27 % to 47 % for the low capacitance design. However, an approximate 15 % increase in power losses was observed in both high and low capacitance designs, which led to an approximate 0.5 % decrease in operation efficiency.

The initial aim of the series inductor implementation was to reduce current transients in the switching device to both prevent over-current and reduce conduction losses. The data in Figure 4.26 demonstrated the potential of the series inductor in the reduction of switch current transients for low capacitance designs; however, the experimental data

showed that the power saved from potential reductions in conduction losses was exceeded by the additional losses from implementing a new component into the converter.

From this, it is noted that further exploration of low-value series inductors could offer improved performance in low-capacitance Cockcroft-Walton designs. However, additional work would be required to minimise power losses presented by the series inductor. Furthermore, when efficiency is the primary focus, the series inductor is not likely to be beneficial in converter operation.

4.6.3 Conclusion

This chapter presented the design and analysis of a novel DC-DC converter with both a scalable input VLSI and a scalable output switch capacitor ladder. The discussed topology demonstrated both an ultra-high voltage conversion ratio potential and complementary scalability of the voltage lift-switched inductor with the Cockcroft-Walton topology. A demonstrator unit was developed to experimentally validate both simulated operation and theoretical analysis, demonstrating a 97.5 % power efficiency. For steady-state operation, the simulated and experimental results both support the analysis presented in Sections 4.2.1 and 4.3. This demonstrates that the proposed design is capable of a voltage conversion ratio in excess of 40 while maintaining high power efficiency above 97 %.

Following this, a secondary study was conducted to explore the potential of a transient current-limiting inductor in the Cockcroft-Walton ladder. This variant of switched capacitor design has been highlighted but not fully explored in the literature. The secondary study aimed to investigate a method of transient mitigation. It was observed that the series inductor presented a trade-off between reduced transient voltage magnitude at the expense of reduced power efficiency. While potentially beneficial for other applications, the reduction in power efficiency was undesirable for high efficiency low to medium voltage

boost converters.

When considering this design in relation to the project aim of designing a DC-DC converter capable of stepping up a range of low voltage DC inputs into a stable DC output capable of inversion to 3.3 kV_{AC}. A design capable of complementary scalability at 2 different stages was demonstrated, which is theoretically capable of achieving the target voltage conversion ratios. However, the specified medium voltage was not met due to the large input current ripple and input voltage ripple of 20 %. These ripples were anticipated to cause overvoltages and potential component failure during transients at higher operating voltages, in addition to thermal degradation from increased conduction losses due to increased currents. As a result, a strategy to minimise transient overshoots at the output and switch stage was explored but ultimately rejected due to the losses in system efficiency. It can be observed that for higher operating voltages, the ripple is proportionally lower than that observed in Chapter 3. The data in Figure 4.15 demonstrated an output ripple voltage of 3 %, which was within the target parameter of 5 %. To achieve the target converter specified in the project outlines, further developments in the mitigation of input current ripple and voltage conversion were required to allow for reliable high voltage operation. Sufficient voltage gain methods had been explored with the VLSI and Cockcroft-Walton to achieve the target gain of 4.7 kV_{DC}; therefore, following these findings, the primary focus of the project was input current ripple mitigation and transient reduction.

CHAPTER 5

Design and Analysis of an Ultra-High Gain Bipolar DC-DC Converter

5.1 Introduction

With the analysis and demonstration of a high-efficiency bipolar design in Chapter 3 and an ultra-high voltage gain scalable topology in Chapter 4 came the opportunity to demonstrate an ultra-high gain bipolar topology. Such a design would be able to step up a range of low-voltage inputs into a stable, unipolar or bipolar medium voltage output. This would allow for the integration of low voltage wave energy converters into medium voltgage networks. An important consideration when developing DC-DC converters was to consider the impact of input current ripple, because high current ripple can result in reduced device performance and increased power losses at generation sources [38, 90]. As observed in the concepts previously presented, the utilisation of single switch DC-DC converter designs often results in large input voltage and current ripples due to the large variance in current demands during different switching modes. Potential solutions to this

large input current ripple include large input capacitor banks to smooth the ripple while supplying excess current to the converter during switch conduction, such as that used in Chapter 4; however, these capacitor banks reduce the power density of the overall system due to the positive relationship between current ripple and required input capacitance. Alternatively, interleaved designs which utilise multiple switch and input stages with a staggered operation, have been demonstrated to reduce input current ripple in exchange for increased circuit and control complexity [38, 60, 91, 92].

This chapter combines the key novel features of the continuous operation bipolar multilevel boost converter and the scalable voltage lift switched inductor multilevel boost converter, explored in Chapters 3 and 4. The topology was further innovated upon with the implementation of an interleaved design and a a full-wave Cockcroft-Walton, to minimise voltage ripple. These contributions allowed for the demonstration of a novel ultra-high voltage gain bipolar interleaved DC-DC converter, which required only 2 switching devices to achieve a wide range of continuous low-to-medium voltage conversion. The theoretical circuit analysis is presented and proven via a 2 kW simulated and experimental demonstration unit. A power loss analysis was then conducted to identify potential optimisations for efficiency improvement. Finally, a DC sweep was conducted in both unipolar and bipolar operations to demonstrate the range of low voltage inputs in which the proposed topology is capable of stable MVDC conversion. This, in turn, demonstrated the partial achievement of the aim of the project to develop a converter capable of high voltage gain conversion for the integration of low voltage generation into medium voltage networks.

5.2 Proposed Topology

The proposed topology was built upon the previously presented designs by integrating the bipolar Cockcroft-Walton multipliers presented in Chapter 3 with the 3-stage voltage

lift switched inductor (VLSI) stage presented in Chapter 4. Furthermore, to reduce input current ripple, an interleaved design for the input stage was utilised, doubling the component usage for the input stage. To maintain a DC output with an interleaved design, the half-wave Cockcroft-Walton utilised in previous designs was replaced with full-wave Cockcroft-Walton (FWCW) switched capacitor multipliers. This resulted in increased output stage component usage of 75%. The proposed design used two 3-stage VLSI input multipliers, two switching devices and two 6-stage FWCW output multipliers to achieve ultra-high voltage conversion ratios. Overall, the design consisted of a total of 40 capacitors, 56 diodes, 6 inductors and 2 switching devices. Figure 5.1 illustrates the circuit diagram for the proposed topology.

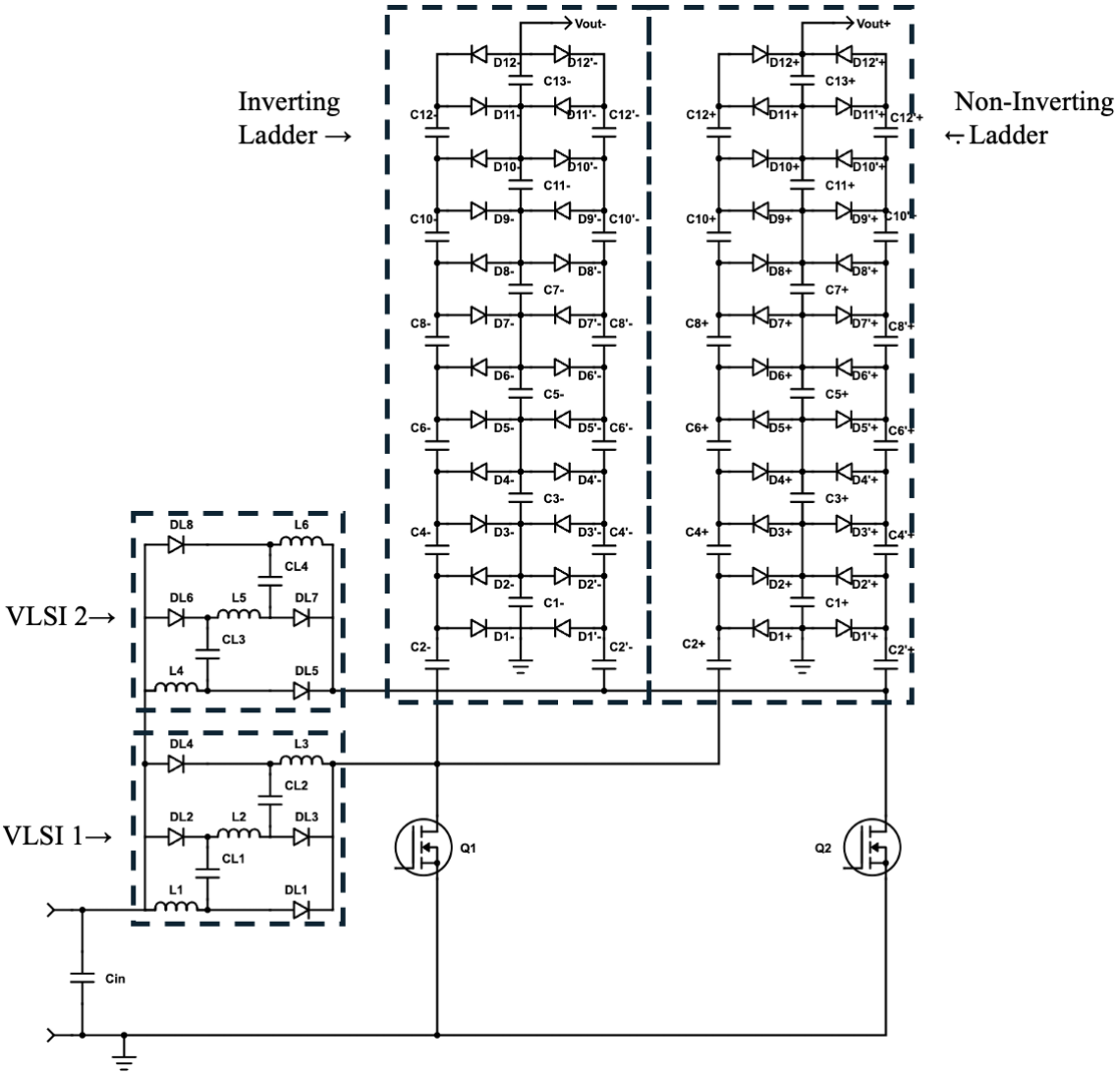

Figure 5.1: Circuit diagram of proposed topologies full wave bipolar voltage lift switched inductor multi-level boost converter (FWBVLSIMBC).

5.2.1 Modes of Operation

With the addition of a second switch, two further modes of operation were present within the FWBVLSIMBC topology in comparison to those presented in Chapters 3 and 4. Figure 5.2 illustrates the possible switch modes of operation.

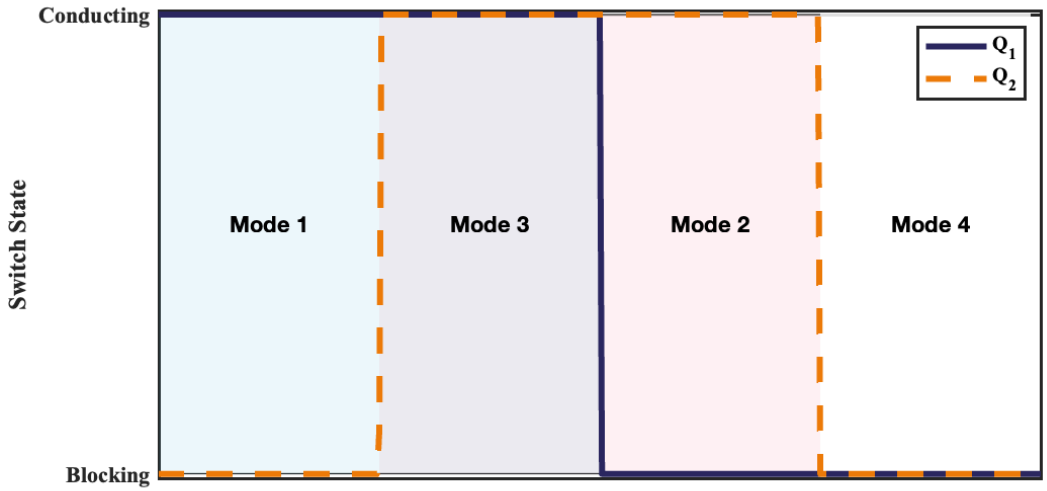

Figure 5.2: FWBVLSIMBC switch modes of operation

During Mode 1: Switch Q1 conducts and Q2 blocks. Inductors L1, L2 and L3 charge in parallel via switch Q1. Inductors L4, L5 and L6 discharge in series via the C' capacitors and D' diodes into the odd output capacitors.

During Mode 2: Switch Q1 blocks and Q2 conducts. Inductors L4, L5 and L6 charge in parallel via switch Q2. Inductors L1, L2 and L3 discharge in series via the even C capacitors, D diodes into the odd smoothing capacitors in the central line of the inverting and non-inverting ladders.

During Mode 3: Switch Q1 and Q2 both conduct. Inductors L1, L2 and L3 charge in parallel via switch Q1. Likewise, Inductors L4, L5 and L6 charge in parallel via switch Q2. The operation of the capacitor ladder diode is dependent on which switch blocked most recently in the switching cycle. Mode 3A occurs when switch Q1 blocked most recently, all odd D diodes conduct, discharging the odd output capacitors via Q1. Mode 3B occurs when switch Q2 blocked most recently; all odd D' diodes conduct, discharging the odd output capacitors via Q2.

During Mode 4: Switch Q1 and Q2, both block. Inductors L1, L2 and L3 discharge in

series via the even C capacitors and D diodes into the odd output capacitors. Inductors L4, L5 and L6 also discharge in series via the C' capacitors and D' diodes into the odd output capacitors.

5.3 Steady State Operation

With the implementation of an additional switching device came the need to select 2 duty ratios as well as the phase shift between them. When considering voltage gain equations, the higher of the 2 duty ratios dictates the output voltage of the converter; as it would provide the greatest voltage to the output stage. An increase in the difference between the duty ratios results in greater input current ripple and output voltage ripple, as well as imbalanced currents between the VLSI stages. Due to this, the duty ratio of the switches was selected to be equal and 180° out of phase, to minimise potential voltage ripple and eliminate imbalances between the interleaved VLSI stages [38, 91, 92].

By utilising an expanded analysis of Section 3.3.1, the ideal voltage gain of the proposed topology may be given as:

$$\frac{V_{out}}{V_{in}} = \pm\frac{N_L N_C}{1-D} \tag{5.1}$$

where V_{out} is the output voltage, V_{in} the input voltage, N_C the number of stages within the switched-capacitor ladder, N_L the number of stages within the voltage lift switched inductor stage and D the duty ratio of the switching devices. With the utilisation of a similar voltage drop analysis to that presented in [93], which was expanded upon in Section 5.4.2, the expected output voltage for a full wave Cockcroft-Walton when considering only

capacitive based losses, may be given by:

$$\frac{V_{out}}{V_{in}} = \pm\frac{N_L N_C}{1-D} \mp \frac{I_{out}(2N_C^3 + 3N_C^2 + N_C)}{12fCV_{in}} \tag{5.2}$$

where f is the switching frequency, I_{out} the output current and C the value of capacitors within the Cockcroft Walton multiplier under the assumption that they are all equal.

Input Inductor Analysis

The VLSI stage of the interleaved converter utilised the same topology outlined in Chapter 4. Assuming that the 2 interleaved stages are identical, the stages operate in parallel, leading to the average current through the individual inductors being halved in comparison to a single VLSI stage design with the same output conditions. Opposing this, the addition of a second switched capacitor ladder, such as that proposed in Chapter 3, results in double the power rating of the converter, compared to a single ladder design. This results in the average current demand, at the input stage, being doubled. In comparison to the unipolar topology presented in Chapter 4, for a given output voltage, the proposed topology would experience double input current, which is equally shared across the 2 interleaved VLSI stages. These characteristics cancel out to allow the average current through any inductor, $< I_L >$ in the circuit to be described with the Equation 4.4. This, in turn, allows the input stage voltage gain, with consideration of equivalent series resistance, to be described with Equation 4.10.

Capacitor Analysis

By expanding upon the ripple analysis reported in Section 4.3.2, assuming the interleaved switches operate 180° out of phase, and all capacitors were equal, the voltage ripple con-

tribution of any output capacitor in a full-wave Cockcroft Walton can be expressed as:

$$\delta V_C = \frac{I_{out}}{8fC} \tag{5.3}$$

For any stage, the combined contribution of the previous capacitors must be considered [74]. For example, in a 2-stage Cockcroft-Walton ladder, the voltage ripple of the 2nd stage smoothing capacitor would be δV_{C3}, and the voltage ripple across the 1st stage smoothing capacitor would be $2\delta V_{C1}$ to account for both its voltage ripple and to provide charge to the 2nd stage smoothing capacitor, thus leading to a total output ripple of $\delta V_{C3} + 2\delta V_{C1}$ or if all capacitors are equal $3\delta V_C$. When this process is summed, the voltage ripple of an N_C stage capacitor ladder may be calculated with:

$$\delta V_{out} = \delta V_C \left(\frac{N_C^2}{2} + \frac{N_C}{2} \right) \tag{5.4}$$

Additionally, the voltage ripple of any stage smoothing capacitor may be determined with:

$$\delta V_{Ck} = \frac{\delta V_{out}}{(N_C + 1 - k)} + \delta V_{Ck-1} \tag{5.5}$$

where k is the stage to be considered. When considering the voltage drop across the capacitor ladder, an adaptation to the derivation of the half-wave Cockcroft-Walton multiplier based on [74] may be utilised. When interleaved stages operate 180° out of phase, the frequency of the smoothing capacitor may be considered $2f$. This consideration would lead to the total charge transferred in a single switching period to be $\frac{I_{out}}{2fC}$ for a given smoothing capacitor. When considering the contributions of individual capacitor stages,

this equation becomes:

$$\begin{aligned}
\Delta V_{C_{N_C}} &= \frac{I_{out}}{2fC_{N_C}}\left(N_C\right) \\
\Delta V_{C_{N_{C-1}}} &= \frac{I_{out}}{2fC_{N_{C-1}}}\left(2N_C + (N_C - 1)\right) \\
\Delta V_{C_{N_{C-2}}} &= \frac{I_{out}}{2fC_{N_{C-2}}}\left(2N_C + 2(N_C - 1) + (N_C - 2)\right)\cdot \\
&\ldots \\
\Delta V_{C_1} &= \frac{I_{out}}{2fC_{N_1}}\left(2N_C + 2(N_C - 1) + \ldots + 2(2) + 1\right)
\end{aligned} \tag{5.6}$$

This sequence follows the same series of the half-wave Cockcroft-Walton outlined in [74] multiplied by a factor of $\frac{1}{2}$; therefore, when assuming equal capacitance, this sequence may be expressed as:

$$\Delta V_{out} = \frac{I_{out}}{2fC}\left(\frac{2N_C^3}{3} + \frac{N_C^2}{2} - \frac{N_C}{6}\right) \tag{5.7}$$

which may be simplified

$$\Delta V_{out} = \frac{I_{out}(4N_C^3 + 3N_C^2 - N_C)}{12fC} \tag{5.8}$$

Additionally, the output voltage of any given capacitor stage, when assuming an ideal voltage input stage with no losses, may be determined with

$$V_{Ck} = \pm\frac{V_{in}k}{1-D} \mp \frac{I_{out}}{2fC}\left(\frac{2(N_C^3 - k^3)}{3} + \frac{N_C^2 - k^2}{2} - \frac{N_C - k}{6}\right) \tag{5.9}$$

Diode Analysis

The operation of diodes in the VLSI stage and output ladder can be described following the analysis and assumptions outlined in Sections 3.3.1 and 4.2.1.

Input Diodes During Mode 1 operation: diodes D_{L1} - D_{L4} are forward biased with a current I_{DL} of:

$$I_{DL} = \frac{I_{in}}{N_L} \tag{5.10}$$

where I_{in} is the input current. Diodes D_{L5} - D_{L8} are reversed bias with a blocking voltage of:

$$V_{DL5} = V_{DL8} = V_{C1+} - V_{L4} - V_{in} \tag{5.11}$$

$$V_{DL6} = V_{DL7} = \frac{V_{C1+} - V_{L4} - V_{in}}{2} \tag{5.12}$$

During Mode 2 operation: diodes D_{L1} - D_{L4} are reversed biased with a blocking voltage of:

$$V_{DL1} = V_{DL4} = V_{C1+} - V_{L4} - V_{in} \tag{5.13}$$

$$V_{DL2} = V_{DL3} = \frac{V_{C1+} - V_{L1} - V_{in}}{2} \tag{5.14}$$

Diodes D_{L5} - D_{L8} are forward biased with a current given by Equation 5.10.

During Mode 3 operation: all input diodes are forward biased with a current equal to that expressed in Equation 5.10.

During Mode 4 operation: all input diodes are reverse biased with blocking voltages equal to those specified in Equations 5.11 - 5.14.

Output Diodes The diodes on the output capacitor ladder operate similarly to those described in Section 3.3.1. The data summarised in Tables 5.1 & 5.2 details the diode bias based on a given operation mode for the non-inverting and inverting ladders, respectively.

Table 5.1: Non-inverting capacitor ladder output diode bias under different modes of operation in the FWBVLSIMBC.

	Odd D+	Even D+	Odd D'+	Even D'+
Mode 1	Forward	Reverse	Reverse	Forward
Mode 2	Reverse	Forward	Forward	Reverse
Mode 3	Forward	Reverse	Forward	Reverse
Mode 4	Reverse	Forward	Reverse	Forward

Table 5.2: Inverting capacitor ladder output diode bias under different modes of operation in the FWBVLSIMBC.

	Odd D-	Even D-	Odd D'-	Even D'-
Mode 1	Reverse	Forward	Forward	Reverse
Mode 2	Forward	Reverse	Reverse	Forward
Mode 3	Reverse	Forward	Reverse	Forward
Mode 4	Forward	Reverse	Forward	Reverse

When under reverse bias, the voltage across any output diode, V_D, may be ideally expressed according to:

$$V_D = \frac{V_{out}}{N_C} \tag{5.15}$$

Switch Analysis

Using the same analysis outlined in Section 4.2.1, the maximum drain-source voltage of the switch, V_{DSmax}, without considering transient voltage overshoots and assuming the first stage of the inverting and non-inverting output ladders are equal in magnitude, may

be expressed as:

$$V_{DSmax} = \frac{V_{in} N_L}{1 - D} = \frac{V_{out}}{N_C} \tag{5.16}$$

and the drain-source current of the transistor may be calculated as:

$$I_{DS} = \frac{I_{in} - I_{out+} - I_{out-}}{2} \tag{5.17}$$

where I_{DS} is the drain-source current, I_{out+} the non-inverting output current, I_{out-} the inverting output current.

5.4 Design Considerations

With the introduction of the interleaved input stages, the implications of transitioning to and from Modes 3 and 4, as well as imbalances between the interleaved stages, should be considered. Similarly, the design change from half-wave to full-wave Cockcroft-Walton output ladder brings different optimisation requirements for minimising voltage ripple and voltage drop across the ladder capacitors.

5.4.1 Imbalanced Voltage Lift Switched Inductor

Due to the doubling of the input current from the additional output voltage multiplier, negating the halving of the individual inductor current from the second VLSI stage, Equation 4.27 may be utilised to identify the parameters for boundary conduction mode (BCM) operation. The impact of imbalanced inductors within a VLSI stage has been explored in Section 4.3.1.

With the introduction of the interleaved design comes the opportunity to explore the impact of inductor imbalance between VLSI stages. As the stages operate independently of one another, differences in inductor size between stages only affect the current ripple

of the inductors within the specific stage. With this capability to individually vary the ripple current within the VLSI stages, there is the potential to have each sub-topology function in different conduction operation modes. When considering equal duty ratios between switching stages, it is possible that one VLSI stage operates within discontinuous conduction mode (DCM) and the other operates in continuous conduction mode (CCM) due to the difference in inductance values between the interleaved stages. The output voltage of the DCM stage would be greater than the CCM stage, and thus, dominate operation with the output voltage multipliers, preventing current flow from the CCM stage. This imbalance of VLSI stages would result in the proposed converter operating in DCM and utilising a single VLSI stage. This type of imbalance would result in increased input current ripple and reduced power efficiency due to increased conduction losses, in comparison to the proposed converter utilising DCM for both VLSI stages. To minimise the likelihood of divergent modes of operation between the VLSI stages and maintain simplicity, Equation 4.27 may be used to determine the potential conduction modes for inductors of a given inductance tolerance during component selection.

5.4.2 Capacitor Ladder

By expanding Equation 5.5, the fundamental output voltage ripple equation reported in [74] may be observed:

$$\delta V_{out} = \frac{I_{out}}{f}\left(\frac{1}{C_{11}} + \frac{2}{C_9} + \frac{3}{C_7} + \frac{4}{C_5} + \frac{5}{C_3} + \frac{6}{C_1}\right) \tag{5.18}$$

When following the same ripple reduction approach outlined in Section 4.3.2 and following previously reported recommendations to double the value of the most influential capacitor stage [74], effective reductions in voltage ripple may be achieved by modifying the capacitance at the first stage of the switched capacitor ladders. By substituting $C_1 = 2C_{3-11}$,

where $C_{3-11} = C_3 = C_5 = \ ... \ = C_{11}$, the output voltage ripple may become:

$$\delta V_{out} = \frac{9 I_{out}}{4 f C_{3-11}} \tag{5.19}$$

The doubling of C_1 results in a 14% reduction in output ripple voltage in comparison to the single-value homogeneous capacitor design. The increase in C_1 to $2C_{3-11}$ results in the voltage drop expressed in Equation 5.6 being amended to:

$$\Delta V_{out} = \frac{I_{out}}{f C_{3-11}} \left(\frac{N_C^3}{6} + \frac{N_C^2}{4} + \frac{N_C}{12} \right) \tag{5.20}$$

With this, it was observed that by doubling the capacitance of first stage capacitor, the capacitive-based voltage drop of a 6-stage Cockcroft-Walton could be reduced by approximately 20 %, compared to homogeneous capacitor selection.

5.4.3 Proposed Operation Range

By utilising the method outlined in Section 4.3.3, Equations 4.10 and 5.2 may be combined to provide an estimate of voltage gain without knowledge of I_{out} so that:

$$\frac{V_{out}}{V_{in}} = \pm N_L N_C \left(\frac{(1-D) R_{out}}{(1-D)^2 R_{out} + R_{esrL} N_L N_C^2} \mp \frac{(2N_C^3 + 3N_C^2 + N_C)}{12 f C (1-D) R_{out}} \right) \tag{5.21}$$

Hence, the estimated gain of the proposed converter, under bipolar operation, may be identified.

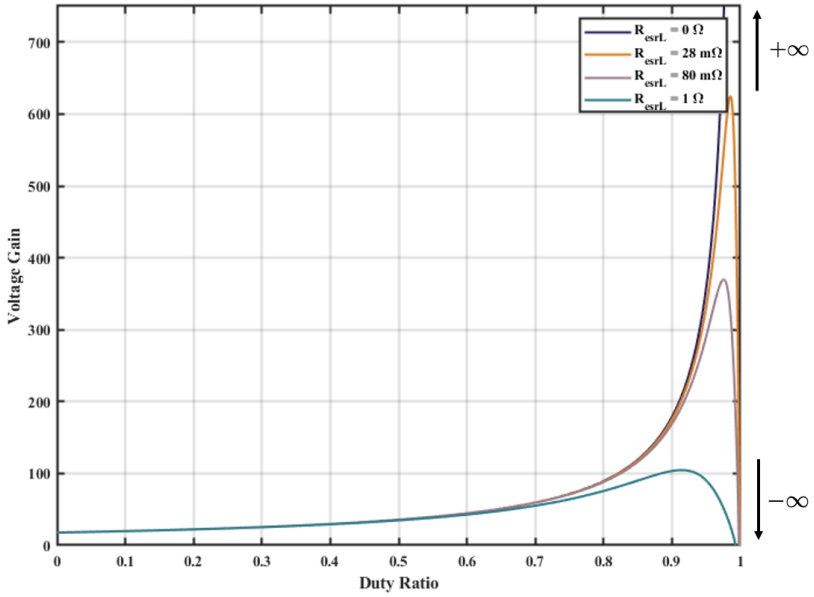

Figure 5.3: Voltage gain of a single output capacitor ladder against duty ratio for a 3 inductor stage, 6 capacitor stage, FWBVLSIMBC with 2.2 μF capacitors and 50 kHz switching frequency.

Similar to the estimated gain analysis in Chapters 3 and 4, the data in Figure 5.3 show that excessively high duty ratios (> 0.75) can lead to divergences in the predicted gain proportional to the equivalent series resistance of the input inductors. However, for non-excessive duty, the equivalent series resistance of any inductor commonly used in DC-DC applications should not have an observable impact on converter voltage gain.

To observe the maximum possible voltage gains from the proposed converter, the voltage across the non-inverting output could be referenced to the inverting ladder output rather than the input reference, modifying the design from a bipolar topology with common grounding to a unipolar design. This would double the estimated voltage gain to:

$$\frac{V_{out+} - V_{out-}}{V_{in}} = 2N_L N_C \left(\frac{(1-D)R_{out}}{(1-D)^2 R_{out} + R_{esrL} N_L N_C^2} - \frac{(2N_C^3 + 3N_C^2 + N_C)}{12fC(1-D)R_{out}} \right) \quad (5.22)$$

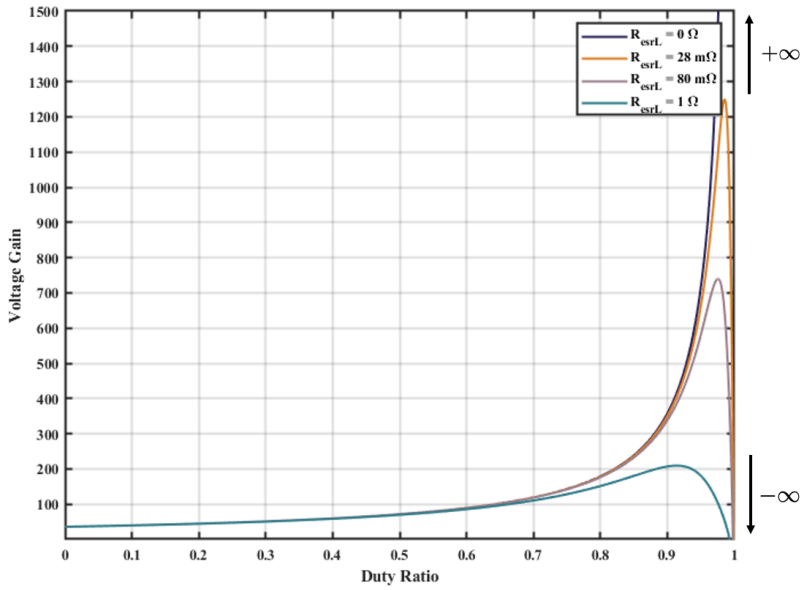

Figure 5.4: Voltage gain against duty ratio for a 3 inductor stage, 6 capacitor stage, FWBVLSIMBC with 2.2 μF capacitors and 50 kHz switching frequency

The data in Figure 5.4 show that by changing the reference point, the proposed device demonstrated double the voltage gain to that outlined in Figure 5.3, and has the potential to achieve voltage gains of over 100 without utilising duty ratios greater than 0.75. As this approach connects both outputs, the 2 multipliers could not be considered to operate independently, potentially increasing output voltage ripple and drop as well as power losses within the ladder due to increased current transients.

5.4.4 Practical Impact of Modes 3 and 4

When analysing the new operating modes, the current demands and subsequent requirements and changes in demand when switching between modes must be considered. During Modes 1 and 2, one switching device conducts while the other blocks. From this, one input stage charges while the other discharges. This results in a current draw of:

$$I_{inm1} = I_{inm2} = ((N_L + 1) < I_L > + I_{Ccharge}) \tag{5.23}$$

where I_{inm1} and I_{inm2} are the input currents during Mode 1 and Mode 2, respectively and $I_{Ccharge}$ the current required to recharge the voltage lift capacitors to V_{in}. During Mode 3 operation, both switching devices conduct simultaneously, and both voltage lift stages charge. The ramped current draw would be approximately:

$$I_{inm3} = 2(N_L < I_L > + I_{Ccharge}) \tag{5.24}$$

where I_{inm3} is the input current during Mode 3. When the converter switches from Mode 3 to Modes 1 or 2, the maximum current ripple would be $(N_L - 1) < I_L > \ + I_{Ccharge}$, however, for practical applications in CCM operation, where the ratio of Mode 3 operation is significantly less than Mode 1 or 2 operation (e.g. $< 10\%$) the ramped current ripple may be approximated to $I_{Ccharge}$.

During Mode 4 operation, both switching devices block simultaneously, both voltage lift stages will discharge, and the inductors within each stage operate in series. With this, the current draw from the input is:

$$I_{inm4} = 2 < I_L > \tag{5.25}$$

where I_{inm4} is the input current during Mode 4. When the converter switches from Mode 4 to Modes 1 or 2, the maximum step current ripple would be $(N_L - 1) < I_L > \ + I_{Ccharge}$.

The greatest current ripple would be present during the transition from Mode 3 to Mode 4 operation. This would result in an input current ripple, during the Mode transition, of

$$\Delta I_{m3-m4} = 2((N_L - 1) < I_L > \ + I_{Ccharge}) \tag{5.26}$$

Moreover, the transition from any other Mode to Mode 4 would result in a step change

in current, leading to large $\frac{dI}{dt}$ and undesirable transients. To minimise the impact of these transitionary input current ripple within the interleaved topology, Mode 4 operation should be avoided and when necessary, i.e. for output voltages which require $D < 0.5$, the phase difference between the switching devices should be such that transitions between Mode 3 and Mode 4 operation do not occur, rather if Mode 4 operation is an inevitability transitions between it should be via Modes 1 or 2 operation to minimise transient $\frac{dI}{dt}$. Further Mode 4 mitigation strategies are discussed in Section 5.5.2

5.5 Simulation and Experimental Validation

To demonstrate the potential of the proposed FWBVLSIMBC, the proposed design was experimentally characterised and compared against LTSpice-based simulations and the previously presented analysis. The device parameters for the converter were outlined in Table 5.3.

Table 5.3: Experimental component parameters of the FWBVLSIMBC

Parameters	Value
L	1 mH
C	2.2 μF
f	50 kHz
R_{esrL}	28 mΩ
R_{esrC}	5.7 mΩ

5.5.1 Single Duty Ratio, Single Input

To validate the base operation and provide a point of comparison to the previously proposed converters, an open-loop test was conducted by utilising the same input voltage and target output voltage in Section 4.4. Table 5.4 summarises the operating parameters used in the experiment.

Table 5.4: Experimental parameters for the single duty ratio single input study of the FWBVLSIMBC

Parameters	Value
V_{in}	100 V
Target V_{out}	±4000 V
R_{out}	15 kΩ
D	0.57

To outline the switch mode of operation, the data in Figure 5.5 show the gate source voltages of the normally off MOSFETS utilised in the proposed topology.

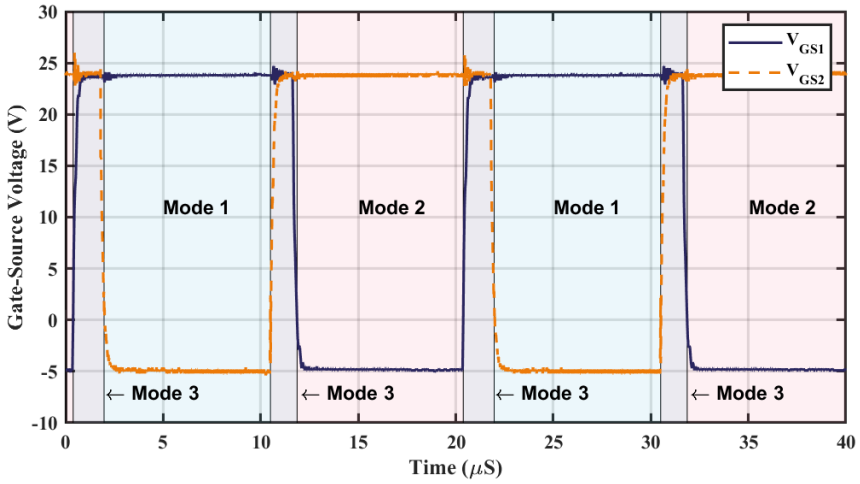

Figure 5.5: Experimental Gate-Source voltage waveforms of the proposed FWBVLSIMBC topology.

Input Stage Operation

The data in Figure 5.6 show both the experimental and simulated input voltage and current waveforms. The average experimental input values of 99.96 V and 23.23 A are complemented by simulated values of 101.8 V and 22.86 A. The experimental input power was calculated to be 2322 W. It was also noted that a transient voltage ripple of approximately 17 % was observed during the experimental characterisation test, when the device transitioned into Mode 3. This was approximately 23 % lower than the ripple voltage observed for the VLSIMBC under similar operating conditions, demonstrated in Section 4.4.

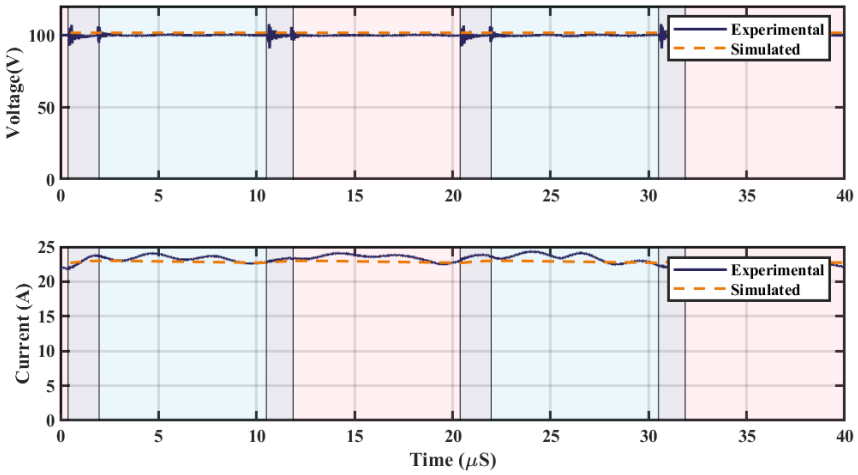

Figure 5.6: Experimental and simulated input voltage and current waveforms of the proposed FWBVLSIMBC topology.

To demonstrate interleaved operation, the data in Figure 5.7 show the total experimental voltage across the interleaved VLSI stages. It was also observed in Figure 5.7 that the voltages across the interleaved VLSI stages, V_{L1} and V_{L2}, were operating 180° out of phase. The peak and minimum VLSI stage voltages V_{L1} and V_{L2} were observed to be 584 V and 590 V, respectively, at peak and -100 V and -103 V at minimum. These values were equal to each other within a 3% error. This demonstrated balanced voltage sharing and equal inductances within each VLSI stage, as well as across the interleaved

VLSI sub-circuits. The individual inductors of both V_{L1} and V_{L2} were observed to oscillate around 130 V during Q_1 blocking and maintain -100 V during their respective switch conduction mode. This also demonstrates that the differences between the inductances of the inductors were small enough such that no voltage spike was present at the VLSI stages during operation, as would be expected based on the imbalance inductor analysis presented in Section 4.3.1.

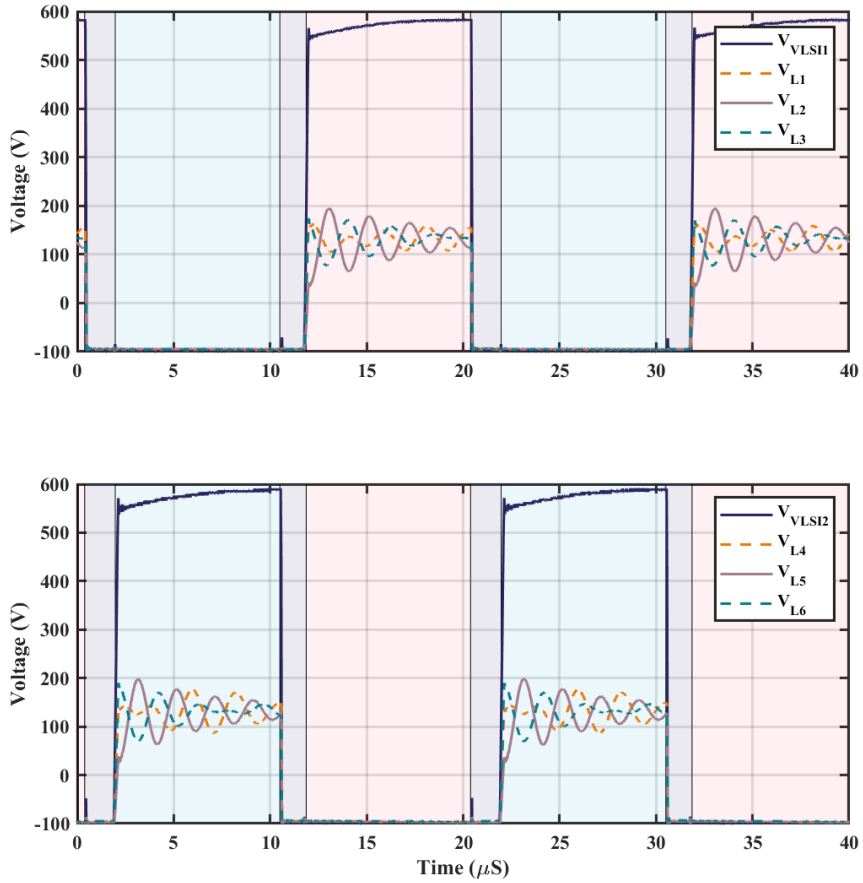

Figure 5.7: Experimental inductor voltage waveforms of the proposed FWBVLSIMBC topology.

From the data in Figure 5.8 the average experimental currents through $L11$, $L12$ and $L13$ over a complete switching period were observed to be 3.85 A, 3.81 A and 3.87 A, with a measured experimental input current through L1 to be 11.53 A. This is in agreement within a 3% error with the simulated current through the individual inductors within the $L1$ VLSI stage, with average currents of approximately 3.81 A and a total current through

L1 of 11.4 A. These values are also in agreement with the analytical value of the inductor current of 3.81 A determined with Equation 4.4, and the average value of V_{C1+} and V_{C1-} as the output voltage of the VLSI stage.

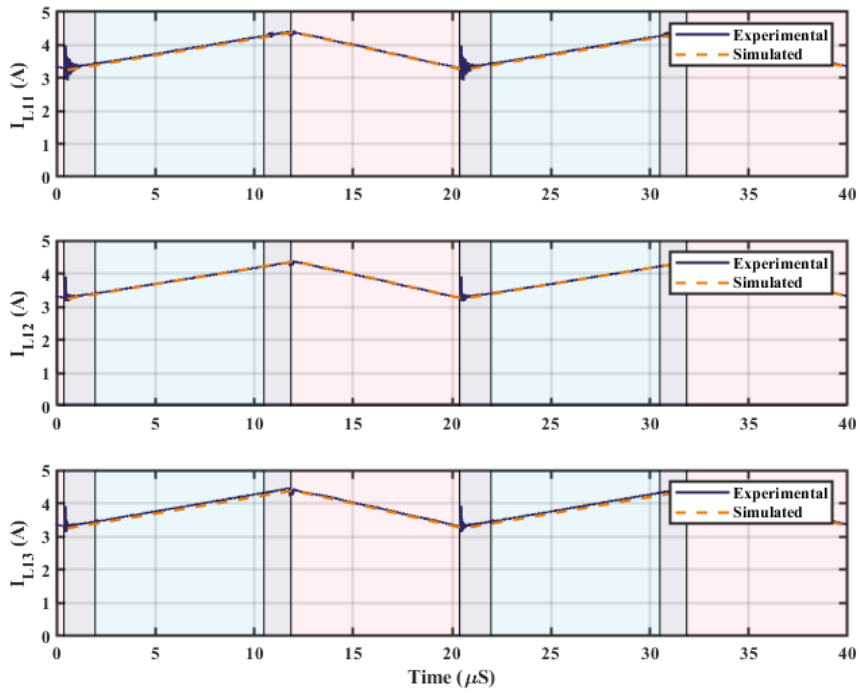

Figure 5.8: Experimental inductor current waveforms of the proposed FWBVLSIMBC topology.

From the data in Figure 5.9, the average experimental currents through L_{21}, L_{22} and L_{23} were measured as 3.76 A 3.75 A and 3.77 A over a complete switching period. With a measured experimental input current, through L2, of 11.28 A, this is in agreement, within a 3 % error, with the simulated current and the analytical value previously stated.

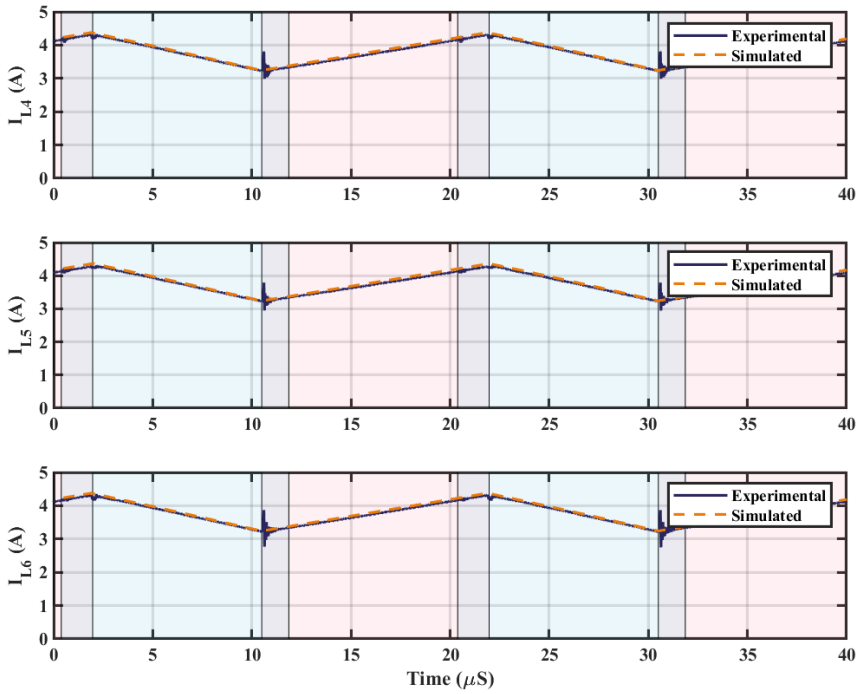

Figure 5.9: Experimental inductor current waveforms of the L2 VLSI stage within the proposed FWBVLSIMBC topology.

The total currents of the interleaved VLSI stages were observed to be 11.53 A and 11.28 A, demonstrating agreement within a 4 % error. These findings also provided agreement with the previous analysis and demonstration of the VLSI stage presented and observed in Sections 4.2.1 & 4.4.1.

Output Stage Operation

The data in Figure 5.10 show the output waveforms of the non-inverting ladder with average experimental values of 4072 V and 269.0 mA complemented by simulated values of 4089 V and 272.6 mA. Both simulated and experimental output voltages were found to be in agreement with analytical values, calculated with experimental input voltage and Equation 4.44 of 4064 V within a 1 % error. The experimental and simulated output powers were found to be 1095 W and 1115 W, respectively. When assuming that half the input power, 1161 W, was dedicated to the supply of the non-inverting ladder, the approximate

experimental efficiency of non-inverting operation was calculated to be 94.3 %.

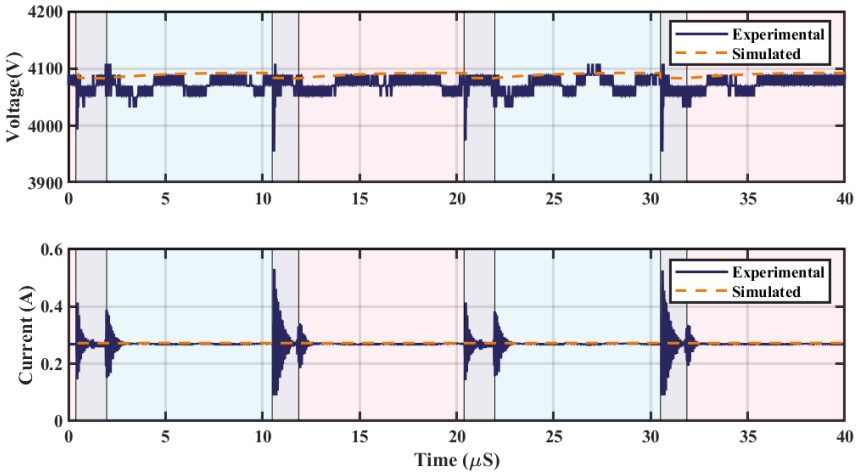

Figure 5.10: Experimental and simulated positive output voltage and current waveforms of the proposed FWBVLSIMBC topology.

The data in Figure 5.11 show the output waveforms of the inverting ladder with average experimental values of -4065 V and -277.1 mA, which were in agreement with the simulated values of -4097 V and -273.1 mA. Both simulated and experimental output voltages were found to be in agreement, within a 1 % error, with the analytical value, based on the experimental input voltage and Equation 4.44, which predicted the inverting voltage output of -4064 V . The experimental and simulated output powers were found to be 1126 W and 1119 W, respectively. Based on the same power operation assumptions as the non-inverting topology, the approximate experimental efficiency of the inverting operation was calculated to be 97.0 %, which was 2.3 % greater than the non-inverting efficiency. The difference in approximate efficiencies between the inverting and non-inverting components of the proposed topology can be analytically accounted for with the 2.9 % or 8.1 mA, which is a larger magnitude of output current within the inverting ladder, while the output voltages were equal within a 0.2 % error. Due to the small size of the current, there were many potential explanations for the increased power efficiency of the inverting ladder, in comparison to the non-inverting ladder, including: manufacturing tolerances in the

components leading to a lower overall equivalent series resistance in the inverting ladder; undersampling the oscillations of the switching transients from the oscilloscope, leading to a partially biased current reading or an inherent aspect of the inverting operation leads to reduced power dissipation in comparison to the non-inverting design.

When considering the holistic power dissipation of the proposed topology, the total experimental and simulated output power of the proposed topology was found to be 2221 W and 2234 W, respectively. This led to a calculated experimental power efficiency of 95.7 % and a simulated efficiency of 96.0 %.

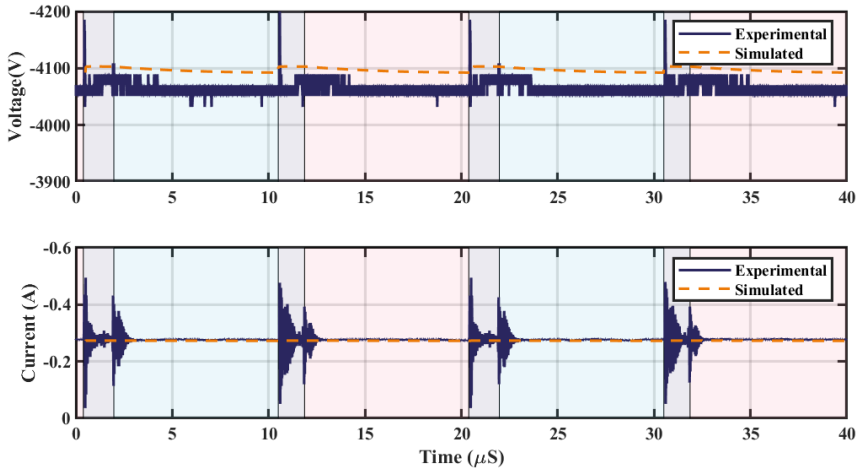

Figure 5.11: Experimental and simulated negative output voltage and current waveforms of the proposed FWBVLSIMBC topology.

The data in Figure 5.12 outline the voltage across the first and sixth stage capacitors for the non-inverting output ladder. The average voltage of the first-stage output capacitor was observed to be 677 V, and the average voltage of the sixth stage output capacitor was observed to be 661.9 V. This demonstrated a maximum voltage imbalance of the non-inverting topology to be 15.1 V, which was 5.9 V lower than the observed imbalance for the 7-stage 11 μF capacitor series inductor topology presented in Section 4.4.2. While the design in Section 4.4.2 possessed an additional multiplication stage, which contributes to increased voltage and power losses, the proposed design in this chapter utilised capacitors

which were 19 % of the capacitance in comparison to those used in Chapter 4, which would be expected to result in a significantly larger voltage drop based on Equations 4.41 & 5.20. This highlights the potential of the full-wave topology in reducing voltage imbalance across capacitor stages while using smaller-sized capacitors.

The simulated voltages across the first and sixth stage capacitors, C_1 and C_{13}, were 692.5 V and 676.0 V, respectively. This demonstrated a simulated capacitor voltage imbalance to be similar to the experimental findings, of 16.5 V. The observed difference in simulated voltages of 15.5 V compared to the experimental voltages significantly coincides with the 1.8 V higher simulated input voltage. Based on Equation 4.10, the difference in input voltage would result in an increase at V_{C1} of 11.5 V, and the remaining difference of 3.5 V can be considered as approximately 0.5 % of the total voltage across the sixth stage capacitor. It was concluded that the simulated voltages across the non-inverting ladder were consistent with the experimental equivalent within a margin of error to be less than 3%.

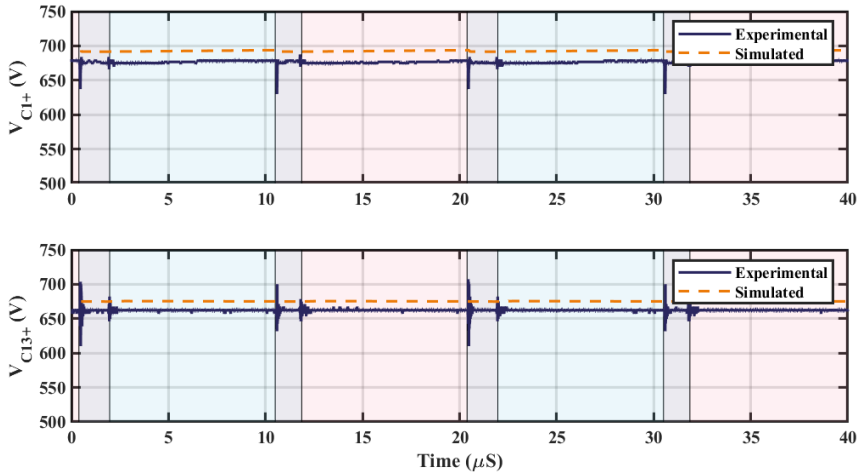

Figure 5.12: Experimental and simulated first and last stage non-inverting ladder capacitor voltage waveforms of the proposed FWBVLSIMBC topology.

The data in Figure 5.13 outline the voltage across the first and sixth stage capacitors for the inverting output ladder. The average voltage of the first-stage output capacitor

was observed to be 689 V. The average voltage of the highest stage output capacitor was observed to be 675 V. This demonstrated a voltage imbalance, similar to the non-inverting ladder, of 14 V and further supports the potential of the full-wave design in voltage imbalance reduction in comparison to the previously presented half wave designs.

The simulated voltages across the first and sixth stage inverting ladder capacitors were -694 V and -676 V, respectively, demonstrating a simulated imbalance of 18 V. A voltage difference of 5 V was observed between the voltages across the experimental and simulated first stage, which highlighted a discrepancy between the simulated and experimental findings. This overestimation of voltage drop in the simulated findings suggests an aspect of operation was not fully considered; due to the symmetry of the simulated ladders, and that there was little discrepancy between identified in the non-inverting ladders, this difference was likely due to how the inverting operation was simulated in LTSpice. Similar to the analysis proposed in Section 3.8.1, in the inverting ladder, the sixth stage smoothing capacitor and associated diodes form part of the low impedance loop when either switch begins conduction. From this, the simulation may have calculated higher conduction losses in the inverting capacitor ladder, compared to the non-inverting ladder. This could be used to explain the discrepancy between the expected and observed difference in capacitor voltage due to the increased simulated input voltage. As the overall difference in voltage drop accounted for less than 2 % of the voltage across any individual smoothing capacitor, the discrepancy was deemed non-confounding for the analysis of the proposed converter.

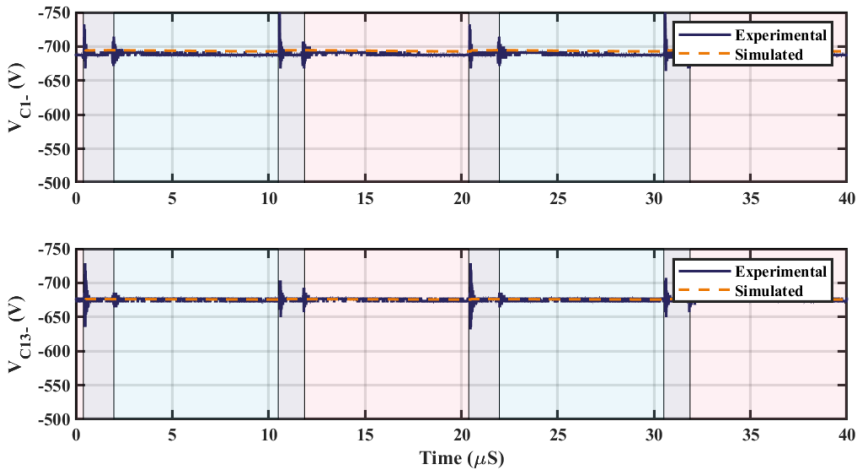

Figure 5.13: Experimental and simulated first and last stage inverting ladder capacitor voltage waveforms of the proposed FWBVLSIMBC topology.

To validate output diode operation, the data in Figure 5.14 demonstrate the switching operation of the 4 diodes in the first capacitor stage of the non-inverting capacitor ladder. Diode D1+ conducts during Modes 1 & 3, D1'+ during Modes 2 & 3, D2+ during Mode 2 and D2'+ during Mode 1. The experimental data were observed to be consistent with the simulated results; furthermore, both sets of data were in agreement with the operational analysis summarised in Table 5.1.

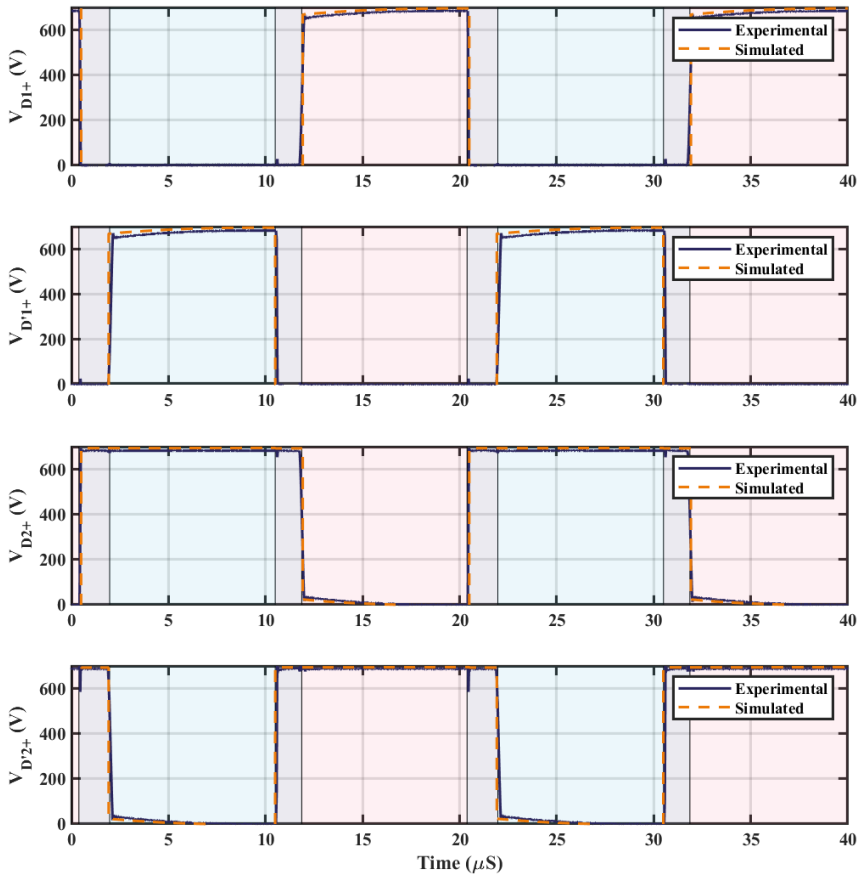

Figure 5.14: Experimental and simulated voltage across the first stage diodes of the proposed FWBVLSIMBC non-inverting output capacitor ladder.

The data in Figure 5.15 demonstrate the switching operation of the 4 diodes at the first capacitor stage of the inverting capacitor ladder. Diode D1- conducts during Mode 2, D1'- during Mode 1, D2- during Modes 1 & 3 and D2'- during Modes 2 & 3. All observed experimental first stage output diodes had a maximum reverse-bias voltage of 680 V, which is equal to both the voltages across the first stage inverting and non-inverting capacitors, as well as the proposed reverse-bias analytical value proposed in Equation 5.15. Additionally, the simulated first stage output diodes had a maximum reverse-bias voltage of 695 V, which was also consistent with the voltage across the first stage capacitors as well as Equation 5.15. From these observations, it was concluded that both the experimental and simulated diode operations were consistent with the proposed operational analysis summarised in Table 5.2 as well as the proposed voltage analysis.

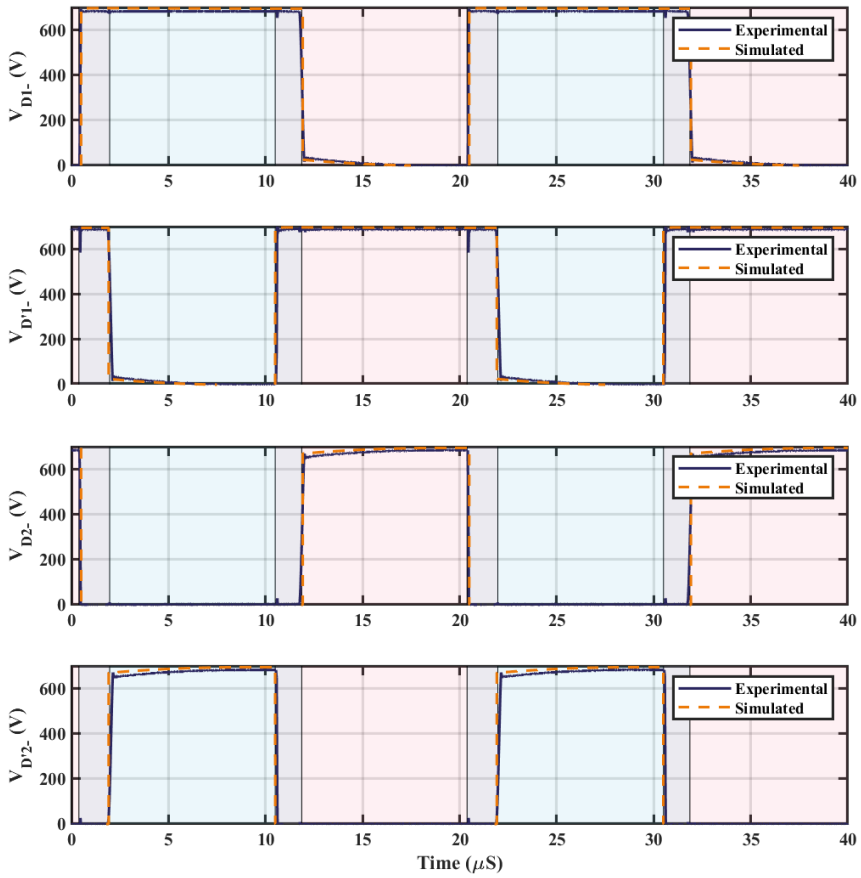

Figure 5.15: Experimental and simulated voltage across the first stage diodes of the proposed FWBVLSIMBC inverting output capacitor ladder.

The experimental data in Figure 5.16 demonstrate relatively low voltage drop across the first stage smoothing capacitors with an average voltage of 0.99 V and 0.65 V across the left and right capacitors, respectively. These values were greater than and of opposite polarity to the average simulated voltages of -2.21 V and -2.20 V across the left and right capacitors.

This suggested that during simulation, the voltage across the switch on the same side as the capacitor (e.g. $< V_{Q1} >$ for C_{2+}) was greater than the voltage across the connecting ground diode (e.g. $< V_{D1+} >$ for C_{2+}), whereas the converse was true experimentally. To explore this, the average voltages across a complete switching cycle, for Q_1 and $D1+$, were identified. Based on the data outlined in Figure 5.14, the average experimental and simulated voltages of $D1+$ were 290 V and 294 V, respectively. The average voltage

across Q_1 was determined based on the data shown in Figure 5.18 in Section 5.5.1, which explores the experimental and simulated characterisation of switching devices within the proposed topology. Hence, the average experimental and simulated voltages of $Q1$ were 289 V and 296 V, respectively. When comparing the experimental and simulated voltages, it was evident that $< V_{DS1} >$ was greater than $< V_{D1+} >$ during simulation, with the opposite being true for experimentation. This inconsistency was expected to be due to the simulation calculating that, during conduction, the voltage across D_{1+}, varied between -1.8 V and -0.7 V. Practically, as the anode of D_{1+} was connected to ground, the voltage across the diode should never be lower than zero, which was observed experimentally. From this, it was concluded that the discrepancy between the simulated and experimental capacitor values in the data shown in Figure 5.16 was due to an error in how the simulation calculated the voltage across ground-referenced diodes and that the general operational waveforms of the datasets were otherwise in agreement.

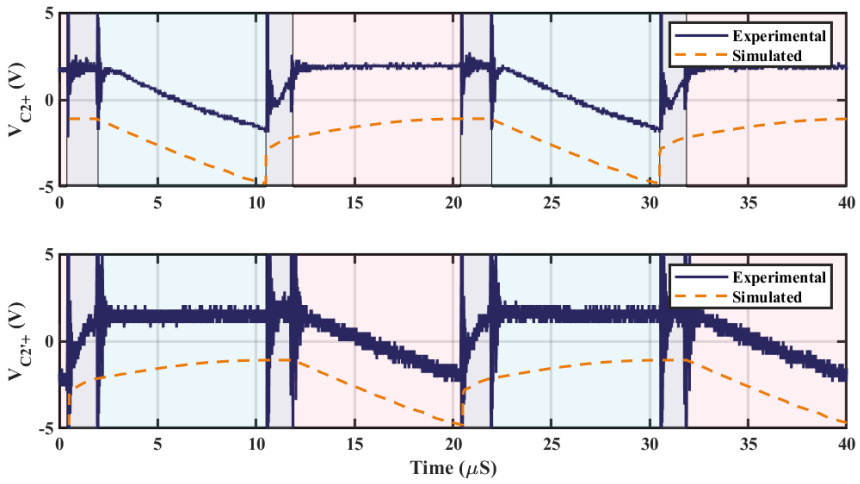

Figure 5.16: Experimental and simulated left and right non-inverting first stage capacitor voltage waveforms of the proposed FWBVLSIMBC topology.

The experimental data in Figure 5.17 demonstrate the voltage across the first stage smoothing capacitors, with an average voltage of -682.6 V and -689.0 V for the left and right capacitors, respectively. These values were in agreement with the simulated average

voltages of -696 V for both left and right capacitors. This showed that the first stage oscillating capacitors acted as the point of inversion for the inverting output ladder, by allowing charge to accumulate on the capacitor plates connected to the VLSI input stage sub-circuits. As a result, a negative potential was generated in the same manner as the inverting ladder described in Section 3.2.

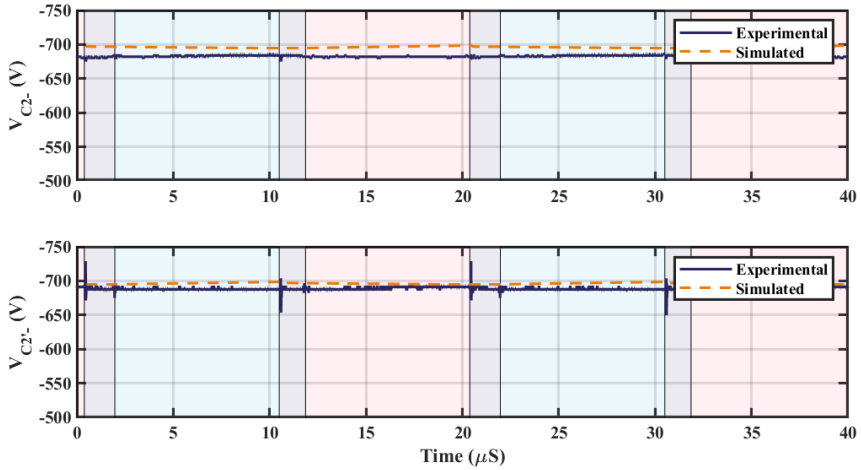

Figure 5.17: Experimental and simulated left and right inverting first stage capacitor voltage waveforms of the proposed FWBVLSIMBC topology.

Switch Operation

The data in Figure 5.18 show the Drain-Source voltage across both switching devices utilised in the proposed topology. During blocking (transition to Mode 1 for Q1 and Mode 2 for Q2), the voltage across both switches began at 650 V and rose to 691 V for V_{DS1} and 684 V for V_{DS2}. This demonstrated a high level of symmetry between the switches and input stages.

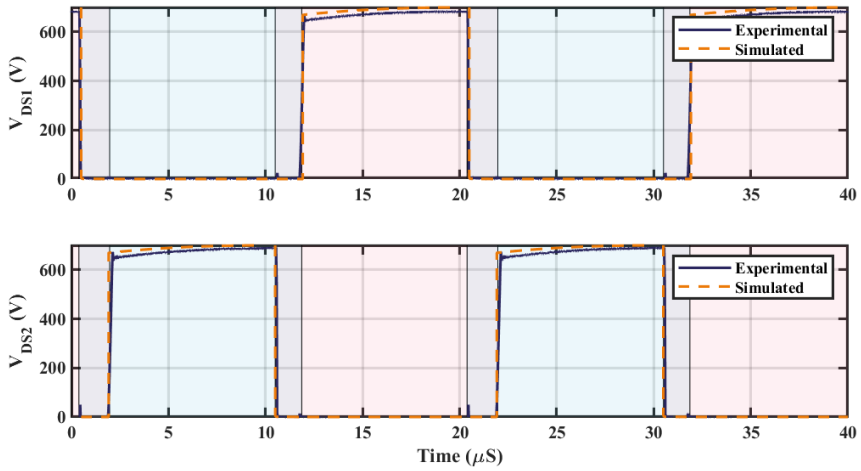

Figure 5.18: Experimental and simulated Drain-Source voltage waveforms of the proposed FWBVLSIMBC topology.

Due to the physical design of the proposed converter, both switches were placed as close as possible to their respective voltage lift switched inductor stage and the shared ground plane; consequently, the experimental Drain-Source current for the individual switching devices could not be feasibly obtained. By utilising Equation 5.17 in addition to the experimental input and output currents, an analytical experimental value of the average Drain-Source currents was calculated as 10.84 A. This value was found to agree with the simulated average Drain-Source current of 11.5 A, outlined in Figure 5.19. As previously explored in Section 4.4.3, the overshoots present in the simulated data are due to the low impedance loop temporarily created during the onset of switch conduction. These current overshoots do not appear experimentally due to inductive elements present in the experimental circuit. However, as the average experimental and simulated currents were consistent, the analytical value was utilised as an approximation for $< I_{DS} >$. With this, it was determined that the simulated Drain-Source currents were suitably similar to the average currents of the proposed experimental converter, to corroborate with the analytical current based on experimental results. Additionally, the simulated findings were suitable to demonstrate switch operation during different operating modes. However, it was not

deemed appropriate to conclude that instantaneous values during switch conduction would be consistent with experimental operations.

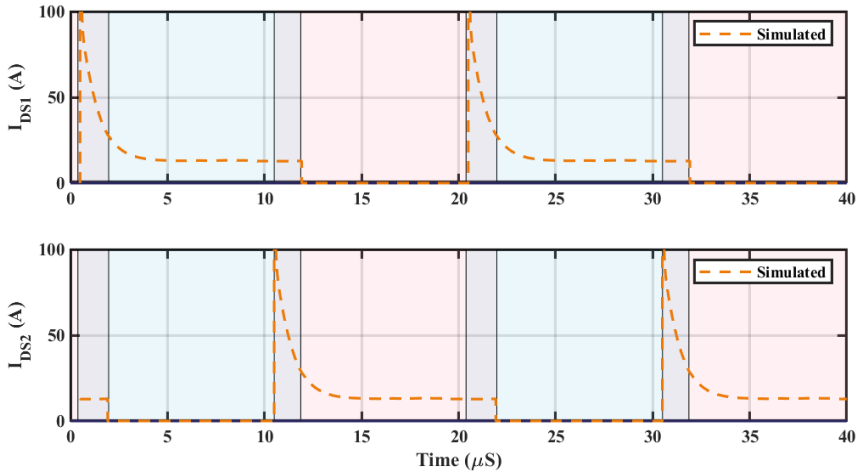

Figure 5.19: Simulated Drain-Source current waveforms of the proposed FWBVLSIMBC topology.

Power Efficiency Analysis

Based on the initial power calculations in Section 5.5.1 and the efficiency calculation described in Equation 3.25, the converter efficiency was calculated as 95.7 %, with 99.85 W dissipated within the converter.

Input Stage Power Losses The DC inductor losses were calculated with Equation 3.26, the individual inductor currents and the R_{esrL} of the inductors, which were 28 mΩ. With this, the total DC losses enabled the calculation of $P_{LDC} = 6.0$ W. With the utilisation of the manufacturer's analysis tool [83], the total power dissipation due to coil windings was found to be 2.7 W. Based on the experimental findings and the manufacturer's information, the combined power dissipation of all input inductors was calculated to be 8.7 W. This accounted for 0.037 % of the total input power. The implementation of the interleaved VLSI stages reduced the current through each inductor, which led to a reduction in conduction losses, compared to the inductor losses observed in Section 3.6.1

When observing the reported manufacturer characteristics of the input diodes switching based power dissipation was assumed to be insignificant in comparison to conduction losses, due to the diodes zero reverse recovery current and typical switching speed below 10 ns [84]. Furthermore, reverse conduction losses were also identified as negligible due to the characterised reverse leakage current, for the observed experimental voltages, being under 10 nA. With this, conduction based power dissipation was determined to be the most significant contributor of power dissipation in an individual input diode. Conductor based power dissipation was calculated based on the forward power loss equation from the manufacturer's data sheet [84], as:

$$P_D = 2(N_L + 1)(R_D < I_{DL}^2 >) \tag{5.27}$$

where R_D is the on-state resistance of the diode and $< I_{DL} >$ the diode current. Equation 4.19 may be modified to account for the interleaved nature of the proposed converter to determine $< I_{DL} >$, such that

$$< I_{DL} >= \frac{< I_{in} >}{2N_L} \tag{5.28}$$

For the experimental input current of 23.23 A, $< I_D >$ was calculated as 3.87 A. Based on this diode current, the forward voltage of the diode was expected to be approximately 1.4 V [84]. To determine R_D, the diode forward current, I_f, was also required, which may simply be determined with

$$I_f = \frac{< I_{DL} >}{D} \tag{5.29}$$

With this I_f was found to be 11.98 A, hence, the forward voltage and the forward curve model sourced from the manufacturer, R_D was calculated to be 59 mΩ [84]. With Equation 5.27, the diode-based losses were calculated to be 21.76 W.

Output Stage Power Losses Based on the same assumptions outlined in Section 5.5.1 and with the utilisation of the capacitive voltage ripple of the FWCW established in Equation 5.3, the capacitive power dissipation for a homogenous output ladder may be determined using:

$$P_C = 3N_C \left(\frac{I_{out}}{4}\right)^2 R_{esrC} \tag{5.30}$$

However, because the first stage possesses 2 capacitors, the power dissipation for the capacitor ladders of the proposed converter may be described using:

$$P_C = 3(N_C + 1) \left(\frac{I_{out}}{4}\right)^2 R_{esrC} \tag{5.31}$$

With this, the output capacitor based power dissipation was calculated to be 0.5 mW and 0.6 mW for the non-inverting and inverting ladders, respectively. The increased dissipation in the inverting ladder was due to the comparatively larger output current observed during experimental characterisation.

As the current behaviours of each output diode, in a full-wave Cockcroft-Walton had not been properly explored, a simplified model based on Equation 3.32 was utilised to calculate output diode based power dissipation. Due to the symmetrical nature and each diode in the output ladder to possess a current equal to half the output, Equation 3.32 was modified to describe the power dissipation of the output diodes for a single capacitor ladder:

$$P_D = 2N_C V_f I_{out} \tag{5.32}$$

Due to the low current of the capacitor ladders, V_f was estimated to be 0.7 V based on the manufacturer's datasheet [84]. Hence, the output diode-based power dissipation was

calculated to be 2.3 W in both the non-inverting and inverting ladder, totalling 4.6 W.

Switch Power Losses By applying Equation 3.16 to both switching devices and summing the results, with the calculated drain source current 10.84 A and MOSFET on resistance 12 mΩ [94], the total switch conduction dissipation was calculated to be 2.8 W. From the data in Figure 5.18, the rise and fall times of both Q1 and Q2 were found to be 153 ns and 31 ns, respectively. These values were larger than those reported in the data sheet by a factor of approximately 10 and 2, respectively [94]. This was likely due to the use of a generalised gate driver, which was used across all the developed converters to maintain consistency. The gate driver used a 7 Ω gate resistance, which was over three times higher than the resistor used in the manufacturer's characterisation. Additionally, a 10 nF gate capacitor was utilised to reduce ringing and false turn-on. Both of these factors lead to a comparative increase in switch rise and fall time, but were deemed essential in minimising potential damage to the switch and ensuring consistency of gate driving between all developed converters.

Due to the difference in initial and final Drain-Source voltages during blocking operation, Equation 3.17 was modified to account for the differences to give:

$$P_S = 0.5 I_{DS} f (V_{DSinit} t_{Rise} + V_{DSmax} t_{Fall}) \tag{5.33}$$

where V_{DSinit} was the initial blocking voltage after turn-on and V_{DSmax} the maximum blocking voltage before turn off. The individual switching losses for Q1 and Q2 were calculated as 32.6 W, and the combination of switch and conduction dissipation resulted in a total switching power dissipation of 68.0 W

Converter Effieicncy Based on the component and operation parameters outlined in Tables 5.3 and 5.4, the total calculated power dissipation was 103.1 W, which was in agreement with the experimental power dissipation of 99.85 W within a 3.5 % margin of error. The data in Figure 5.20 show the power dissipation ratio for each component group within the proposed topology observed during experimental characterisation.

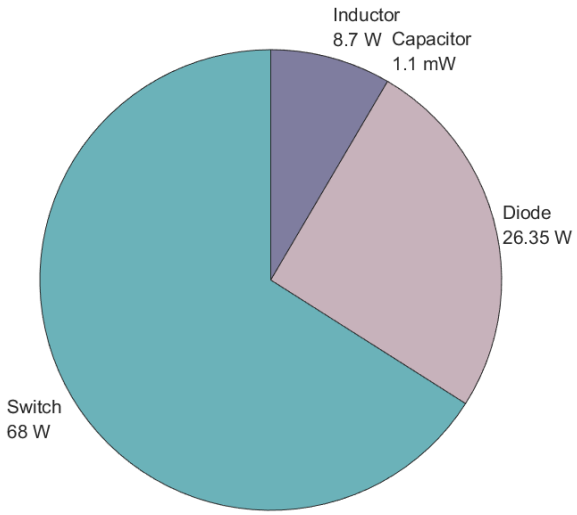

Figure 5.20: Calculated distribution of the 103 W power dissipation within Experimental 2 kW FWBVLSIMBC

As with the power analysis in Chapter 3, the greatest proportion of power dissipation was identified to originate from the switching devices. While higher quality switches were utilised, in comparison to those used in Chapter 3, the need for low R_{DSon} devices was the main focus, which led to the selection of devices with higher gate capacitances. This resulted in the switch conduction dissipation of the proposed converter being similar to that reported for the 1 kW bipolar converter in Section 3.6.3, whilst the switch switching losses were triple those reported in Section 3.6.3. When accounting for differences in input power, the switching device dissipation observed for the proposed converter was 1.5 times greater than that observed in the 1 kW converter proposed in Chapter 3. The primary diode-based power dissipation resulted from the forward voltage drop of the input diodes. While efforts were made to select components with a low V_f, the practical consideration of

cost limited the selection of devices with values below 1.2 V for high currents. To reduce input diode-based power dissipation, higher quality diodes with a lower V_f would be required. Due to the reductions in individual inductor current, resulting from the interleaved design voltage lift switched inductor topology, power dissipation due to the input inductors was relatively low. The selection of inductors with reduced equivalent series resistance, to reduce dissipation, was not feasible due to both cost and restrictions in physical dimensions. An alternative strategy to reduce inductor-based power dissipation would be the introduction of a greater number of voltage lift stages, further reducing the current through an individual inductor; however, this would have a trade-off with an increased number of input diodes that would increase diode-based losses. The dissipation due to the output capacitors was calculated to be less than 1% of the total power dissipation, and was not considered for further optimisation.

Comparison of Other Topologies

The data in Table 5.5 compares the operating characteristics of the proposed design against similar topologies reported within the literature and the previously developed converters.

The proposed FWVLSIMBC combines the high voltage gain equation of the VLSIMBC topology described in Chapter 4, with the bipolarity of the MBC topology proposed in Chapter 3. As a result of this combination, a comparatively lower efficiency was reported in relation to the previously proposed converters, but greater than both high-gain and bipolar topologies presented in the literature.

5.5.2 Variable Duty Ratio, Variable Input

To examine the potential of the proposed converter to step up a range of rectified low voltage wave energy converter sources into 4.7 kV_{DC}, the input was varied across a range

Table 5.5: Comparison of the proposed FWBVLSIMBC converter with other topologies reported in the literature

Topology	Voltage Gain	Efficiency (%)	Test Power (W)
Bipolar Cuk-SEPIC [85]	$\pm\frac{D}{1-D}$	92	4000
Bipolar Interleaved Boost-Sepic [87]	$\pm\frac{1}{1-D}$	92	200
Interleaved Cascade [38]	$\frac{4+2n+2nD_2}{(1-D_1)(1-D_2)}$ *	95.5	500
Interleaved Coupled Inductors [60]	$\frac{4+2nK}{1-D}$ *	94.2	500
Bipolar MBC	$\pm\frac{N_C}{1-D}$	98	1000
VLSIMBC	$\frac{N_C N_L}{1-D}$	97.5	1000
FWVLSIMBC	$\pm\frac{N_C N_L}{1-D}$	95.7	2000

* n is the number of turns in a coupled inductor, K the coupling coefficient

of low voltages and the duty ratio adjusted to meet a target output voltage. The data in Figure 5.21 outlines the analytical range of operation based on Equation 5.22, the required duty ratio to achieve 4.7 kV_{DC}, and limitations of the input power supply.

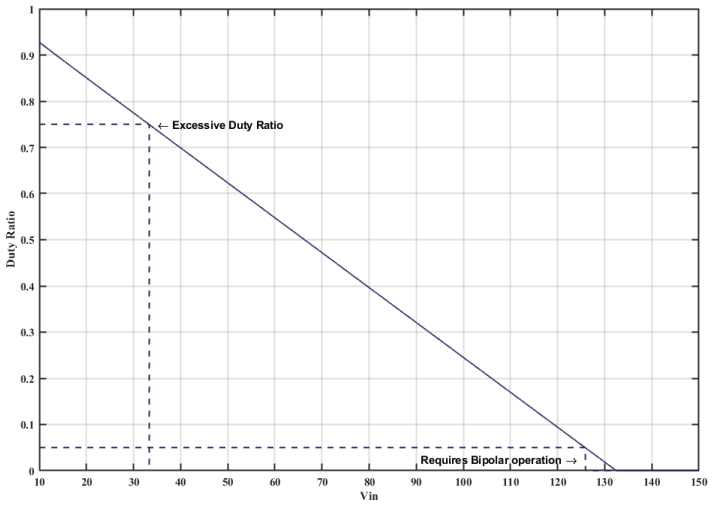

Figure 5.21: Analytical parameters of the proposed topology to achieve 4.7 kV_{DC} during unipolar operation at 1 kW.

The limitations of the proposed topology were based on the upper limit of the duty ratio discussed in Section 5.4.3 and an estimation for safe Mode 4 operation based on the reasoning in Section 5.4.4. This range was identified as 20 - 75 %; however, to reduce the risk of topology damage. This offered an operational duty ratio range of 20 - 70 %, which allowed for a voltage test range of 40 - 120 V for unipolar operation and 70 - 200 V for bipolar operation. The complete voltage conversion range of the FWBVLSIMBC was highlighted in Figure 5.22

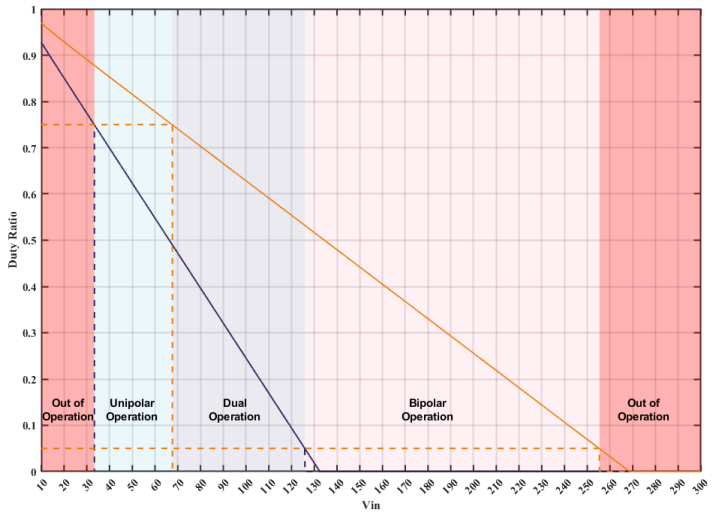

Figure 5.22: Operational range of the proposed FWBVLSIMBC topology with target output voltage of 4.7 kV_{DC}.

When considering bipolar operation and a 5 % safety margin, the effective voltage range for the highest stage output became 40 - 200 V. This could have been further extended with the utilisation of lower stage outputs in the capacitor ladder; however, for the purposes of demonstration, only the sixth stage outputs were considered. An overlap in viable operation occurs between 67 - 125 V, where both modes of operation are potentially viable. To demonstrate the capability of the proposed converters to convert a range of LVDC voltages into a stable MVDC output, as well as to determine the benefits of each mode in the range, both were viable. 2 DC sweeps were conducted with the duty ratio

adjusted to maintain an output voltage of 4.7 kV_{DC}. Table A.1 outlines the operating parameters used in the unipolar and bipolar DC sweep experiments.

Table 5.6: Experimental parameters for the variable duty ratio, variable input study of the FWBVLSIMBC

Parameters	Value
V_{in} Unipolar	40 - 125 V
V_{in} Bipolar	70 - 200 V
Target V_{out}	4700 V
R_{out} Unipolar	22 kΩ
R_{out} Bipolar	44 kΩ
f	50 kHz
D	0.2 - 0.7

To achieve the target output voltage for the range of input voltages studied, the operation of the converter was changed from bipolar, with the common ground as the reference point, to unipolar with the negative output as the reference point, functionally doubling the output voltage. The data in Figure 5.23 outlines the experimental and simulated duty ratios utilised to achieve a 4.7 kV output voltage for a given input voltage.

When considering unipolar operation, the change in duty ratio required between both experimental, simulated and analytical voltages was relatively consistent for input voltages between 45 - 110 V. Deviations of experimental duty ratio to simulated and analytical duty ratios became apparent above this voltage range. Furthermore, the experimental unipolar duty ratio required to achieve 4.7 kV was consistently 0.2 greater than both the simulated and analytical duty ratio. This was likely due in part to the capacitive based voltage

losses not being fully modelled for unipolar operation in Equation 5.22, leading to an underestimation in duty ratio requirement. This shift difference was not observed for the bipolar bipolar test, this demonstrated the suitability of the FWBVLSIMBC for a broad range of input voltage operations.

When bipolar operation was observed, the experimental, analytical and simulated results were almost exactly equal for all input voltages tested, which demonstrated strong agreement between the analytical, simulation and physical models of the converter, during bipolar operation mode.

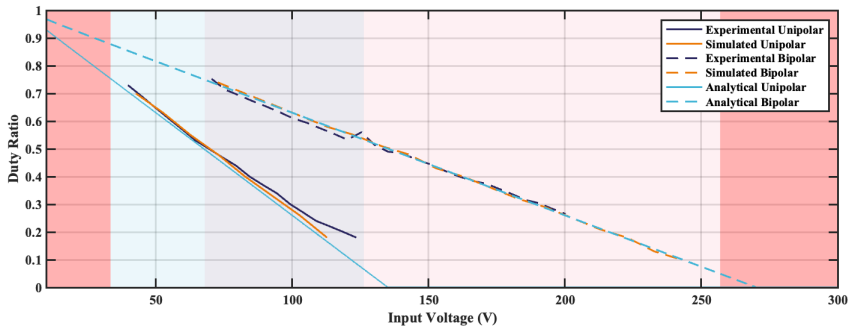

Figure 5.23: Duty ratio required to achieve an output of 4.7 kV_{DC} in the proposed FWBVLSIMBC topology operating at 1 kW.

The deviations of unipolar gain requirement were suspected to be due to increased losses at lower duty ratios; as such, the power efficiencies at each input voltage were calculated to examine performance and potential cause for duty ratio deviations. The data in Figure 5.24 show differences in unipolar efficiency for input voltages above 70 V up to 4.3 %. Furthermore, similar efficiency deviations were observed for input voltages below 50 V. This was likely due to the proportion of voltage loss from the input diode forward voltage being greater at lower input voltages. This, in turn, led to increased power losses within the converter.

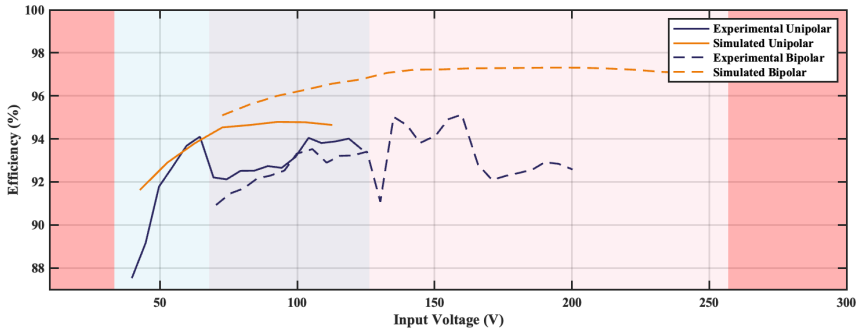

Figure 5.24: Efficiency for a given input voltage with an output of 4.7 kV_{DC} in the proposed FWBVLSIMBC topology operating at 1 kW.

It was also observed that the experimental bipolar efficiency was consistently lower than the simulated bipolar efficiency and, the operational efficiency at an input voltage of 100 V was 2 % lower than the reported efficiency during 2 kW experimental testing. This was expected to be due to the order of testing and the impact of Mode 4 operation. During experimentation, the unipolar sweep was first conducted, where over half the input voltages utilised Mode 4 operation. As outlined in Figure 5.25, the input ripple coincides with the description offered in Section 5.4.4, with rapid reductions in current demand, after the transition into Mode 4, leading to high $\frac{dI}{dt}$, which in turn resulted in a transient input voltage up to $2V_{in}$. This, in turn, led to unanticipated large voltages across on electrical components within the converter. Furthermore, it can be observed that the transitions between Modes 1 & 2 to Mode 4 possess a current ripple approximately 3 times greater than that outlined in Section 5.4.4, which increases at lower duty ratios (see Appendix C). This behaviour was suspected to be due to the reduced time during which the converter was receiving energy from the power supply. As the proportion of Modes 1 & 2 operation, over a complete switching period, decreased with the reduction in duty ratio, an increase in current was observed to maintain the energy requirement for constant 1 kW operation.

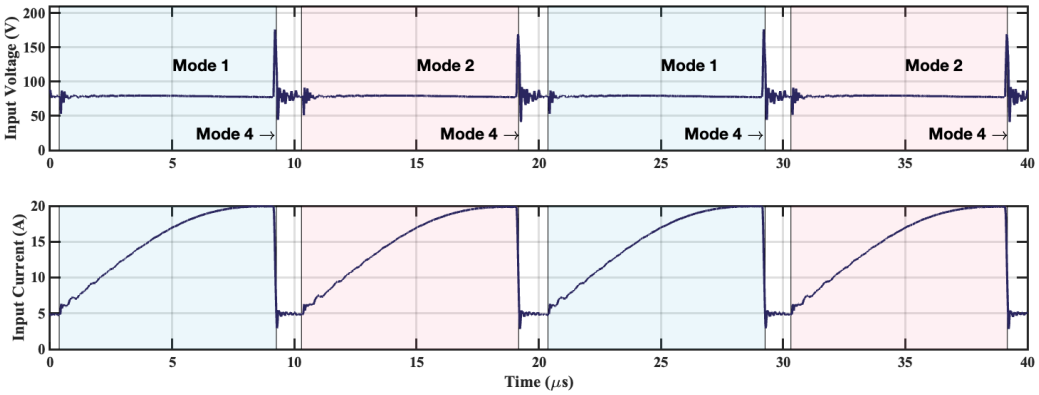

Figure 5.25: Input Current ripple the proposed FWBVLSIMBC topology, with an input of 80 V and Output of 4.7 kV_{DC}.

This repeated use of Mode 4 was expected to have caused degradation to the components within the prototype, reducing performance. Hence, when bipolar operation was examined, experimental efficiencies were lower than expected due to the degraded components. However, operational behaviour was validated through the data shown in Figure 5.23.

The voltage sweep demonstrated the potential of the converter to achieve the target voltage conversion ratios in both unipolar and bipolar operation. The reduced efficiency during the final test of bipolar operation demonstrated the potential risk to reliability associated with Mode 4 operation; as such, further work into improving device reliability would be highly beneficial in demonstrating the feasibility of ultra-high gain DC-DC converters

A potential solution to achieve a larger input voltage range would be the exploration of a multi-stage output of the switched capacitor ladder. By connecting the output to lower stages of the ladder, the voltage conversion ratio may be reduced without lowering the duty ratio, offering a strategy to minimise the use of Mode 4 operation. Furthermore, additional interleaving stages may be achievable to reduce input conduction losses and reduce the duty ratio threshold into Mode 4, allowing for the use of lower duty ratios

without the risk to reliability, from the high $\frac{dI}{dt}$ from Mode 4 transition.

5.6 Chapter Summary of Ultra-High Gain Bipolar DC-DC Converter

5.6.1 Experimental Method to Achieve Anti-Phase Switching

To achieve anti-phase PWM operation 2 single output, Tektronix AFG 31000 series arbitrary function generators were utilised. The function generators possessed a built-in synchronisation function, allowing for a consistent triggering operation. To achieve anti-phase, a trigger delay of 10 μs was set. Due to inconsistencies in the devices, an inherent trigger delay ranging from 200 ns $-$ 400 ns occurred during start-up, which required calibration to properly achieve the set trigger delay. While adjusting the delay was relatively simple, the inconsistent delay prevented consistent anti-phase from being achieved between tests, thus leading to minor variations, approximately $<$ 50 ns in switch operation. When the data was compared against the initial V_{GS} operation outlined in Figure 5.5, it was observed that there were no sufficiently large deviations which could have affected the experimental findings. Therefore, while this likely had little impact on voltage output and power efficiency, this methodology may have introduced small variations in voltage ripple between experimental characterisations.

5.6.2 Low to Medium Voltage Conversion Applications

The motivation of this work was to design a device capable of increasing the low voltage of wave energy converters into a medium voltage that could integrate into offshore wind farm electrical infrastructure via the isolated power converters which, step up offshore wind turbines into an inter array voltage. The proposed topology has demonstrated the

ability to produce a stable MVDC output, from a range of low voltage inputs, which could then be inverted into 3.3 kV_{AC}, the specified voltage for electrical integration. Although the initial motivation was to facilitate conversion for low voltage wave energy converters, the demonstrated voltage range would also facilitate conversion for industrial, 48 V, PV solar farms, offering an additional application oppotunity for the proposed design, beyond the initial scope of the project.

5.6.3 Conclusion

This chapter demonstrated a novel DC-DC converter topology that conceptually combines the topologies presented in Chapters 3 & 4. The design demonstrated a bipolar voltage conversion ratio double what was considered ultra-high in the literature. Furthermore, the presented topology demonstrated the capability of continuously converting a wide range of low voltage inputs into a medium voltage output while only requiring 2 active switching devices. New analysis was developed based on the previous chapters to effectively describe the operation of the proposed topologies. Following this, a demonstrator unit was presented to experimentally validate both operation and analysis, demonstrated a 95.7 % power efficiency. For steady-state operation, the simulated and experimental results both support the analysis presented in Sections 5.3 and 5.4. A subsequent power loss analysis identified that the reductions in power dissipation could be achieved by prioritising devices which are optimised for the minimisation of switching losses rather than conduction losses.

To demonstrate the capability of the designed converter to achieve LVDC to MVDC conversion, the FWBVLSIMBC was set to maintain a constant output voltage of 4.7 kV_{DC} for a range of low voltage inputs. It was determined that, during 1 kW operation, the proposed topology could maintain the target MVDC output, for an input voltage range of 40 - 200 V, which demonstrated a voltage conversion range of 24 - 118, which encompassed

90 % of the target voltage range of 20 - 124. Strategies to increase this range to achieve the full target specification include connecting to lower output stages during operation, to achieve lower voltage conversion ratios, and further expanding the scalable submodules of the FWBVLSIMBC to achieve greater conversion ratios.

When reflecting upon the project aim, the learnings from the previous chapters have been integrated and allowed for the development of a non-isolated DC-DC converter capable of achieving the target output voltage for a range of low voltage inputs, meeting the objective of this project. During the experimental demonstration, an operating efficiency of 91 % was maintained for input values between 50 V and 200 V. Future developments to this converter should include exploration of power loss reduction techniques to achieve greater operating efficiencies across a range of input values, as well as the development of a higher power design which could operate at the operating power of commercial generation. The proposed converter offered a novel demonstration of the potential of non-isolated DC-DC for low-to-medium voltage conversion applications as an alternative to conventional, transformer-based, power converters.

CHAPTER 6

Conclusions and Further Research

6.1 Conclusion

With the rise in renewable generation technologies comes the opportunity to explore multi-use renewable power stations. The motivation of which is to optimise marine spatial use and reduce infrastructure costs. This comes with the challenge of developing solutions which allow for low voltage sources to be integrated into existing medium voltage infrastructure and the opportunity to explore non-conventional power conversion strategies to avoid the need for step-up transformers at the point of generation. This project sought to explore a potential strategy of integrating low-voltage renewable generators into medium-voltage collection networks present in offshore wind farms. The greatest challenge identified was the voltage conversion ratio required in a transformerless DC-DC step-up stage to convert low-voltage inputs into medium-voltage outputs. From this, different high voltage conversion ratio DC-DC converter topologies were explored, with a focus on power

efficiency, bipolarity and scalability. A family of switched-capacitor-based boost converters were developed and demonstrated. Firstly, the novel continuous operation of a high efficiency, single switch bipolar boost converter capable of a scalable high voltage conversion ratio, single switch initially realised as a foundation for further voltage conversion ratio developments, while demonstrating an operation of the topology which had not been previously observed in the literature. The converter demonstrated a voltage conversion ratio of ±10 at 1 kW with an efficiency of 98.2 %. Following this, a novel way to scale the voltage lift-switched inductor topology was explored in combination with an initial scalable design. With this, an ultra-high voltage conversion ratio unipolar design was developed, which demonstrated a voltage conversion ratio of 41 at 1 kW with an efficiency of 97.5 %. This ultra-high voltage conversion ratio of the converter showed a significant development in voltage conversion capabilities compared to other non-isolated DC-DC converters reported in the literature. Finally, a novel ultra-high voltage conversion ratio converter, which combined the innovative aspects of the previous designs, was realised. The final converter capable of stepping up a 40 V to 125 V input to a continuous 4.7 kV output, and 70 V to 200 V to a continuous ±4.7 kV output for 1 kW operation with an experimental efficiency range of 87.5 % - 95.0 %. This design was built upon the novel demonstration of continuous bipolar high voltage conversion, with the significant development in ultra-high conversion capabilities to achieve bipolar ultra-high voltage conversion ratios for a range of low voltage inputs. This, in turn, demonstrated the potential of DC-DC converters for ultra-high voltage conversion applications.

6.2 Future Research

The following sections consider areas for further development and exploration based on the findings from this project, the proposed field of application and relevant literature.

6.2.1 Implementation into Solid-State Transformer

This project initially explored the potential of DC-DC converters in low to medium voltage conversion as a means of a transformerless step-up stage in a solid-state transformer (SST). With the project aim of demonstrating that this converter has been achieved, the next logical step would be to explore the implementation of such technology in a low voltage AC to medium voltage AC SST. Figure 6.1 illustrates the expected block diagram of a solid-state transformer with the presented DC-DC link stage that was initially outlined in Chapter 1.

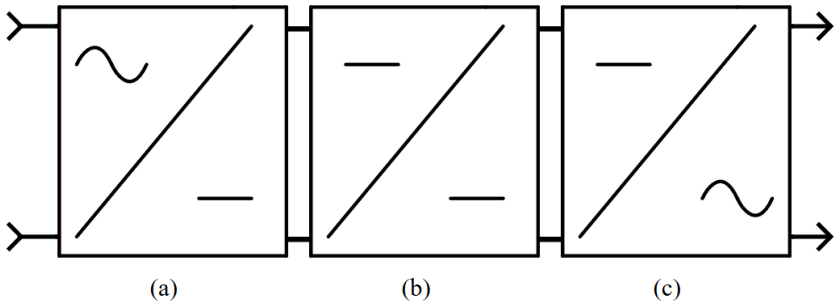

Figure 6.1: Block diagram of a potential use of proposed DC-DC in a SST where: (a) Is a low voltage rectifier (b) Is the proposed DC-DC converter, and (c) Is a medium voltage inverter.

A simple yet robust rectification topology is the passive full-wave rectifier [20] with a large DC link capacitor, both smoothing voltage ripples and operating as the input capacitor outlined in Chapter 4 and briefly discussed in Chapter 5. Alternatively, to account for changes in power factor and maximise extraction, active rectifiers may be preferable [21].

Due to the medium voltage output any inversion circuit would either be an already established, IGBT based, design such as the 3-phase inverter, or a design capable of voltage sharing across switching elements to facilitate the use of MOSFETs. Additionally, without the use of a step up transformer, some form of signal filtering circuit, such as an LCL filter, would also be required to achieve a medium voltage AC output with low

harmonic distortion [22].

6.2.2 Bidirectionality

An additional use case for DC-DC converters is in the integration of energy storage systems into power networks [32–35]. The high voltage conversion ratio converter designs offer the potential to integrate low voltage electrical storage solutions into medium voltage networks. However, in this application, an integration device is required to both extract and deliver energy into the storage device, requiring the DC-DC converter to be capable of bidirectional power flow. The key aspects of this would include the consideration of bidirectional bipolar Cockcroft-Walton multipliers and bipolar voltage lift switched inductor designs.

Some work has already explored bidirectional unipolar Cockcroft-Walton multipliers [36, 95], and exchanged the output diodes for switching devices, which allowed for direct control of the ladder switch operation. This modification, gave opportunity for bidirectional operation. However, the experimental designs demonstrated comparatively lower operating efficiency (approx 94 %) compared to the closest equivalent design demonstrated in Chapter 3. Therefore, further work to explore the power losses associated with bidirectional functionality would be required to ensure acceptable power efficiency operation within Cockcroft-Walton multipliers.

As of writing, no literature could be found exploring bidirectional voltage lift switched designs; however, bidirectional switched inductor designs have been reported [36, 64]. These switched inductor designs require two switching devices and scale in series, rather than the parallel scaled designs presented in Chapters 3, 4 & 5. Shown in Figure 6.2 one inductor is placed in the same manner as that in Chapter 3, and the other on the return path, which allows for parallel charge and series discharge, for a 2-stage design. Multiple

2-stage switched inductor topologies operate in series to achieve scalable voltage multiplication. Further research into associated loss functions and input current ripples would be required to establish the potential of this topology.

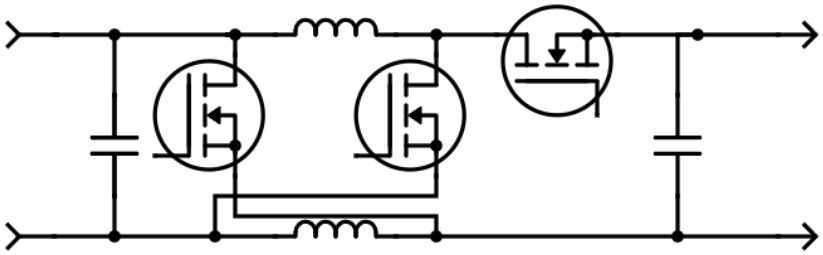

Figure 6.2: Circuit diagram of a bidirectional switched inductor boost converter

6.2.3 Upscaling Power Output

Some of the smallest current commercial wave energy converters operate at 15 kW [96], the highest demonstrated operating power of the proposed converter was 2 kW. This is 13 % of the smallest commercial design; therefore, to demonstrate viability in wave energy converters applications, further work aimed at increasing operating capacity while maintaining power efficiency would be required. Furthermore, all practical voltage voltage conversion ratio equations possessed a loss function proportional to output current. Therefore, as operating power increases, output voltage decreases, this factor would also require consideration to maintain the desired output voltages. One solution to this challenge would be to to increase the size of the output capacitors proportionally to the increase in output current. This would limit the loss function of the voltage conversion ratio Equations 5.21 and 5.22, at the trade-off of physically larger and higher cost capacitors. This would allow the target voltage to be reached at higher operating powers; however, the interleaved MOSFETs would then become the limiting factor due to the larger operating current. An alternative solution could be to parallelise stages within the converter to reduce the operating current of individual components, as shown in Figure 6.3.

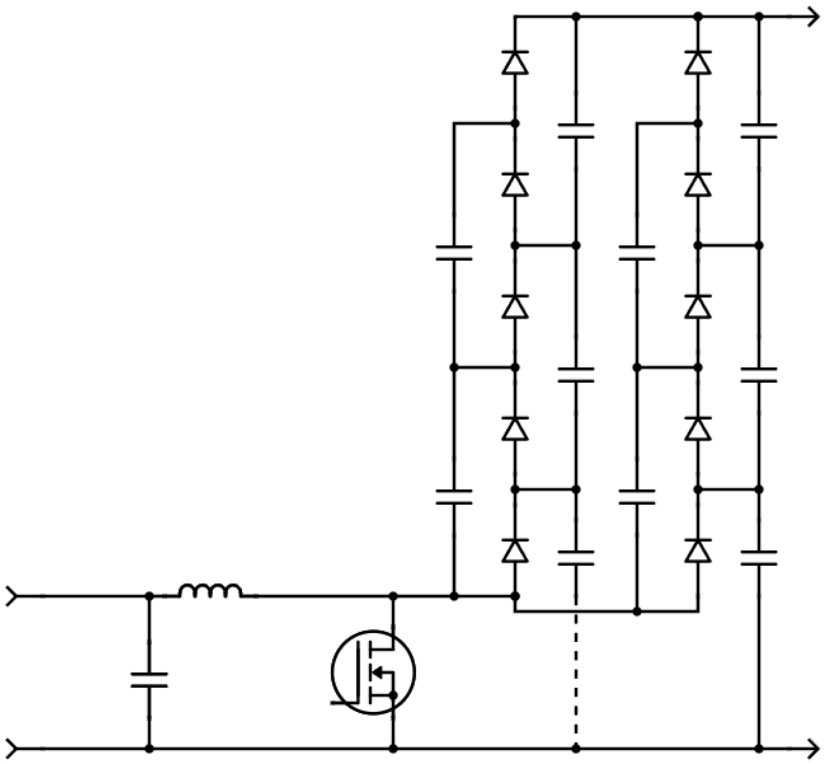

Figure 6.3: Circuit diagram of a 3-stage Cockcroft-Walton boost converter with parallel output stages

This potential has been identified [97], exchanging increased component usage for upscaled operating powers. However, considerations of voltage balancing, changes in operating characteristics and potential failure mechanisms would need to be explored for this alternate solution.

6.2.4 Alternative Applications

While the primary research focus was the integration of wind and wave technologies, the findings of this work may be utilised in alternative applications. As similar voltage conversion ratios to those demonstrated in this work are required for the integration of photovoltaic solar panels to the distribution network [98], maximum power point tracking control techniques could be explored and implemented to demonstrate the feasibility of the converter for photovoltaic solar panel applications. The low switch count and high

voltage conversion ratios demonstrated would offer an efficient DC-DC converter topology with simple control requirements for microgrid applications [99]. As this application requires designs to operate at powers greater than those experimentally demonstrated in this work, the proposed topology would likely require some form of high-power validation for this application. Due to the consistent agreement between simulated and experimental results, an initial validation of high power operation could be achieved based on simulated high power operation, before committing to costly experimental demonstrators. The final topology utilises 2 scalable components, allowing for output voltages beyond those demonstrated in this work. With this and the low to medium voltage conversion demonstrated, the proposed topology may be modified for pulsed power applications, which require repetitive high voltage pulses from low voltage inputs [100]. A competitive benefit would be the solid-state nature of the design, allowing for a power-dense solution that is independent of gaseous or liquid-based components.

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A Experimental Setups

Table A.1: Experimental Measurement Equipment List

Equipment	Model	Range
Oscilioscope	Tektronix MSO58B	
Low Voltage Probe	Tektronix THDP0200	1.5 kV
High Voltage Probe	Tektronix P6015A	20 kV
Current Probe	Tektronix TCP0030A	30 A

During testing, the scale of the oscilloscope was set in a manner such that the maximum readable voltage on the scope was approximately equal to the maximum voltage/current of a given waveform. This resulted in an approximate scale of

$$Scale = \frac{2^{n_b-1} - 1}{X_{max}} \tag{.1.1}$$

where n_b is the number of bits used by the oscilloscope analogue to digital converter and X_{max} the maximum value observed in a given waveform. The Tektronix MSO58B utilises a 12-bit analogue to digital converter, which offers a scale accuracy of $\frac{2047}{X_{max}}$.

The following images are photos of the experimental prototypes and set up described in Chapters 3, 4 and 5.

Figure A.1: Experimental set-up utilised for converter characterisations.

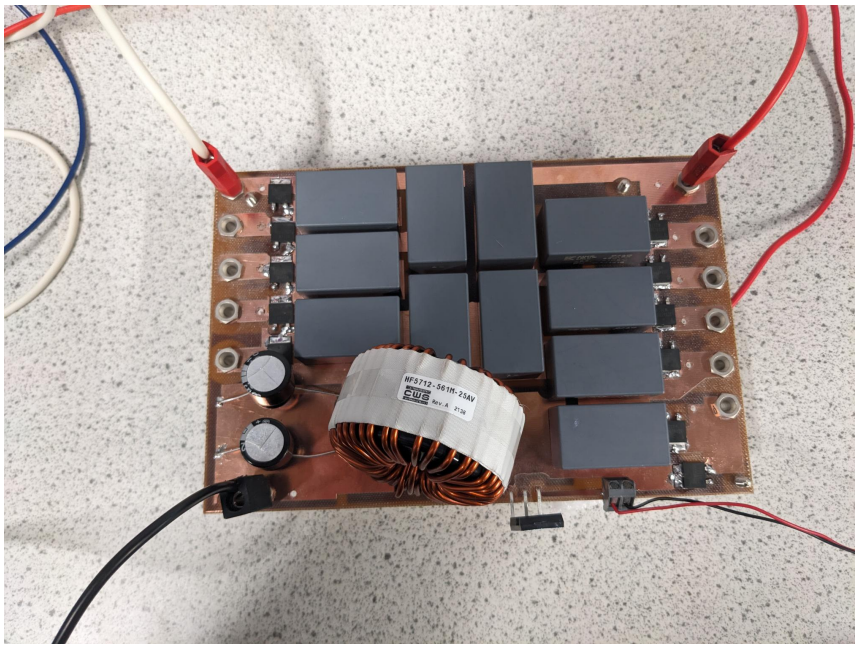

Figure A.2: Experimental prototype of the bipolar multi-level boost converter

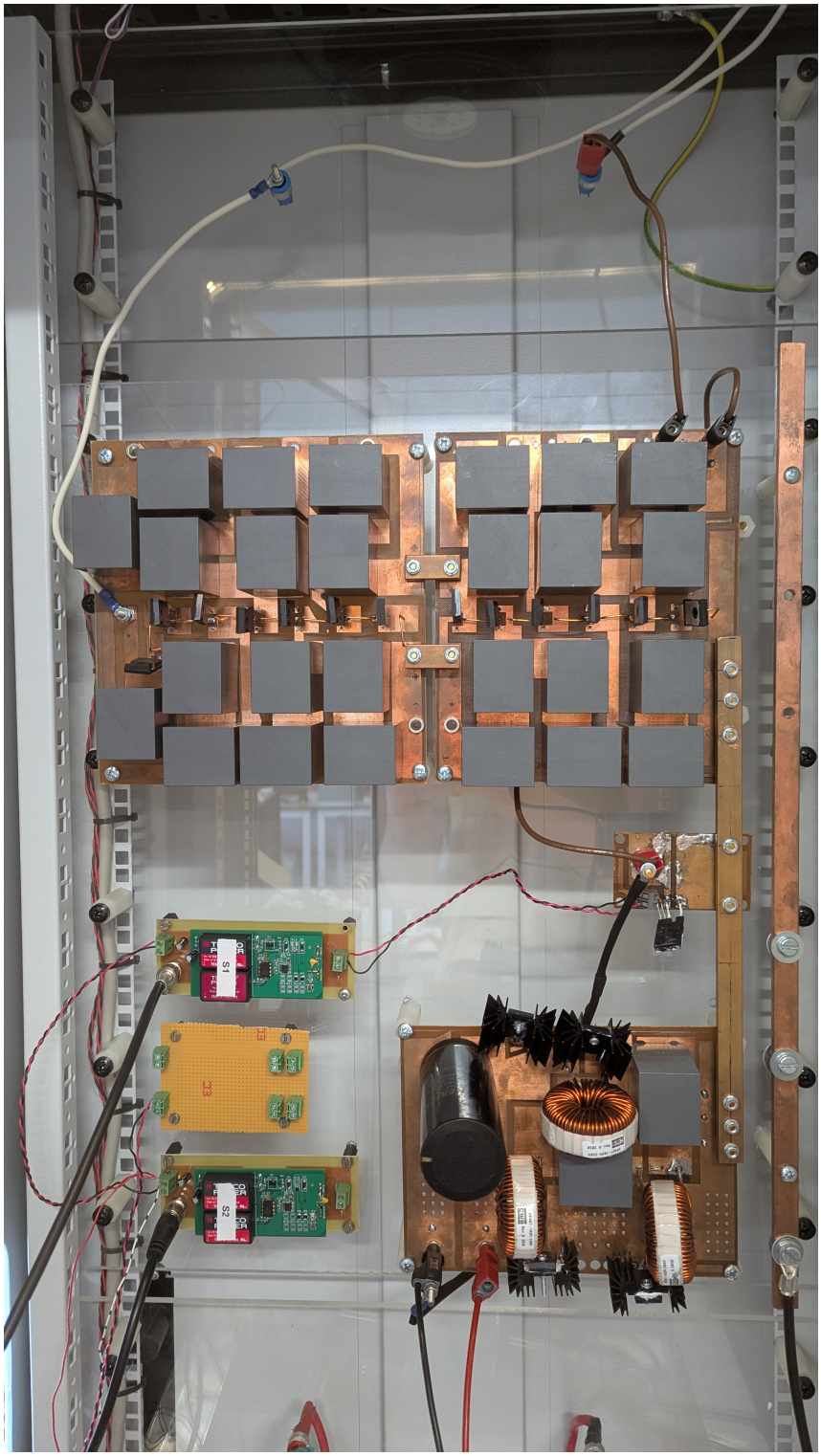

Figure A.3: Experimental prototype of the VLSIMBC-HC converter

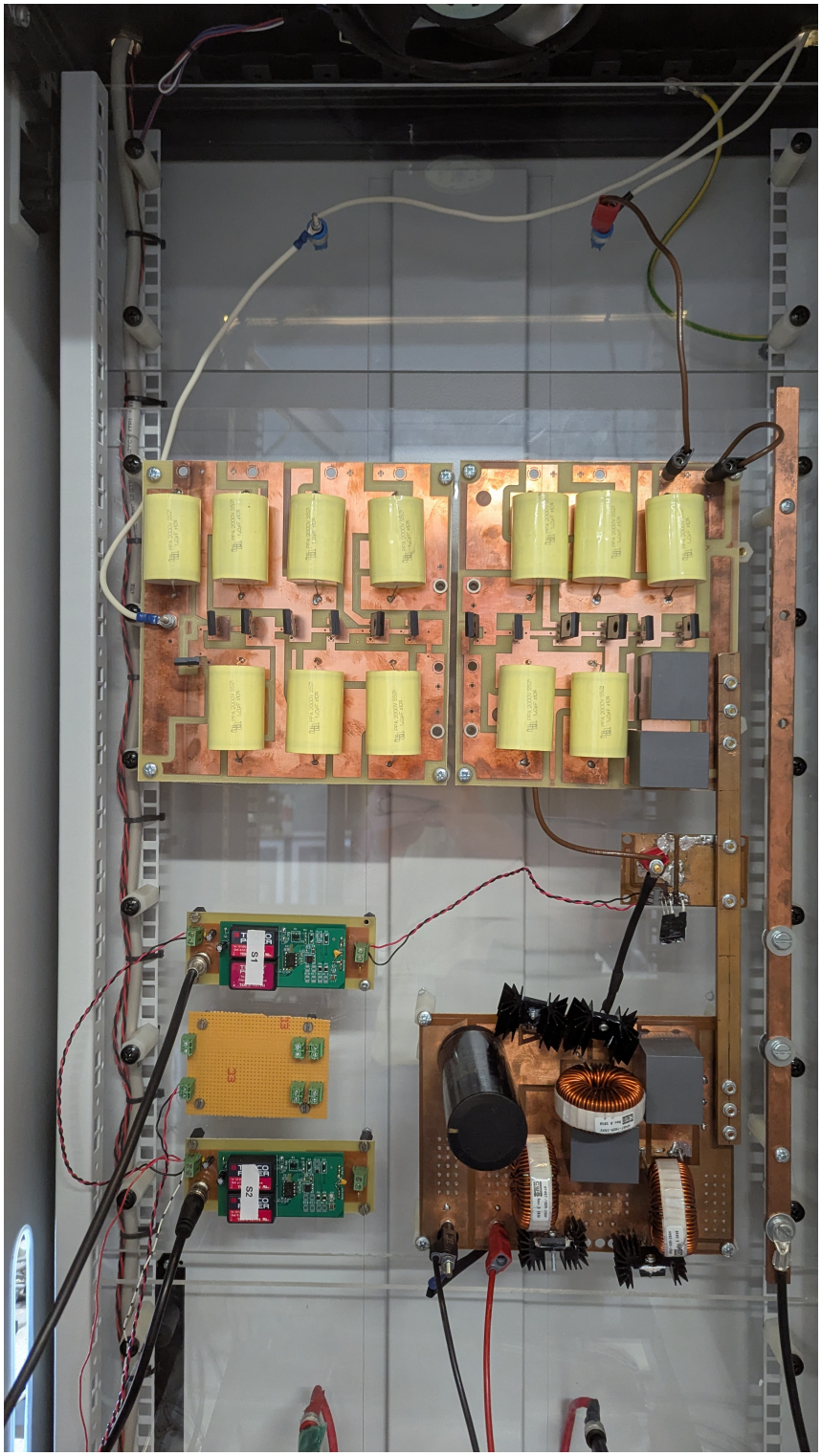

Figure A.4: Experimental prototype of the VLSIMBC-LC converter

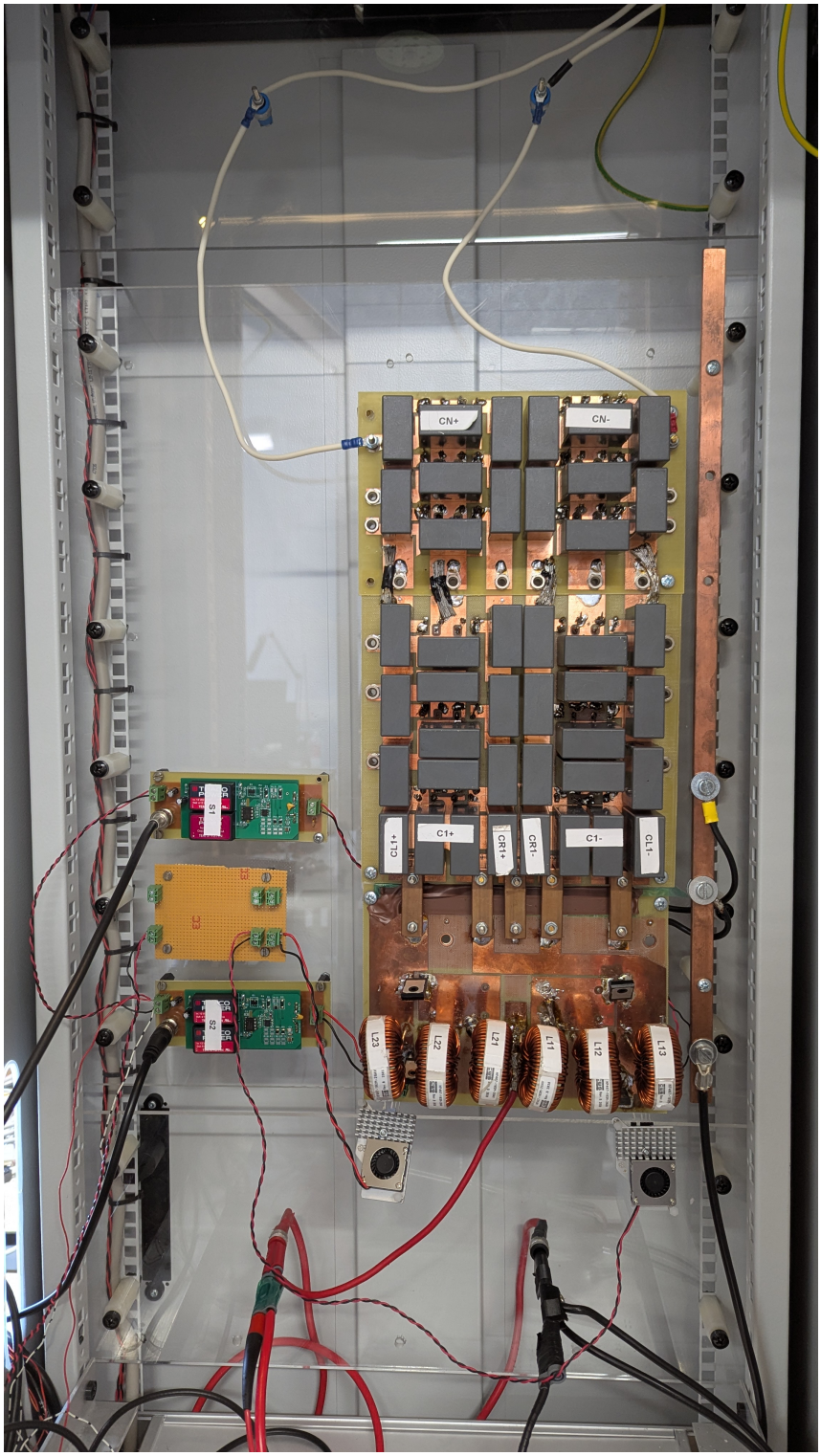

Figure A.5: Experimental prototype of the FWBVLSIMBC converter

B Low Capacitance Bipolar Experiment

The following figures were obtained from a follow-up experiment utilising a similar prototype to that outlined in Chapter 3. The output capacitors were reduced to 2.2μF, and operational efficiency against duty ratio was obtained.

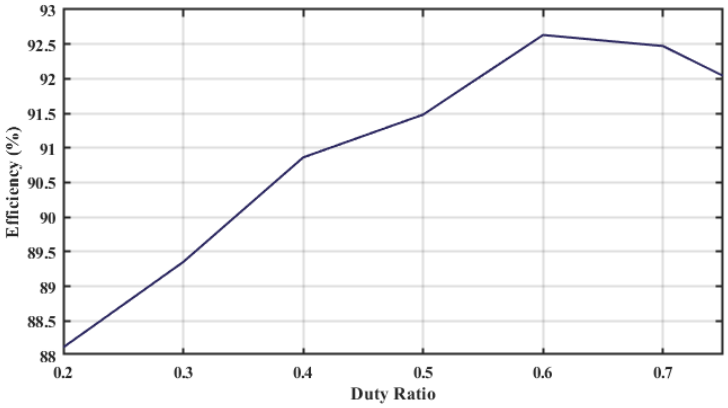

Figure B.1: Experimental efficiency against duty ratio for a 2.2 μF bipolar multilevel boost converter operating at 50 kHz

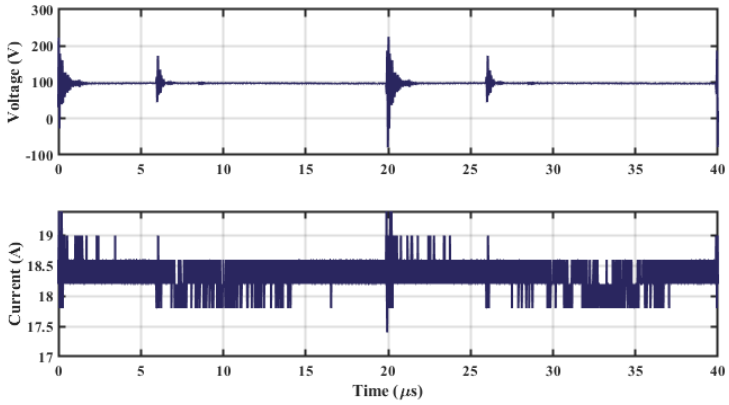

Figure B.2: Experimental input voltage and current waveforms for a 2.2μ F bipolar multilevel boost converter operating at 50 kHz

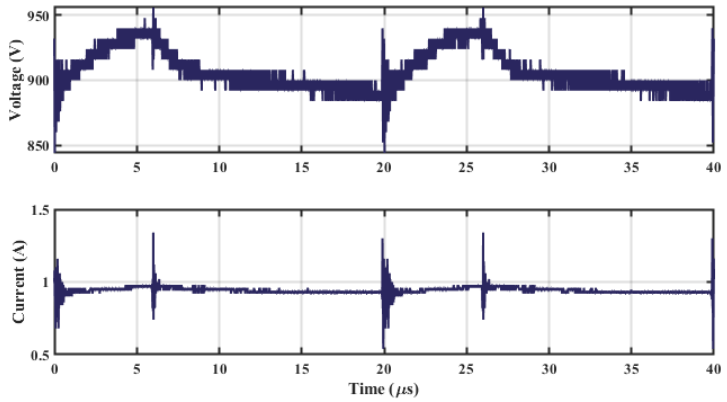

Figure B.3: Experimental non-inverting output voltage and current waveforms for a 2.2 μF bipolar multilevel boost converter operating at 50 kHz

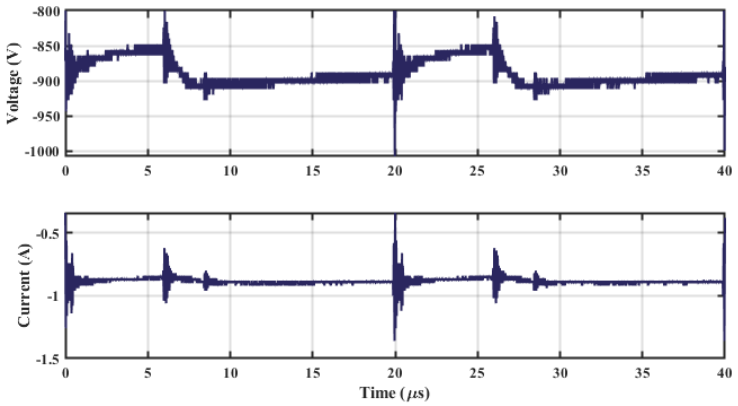

Figure B.4: Experimental inverting output voltage and current waveforms for a 2.2 μF bipolar multilevel boost converter operating at 50 kHz

C FWBVLSIMBC Unipolar DC Sweep Inputs

The data in the following images show the input voltage and current waveforms obtained during unipolar operation of the variable duty ratio, variable input test, at 25 V intervals.

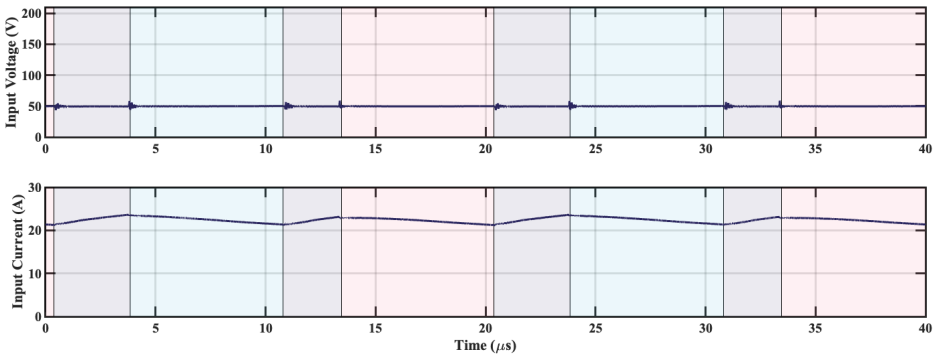

Figure C.1: Experimental input voltage and current waveform of FWBVLSIMBC variable duty ratio, variable input test where $V_{in} = 50$ V

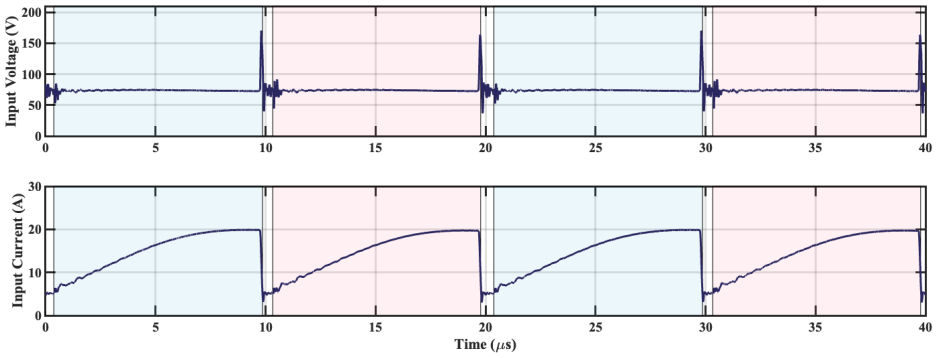

Figure C.2: Experimental input voltage and current waveform of FWBVLSIMBC variable duty ratio, variable input test where $V_{in} = 75$ V

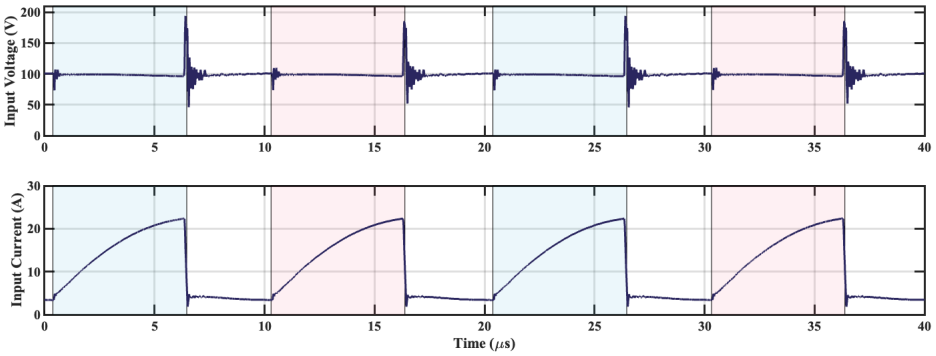

Figure C.3: Experimental input voltage and current waveform of FWBVLSIMBC variable duty ratio, variable input test where $V_{in} = 100$ V

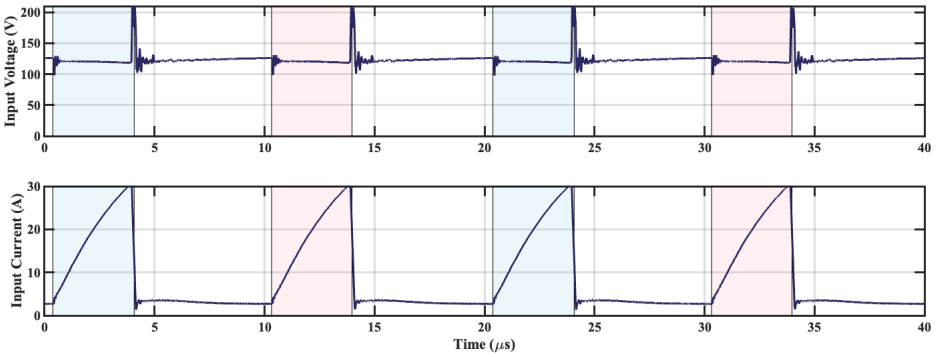

Figure C.4: Experimental input voltage and current waveform of FWBVLSIMBC variable duty ratio, variable input test where $V_{in} = 125$ V