Mitigation of Single Event Burnout for Future Aerospace Applications

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Abstract

With the global challenge to achieve Net Zero, the balance between greenhouse gasses produced and removed from the atmosphere, by 2050, aviation, a major contributor to the generation of greenhouse gas emissions, producing over 900 million tonnes of CO_2 emissions annually, is committed to a step change in propulsion technology. The most realistic strategy to achieve these drastic CO_2 reductions is through the electrification of aircraft, which will utilise the all-electric and hybrid power systems. The realisation of these MW scale power systems will inevitably rely on the incorporation of wide bandgap semiconductors, such as SiC - a semiconductor with excellent material properties, including critical electric field strength, high thermal conductivity and high electron saturation drift velocity. To make this goal a reality, the superior properties of SiC are required - through offering the ability to operate at power levels significantly beyond those of traditional Si. However, at the current time, knowledge of the interaction of radiation from cosmic rays with SiC power electronic devices is unknown, limiting their adoption in flight critical aerospace applications.

The increasing supply voltages required to make the future of flight a reality will generate extremely high electric fields within devices. Coupled with the elevated concentration of cosmic rays at flight altitudes, these conditions create the perfect storm for the Single Event Effect (SEE) - the instantaneous alteration of device response to radiation interaction. The destructive form of the SEE is the Single Event Burnout (SEB), which results in the catastrophic failure of a device, with often explosive consequences. SiC is rapidly becoming the semiconductor of choice to enable circuits to operate with high supply voltages. However, the response of SiC power devices during operation to radiation is unknown. In this research it is shown that SiC, in comparison to Si, offers a 60% reduction in cosmic ray sensitivity when equivalent voltage ratings are considered. It has been found that Si fails when a deposited charge equivalent to 0.2% that of a silver ion commonly used in SEB testing. In contrast the radiation response of SiC is superior, with no failures occurring for any deposited charge up to three times greater than those used in testing for any bias derating up to 99% of the breakdown voltage. Here the data show that SiC is robust against aerospace specific operating conditions and has the potential to replace Si as the material of choice for high reliability aerospace applications. The suitability of 2D SiC structures for aerospace, however, remains unclear.

For future aerospace applications the SiC JFET is the device of choice for use in power systems and flight control surfaces. With strong electrical performance and minimal response to total dose effects it seems to be the ideal candidate, however, questions still exist with regards to its single event response. For the first time the SEB sensitivity of a JFET designed for real world aerospace specific scenarios has been examined. The 2D nature of the device results in increased SEB sensitivity with elevated electric fields at the gate and source - leading to catastrophic failure and device melting at drain - source bias deratings as low as 40%. To mitigate this the separation between the gate and source has been increased - leading to radiation hardened designs which reduce the SEB sensitivity. By increasing the gate - source separation of the original JFET by 4.0 μm a peak electric field reduction of 64% is observed which had resulted in a 99% reduction in peak drain - source current density of the radiation hardened structure in comparison to that of the original. Despite these modifications, high peak temperatures existed for the SiC JFETs studied, with even the modified device reaching over 1500 K after heavy ion impact. A bespoke SiC JFET with an additional channel was investigated as a potential device to mitigate the SEB induced currents.

The SiC Lateral JFET (LJFET), consisting of both a vertical and a lateral channel provides enhanced current control over the standard JFET studied. Through simulation of an array of real world aerospace specific scenarios this bespoke device showed no regions of heightened SEB sensitivity with no failures at a 40% drain - source bias derating with a deposited charge equivalent to 300% that of a silver ion commonly used in SEB testing. Like the standard JFET SEB did occur, however, at elevated biases. At an industry standard drain - source bias derating of 70% the LJFET failed with device melting after impact. Through using the same technique employed to radiation harden the standard JFET a reduction in the SEB sensitivity of the LJFET was observed. Through including an additional 4.2 μm of regrowth between the gate and source of the device it could withstand harsher radiation conditions, due to the creation of a low electric field region below a magnitude of 0.5 MV/cm, 30% that of the original. The modified LJFET at an industry standard drain - source derating is robust against all heavy ion deposited charge conditions studied, up to and including 300% that of a silver ion commonly used in SEB testing. As future aerospace applications will require the use of high voltages in the presence of real world cosmic ray environments, the use of the LJFET and modifications are key towards the mitigation of Single Event Burnout.

Dedication

In loving memory of a dear friend, Michael Cross.

Acknowledgements

From an early age I had been fascinated and intrigued by space and the night sky. Having lived in a rural setting on a farm in the north of England with many crystal clear skies, I regularly enjoyed being able to see stars for miles on an evening. I wanted to learn more and I am truly thankful to a number of people who have supported and guided me on this journey. One which has lead to this PhD opportunity - involving research on the effects of the same stars I would look up to many years ago.

My time in education was thoroughly enjoyable, thanks to the enthusiastic teaching, support and encouragement from the staff at both Staindrop and Teesdale schools. From this, my passion for understanding the world around me grew, and a physics degree was the next logical step. I had three fantastic years of studying physics at Newcastle University - my thanks to all the staff and team there - this was a wonderful time for me.

When an opportunity to study for a PhD in my dream field of research at Durham University arose, I was delighted to accept. I would like to thank my supervisors. To Alton Horsfall, thank you for your guidance, expertise and wisdom - not only has this time been filled with learning, but also many laughs! Thanks also to Chris Groves for your tremendous insight, knowledge and encouragement over this time - it is really appreciated.

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1 Introduction

Rising sea levels, forest fires and increased droughts are now commonplace in the world due to the rampant effects of global warming. With the number of annual flights set to return to pre-pandemic levels, far earlier than the predicted 2024, it is clear that society is not going to stop flying. The most popular flight route from Heathrow is to JFK New York, for a single passenger taking a return flight over 1 tonne of CO_2 is produced, for an aircraft, around 300 tonnes [1]. This is one route of many constantly producing vast amounts of CO_2 which in turn contributes to the 900 million tonnes produced annually [2]. Change needs to happen quickly, and the solution is the electrification of aircraft.

The electrification of aircraft is a method to drastically improve the efficiency of aircraft processes through the utilisation of electrical systems rather than through the traditional operation methods which are through a combination of pneumatic, hydraulic and electric systems [3]. Development of these more-electric and all-electric aircraft is happening at a rapid pace with a diverse range of solutions reaching the market to cater to the needs of many, including the Island Hopper, ideal for use on the Outer Hebrides where regular battery recharging is an option and only short distances need to be covered. Urban Air Vehicles (UAVs) and electric Vertical Take Off and Landing (eVTOLs), known as air taxis, would support already stretched transport networks in cities across the world by offering short trips with a range of tens of miles [4]. Additionally, demonstrator aircraft are showcasing the potential of electric motors for regional distances (100s of miles). For heavier commuter aircraft the use of all-electric power systems is unsuitable - largely due to the lack of energy density provided by current battery technology [5], however, alternative hybrid propulsion systems are a potential option. The electrification of aircraft is not restricted to propulsion, rather, it can also be used for flight control surfaces - offering a number of methods to strive towards achieving carbon free flight. Central to achieving these future carbon savings are power electronics, the combination of electrical components which condition and control power into application suitable forms.

Semiconductor devices determine the size, weight and performance of the power electronic systems and are used for the operation of variable-speed motor drives, a crucial

feature of many aircraft. These devices need to be able to support a very large voltage in the off-state, carry high currents in a small area with a low on-state voltage drop and be able to switch rapidly between on and off states [6]. Traditionally, Silicon MOSFETs and IGBTs have been suitable devices of choice for these applications, but in the search for higher efficiencies, alternative materials and device structures have been considered, and are currently in use, in place of these Si devices. Gallium Nitride (GaN) and Silicon Carbide (SiC) are the front-runners offering superior switching and higher voltage operation credentials over Silicon. These materials have only been accepted over the past 20 years due to the resolution of the fabrication issues that have hindered the manufacture of these devices in the past. Both of these materials offer lower on state resistance, better thermal performance and higher switching speeds in comparison to Silicon. Despite GaN having a higher critical electric field at 3.3 MV/cm to SiC at 2.2 MV/cm, SiC is considered to be the more robust of the two due to its superior thermal conductivity which is between 400 and 500 W/m K, four times greater than that of GaN, enabling the use of SiC in a range of extreme environments [7, 8, 9, 10]. SiC looks to be the solution to the needs of the electrification of aircraft, however, there is a hidden threat lurking in the skies.

Cosmic rays are high energy particles created through stellar explosions which bombard the earth's atmosphere at speeds of up to 1 million miles per hour [11]. These high energy particles interact with the oxygen and nitrogen in the atmosphere to generate secondary cosmic ray showers which filter down towards sea level where they are at their lowest energy [12]. There is a small concentration of cosmic rays at sea level, a few thousand neutrons/cm^2/year, with a considerable concentration at flight altitudes of 35,000 ft at around a few million neutrons/cm^2/year [13]. Cosmic rays have been known to interact with electronics and alter their operation, occasionally with devastating consequences. In Belgium in 2003 there was an election using electronic voting machines where one candidate gained more than 4096 votes, more than the number of voters - due to the spontaneous creation of a bit in position 13 of the memory of the computer caused by cosmic ray interaction with the memory [14]. Later in 2009 Qantas Flight 72 between Singapore and Perth suffered from violent pitching issues where cosmic rays were the cause when they interacted with the on-board flight computers, altering the indicated altitude [15]. If cosmic rays are known to cause an issue in these situations where low voltages are used, the question is raised of what potential issues arise when high voltage high efficiency electronics are considered.

It is known that when cosmic rays interact with devices under high bias conditions, typical for aerospace applications, that device failure can occur - often with the potential of an explosion [16]. With the growing popularity and potential of autonomous air mobility, which will rely heavily on high efficiency electronics, there seems to be the possibility of a perfect storm on the horizon for a number of cosmic ray induced issues on-board aircraft, casting the electrification of aircraft concept into doubt. The focus of this research is on understanding the critical interaction between cosmic rays and the electronic components, which are pivotal to the realisation of the future of carbon free flight. The breakdown of chapter contents are as follows:

Chapter 2 focuses on the current understanding of radiation effects on electronics for power systems. Here the findings over the past 70 years from the early works and primitive studies to the latest cutting edge discoveries from the key players, NASA (National Aeronautics and Space Administration), NRL (United States Naval Research Laboratory), CERN (European Council for Nuclear Research) and the ESA (European Space Agency), amongst others, are shown. This section also provides detail on the suitability and novelty of the methods used in this work and the benefits they provide in comparison to the standard test methods used by many in this field.

Chapter 3 delves into the question of material suitability for use in electronics for power systems with a focus on the simulation of 1D p–i–n power diode structures to eliminate other potential influences. Despite the electrical superiority of SiC it is still unknown as to whether it can actually out perform Si in terms of its radiation response. Through the use of simulation the sensitivity of both SiC and Si have been determined - providing clear insight into the preferred material to be selected for the market.

Chapter 4 investigates the potential implications of 2D structures on the radiation response of SiC. The JFET is a robust structure under standard testing but questions still remain around its radiation response. Through simulation, a unique power JFET structure has been examined under a range of aerospace specific operating conditions - allowing the region specific sensitivity of the device to be understood for the first time. Radiation sensitive regions of the device have been identified, remedies have been suggested and their suitability has been proven showing reductions in radiation sensitivity.

Chapter 5 builds on the findings to date and probes the sensitivity of a bespoke JFET designed to be robust in the most extreme of environments. Through simulation at a range of real world aerospace specific conditions, the device sensitivity to radiation has been determined. In search of further reductions to device radiation sensitivity, modifications to the original device have been made. From this, an optimised device has been created with the potential to make additional reductions to the radiation sensitivity.

Chapter 6 compares the suitability of all devices studied and looks forward to the exciting future of aircraft electrification in which these findings will play a key role.

2 Literature Review

In order to gain a thorough understanding of the interaction between cosmic rays and power electronics, it is important to delve into the key discoveries that have lead to the latest cutting edge findings. This chapter summarises the pivotal moments spanning over the past 130 years which have been influential on this field of research.

2.1 Avalanche Breakdown

The avalanche breakdown of a semiconductor device is the sudden change from a high dynamic resistance to a much lower one caused by the cumulative multiplication of free charge carriers under the action of an applied electric field [17]. The avalanche breakdown voltage imposes an upper limit on the reverse bias for an array of devices, including the drain voltages of JFET and MOSFET. Regions of high electric field within the depletion region of the device leads to the acceleration of carriers; these carriers then gain sufficient kinetic energy to collide with atoms in the depletion region, forming electron-hole pairs through impact ionization. These generated electron-hole pairs are then subjected to the same high electric field, resulting in the further generation of electron-hole pairs, leading to a surge in current and device breakdown through the generation of an avalanche of carriers.

2.1.1 Impact Ionization Coefficients

The impact ionization coefficient for holes (α_p) is defined as the number of electron–hole pairs created by a hole traversing 1 cm through the depletion layer along the direction of the electric field [18]. The impact ionization coefficients for semiconductors are described by Chynoweth's Law

$$\alpha = a \exp\left\{\frac{-b}{E}\right\} \tag{1}$$

where E is the electric field component in the direction of current flow, a and b

are constants that depend on the semiconductor material and temperature. The impact ionization coefficients for silicon carbide have been measured as a function of temperature by using an electron beam excitation method by Raghunathan and Baliga in 1999 [19]. The impact ionization rates for silicon have been measured as a function of both electric field and temperature. The impact ionization coefficients for both 4H-SiC and silicon can be seen in Figure 2.1, there is a strong dependence of the impact ionization coefficients upon the electric field, the result being that the breakdown voltage of devices can be severely reduced by the presence of a highly localised electric field within the structure [18]. It is also noted that the ionization coefficients of 4H-SiC are lower than those for Si due to the large bandgap of SiC.

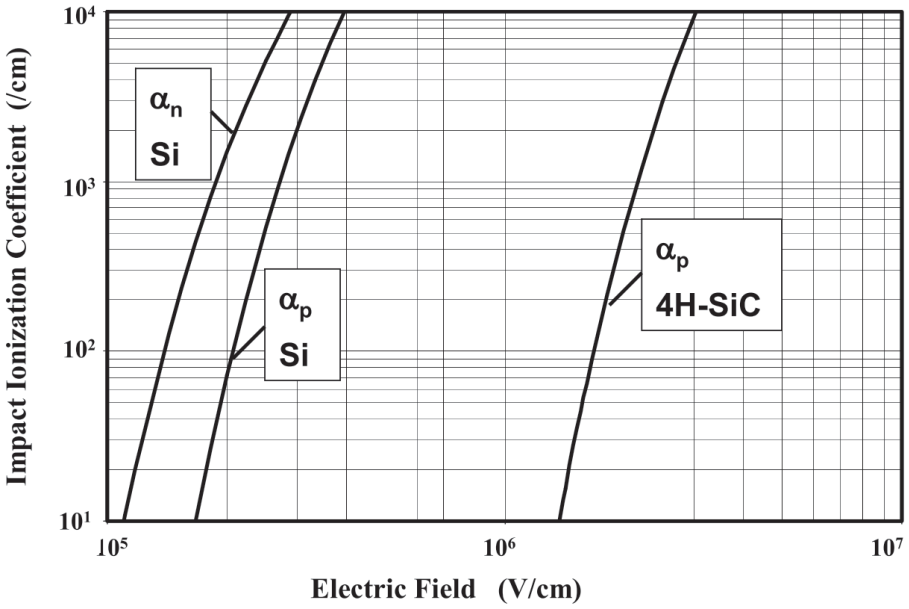


Figure 2.1: Impact ionization coefficients for silicon and 4H-SiC [18].

2.1.2 Dead Space

Dead space is a term which is used to describe the distance carriers injected 'cold' (at thermal energies close to the band edge) must travel down the electric field before their distribution in energy heats and their ionization coefficient reaches equilibrium with the field. Within this 'dead space' ionization is suppressed [20]. At high fields a lower limit on dead space can be estimated as

$$d = \frac{E_T}{\exp\{F\}} \tag{2}$$

where d is the distance travelled by a carrier before acquiring from its electric field, F, the threshold energy, E_T for ionization [21].

2.1.3 Multiplication Coefficient

Avalanche breakdown is defined by the impact ionization rate becoming infinite. A one-dimensional reverse-biased n^+-p-p^+ diode, equivalent to a highly doped n^+ region above a lightly filled drift region which is on top of a highly doped substrate, with a depletion region extending primarily in the p^+ substrate, is used to analyse this. If an electron–hole pair is generated at a distance x from the junction, the hole will be swept toward the contact to the p^+ region, while the electron is simultaneously swept toward the junction with the n^+ region. If the electric field in the depletion region is large, these carriers will be accelerated until they gain sufficient energy to create electron–hole pairs during collisions with the lattice atoms. When traversing a distance dx through the depletion region a hole will create $(\alpha_p\, dx)$ electron-hole pairs whereas an electron will create $(\alpha_n\, dx)$ electron-hole pairs, where α_p and α_n are the impact ionisation coefficients for holes and electrons respectively. The total number of electron-hole pairs created in the depletion region due to a single electron hole pair generated at a distance x from the depletion region is known as the multiplication coefficient *M(x)*, given by

$$M(x) = 1 + \int_0^x \alpha_n\, M(x)\, dx + \int_x^W \alpha_p\, M(x)\, dx \tag{3}$$

where W is the width of the depletion layer. A solution to this is given by

$$M(x) = M(0)\, \exp\left\{ \int_0^x (\alpha_n - \alpha_p) dx \right\} \tag{4}$$

where *M(0)* is the total number of electron hole pairs at the edge of the depletion

region. Substituting equation 4 into equation 3 with $x = 0$ provides a solution for *M(0)*

$$M(0) = \left\{1 - \int_0^W \alpha_p \exp\left\{ \int_0^x (\alpha_n - \alpha_p)\, dx \right\} dx \right\}^{-1} \tag{5}$$

Substituting this in to equation 4 gives

$$M(x) = \frac{\exp\left\{ \int_0^x (\alpha_n - \alpha_p)\, dx \right\}}{1 - \int_0^W \alpha_p \exp\left\{ \int_0^x (\alpha_n - \alpha_p) dx \right\} dx} \tag{6}$$

The avalanche breakdown condition is defined to occur when the total number of electron hole pairs generated within the depletion region approaches infinity, corresponding to the multiplication coefficient *M(x)* also becoming equal to infinity. This condition is achieved when the denominator of equation 6 is zero and so

$$\left\{ \int_0^W \alpha_p \exp\left\{ \int_0^x (\alpha_n - \alpha_p) dx \right\} dx \right\} = 1 \tag{7}$$

The left hand side of the equation, contained within large braces, is known as the ionization integral. If the impact ionization coefficients for holes and electrons are assumed to be equal, the avalanche breakdown condition can be written

$$\int_0^W \alpha\, dx = 1 \tag{8}$$

2.1.4 Abrupt One-Dimensional Diode

The p^+ gate and the lightly doped n channel, commonly found in power electronic devices, can be analysed in the form of an abrupt one-dimensional diode model for avalanche breakdown - as shown schematically in Figure 2.2. When this junction is reverse biased a depletion region is formed in the n^-region and a strong electric field

is generated within it that supports the voltage. Poisson's equation in the n^- region can be expressed as

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\epsilon_s} = -\frac{q\,N_D}{\epsilon_s} \tag{9}$$

where V is the potential, E is the strength of the electric field, $Q(x)$ is the charge within the depletion region due to the presence of ionised donors, ϵ_s the dielectric constant for the semiconductor, q the electronic charge, and N_D the donor concentration in the uniformly doped n^- region.

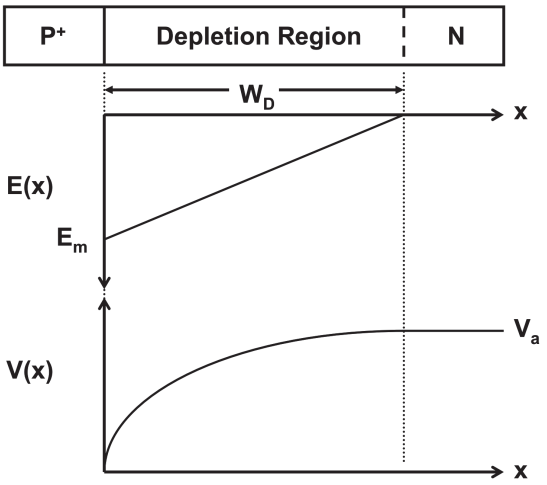


Figure 2.2: Electric field and potential distribution for an abrupt parallel-plane P^+/N junction [18].

The electric field distribution is the integral of equation 9 with the boundary condition that the electric field must go to zero at the edge of the depletion region

$$E(x) = -\frac{q\,N_D}{\epsilon_s}(W_D - x) \tag{10}$$

where W_D is the depletion region width.The electric field maximum occurs at the P^+/N junction and decreases linearly to zero at $x = W_D$. The potential distribution is the integral of the electric field distribution through the depletion region, resulting in

$$V(x) = \frac{q\,N_D}{\epsilon_s}\left(W_D\,x - \frac{x^2}{2}\right) \tag{11}$$

The potential varies quadratically and the thickness of the depletion region can be related to the applied reverse bias (V_a) by using the boundary condition

$$V(W_D) = V_a \tag{12}$$

Coupled with the assumption that the applied reverse bias is much greater than that of the built-in potential, equation 12 can be substituted into equation 11 to relate the depletion width to the applied reverse bias, resulting in

$$W_D = \sqrt{\frac{2\,\epsilon_s\,V_a}{q\,N_D}} \tag{13}$$

An expression for the maximum electric field in the diode, E_m, is obtained by substituting equation 13 into equation 10

$$E_m = \sqrt{\frac{2\,q\,N_D\,V_a}{\epsilon_s}} \tag{14}$$

A rearrangement of equation 14 allows the applied voltage of the diode to be determined for a given electric field

$$V_a = \frac{E_m\,W_D}{2} = \frac{E_m^2\,\epsilon_s}{2\,q\,N_D} \tag{15}$$

To calculate the critical electric field for 4H-SiC knowledge of the breakdown voltage is required - the primary method to obtain this is through photomultiplication experimentation on avalanche diodes [22], which in turn provides understanding on the electron and hole impact ionization coefficients.

2.2 Superiority of Silicon Carbide for Power Applications

SiC is a wide bandgap semiconductor with properties that are highly suitable for devices working at high power, high frequency, high temperature and in harsh environments in comparison to traditional Si, as seen in Figure 2.3. SiC is a material with a high breakdown electric field strength, high saturation drift velocity of electrons and high thermal conductivity. SiC is used in power devices where the demand for improved energy efficiency is driven by reducing switching and conduction losses. SiC is a tetrahedrally bonded compound comprising a stoichiometric mixture of silicon and carbon atoms. Every silicon atom shares electrons with four carbon atoms, resulting in strong covalent bonds.

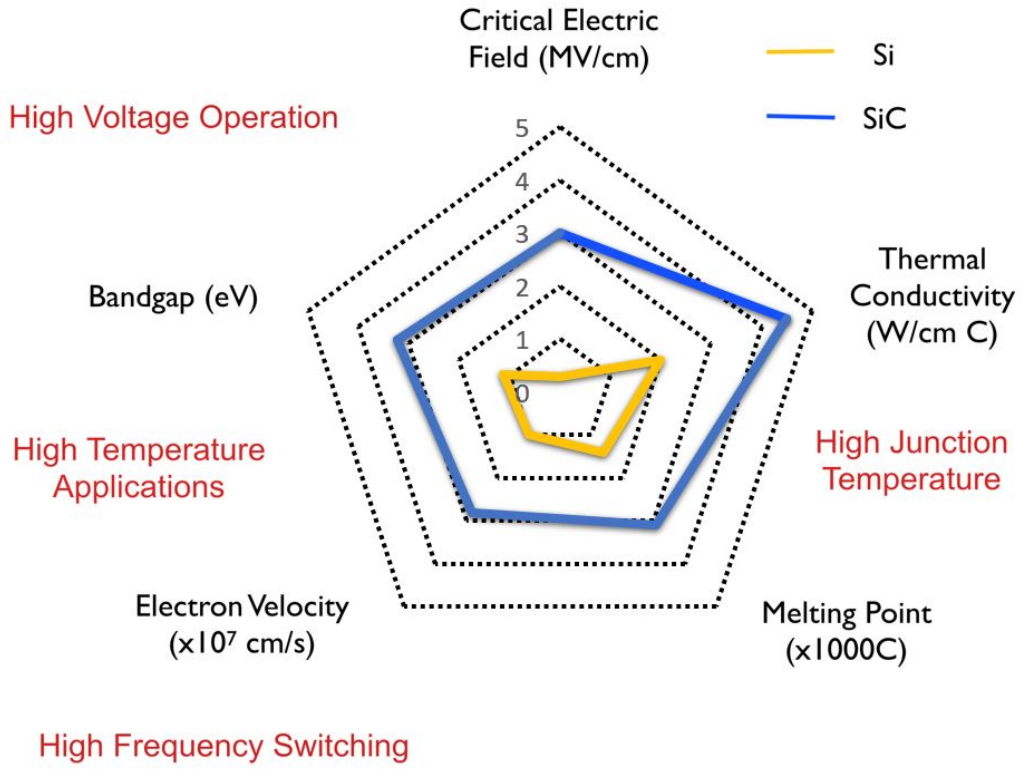


Figure 2.3: Material property rosette plot for SiC and Si.

The synthesis of SiC first occurred in the 19^{th} century in small scale. The first mass produced synthesis of SiC was performed by Edward Goodrich Acheson in 1892 when an attempt was made to combine carbon with other materials, namely silica, whilst heated to create a crystalline carbonaceous material that would be a practical sub-

stitute to diamond [23]. Naturally occurring SiC, namely Moissanite, was discovered by Dr. Henri Moissan in 1905 [24].

Defects in the SiC crystal coupled with issues interfacing the SiC with SiO_2 to make MOSFETs lead to emphasis being placed on the use of silicon as the main device material in the mid 20^{th} century. The density of charged interface defects and interface states in SiC/SiO_2 structures is in the 10^{11} to $10^{12}\,cm^{-2}$ range, approximately two orders of magnitude higher than than Si/SiO_2 interfaces [25]. Over the past 50 years the growth methods for SiC crystals have improved resulting in higher quality SiC wafers leading to the development of SiC devices.

2.2.1 Polytypism

Silicon Carbide is a polymorphic materials, one which can crystallize in different structures for an identical chemical composition. In 1912 different crystalline modifications of SiC were discovered [26]. As SiC exhibits 2D polymorphism the different SiC modifications were named polytypes. There are three forms of polytypes that exist for SiC, cubic (C), hexagonal (H) and rombohedral (R) - they share the same chemical composition whilst demonstrating different electrical properties. All polytypes have a hexagonal form of SiC bilayers which should be viewed as sheets of spheres of the same radius and touching radii. The sheets are the same for all lattice planes. The position of the planes above and below are shifted relative to the reference plane. The possible positions of SiC sheets are referenced to by either A, B or C. Different polytypes of SiC are then constructed by repeating a particular order of sheets. There are an array of SiC polytypes, with over 250 identified to date [27], with the majority of research concentrated on 3C, 4H and 6H [28] - the stacking sequences can be seen in Figure 2.4. The most notable polytype used for power electronic devices is 4H-SiC due to its higher electron mobility, smaller anisotropy and larger bandgap [9].

2.2.2 Mechanical and Chemical Properties

SiC is one of the hardest known materials with a Young's Modulus of 700 GPa [29] which is much higher than Si at values between 130 GPa and 169 GPa [30]. SiC is chemically inert and reacts poorly with any known materials at room temperature.

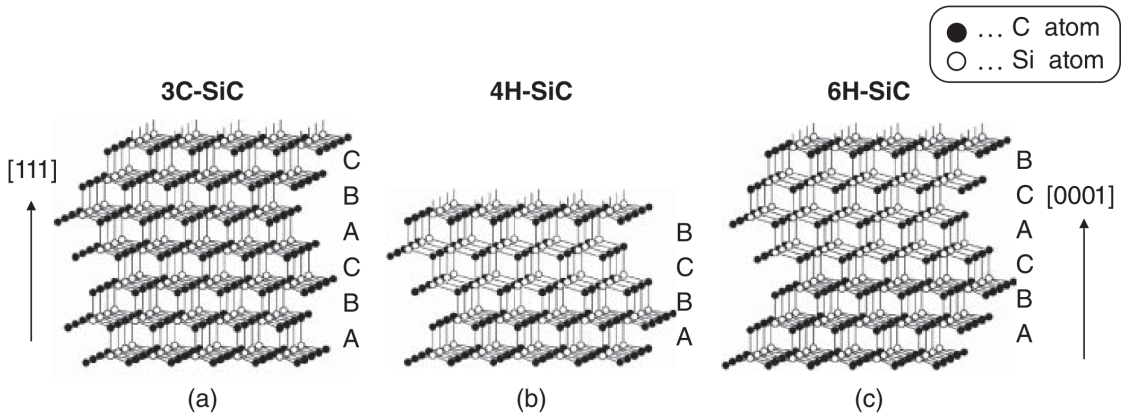


Figure 2.4: Structures of (a) 3C-SiC, (b) 4H-SiC, and (c) 6H-SiC in a ball-stick model [9].

SiC does not have a liquid phase but does sublime at temperatures above 1800 °C.

2.2.3 Bandgap

The bandgap of SiC varies depending on the polytype with the lowest bandgap value at 2.39 eV from the 3C-SiC arrangement and the highest bandgap value at 3.33 eV for 2H-SiC with the 4H-SiC polytype having a bandgap of 3.265 eV, with all measurements performed at 300 K [31]. The intrinsic carrier concentration of a semiconductor is both temperature and bandgap dependent - with the bandgap of 4H-SiC being approximately three times that of Silicon (1.12 eV) at room temperature. As the reverse leakage current is proportional to the square of the intrinsic carrier concentration, the leakage current of a SiC device can be as little as 0.1% that of a Si device with a similar voltage rating, enabling SiC to be used in high temperature environments.

2.2.4 Critical Electric Breakdown Field

The maximum E-field that a material can support before suffering physical breakdown and unsupported current flow is the critical electric field, E_c. The majority of wide bandgap materials have a high breakdown electric field, leading to a high impact ionization energy. SiC can withstand an electric field 10 times greater than Si without undergoing avalanche breakdown [32]. High breakdown electric field enables the fabrication of high voltage, high power devices [33]. It can be seen from equation 15

that for the same value of breakdown voltage the depletion width of a SiC device can be an order of magnitude less than that of a silicon based device, resulting in lower on-state resistive losses.

2.2.5 Saturation Drift Velocity and Carrier Mobility

The saturation drift velocity is an important parameter in the determination of the device speed of response and maximum switching frequency. The drift velocity at low electric fields is given by [34]

$$v_d = \mu E \tag{16}$$

where μ is the carrier mobility.

At high values of electric field equation 16 does not hold due to the heating of free carriers; resulting in velocity saturation, which acts as an upper limit on the carrier speed in a semiconductor. In order to obtain high frequencies and channel currents high saturation velocities are required. SiC with a saturation velocity of $2 \times 10^7 \mathrm{cm\,s^{-1}}$ [35], twice that of Si, is a suitable material for high speed devices.

2.2.6 Thermal Conductivity

The thermal conductivity is of paramount importance for high power and high frequency device applications. Usually, increasing device temperature results in the alteration of the physical properties of the device. The carrier mobility decreases with increasing temperature. Heat generated through various resistive losses must be conducted away from the device into the package to avoid these issues. At room temperature SiC has a very high thermal conductivity at $4.8\,\mathrm{Wcm\text{-}K^{-1}}$ [35] compared to a value of $1.56\,\mathrm{Wcm\text{-}K^{-1}}$ for Si [36]. These high values enable SiC devices to operate at extremely high power levels and dissipate large amounts of excess heat. Due to this, coupled with low power losses and high temperature capability, SiC devices can operate without a thermal cooling system, contrary to Si, resulting in the benefit of a reduction in cost, weight and size of the power electronic system [37].

2.3 Power Electronics for Aerospace

The development of the More Electric Aircraft (MEA) is recognised as one of the major next steps in the advancement of aerospace technology [3], [38], [39]. The industry's need for improved efficiency, reliability and the ability to withstand harsh environments are crucial factors in development of future generations of aircraft. The traditional three optimised power systems of electrics, hydraulics and pneumatics are to be replaced by a single electrical system which can be used by all aircraft sub-systems. An array of technologies are proposed in the development of the MEA - as summarised schematically in Figure 2.5.

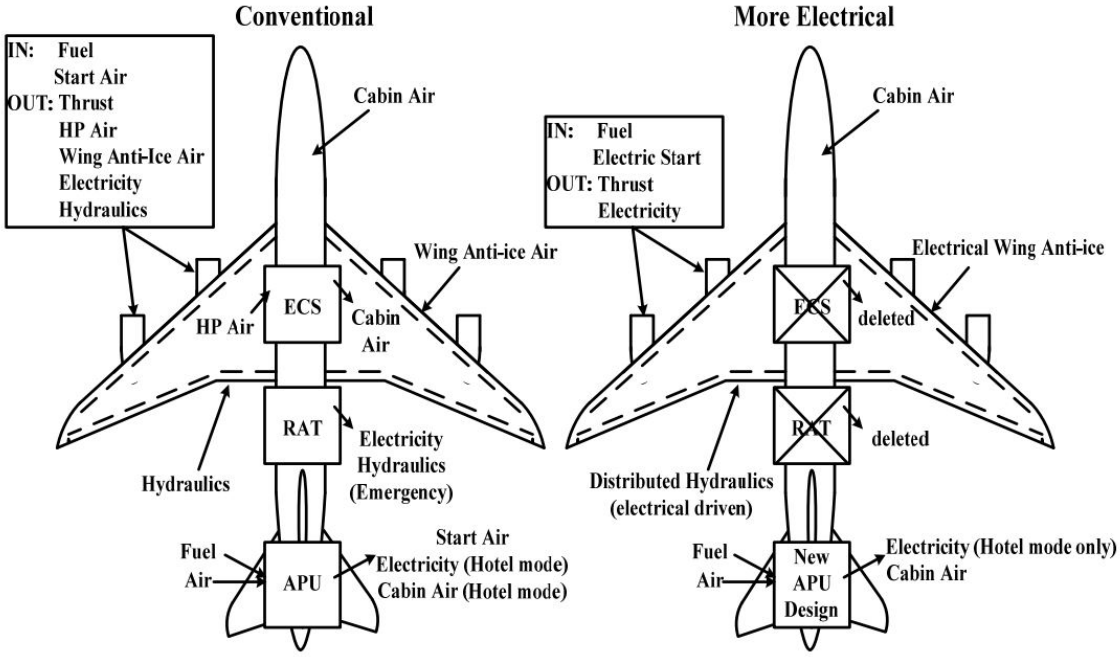


Figure 2.5: Comparison of Conventional and More Electric Aircraft Systems [3].

It can be seen from Figure 2.5 that the Ram-Air-Turbine (RAT), a smaller turbine that is deployed in the event of main turbine failure, has been removed from the Conventional Aircraft system for the More Electrical Aircraft system. High power, high efficiency and lightweight motors and generators connected to each of the main shafts of the engine enables power extraction from windmilling engines, a process where an idle fan is rotated due to the air flow across it, making the provision of RATs unnecessary [3]. It can also be seen that the Environmental Control System (ECS)

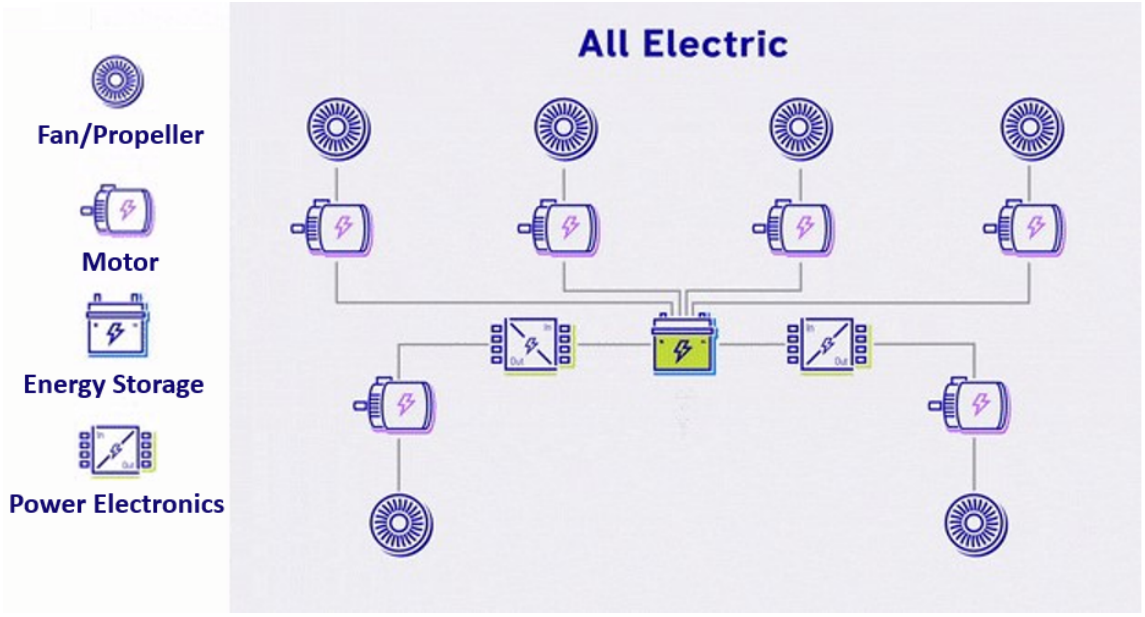


Figure 2.6: The All Electric propulsion system [40].

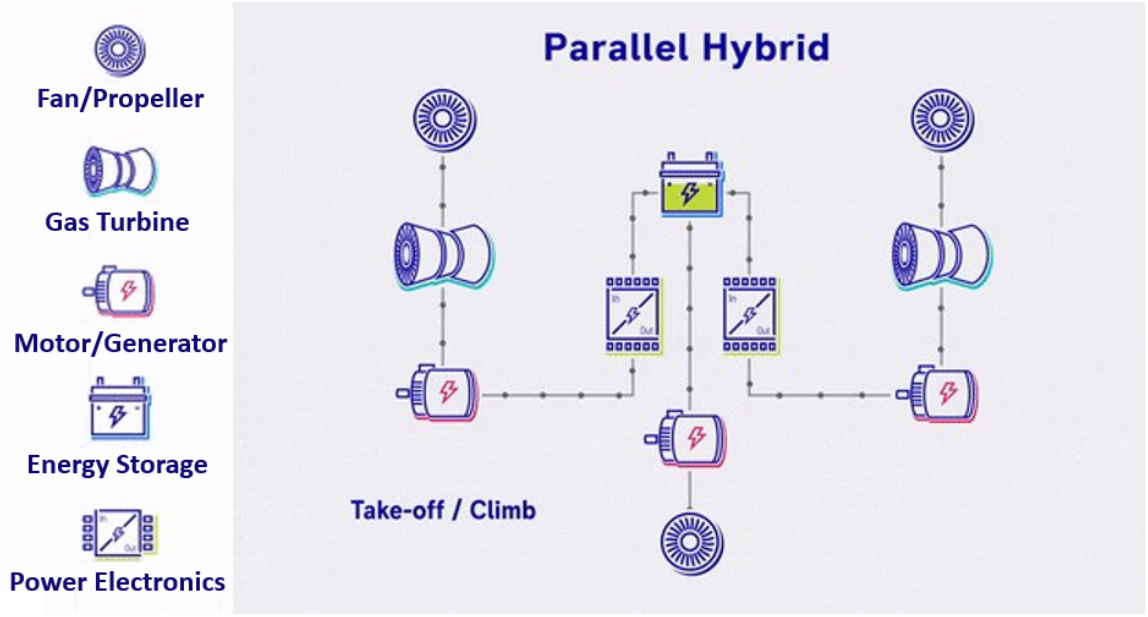


Figure 2.7: The Parallel Hybrid propulsion system [40]

which is used in Conventional Aircraft systems to cool and depressurize engine air off take has been removed - the MEA system makes use of electrically driven compressors, heater and cooler units to pressurize and condition the air in the aircraft cabin.

The MEA concept is currently under development, and from this, four key markets are expected to form the next generation of sustainable aviation, these are: small pro-

peller aircraft, Urban Air Mobility, Commuter Aircraft and Regional Aircraft. These transport systems are intend to drastically reduce CO_2 and noise production levels in comparison to conventional air travel through their reliance on electrical energy. Small propeller aircraft and Urban Air Mobility are both forms of lightweight aircraft intended for small numbers of passengers travelling relatively short distances - these aircraft will rely on an all-electric propulsion system, which can be seen in Figure 2.6. This propulsion system relies solely on battery technology and can be quickly recharged for the next use and is therefore the ideal candidate to achieve the Net Zero targets by 2050. However, this technology is currently not practical for heavier commuter and regional aircraft which can carry 10s to 100s of passengers. Battery technology is currently the hurdle stopping the realisation of the all-electric propulsion systems for these types of aircraft [5]. Alternative systems are both in use and under development which utilise current technology to achieve enhanced energy efficiency for these types of aircraft known as the Parallel Hybrid propulsion system, as seen in Figure 2.7. Here, the propulsive power is a mix of conventional gas turbine-driven fans and electric-driven fans with active energy storage. A feature which is pivotal in both propulsion systems are the power electronics, a carefully selected combination of electronic devices which when correctly integrated, can condition and control energy into suitable forms for a specific application. Electric propulsion of aircraft has only recently been made possible through the advancement of semiconductor technology, where new high-voltage devices offer enhanced efficiency and lower on-state losses. When selecting devices for these applications, the device internal structure plays a crucial role on both their operation and performance. The PiN diode and the JFET are devices which are being considered for use in high performance aerospace power electronic applications due to their high voltage operation capability. Their operation and response to aerospace specific conditions is to be understood. The background of the operation of these devices is shown in the following section.

2.3.1 PiN Diode Overview

The PiN diode is a key element of many power electronic systems due to its ability to block high voltages a capability that arises from the physical structure. A basic p-n junction with an added thick lightly doped intrinsic region provides a region that will support high reverse bias voltages. In the forward bias mode of operation the

diode is conducting and the intrinsic (lightly doped) region, which begins with a relatively high resistance receives carriers from both of the more heavily doped ends and is therefore conductivity modulated to reduce the resistance of this region [10] - allowing the device to have lower effective on-state resistance. From this behaviour lower conduction losses are realised whilst possessing a region that can support high voltages in reverse bias - a crucial requirement for high efficiency power electronic systems.

A balance of trade-offs in device design play a major role on the final device characteristics and it is therefore crucial that the correct balance is obtained for specific applications. The design of the drift region has major implications on the overall device's blocking ability - with a wider width and lighter doping the breakdown voltage is optimised, however, this is done so at a cost to the diodes switching characteristics. The charge that is injected into the drift layer when the device is in its on-state must be removed before the device is turned off - the removal of this charge is the transient phenomenon known as reverse recovery. During the turn-off of the device the diode remains conductive, and a reverse current passes through the diode until the stored carriers disappear either by diffusion or recombination. Due to the drift layer thickness of SiC being on average an order of magnitude lower than that of Si coupled with the associated 100 $\times$ higher doped drift layer, this allows the device to switch faster due to less charge being stored in the device for equivalent breakdown voltages for both Si and SiC.

The purpose for selecting the PiN diode as a case study is that it acts as a simplified structure in comparison to that of the more complex JFET. From thorough understanding of the PiN diode response, indications and predictions towards the response of the JFET can be made prior to any testing or simulation due to key similarities in their structures. Both the PiN diode and the JFET are key avionic components and thorough understanding of their performance is required.

2.3.2 JFET Overview

The JFET is a FET which can consist of 3 or 4 terminals - source, drain and gate, in either the single or double gate configuration. A n-channel device consists of a source and drain which are n^+, a p^+ gate, and an n^- channel. When a negative bias is

applied to the p^+ gate the depletion region widens into the lightly doped n^- channel - reducing the cross sectional area for electron conduction. The pinch-off voltage, V_P, is the gate voltage that just pinches off the channel at the source. V_P can be regarded as the threshold voltage of the JFET, as for gate voltages more negative than V_P there can be no current in the channel. For gate voltages above V_P and when a positive drain - source bias is applied current flows through the device. Initially, the drain - source current increases linearly with applied drain - source bias - this is up until the drain saturation voltage is reached. As the drain - source bias increases the the gate - channel depletion region widens at the drain end of the channel. Eventually the depletion region fills the channel at the drain end - the drain voltage that this occurs at is the saturation drain voltage. For drain voltages beyond the saturation drain voltage, the drain current is assumed to remain essentially the same as the saturation current. As the drain voltages increase further, breakdown occurs when the current raises sharply with drain bias. The breakdown occurs at the gate edge towards the drain side where the electric field is at its highest [34].

The SiC JFET is renowned as having high reliability due to the lack of oxide for a voltage driven device with superior temperature performance in comparison to MOS devices [41]. SiC oxides have demonstrated a lower mean time to failure in comparison to those on silicon, and therefore result in SiC MOS controlled devices are prone to threshold voltage shifts, gate leakage and premature oxide failure. The JFET can be realised through epitaxial growth for the conducting channel and junctions, producing regions on high quality [42]. The normally-on JFET design is capable of extremely low on-state resistance, but this design, however, is not widely accepted by the market due to its safety requirements and the need for additional circuitry to achieve normally-off behaviour. The normally-off JFET design requires a narrow and relatively low doped channel to ensure the normally-off performance and therefore pays a penalty in terms of the on-state performance. Additionally, the small range of gate control voltages make the normally-off JFET vulnerable to electromagnetic interference. For these reasons, much care and consideration is required when selecting the appropriate JFET for the desired application.

2.4 Space Radiation Environment

In order to consider the environment in which electronics used in power systems for aerospace must operate, the origin of the particles responsible for the potential Single Event Effect (SEE) interaction need to be considered first. There are three categories of high-energy particles found in the natural space environment; the first is the background flux of ions that originates outside the solar system, called galactic cosmic rays (GCR); the second are particles that are emitted from the sun during solar particle events, namely coronal mass ejections (CMEs) and solar flares; and the third type are particles trapped by planetary magnetic fields, like the Earth's Van Allen Belts [43]. The space environment is dynamic with GCR fluxes and the frequency of solar particle events being cyclicly modulated by the sun - having a primary period of approximately 11 years of which 4 years when solar activity is low, the solar minimum, and 7 years of heightened activity, the solar maximum. The majority of cosmic ray particles are atomic nuclei; electrons, positrons and other subatomic particles are other forms - their energies vary from a few MeV to around 10^{20} eV [44]. These high energy cosmic rays and solar particles are termed primary cosmic rays as when they enter the top of the Earth's atmosphere, they are attenuated by the interaction with nitrogen and oxygen atoms, resulting in a shower of secondary particles. The high energies of the primary cosmic rays are well in excess of the binding energies of atomic nuclei (typically 7–9 MeV per nucleon), this leads to the predominant nuclear reaction in the atmosphere being spallation, the process where fragments of a material (spall) are ejected from a body due to impact. High energy primary cosmic rays impact atoms in the atmosphere - resulting in a spallation, where nucleons are produced. These spallation-produced nucleons induce spallation in other nuclei in the atmosphere, creating a cascade as seen in Figure 2.8. As neutrons do not undergo the same ionization losses as protons, the composition of the cosmic ray flux varies from the earths atmosphere to sea level.

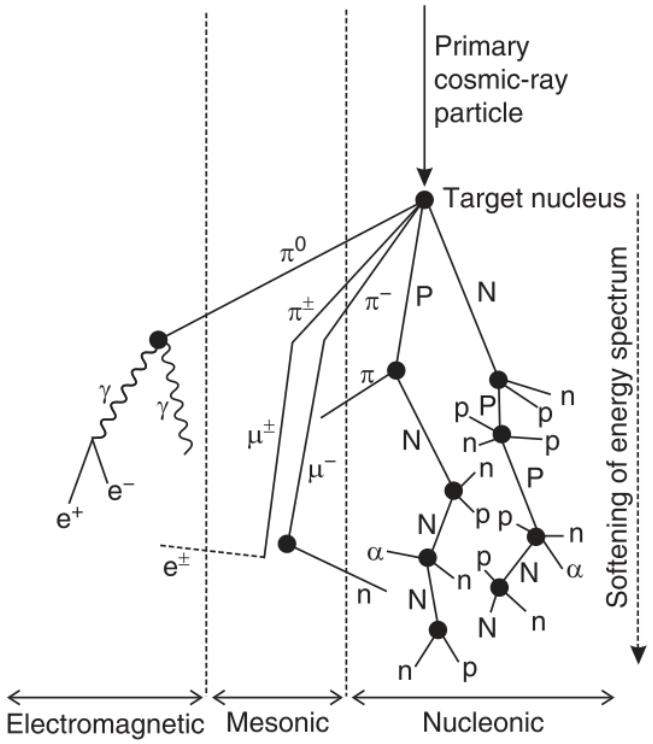


Figure 2.8: The secondary cosmic ray cascade in the atmosphere. Abbreviations used: n, neutron, p, proton (capital letters for particles carrying the nuclear cascade), α, alpha particle, $e^{\pm}$, electron or positron, γ, gamma-ray photon, π, pion, μ, muon [44].

High energy neutrons are a major factor in the design of power electronics for the MEA. At commercial flight altitudes of 30000 ft+ there is typically a neutron flux of 0.4 neutrons $cm^{-2}\,s^{-1}$ [13], as seen in Figure 2.9, resulting in over 1 million neutrons striking a transistor every year. Each of these neutrons have the potential to induce Single Event Burnout within the devices used on aircraft - a critical failure that could result in devastating consequences. As can be seen from Figure 2.9, neutron interaction with electronics are not limited to avionics, there is also potential for interaction which electronics at other high altitude locations, namely Bolivia, situated 11900 ft above sea level. The influence of cosmic rays on power electronics and their potential impact on solid state transformers is described in [45].

A whole host of high energy radiation is present at flight altitudes with neutrons being the most prominent form, as shown by the data in Figure 2.10. Despite this, heavy ion testing is widely regarded by the Single Event Effects community as the best method in the determination of device SEE sensitivity. This is shown through by a number

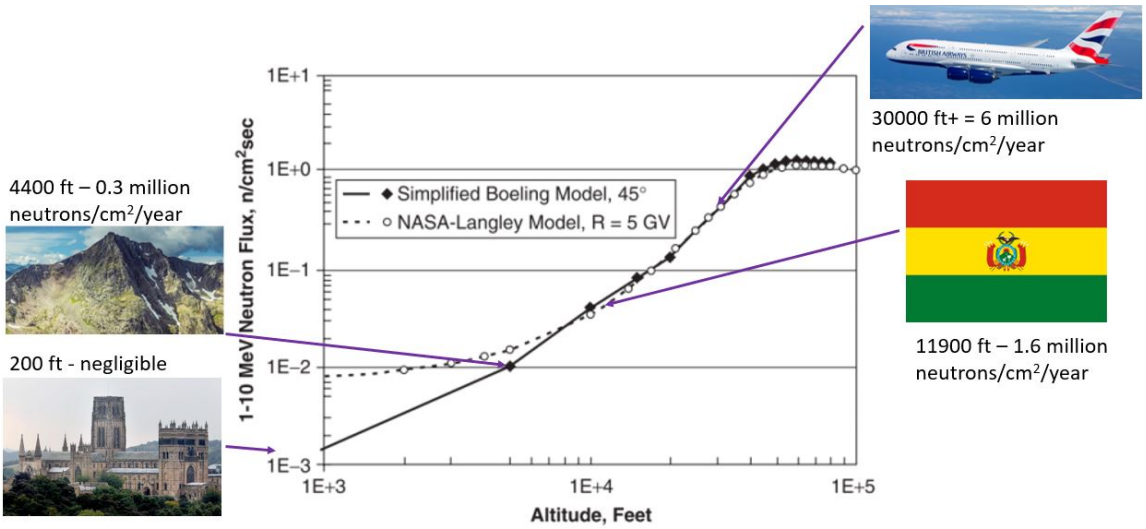


Figure 2.9: The 1–10 MeV atmospheric neutron flux as a function of altitude with important markers identified [12], [13].

of SEE test methods which have been published in the literature, acting as guidelines by defining procedures for accelerator testing of devices [46, 47, 48]. As SEE testing is application specific, these documents can only be considered as guidelines to enable comparative testing, they do not ensure that if the outlined procedures are followed, that the tested device will be robust against radiation. However, these methods suggest the use of heavy ions for the determination of SEE sensitivity of devices due to their flexibility in comparison to proton and neutron testing. This is summarised by the State of U.S. Electronic Parts Space Radiation Testing Infrastructure report [49], which states that if a device performs sufficiently well in heavy-ion testing, with no error/failure modes of concern for ions with a Linear Energy Transfer (LET, the amount of energy an ionizing particle transfers to the material traversed per unit distance), value of less than 15 MeV-cm^2/mg, proton testing or neutron testing may not be required. Heavy ion testing enables the user to pin-point the sensitivity of devices due to the heavily ionizing nature of the particles in comparison to both neutrons and protons - making heavy ions the ideal choice for understanding the SEB sensitivity of devices. Ball *et al.* [50] studied neutron induced failure through a combination of heavy ion SEB data by means of 3-D TCAD and Monte Carlo radiation transport simulations of secondary particle production. The neutron simulation data agreed well with heavy ion experimentation. The LET and range of the secondary particles generated by the neutron when it traversed the active region of the power device, as shown by the data in Figure 2.11, all had LETs below 15 MeV-cm^2/mg,

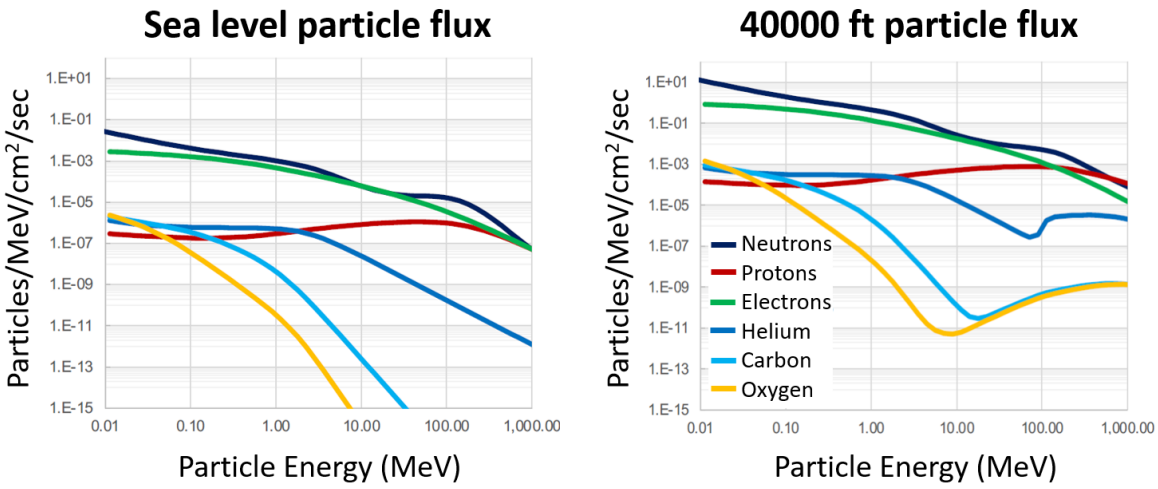


Figure 2.10: Variation in Cosmic Ray Flux at sea level and 40000 ft above [51, 52].

consistent with the work of [49]. These interactions can be replicated through the use of heavy ions which offer the generation of a concentrated charge track in contrast to neutron interaction which results in a multitude of potential distributions of deposited energy from the spallation products. For these reasons, heavy ion testing is the technique of choice for the simulation of power devices to understand and pin-point the SEB sensitivity of SiC based electronics.

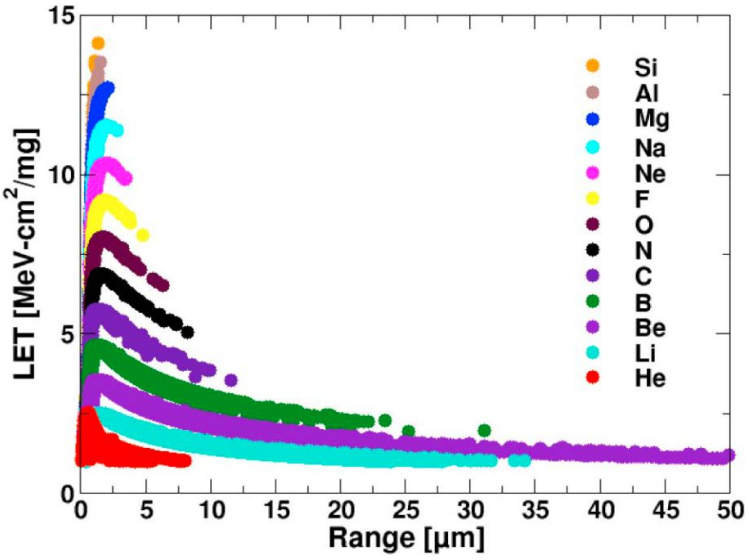


Figure 2.11: Secondary particles (showing range and LET) generated from neutron environment and entering the active region of the device as calculated by simulation for a neutron spectrum which closely matches terrestrial levels [50].

2.5 Radiation Effects on Devices

The cumulative long term damage to the semiconductor lattice that results from the interaction between the atoms in the lattice and the high energy particles generated from solar events is generally described using Total Ionizing Dose (TID) and Displacement Damage (DD). Radiation exposure has been shown to cause leakage current degradation and increased power dissipation in electronic devices similar to those required to support more electric aircraft [53] and reports in the literature show that the radiation response of SiC to cumulative damage is superior to that of Si [54]. However, the instantaneous response of devices caused by the interaction with the high energy particles, known as Single Event Effects, can result in catastrophic failure [55], which is the focus of the work reported in this Thesis.

2.5.1 Total Ionizing Dose

When incident radiation is incident on a semiconductor material such as Si, an electron-hole pair will be created if an electron in the valence band is excited across the band gap into the conduction band. The excited electron leaves a hole behind in the valence band. If an electric field is present, the electrons are swept away as their mobility is much greater than that of the holes. Except for some small fraction of pairs that undergo recombination immediately, the created electrons and holes are free to drift and diffuse in the material until they undergo recombination or are trapped [56]. Oxides contain a distribution of sites which can trap holes, resulting in an alteration in the threshold voltage of the device.

TID effects occur from charge trapped in insulators. The presence of an oxide in a power device provides potential for the occurrence of TID effects. For the SiC JFET and PiN diode studied in the work, TID effects are not the primary concern as these devices do not exhibit a TID susceptibility at dose levels typical for flight altitudes [57, 58]. However, for the SiC MOSFET, which has a similar structure to the Si MOSFET, a key feature of its structure is the thick gate oxide [58]. SiC MOSFETs have been shown to remain with the manufacturers specification up to 100 krad(Si) or higher in commercially available devices whilst also displaying enhanced TID tolerance over their Si counterparts [59].

2.5.2 Displacement Damage

High energy particles such as neutrons, protons, and electrons can impact a power electronic device and scatter off lattice ions, locally deforming the material structure, known as Displacement Damage (DD). From this, the band-gap structure may change, affecting fundamental semiconductor properties [56], including the minority carrier lifetime, majority carrier charge density, resulting in reductions in carrier mobility. Research has found that both SiC JFETs and PiN diodes are practically immune from TID. In the work of McGarrity, it was shown that displacement damage has a minimal effect on the electrical characteristics of SiC JFETs, even at neutron fluences of 10^{15} n/cm^2 [60]. Further, the work of Hazdra *et al.* [54] showed that SiC PiN diodes have superior DD performance in comparison to Si. For these reasons, DD is not considered further as SiC PiN diodes and JFETs are the focus of this work.

2.5.3 Single Event Effects

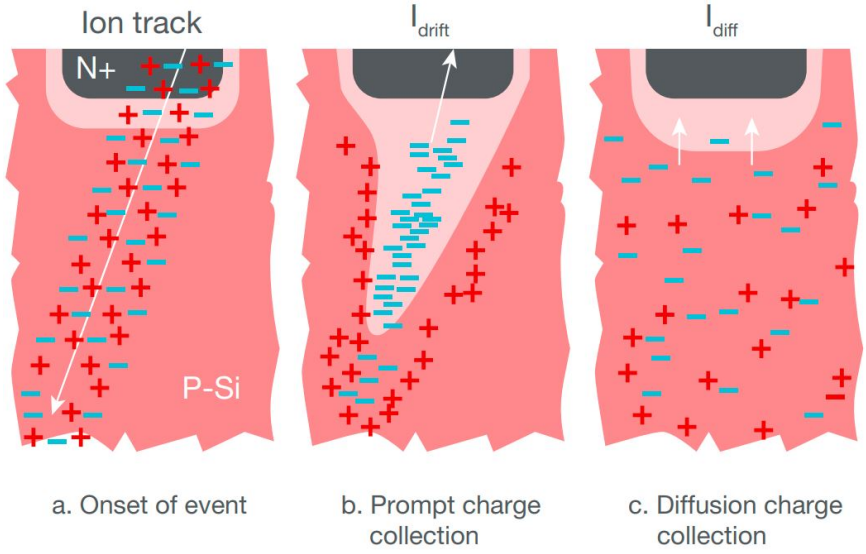
A SEE occurs when a ionizing particle strikes a sensitive region of an electronic device and alters its typical operation under standard conditions. SEEs can influence the operation of both computing electronics and power electronic devices [12]. The concept of the SEE was first proposed by Wallmark and Marcus in 1962. It was predicted that if a device was scaled beyond the 10 μm process, that upon bombardment from cosmic rays, the device would fail as the amount of charge deposited by the cosmic ray would disrupt the operation of the device [61]. The first SEEs in the form of satellite anomalies were identified by Binder *et al.* in 1975. In this work the sensitive transistors of the JK flip-flop circuit were located through the use of a Scanning Electron Microscope beam. The ionizing radiation was generated at depths similar to that of the junction boundaries of the transistors - then confined to an area of approximately 2 μm^2 - simulating the cosmic ray track [62].

In many power devices a reversed bias junction generally creates a far more sensitive region of the device to incident radiation in comparison to a forward biased junction. Radiation detector designers use this knowledge to create devices with high levels of sensitivity to incoming high energy particles through implementing large area reverse biased diodes with a low doped intrinsic layer to maximise the charge-collection effi-

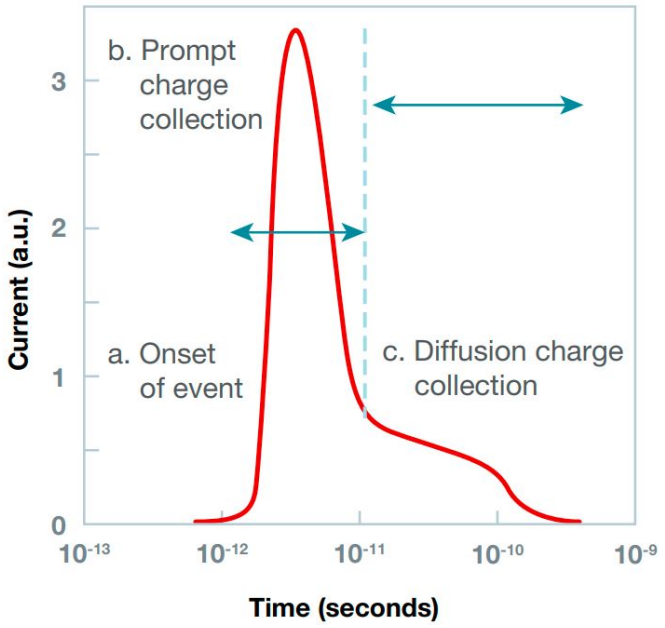
ciency. Even though this is a beneficial feature to radiation detectors, it is potentially a safety critical one for some power devices. When a junction is reverse biased a large depletion region forms, in turn generating a high electric field which separates the electrons and holes from an incident high energy particle on the device - maximising the charge collection at the junction. An example of a reverse biased N/P diode response to interaction with a high energy particle is shown in Figure 2.12. When a high energy ion impacts the reverse biased N^+/P^- junction a trail of electron-hole pairs are generated through the device, this is classed as the onset of the SEE 2.12a(a). When this ionization track is in close proximity to the depletion region, carriers are rapidly separated by the electric field. Electrons are swept to the N^+ node and holes toward the P^+ node (not shown). The influx of electrons injected into the N^+ node produces a large current/voltage transient at that node - corresponding to the current spike shown in Figure 2.12b. A key feature of this interaction is the distortion of the potential into a funnel shape which greatly enhances the efficiency of the drift collection by extending the region of high field deeper into the substrate - occurring over a matter of ns, as shown by Figure 2.12a(b). The funnel size is dependant on substrate doping - the lower the doping concentration of the substrate the greater the funnel distortion. This funnel distortion is then followed by a much slower charge collection process where diffusion dominates, as shown by Figure 2.12a(c). Additional charge is generated as electrons diffuse into the depletion region, usually occurring in the timescale of 100s of ns until all the excess carriers have been collected, recombined or diffused away from the junction. Generally, the smaller the amount of collected charge, the lower the probability of a SEE occurring.

There are two categories of SEE; non-destructive and destructive. The non-destructive SEEs are events which momentarily or permanently change the state of the device without affecting the functionality, these include [65]:

- Single Event Upset (SEU) - the change in state of a circuit caused by a single energetic particle.
- Single Event Functional Interrupt (SEFI) - a SEE that causes a device to malfunction, but does not require power cycling to restore normal operation.
- Single Event Transient (SET) - a momentary voltage or current spike at a node of a circuit caused by the passage of a single energetic particle.



(a) Passage of a high energy ion through a reverse biased N/P diode.



(b) N/P diode transient response.

Figure 2.12: Phases in a reverse-biased N/P diode and the resulting current transient caused by the passage of a high-energy ion through the junction [63], [64].

- Single Event Latch-up (SEL) - an abnormally high-current state in a device or circuit of a device caused by the passage of an energetic particle and leading to localised latch-up in that region.

The destructive SEEs are events which permanently interrupt device function and permanently damage the device, these include Single Event Gate Rupture (SEGR)

and SEB. Some SEEs are of particular interest to the power electronic industry for their characteristics at high electric fields in JFETs, MOSFETs and IGBTs - SEGR and SEB which shall be discussed further.

A Single Event Gate Rupture occurs when the field across the gate oxide for certain MOSFET device bias conditions has an additive relationship to the field created by the separation of mobile charges created by the primary ionizing particle or photon. The electric fields from the applied bias at the terminals, and the electric field from the separated ionizing track charges in this case, make the device especially sensitive to an SEU strike. This can create an electric field that temporarily exceeds the dielectric breakdown field strength of the gate oxide, resulting in a permanently damaged device [66].

2.6 Single Event Burnout

A SEB occurs when an ionizing particle interacts with the atoms within an electronic device in the blocking state, depositing charge in the form of a trail of electron-hole pairs and hence shifting the operating conditions away from equilibrium in a ns timescale, in a similar manner to the SEE. However, the difference between the two device responses is represented in the variation in device current generation. For a SEE the generated current returns to pre-strike levels, whereas, for the SEB the generated current peaks and does not return to pre-strike conditions, instead a self sustaining current will eventually spread throughout the device as the electrons and holes can multiply in regions of high electric field and generate an avalanche of charge – resulting in temperature hotspots in excess of 2000 K and thermal runaway, where device explosion can be a consequence if insufficient quenching measures exist [67].

SEB is a destructive form of SEE and clearly has the potential to disrupt power electronic systems exposed to radiation – one of the most notable being the aerospace sector. To mitigate these potentially catastrophic failures in aerospace applications, system level redundancy is a proven method. However, the influence of a SEB on a power electronic component that forms part of the propulsion system for an aircraft has the potential to be life threatening. At commercial flight altitudes the flux of incident particles originating from cosmic rays is approximately 1000 times greater

than at sea level, placing global pressure on the inclusion of SEE and SEB hardness assurance certification for avionics. The SEB failure of pivotal devices to the aerospace industry are now discussed.

2.6.1 PiN Diode Burnout

Cosmic rays incident on power devices in their blocking region have a probability of causing a Single Event Burnout (SEB). If incident on the device, the cosmic ray will deposit its energy, which is typically in the range of hundreds of MeV, in the device through the creation of electron-hole pairs [68, 69] . If the device is operating in conduction mode, the creation of additional carriers does not have a significant effect on the characteristics. However, in the blocking state, a trail of electron-hole pairs within the field zone shields its interior from the electric field [70]. The voltage drop in the device occurs at the pronounced field spikes at the edge of the trail of electron-hole pairs instead. These field spikes might exceed the critical field strength of the semiconductor and and therefore create more charge carriers through impact ionization, extending the trail of electron-hole pairs. Due to this avalanching effect a dense trail of charge, known as a streamer, develops, locally shorting the device as seen in Figure 2.13. This process occurs in a timescale of approximately one nanosecond. The charge carriers may diffuse away sufficiently quickly so that the shorted region may return back to the blocking state, as shown by the data in Figure 2.13(d). If sufficient energy is deposited into the device to melt it locally, the device permanently loses its blocking capability, leading to a permanently damaged device and, without the provision of fast short circuit protection, a catastrophic failure.

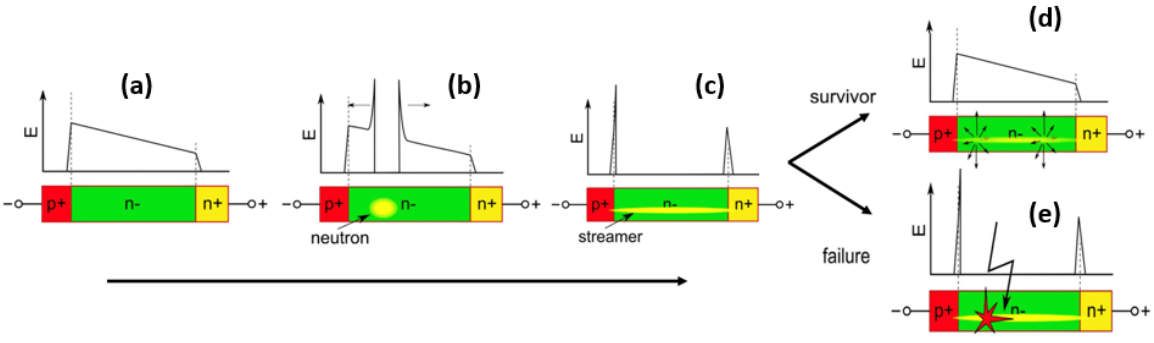


Figure 2.13: PiN Diode Cosmic Ray Failure Mechanism [71].

For power diodes three responses to heavy ion irradiation have been identified, as seen in Figure 2.14 [72] - no permanent effects, a permanent increase in leakage current (degradation) or SEB. All device responses are dependent on the ion energy, device reverse bias, and prior beam exposure. Region 1 is the non-destructive region, where the collected charge increases with applied bias whilst no permanent shift in the device characteristics are observed. In region 2 there is a permanent increase in leakage current which is dependent on the ion fluence - this region is not catastrophic. Region three is catastrophic as SEBs are observed with instantaneous failure of the device.

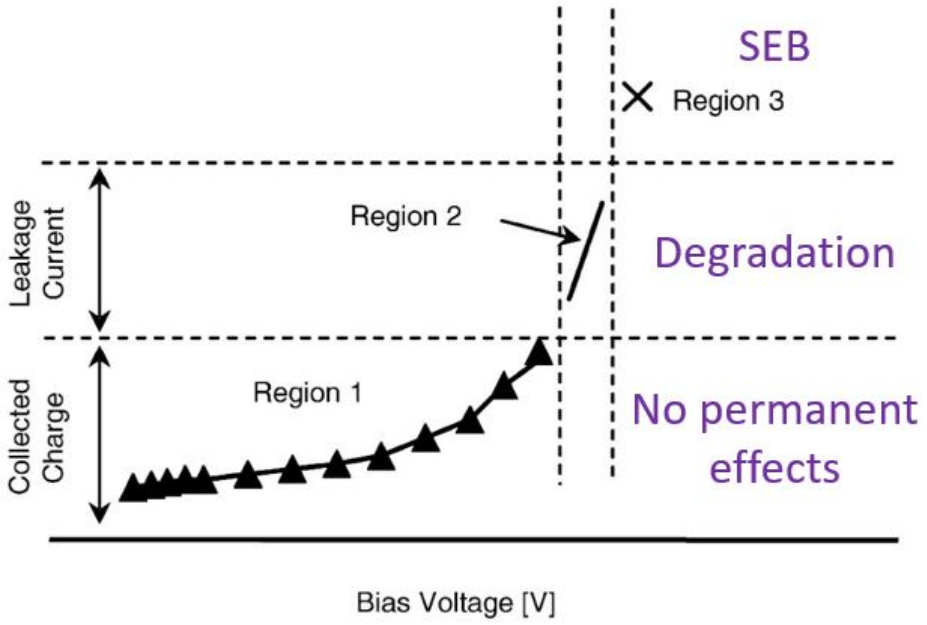


Figure 2.14: Characteristic regions observed by heavy ion irradiations on SiC Schottky diodes (The image was derived from experimental data with Ar ion). [72].

A key issue of heavy ion irradiation when probing the SEB sensitivity of devices is that prior degradation from heavy ions resulted in higher measured threshold at which SEB occurred - an issue observed in the work of Kuboyama *et al.* [72]. When examining the SEB sensitivity of a commercially available Infineon SiC Schottky barrier diode with Ar ion irradiation they found that a pre-irradiated device showed the non-occurrence of SEB at a reverse bias voltage of 340 V. However, for a fresh device which had not undergone any irradiation they identified that when this device was irradiated SEB occurred at a lower reverse bias voltage of 320 V - making it impossible to identify the SEB sensitivity of each device.

The literature has reported on the SEB sensitivity of Si power devices [73]. Casey *et al.* irradiated commercially sourced Si power Schottky diodes held at a range of reverse bias voltages and operating at different forward currents, with a 1233 MeV Xe ion beam. The findings showed that devices tested with reverse bias voltages below 50% of the specified rating are unlikely to undergo SEB failure. Initial research on the SEB sensitivity of SiC devices has also been reported [74]. The data demonstrated evidence of device failure resulting from SEB after exposure to ion LETs as low as 3 MeV-cm^2/mg, (0.02 pC/μm) when the reverse bias was held at values greater than 65% of the device rated voltage. Data published by Lauenstein *et al.* reported that SiC devices show evidence of SEB related failures when the reverse bias is 30% of the specified breakdown voltage for the lowest LET value studied of 3 MeV-cm^2/mg, (0.02 pC/μm).

Through the study of a device response to a range of heavy ion LETs and deposited charges a thorough understanding of its single event sensitivity can be created. Soelkner *et al.* investigated the SEB sensitivity of power diodes, and the data in Figure 2.15 show the charge generated in a 4 kV power diode depending on ion species, ion energy and applied bias [75]. Here, the dashed lines correspond to the threshold of large scale multiplication - the point which results in the occurrence of a SEB. It is planned in this work to utilise this method - the application of a range of heavy ion LETs and device bias conditions - to create a clear impression of the SEB sensitivity of the selected PiN diode studied.

It is therefore of great importance to map the electric field distribution within these devices to determine the most sensitive regions of the devices to SEB. This stage can be performed through the use of simulation studies using TCAD, where, from this, radiation hardening design procedures for the devices can be produced and tested leading to new iterations of the devices being created, eliminating extreme regions of high electric field and in turn reducing SEB sensitivity.

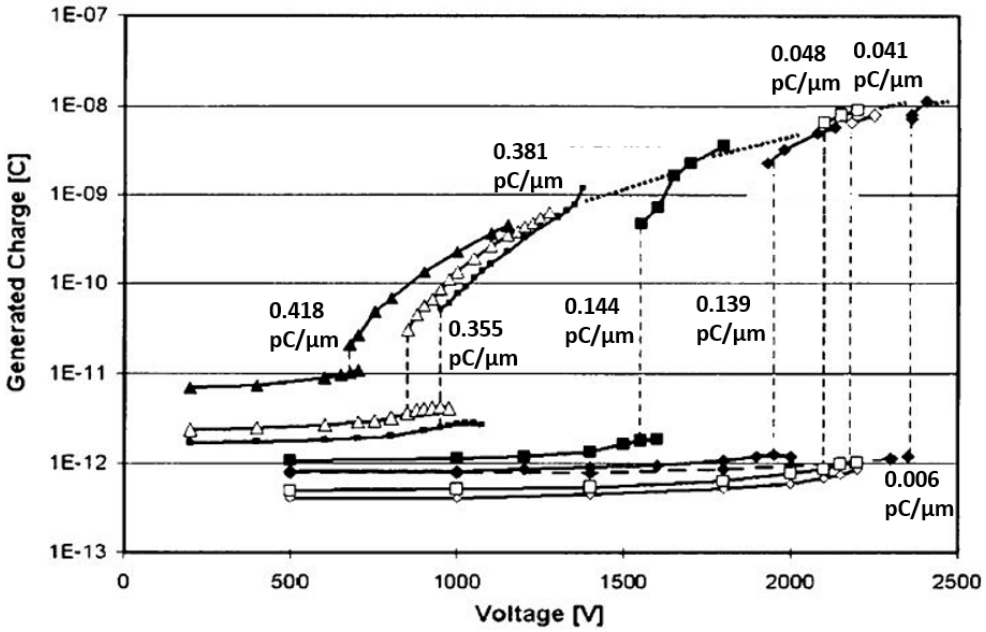


Figure 2.15: Charge generated in a 4 kV SiC power diode for a range of ion species, ion energy and applied bias [75]. Values of LET displayed have been approximated through the use of the stopping range of ions in matter (SRIM) software [76].

2.6.2 MOS Controlled Transistor Burnout

The SEB sensitivity of MOSFETs and IGBTs have been studied extensively over the past 30 years [77, 78, 79, 80]. This section will focus on the SEB sensitivity of both of these MOS controlled device types and their potential suitability for use in future aerospace applications. Firstly, the Si MOSFET shall be the focus.

Si MOSFET devices are the dominant switching device in power electronic applications and require high voltage operation in order to maximise efficiency - an issue when considering the SEB sensitivity of the device. For a MOSFET in the off-state with sufficiently high drain-source bias a SEB will occur when a heavy ion is incident, generating electron-hole pairs in the epilayer. Impact ionised current then turns on the parasitic BJT, creating a feedback loop which results in local temperature rises and melting of Si - the occurrence of a SEB. The Si melting creates a current path that is an order of magnitude more conductive and results in a sudden drop of the drain-source voltage [81], leading to second breakdown and SEB failure of the device. To avoid SEB through the BJT turn-on the additional charge generated by impact ionization in the drain region can be interrupted by quenching the drain voltage be-

fore second breakdown occurs [78] - resulting in an undamaged device. The MOSFET I-V curve depicting a device showing transition from its normal off-state operation into avalanche breakdown, bipolar turn-on then secondary breakdown is shown in Figure 2.16. The Si MOSFET SEB sensitivity is both current and voltage dependent, if enough charge is deposited the device will transition from its normal off-state blocking voltage into its bipolar turn-on state or second breakdown state, resulting in the occurrence of a SEB [82].

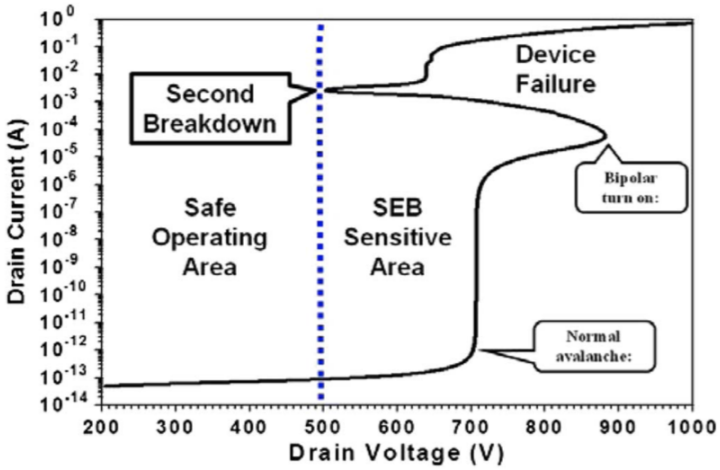


Figure 2.16: Illustration of a MOSFET I-V curve depicting a device showing transition from its normal off state operation into avalanche breakdown, bipolar turn-on then secondary breakdown [83].

Despite the Si MOSFET dominance over the past 50 years, the SiC MOSFET is now in a position to challenge thanks to improvements in the SiC crystal growth methods which have reduced the number of crystal defects - enabling the recent realisation of SiC power devices. For SiC MOSFETs the occurrence of SEB is not dependant on the turn-on of the parasitic BJT, rather, it shows similar SEB sensitivity to that of a SiC diode [84]. This was the focus of the 2015 work by Shoji *et al.* where they simulated ion impacts at a bias greater than that required to induce SEB on both a standard SiC MOSFET and an adapted structure without the inclusion of the n^+ source region (a diode from the MOSFET), as shown by the data in Figure 2.17 - no significant variation in currents or temperatures were shown between the two structures.

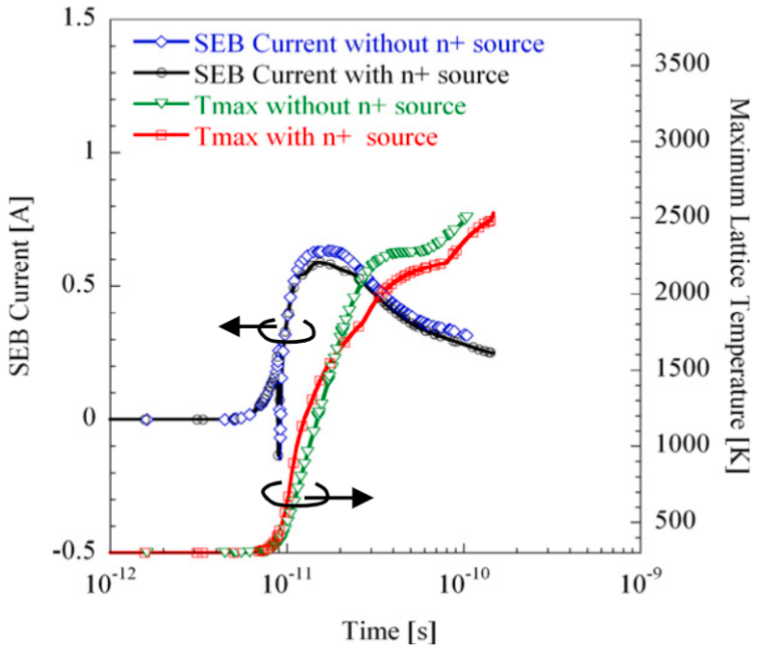


Figure 2.17: Simulated SEB currents and maximum lattice temperatures with and without n^+ source diffusion region in SiC power MOSFET [16].

An alternative structure which is renowned for its high efficiency and fast switching is the IGBT. The Cree p- and n-type SiC IGBTs offer the largest voltage ratings of any semiconductor switching device at 15 kV and 12.5 kV respectively, however, despite the promise of these devices more development is required to improve yields [85]. Limited research on the radiation response of SiC IGBTs has been performed [79], and for this reason, this device type shall not be considered further. The SEB sensitivity credentials of the Si IGBT shall now be discussed. Simulations performed to determine the electrical characteristics of the Si IGBT by Shoji [80] demonstrate the SEB triggering action within devices when they are impacted by ionizing radiation. A schematic of the simulated IGBT cross-section can be seen in Figure 2.18, and data from simulations performed can be observed from Figures 2.19a, the device collector current dependency on collector voltage in time, and 2.19b, the device electric field distribution along ion track after ion impact.

When a IGBT device is impacted by a high energy ion, electron hole pairs are generated along the ion track - which are then accelerated by the electric field in the depletion region at time (2) as seen in Figure 2.19a. The peak electric field strength shifts from the n^- drift/p- body junction to the n^- drift/n^+ buffer junction (nn^+

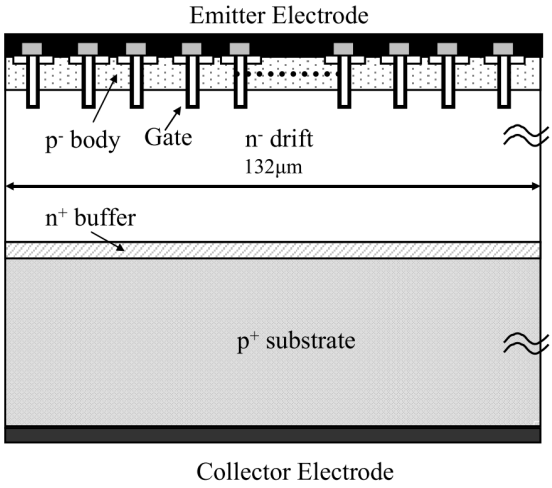
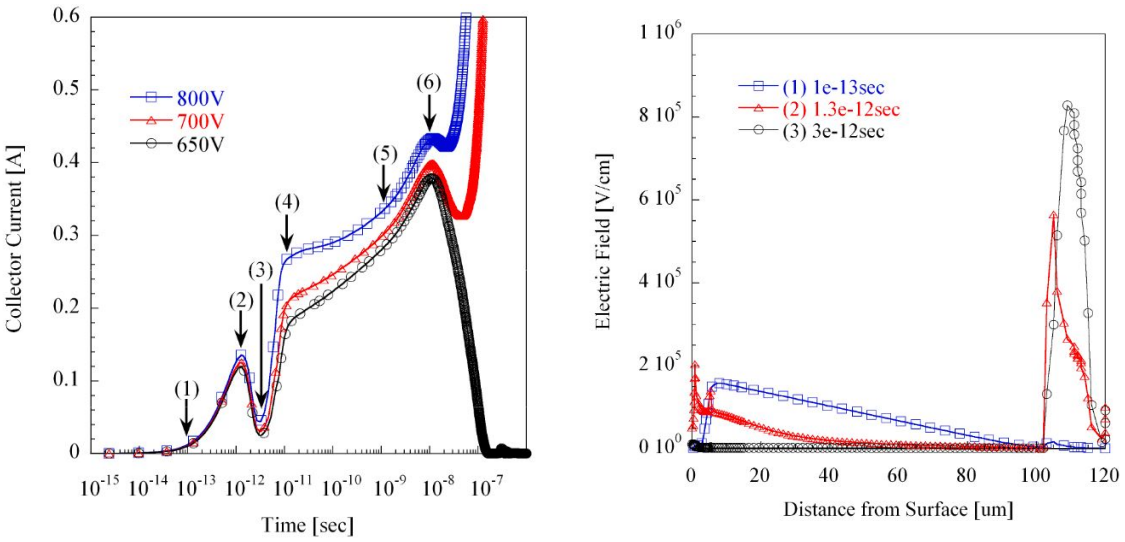


Figure 2.18: Schematic cross-sectional view of a simulated IGBT [80].

junction). Therefore, the electric potential distribution is changed to a funnel-like shape and carriers are generated at the n^-/n^+ junction due to the impact ionization. Injection of the generated carriers into the base neutral region triggers the turning-on of the inherent parasitic pnp transistor (p- body/n- drift/p^+ collector). The hole carriers are injected into the n^- drift region from the backside of the device. At the second current peak at time (6) in fig 2.19a, the inherent parasitic npn transistor (n^+ emitter/p- body/n- drift) turns on, and electrons are subsequently injected into the n^- drift region. Therefore, the electric field strength at the n^-/n^+ junction decreases due to the electron injection at this time. The lowering of the electrical potential between p-body and n^+ emitter junction due to the electron injection leads to a temporary decrease in the collector current. The latch up of the parasitic transistor results in positive feedback of the collector current and leads to device destruction.

The SEB sensitivity of the Si IGBT is poor as shown by the research of Wu *et al.* [86]. Heavy ion simulation studies on a 550 V lateral-IGBT indicated that for charge deposition matching a silver ion commonly used in SEB testing, that SEB would occur at collector-emitter deratings as low as 5%. Additionally, the oxide of the IGBT is also responsible for the failure of the device. In an experimental investigation Wei *et al.* studied the radiation response of a 600 V trench IGBT under heavy ion charge deposition conditions at twice that of Wu *et al.* [87]. The Gate oxide failure of the device occurred at a collector-emitter derating of 17% - due to the accumulation of holes at the bottom of the trench gate increasing the electric field.



(a) Collector current dependency on collector voltage in time.

(b) Electric field distribution along ion track at the times shown in Figure 2.19a.

Figure 2.19: Triggering process of SEB in a simulated IGBT [80].

The SEB sensitivity of the SiC MOSFET is superior to that of the Si IGBT. Heavy ion simulation studies of a 1200 V 4H-SiC Power MOSFET by McPherson *et al.* showed that when the device was subject to a silver ion commonly used in SEB testing it underwent SEB at a drain-source derating of 40% [88]. The failure occurred near the interface between the epitaxial layer and the substrate layer due to the rapid increase of the electric field in the region, resulting in the destruction of the device from impact ionization. For the Si MOSFET the SEB sensitivity is similar to that of the SiC MOSFET. Both experimentation and simulation studies of heavy ion impacts on devices show that when a silver ion commonly used in SEB testing is incident SEB occurs at drain-source deratings as low as 35% [89, 90].

The presence of a gate oxide is known to increase the SEE sensitivity of power devices for a range of incident ion energies. At deposited charges equivalent to 25% of the commonly used silver ion latent MOSFET damage can occur - the creation of leakage current pathways which are of higher sensitivity to further ion impacts [91]. Additionally, SEGR with catastrophic device failure can occur at deposited charges equivalent to a silver ion used in SEE testing. Here devices are destroyed at drain-source deratings as low as 8% when under a heavy ion impact the electric field in the gate oxide becomes equal to the oxide breakdown field [92]. It is clear that the gate oxide, a prominent feature in both MOSFETs and IGBTs, is a weak link in terms of

device sensitivity to radiation - for this reason, the JFET appears to be the device of choice for aerospace power system applications due to the lack of oxide.

2.6.3 Junction Field Effect Transistor Burnout

Typical characteristics for JFET SEB sensitivity and degradation through experimental investigations using heavy ion irradiation is shown by the data in Figure 2.20. Four commercial devices at two different breakdown voltage ratings were tested using low LET ion beams [91]. The columns indicate the voltage range at which no events occurred, and the error bars extend to the next step in voltage at which degradation (green and light-grey columns) or SEB (red and black columns) occurred. It can be seen that all JFETs tested undergo SEB at around $\sim 40\%$ of their rated breakdown voltage with the onset of degradation occurring between 30% and 35% of BV_{DS}, the drain - source breakdown voltage. The normalised data show the importance of the internal electric field on degradation and SEB onset.

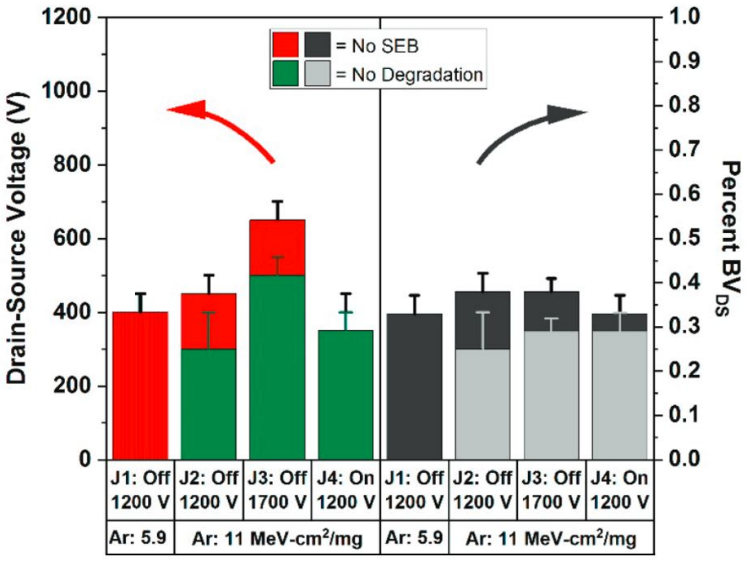


Figure 2.20: JFET SEB sensitivity data showing the maximum V_{DS} at which no current degradation or SEB occurred for 4 commercial devices at low heavy ion LETs [91]. Data plotted for absolute V_{DS} (left) and normalised to the rated device breakdown V_{DS} (right).

Device SEB sensitivity is dependent on the location of radiation impact [93] - for the JFET there are two main potential heavy ion impact locations to result in the occurrence of SEB, both shown schematically in Figure 2.21. The first is a heavy ion

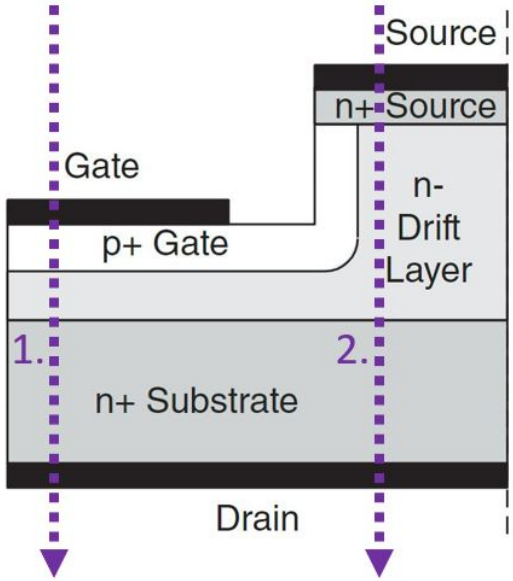


Figure 2.21: Vertical JFET structure [9] with 2 main heavy ion impact locations with the potential to induce SEB.

impact between the gate and drain nodes, whereas the second is caused by an impact through the channel region between the source and drain, which results in damage to the gate. Depletion region dimensions play a key role in determining which of these impact locations is more likely to cause SEB and so this will therefore vary on a device-by-device basis. In this work the sensitivity of JFET SEB response is studied by controlling the heavy ion impact location.

2.7 Radiation Hardened Device Sensitivity

Radiation Hardened (RadHard) devices are components which have been designed for a specific application whilst withstanding enhanced levels of radiation in comparison to Commercial off-the-shelf (COTS) and non-hardened equivalent devices. Device shielding is the primary method used to eliminate or reduce radiation effects on components, in industrial and medical applications operating in radiation environments. However, this is not practical for aerospace applications, as the level of shielding required adds too much mass to the components and systems. Alternative methods used for device hardening are Radiation Hardening by Process (RHBP) and Radiation Hardening by Design (RHBD) solutions. A RHBP solution relies on modifying the baseline semiconductor process - resulting in an improvement to the

device hardness without modifying the design. Alternatively, RHBD can be used to reduce SEB by making structural and doping changes that reduce the maximum electric fields within the device which in turn reduce the amount of charge produced by avalanche multiplication [94, 95]. Guard ring structures can potentially be used, as they have been designed to reduce the electric field at regions of high electric field within the device. However, research has shown that these structures can be prone to inducing SEB when included as a feature of the device. Research by Theiss *et al.* on the SEB sensitivity of a Si Schottky diode through heavy ion simulation found that ion impacts close to the guard rings resulted in the highest maximum device temperature [96]. This failure mechanism has been described as a negation of the effect of the guard ring due to the high concentration of ionised charge along the ion track - allowing the formation of high electric fields within the device at the edge of the anode. The simultaneous existence of high charge density, high electric fields and high voltages can enhance the generated charge from impact ionization - leading to device melting and catastrophic failure, therefore casting doubt on the suitability of guard ring inclusion in device design in an attempt to reduce SEB sensitivity.

Both RHBP and RHBD radiation hardening solutions prove costly due to additional manufacture costs and radiation characterisation to validate their reliability in radiation environments with some parts costing over £40,000 [97]. Companies who invest in RadHard devices tend to use them for a long time, sometimes a number of years after the technology was first created. An example is the technology on-board the NASA Perseverance rover which uses the same processor as an iMac from 1998, costing over $200,000 to produce [98]. A key feature here is that the technology is produced to ensure the highest levels of reliability possible at whatever the cost.

The current market leaders with respect to RadHard devices are STMicroelectronics and Infineon. STMicroelectronics offer RadHard power diodes with TID immunity up to 3 Mrad(Si) and SEB immunity up to 70 MeV-cm^2/mg whereas Infineon have their HiRel Radiation Hard PowerMOS Transistor with TID hardness up to 300 krad and SEB immunity up to 95 MeV-cm^2/mg.

2.8 Simulation Background

Simulations can provide initial predictions as to how the device should behave under specific operating conditions. Simulation of SiC JFET devices will enable the identification of the regions of high electric field within the structure; indicating the regions prone to SEB if a cosmic ray were to be incident. Further simulations of cosmic rays incident on the device at an array of energies, and strike locations will give a detailed map of the sensitive regions within the device. A vast array of simulations have been performed on power devices, notable papers include the work of Hohl and Galloway for the SEB of power MOSFETs [99], the work of Sakai *et al.* for breakdowns in JFETs [100] and the work of Shoji in the simulation of devices to analyse SEB triggering mechanisms in the IGBT [101]. The unique benefit of having performed simulations over physical testing is that true SEB data are produced as there is no influence from prior heavy ion strikes which are typical in heavy ion beam testing, as shown in the work of Kuboyama *et al.* [72] discussed in section 2.6.1.

2.8.1 Simulated Device Response To Cosmic Ray Interaction

To gain an understanding of the performance of devices under the influence of cosmic rays, the commercially available Synopsys Sentaurus TCAD software [102] has been used. There are two main branches of TCAD simulation in Sentaurus – process simulation, the creation of a virtual device, and device simulation, the electrical measurement of the virtual device. Sentaurus Process is the TCAD tool used for process simulation and is an advanced 1D, 2D and 3D process simulator for silicon and other semiconductor materials (including SiC) whilst providing advanced calibration to a wide range of the latest experimental results. In Sentaurus Process, which is based on the finite element method for analysis, a number of standard manufacturing process steps such as ion implantation, diffusion, oxidation, etching, deposition etc. are simulated – allowing for the creation of a virtual device. This virtual device has its physical properties discretized onto a nonuniform mesh of nodes and therefore becomes an approximation of a real device.

Sentaurus Device is the TCAD tool used for device simulation and is a featured 2D and 3D device simulator which provides the capability to simulate a broad range

of devices. It can simulate electrical, optical and thermal characteristics of various semiconductor devices whilst incorporating advanced physics models and robust numerical methods for the simulation. Device simulation can be considered a virtual electrical measurement. It models the physical behaviour of the device from the solution of a set of coupled partial differential equations on a discretized geometry. For each iteration, an error is calculated and Sentaurus Device attempts to converge on a solution with an acceptable error.

For an understanding of the response of a real device to bespoke conditions both Sentaurus Process and Sentaurus Device need to be used, as shown in Figure 2.22. The device structure defined by Sentaurus Process contains the mesh information and doping profiles placement – it is handed to Sentaurus Device for electrical simulation. The Command file of Sentaurus Device defines electrical parameters such as external voltages, temperatures, physics models, solutions to be solved etc., and the Parameter file consists of simulation specific parameters. Sentaurus Device outputs a Current file, a Plot file and an Output log. The Current file contains all the current-voltage simulation results and time-domain characteristics, the Plot file contains the spatially distributed fields data and the Output log records all simulation information. A number of Sentaurus Device instances can be used consecutively to provide an understanding of how the device would response to real world conditions.

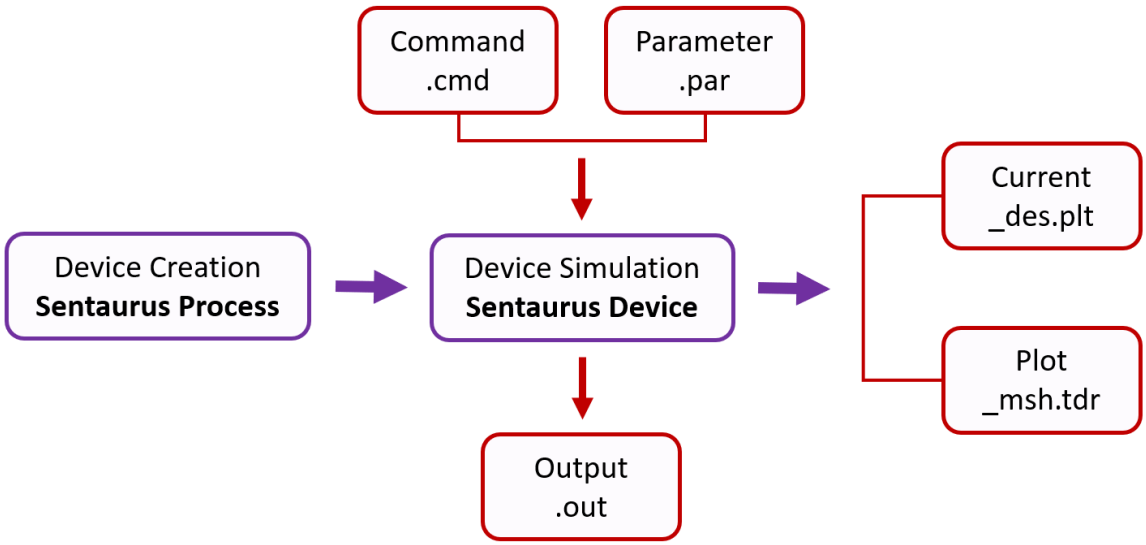


Figure 2.22: Flowchart of Sentaurus TCAD tools used to simulated devices in this work.

A unique feature of Sentaurus TCAD is the ability to incorporate additional models into the simulation of the device, in this work, Heavy Ion impacts on the devices studied through transient simulations are emulated. The physics models used in the software can be turned on and off on a case by case basis to suit the nature of the simulations performed, and along with the material parameters used, have all been experimentally validated. In this work the Heavy Ion impact location has been selected to be perpendicular to the device as at this angle of penetration the Heavy Ion has a lager track length in these simulations than if at an off-normal angle, leading to the worst case scenario for a given heavy ion LET. The Linear Energy Transfer (LET) corresponds to the impact that an incident ion would have on the target material in terms of charge deposition - it is the stopping power of the material divided by the material density.

Heavy charged particles interact with matter primarily through the coulomb forces between their positive charge and the negative charge of the orbital electrons within the absorber atoms. Upon entering an absorbing medium, the charged particle immediately interacts simultaneously with many electrons. For each interaction the electron feels an impulse from the attractive coulomb force as the particle passes its vicinity. Depending on the proximity of the encounter this impulse may be sufficient to ionize the atom, where an energy transfer would result in a reduction in the particle velocity. The particle interacts with many electrons and does so until it stops. The rate at which the particle is stopped is known as the stopping power S, the differential energy loss for that particle within the material divided by the corresponding differential path length - it can be described by the Bethe formula [103]:

$$S = -\frac{dE}{dx} \propto \frac{z^2}{v^2} NZ \tag{17}$$

where z is the charge of the particle expressed in units of elementary charge, v is the velocity (m/s), and N and Z are the number density and atomic number of the absorber atoms [103]. A plot of the specific energy loss of a heavy charged particle in matter is known as a Bragg curve and is shown in Figure 2.23. When the particle enters the matter, the energy loss increases as the particle penetrates further into the material due to its velocity decrease, from equation 17. Near the end of its track

electron binding occurs and the curve falls off. The rate of energy transfer of a heavy ion traversing a semiconductor in this work is considered to be uniform along its path - this is unlike that of the real world interaction with matter and is a key assumption.

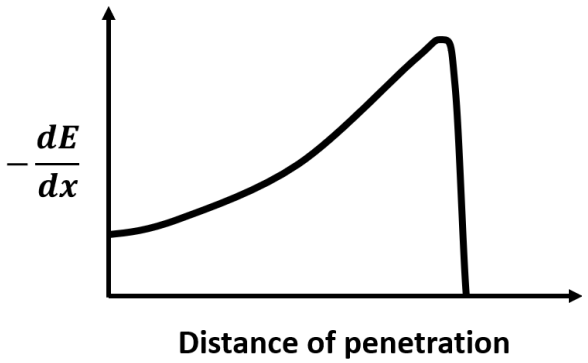


Figure 2.23: The specific energy loss along a heavy ion track [103].

When a heavy ion penetrates a device, it loses energy and generates a trail of electron-hole pairs. The number of electron-hole pairs generated before the initial time of transient is added to the carrier densities at the beginning of the simulation - however, here an impact time of 100 ps has been selected after the simulation start time. This generation rate is computed by equation 18 [102]:

$$G(l, w, t) = G_{LET}(l) \cdot R(w, l) \cdot T(t) \tag{18}$$

where *R(w)* and *T(t)* are functions describing the spatial and temporal variations of the generation rate. G_{LET} is the linear energy transfer generation density expressed in pC/μm. The temporal variations of the generation rate *T(t)* is defined as a Gaussian function, equation 19 [102]:

$$T(t) = \frac{2\ \exp\left(-\left(\frac{t-t_0}{s_{hi}}\right)^2\right)}{s_{hi}\sqrt{\pi}\left(1-\mathrm{erf}\left(\frac{t_0}{s_{hi}}\right)\right)} \tag{19}$$

where t_0 is the moment of the heavy ion penetration and s_{hi} is the characteristic value of the Gaussian.

In these simulations, the spatial distribution, *R(w,l)* has been defined as a Gaussian function as described by equation 20 [102]:

$$R(w,l) = \exp\left(- \left(\frac{w}{w_t(l)} \right)^2 \right) \tag{20}$$

where w is a radius defined as the perpendicular distance from the track and w_t is the total track radius (both μm).

3 Single Event Burnout Sensitivity of Key Materials for Aerospace Applications

In order to achieve high efficiencies and power densities in high voltage power electronic systems it is necessary to raise the working voltage of converters, silicon carbide (SiC) has therefore become the material of choice for the realisation of state of the art power electronic devices and systems. This is based on the superlative material properties of SiC, which include the wide bandgap, high critical electric field and thermal conductivity in comparison to silicon. One timely application is the development of electric propulsion for aircraft, an area of significant interest worldwide and the key focus of this work. It is crucial that electronic devices used in aerospace applications are robust against radiation and are reliable under aerospace specific operating conditions. The work reported here describes a significant advance in the understanding of the sensitivity of SiC to incident cosmic rays in real world conditions experienced by electronics used in power systems for aerospace through systematic simulation studies. Additionally, the simulations in this work have been performed with real world voltage deratings and potential cosmic ray impact charge depositions, both matching, and exceeding, the SEB testing conditions used by NASA [104].

It is common to use heavy ion beam testing to determine the SEB sensitivity of devices. This is a form of testing where the entirety, or parts of the device under test are exposed to a highly concentrated beam of ions. The heavy ion properties are determined by a number of factors; the ion species is a result of the injected gas flow, the ion energy is a result of the accelerator at the facility and the beam fluence is determined by the aperture size. Many ions impact the device every second and this method therefore cannot be used to understand the sensitivity to a single heavy ion impact on the device. The advantage of simulations over physical testing in this research field is the ability to remove the influence of prior heavy ion strikes from the data, which are typical in practical heavy ion beam testing - therefore removing the potential for leakage current degradation to influence the SEB threshold of the device. Evidence for this issue was first reported by Kuboyama *et al.* who showed that from prior heavy ion impact the threshold at which SEB can occur is higher [72, 105]. The use of simulation enables the identification of the interaction between the material and a single heavy ion impact, where a highly concentrated

charge region is deposited and the evolution of the electric field and charge cloud can be observed in ps intervals. The reported simulations enable a thorough and systematic investigation in to the influence of the charge deposited by the heavy ion, and the bias conditions of the simulated device, which enables the sensitivity of the device in a range of real world conditions to be determined. Further, through the use of heavy ion simulation, a single heavy ion impact on the device can be isolated and the device response determined in picosecond intervals. This work utilises simulations in this way to create an understanding of how the device performs after heavy ion impact for a range of known heavy ion energies - something that is not possible through physical testing methods.

Only sub-micron shifts of structural features of a power device are required to result in varied SEB sensitivity responses for identical test conditions. In order to understand this SEB sensitivity for all new generations of devices thorough research and investment is needed. A novel feature of this work is the selection of the devices simulated - they match the requirements for use in avionic systems. The research described here is the first to provide insights into the resilience of power electronic devices in this environment; offering contributions to both the scientific and industrial domains. From this, future iterations of these devices will be designed with their SEB sensitivity considered through the findings of this work.

The simulation work mentioned provides an indication of how the device responds to heavy ion impact, however, to further understand the physics of failure for these devices, device region specific responses to localised deposited charge need to be identified. The heavy ion model offers insight into the response of power electronics to potential real world conditions, where a heavy ion deposits a dense charge track which passes through multiple junctions and device regions of interest. The use of this model does not allow for the identification of the specific device regions which have the highest sensitivity to radiation, and therefore, the largest contribution to the overall device response. Hence, to gain further understanding of the device response to radiation interaction, simulations have been performed where charge has been deposited in defined areas of interest within the devices simulated to create charge sensitivity maps - outlining specific regions of the device which are susceptible to enhanced charge generation. Through this, a clear indication of both the radiation response of the material, and the internal device structure, are determined.

3.1 Simulation Purpose and Background

Here, the material response from single heavy ion impacts are determined through the examination of the SEB sensitivity of p-i-n diodes manufactured from Si and SiC for a range of cosmic ray energies that are relevant to aerospace environments, by analysing the generated charge from the respective cosmic ray induced current transients systematically. From this, the optimal operating conditions for both devices in real world avionic applications was determined. Further, a key emphasis has been placed on understanding the transient response of the collected charge within the device, as this enables the determination of the physics of failure for both Si and SiC. As a consequence, the improved SEB resilience of SiC devices as compared to Si in aerospace is demonstrated.

The approach was to focus on the influence of the material properties on the SEE characteristics and therefore a simple p–i–n structure was selected. To ensure consistent breakdown voltages of the diodes different intrinsic region thicknesses were selected at 40.0 μm and 5.0 μm for the Si and SiC devices respectively. The schematic of both the Si and the SiC PiN diode models can be seen in Figure 3.1 and the relevant parameters are summarised in Table 3.1. The breakdown voltage of the diodes was set to 868 V, as can be seen from the data in Figure 3.2. The specifications of the SiC device matches the requirements for use in avionic systems and for a baseline comparison, a Si device had also been simulated with specific device doping and dimensions adjusted to allow for both devices to have matching breakdown voltages.

If a power electronic device were to suffer an impact with a high energy cosmic ray particle when operating in the blocking state, where the internal electric field is close to the critical electric field of the semiconductor, the consequences could be catastrophic - device explosion and potential system failure. The critical electric field, the maximum electric field that a material can support before suffering physical breakdown and unsupported current flow, in SiC (2.07 MV/cm, due to the drift region doping at 10^{16} cm^{-3}) is an order of magnitude higher than that in Si (0.24 MV/cm), which enables the reduction in on–state resistance of power electronic devices, leading to enhanced efficiencies. In this work, thin devices are simulated and therefore the definition of critical electric field cannot be applied in the same way that it is with thicker devices, rather, it is an indication of the severity of the influence of the heavy

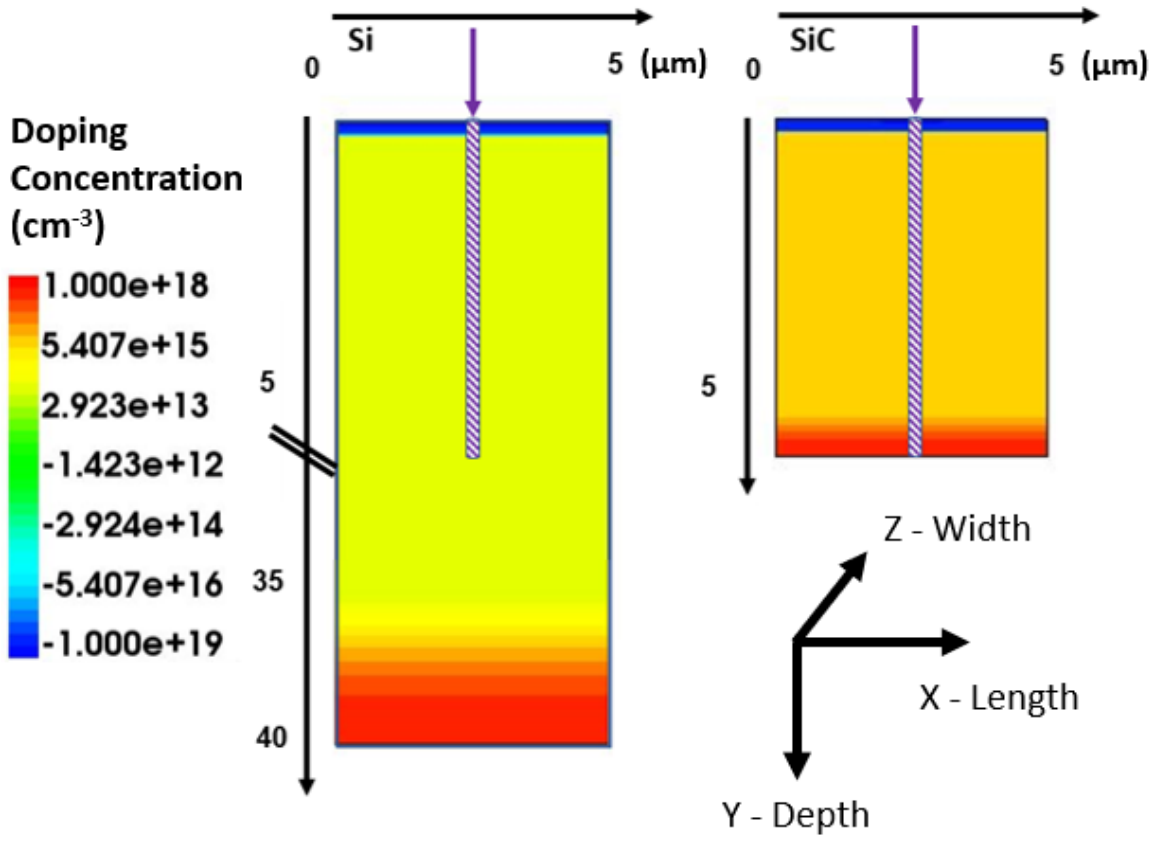


Figure 3.1: Si and SiC device structures with the simulated heavy ion tracks and impact locations.

ion impact on the material response. Regardless of the material, when charge carriers are generated through the device due to ionizing radiation, additional carriers will be generated in regions of high electric field due to avalanche multiplication processes, with a higher electric field resulting in a greater number of carriers.

Single heavy ion injection has been used to determine the response of Si and SiC devices to cosmic ray impacts. To gain an understanding of the performance of devices under the influence of cosmic rays, the Synopsys Sentaurus TCAD software [102] has been used. The parameters used in the heavy ion model are summarised in Table 3.2. For both device types the ambient temperature was set to 300 K. The heavy ion impact location has been selected to be perpendicular to the device as to maximise the heavy ion track length, leading to the worst case scenario for a given heavy ion Linear Energy Transfer (LET) [93].

Table 3.1: TCAD simulation parameters used in this study.

Parameter	**4H-SiC**	**Si**
Material Bandgap	3.23 eV [31]	1.12 eV [106]
Density	3211 mg/cm^3 [9]	2328 mg/cm^3 [107]
Ion pair generation energy	7.8 eV [108]	3.6 eV [109]
Critical Electric Field	2.07 MV/cm	0.24 MV/cm
P^+ Doping/Depth	10^{19}cm^{-3}, 0.25 μm	10^{19}cm^{-3}, 0.25 μm
N-Epi Doping/Depth	10^{16}cm^{-3}, 5.0 μm	10^{14}cm^{-3}, 40.0 μm
N^+ Doping/Depth	10^{18}cm^{-3}, 1.0 μm	10^{18}cm^{-3}, 1.0 μm
Device Length	5.0 μm	5.0 μm
Device Width	1.0 μm	1.0 μm
Active Area	5.0 μm^2	5.0 μm^2

This study focuses on the influence of a highly localised charge region on a device, based on the heavy ion model that is incorporated within the Sentaurus software. This model, rather than depositing small bursts of charge through the device, delivers a highly concentrated charge track, which replicates the electron – hole pairs formed by the incident radiation quanta. This condition can be considered as the most severe charge deposition condition, where the focus is on the correlation between the intrinsic material properties and the resulting SEE characteristics. The use of TCAD simulations allows the distribution of the internal electric field, impact ionization and current densities to be investigated at picosecond timescales to gain detailed understanding of the behaviour of the diode during the impact. This enables the determination of the response of each material to the same impact conditions and the physics of failure to be identified. Electrothermal simulations have been performed to provide a suitable representation of how physical devices would respond to a range of different cosmic ray environments and biasing conditions. The literature show that devices which undergo radiation testing can exhibit a response of internal temperatures exceeding the sublimation temperature of SiC (3100 K [9]), and therefore, it is important that thermal models are also considered in the simulation of these structures [16].

The purpose of these simulations was to observe the variation in response of the different semiconductor material types after cosmic ray impact. Hence, the heavy ion track length has been selected as 6.25 μm - the total depth of the SiC device. Here, an equivalent number of electron - hole pairs are generated in each material. The track radius of 50 nm has been selected as this is a value which is commonly used

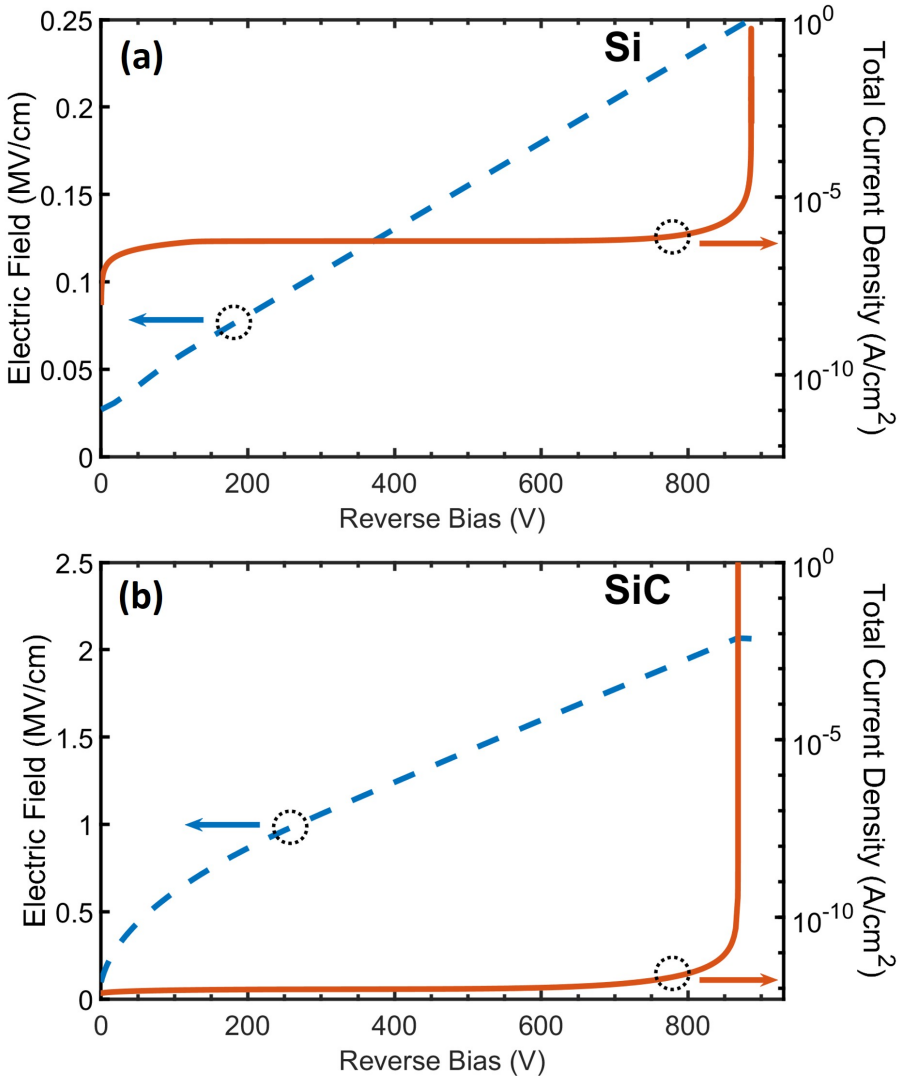


Figure 3.2: Breakdown of a 5 μm^2 device area (a) Si and (b) SiC PiN diodes at 300 K with parameters summarised in Table 3.1. Please note that the electric field in (b) is 10 times greater than that of (a).

in SEE simulations [84] and the initial charge generation time of 100 ps has been selected to provide an example of the device conditions pre-strike. As discussed in the literature review, the generation rate of the heavy ion model consists of functions describing both the temporal and spatial variations of the generation rate. Due to these temporal variations, the generation rate does not return to pre-strike conditions (0 cm^{-3}s^{-1}) until 80 ps after the initial charge generation time.

Due to the nature of the simulations performed here, it was important that a suitable carrier model was selected that caters to the high internal device temperatures

Table 3.2: Parameters for the heavy ion model.

Parameter	**Value**
Track Radius ω_0	0.05 μm
Track Length	6.25 μm
Horizontal Ion Striking Position from origin	2.5 μm
Initial Charge Generation Time T_0	100 ps

expected, with some regions of the semiconductor exceeding 3000 K in some circumstances [104]. Sentaurus TCAD supports several carrier transport models for semiconductors, with each tailored to different applications. Further, this study focuses on high voltage power devices and for these reasons the Thermodynamic transport model had been selected for all simulations performed in this work. In addition to this, the thermoelectric powers in the semiconductors have been calculated through the analytic thermoelectric power model.

To enhance the quality of these simulations, care has been taken to match key properties of the simulated devices to those of known real-world devices. One of these matched properties is the value used for the surface resistance between the semiconductor and the thermodes. The surface resistance is a thermal resistive boundary condition with specific thermal resistance. For these simulations a surface resistance value of 0.005 $cm^{-3}s^{-1}$ has been selected as this is a value which has been experimentally verified for similar physical devices (Rolls-Royce internal technical report).

In this work, transient simulations have been performed to observe the device response to heavy ion impact. The duration of these simulations have been selected to be 100 ns which is a comparable to that of the expected device switching frequency in future electric aircraft power converter systems (beyond 100 kHz) [110]. Simulations have been performed with the device in the off-state as when a heavy ion impacts a device in this condition, it can generate a large amount of charge which can cause localised temperature hotspots, device melting and ultimately device failure. For a device in the on-state, some additional carriers will not cause a significant variation in device response, hence, interest in this type of simulation is limited.

Most flights an aircraft traverse a range of altitudes from sea level to around 40,000 ft, and given that the cosmic ray flux depends on the altitude, a range of heavy ion impact energies have been simulated to obtain knowledge of the sensitivity of the different

materials. The largest heavy ion LET used is three times greater than that of a silver ion with an energy of 46 MeV-cm^2/mg, which is commonly used for SEE testing [111].

3.2 Preparation of the Device Pre-strike

Simulations have been performed for reverse bias voltages ranging from a few percent of the breakdown voltage, through to the industry standard derating of 70%, and up towards 99% of breakdown. When performing comparative studies of two materials with different intrinsic parameters, suitable device structure adjustments can be made to ensure that the simulations are fair. In this study the breakdown voltages of the two structures have been matched to allow for the SiC device to be used as a slot-in replacement device for a traditional power system utilising Si. As the breakdown voltage of a diode is proportional to its drift region width and is inversely proportional to its doping concentration, these parameters need to be adapted for the Si device to match the breakdown voltage of the SiC device. To create a comparable device the intrinsic region of the Si diode had its width increased to 6 times that of the SiC device at 40 μm and doping concentration lowered by 2 orders of magnitude of the SiC device to 10^{14} cm^{-3}. The superior electrical characteristics of SiC are observed in the following potential real world aerospace specific scenario - a 600 V circuit, typically used in power stage applications. The leakage currents of Si and SiC at 600 V are shown in Figure 3.2. The SiC device leakage current density, at 1 pA/cm^2 is 600000 times lower than that of the Si device, at 600 nA/cm^2, in turn, SiC provides lower static losses.

The electric field and current density for the SiC and Si devices as a function of reverse bias are shown in Figure 3.2. The resulting maximum electric fields are 2.07 MV/cm and 0.24 MV/cm respectively, which are of importance when referring to the transient electric field as will be discussed later.

The Okuto-Crowell avalanche model [112] has been selected for both materials. This model incorporates the dead space of the first carrier injected into the high-field region, and thus is more applicable to the current data than purely local models. However, it is noted that in all cases, the dead space, as discussed in section 2.1.2, is a small fraction of the depletion region width. At a derating of 99%, SiC and Si

have dead space values of 0.04 μm and 0.18 μm with depletion region widths of 5 μm and 40 μm, 100 and 200 times greater than the width of the dead space. This model was originally proposed for narrow bandgap materials, however, it has since been adapted for SiC by extracting ionization coefficient parameters from photomultiplication experiments [113, 114], whereas for Si the parameter values from the original work of Okuto-Crowell are used. The model coefficients have been calibrated up to 580 K [113], however it is noted that it is challenging to determine coefficients beyond this temperature. It would be expected that as temperature increases further, the ionization coefficients will continue to fall as a consequence of increased phonon scattering. Thus it has been confirmed that the parametrization continues to reduce beyond 580 K, meaning that the predictions of impact ionization behaviour in this temperature region are reasonable first order estimates. The α and β coefficients are the impact ionization coefficients for electrons and holes respectively, and are used to describe avalanche multiplication by representing the mean rate of ionization per unit distance for a carrier. These coefficients are dependent on the internal electric field, because carriers only gain sufficient energy to result in impact ionization in areas of high electric field [20].

3.3 Device Response

The data in Figures 3.3(a) and (b) show the electric field time evolution along a heavy ion track in both materials biased at 600 V, an industry standard derating to 70% of the breakdown voltage. The simulations have been performed for a heavy ion impact following the parameters summarised in Table 3.2 with a LET of 0.1002 pC/μm, which corresponds to a deposited charge of 0.626 pC, which is equivalent to 30% of a silver ion LET in SiC and 48% of a silver ion LET in Si. This LET value allows a direct comparison to those used in heavy ion beam physical testing as it has a similar order of magnitude to the LET of silver ions. It can be seen from the data in both Figures that the internal electric field profile varies with time for both materials – playing a crucial role on the resulting current density and therefore the magnitude of collected charge at the device terminals. In both cases, the pre-strike electric field is trapezoidal which follows theoretical predictions for p–i–n structures. The SiC data in Figure 3.3(b) are first to be discussed. The 80 ps data show the behaviour when the heavy ion charge generation rate returns to 0 $cm^{-3}s^{-1}$, resulting in a uniform charge

concentration being deposited. The transit of generated carriers to the terminals results in the formation of a 'hammock' profile with the anode peak (at a device depth of 0.25 μm) exceeding the critical electric field leading to enhanced impact ionization. This sustains the current peak displayed in Figure 3.4(b) for a duration of 0.1 ns. Referring to the SiC data in Figure 3.3(b), due to the small drift region in SiC the electric field profile returns to pre-strike (overlapped) conditions within 150 ps. In contrast, the Si data in Figure 3.3(a), at 80 ps, show the electric field profile maximum shifts from the p^+/n- junction deeper into the device as a high concentration of charge is deposited in the first 6.25 μm of the device depth. A prolonged evolution of the electric field profile occurs due to both the smaller pre-strike electric field magnitude and deeper device depth, resulting in a larger carrier transit time. Between 100 ps and 2 ns the profile transforms from a shifted trapezoid to a 'hammock' profile with large electric field spikes observed at the device junctions leading to an elongated high current region as observed in Figure 3.4(a), through enhanced impact ionization in these regions. The electric field profile returns to pre-strike conditions 50 ns after the heavy ion strike.

Single Event Burnout is a form of Single Event Effect in which a single energetic particle strike induces a localised high-current state in a device that results in catastrophic failure and possible device explosion. A heavy ion incident on a device with a reverse bias greater than that required to induce SEB, for the corresponding ion LET, will generate a localised high current state. In this work Single Event Burnout has been defined as when a region of the device exceeds the melting temperature, 1650 K for Silicon or the sublimation temperature for SiC, of 3100 K. At these temperatures the device is no longer deemed to be usable and has undergone irreversible changes. In a system, if this failure was to occur, the result would be a costly and inconvenient unscheduled maintenance activity - even with the redundant back up systems the operation of the aircraft would be restricted.

The total current density after heavy ion impact can be used to predict the ultimate failure of the device resulting from SEB. The data in Figures 3.4(a) and (b) show the transient current density of both device types after impact. For Si, the occurrence of a SEB is observed in the 860 V case, where the characteristics do not return to pre-strike conditions, which is defined here as a current density of approximately 1 μA/cm^2, 0.1 μs after impact. This contrasts with the behaviour of the 600 V and

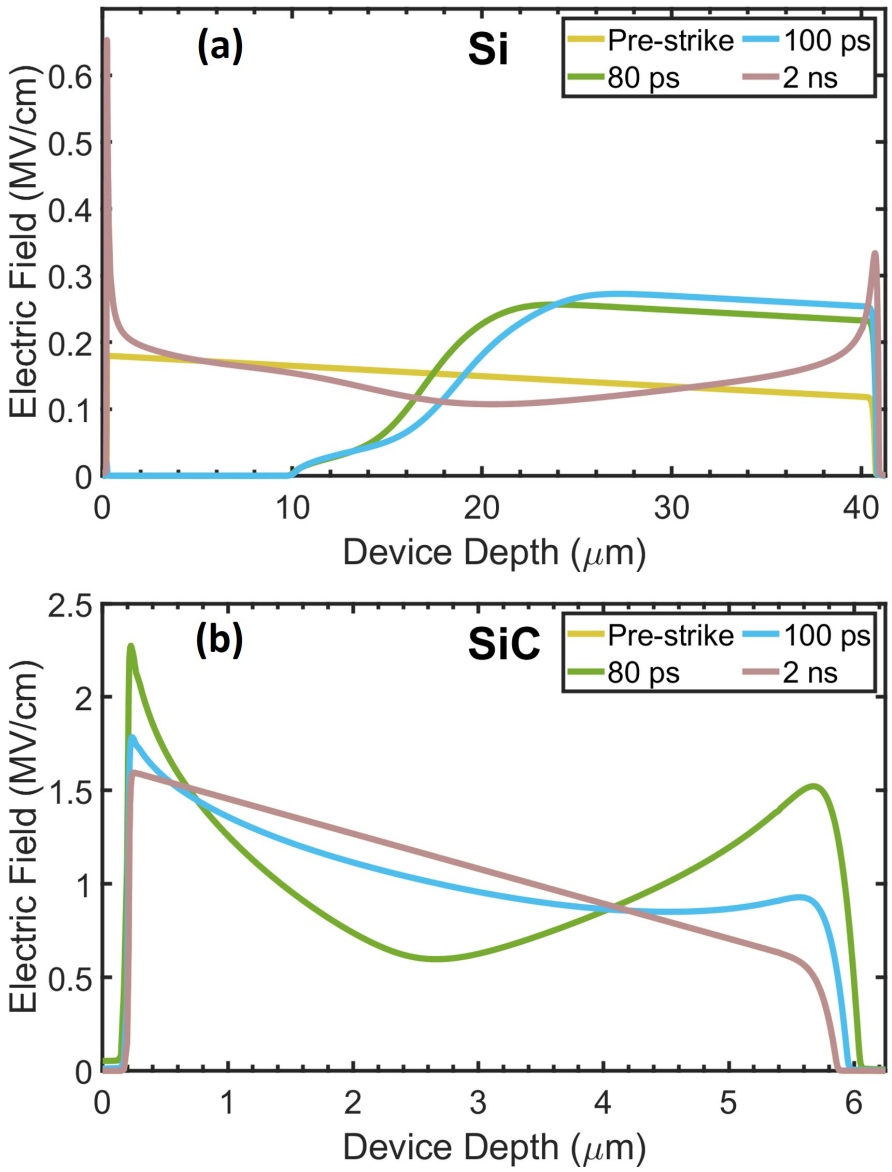


Figure 3.3: Electric field time evolution along a 0.1002 pC/μm LET and 6.25 μm track length heavy ion in (a) Si and (b) SiC, with both biased at 600 V.

400 V cases. The 600 V case is slower to return to equilibrium compared to the 400 V case as the magnitude of the electric field after impact is larger, leading to enhanced current generation over a longer time period. The initial current spike that can be observed in the data at the time of strike increases with increasing bias. A decay of the transient occurs over the next 5 ps, leading to growth towards the maximum value over the next 10 ns.

No indication of SEB is observed in the SiC data shown in Figure 3.4(b). The total

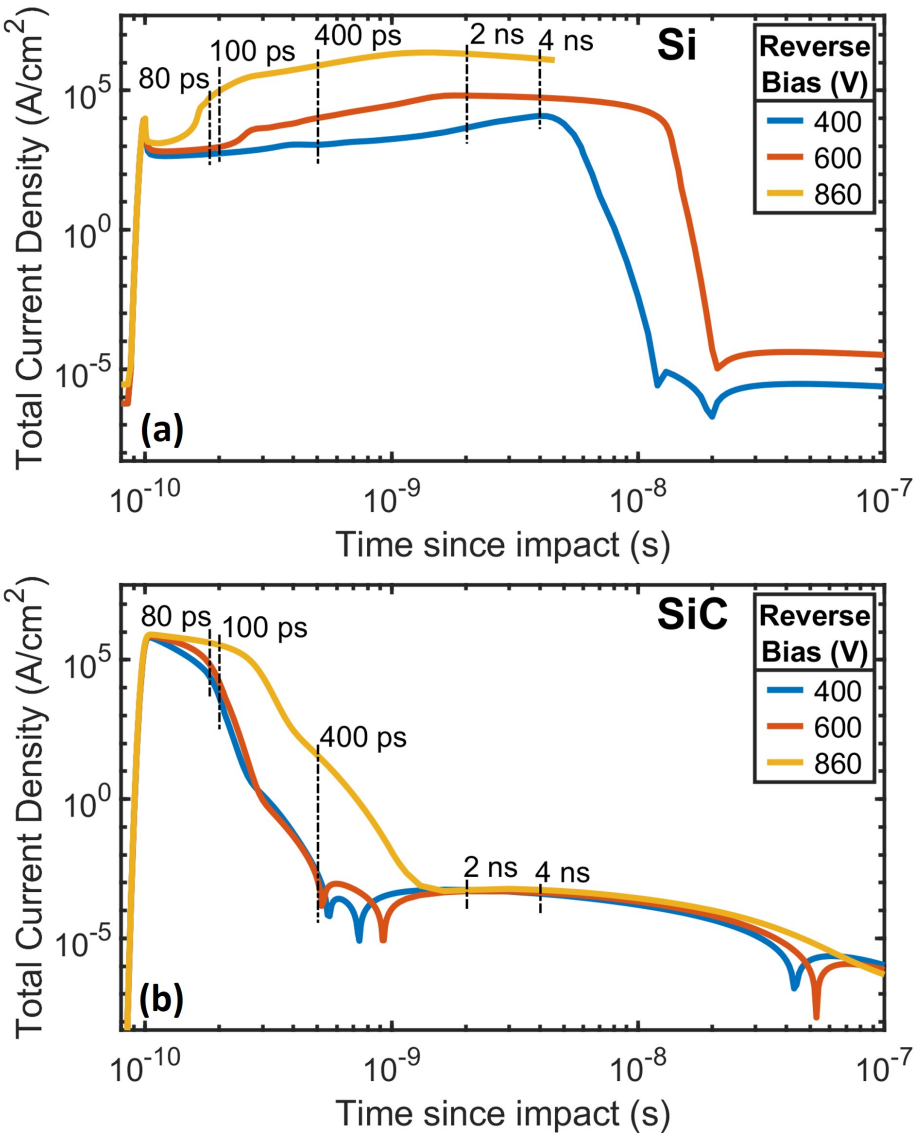


Figure 3.4: Ion-induced transient total current density for a heavy ion with 0.1002 pC/μm LET and 6.25 μm track length in (a) Si and (b) SiC.

current returns to the pre-strike conditions even for the reverse bias of 860 V, 99% of the breakdown voltage. The initial spike in the current density for the SiC device is 50 times larger than that observed in the Si device and the duration increases with increasing reverse bias conditions. This initial spike implies the creation of a low resistance path between device terminals, in SiC which can be observed as a current peak that is sustained beyond the time at which the heavy ion charge generation rate returns to 0 $cm^{-3}s^{-1}$. The duration of this low resistance path is a potential issue when the device is used in a power electronic circuit, as the collected charge at the device terminals could exceed the critical charge to failure - which is a feature of the

destructive SEL [115]. The creation of a low resistance path is not observed in Si due to the drift region width being far greater than that of the heavy ion path length, rather, an increase in current density is observed primarily through impact ionization.

The ion-induced transient total current density internal device snapshots for a heavy ion impact with 0.1002 pC/μm LET and 6.25 μm track length for Si and SiC are shown in Figure 3.5. Here the contrasting behaviours of the two devices are clearly identified - with the 860 V SiC PiN diode showing initial shoot-through at both 80 ps and 100 ps after impact with a 15 MA/cm^2 current track with less than a μm in diameter - a potential location for a temperature hotspot. At these instants the 860 V Si data is starting to show the formation of a current track that does not fully develop until over 400 ps after initial strike. At the lower bias (600 V) condition for Si at 400 ps after impact a higher current has developed and increases slightly over the next 3 ns, prior to a decay to pre-strike current levels. A burnout of the 860 V Si device can be seen at the 4 ns snapshot which is in total contrast to the 860 V SiC device which has returned to pre-strike conditions 2 ns earlier.

The ion-induced transient maximum temperatures for both material types are shown by the data in Figures 3.6(a) and (b). For the Si device, contrasting behaviours are observed. At lower biases the maximum temperature peaks and then decays towards the initial pre-strike temperature, whereas, the 860 V data show thermal runaway, which peaks at 1687 K (beyond the axis limits on the figure) which exceeds the melting point of Si[8]. In contrast, the SiC data show an increase in the maximum lattice temperature with increasing reverse bias, however this returns to the pre-strike temperatures in all cases examined here. The behaviour is due to the greater current in Si shown in Figure 3.4(a).

The total integrated charge collected following impact as a function of heavy ion deposited charges (equivalent to the LET in pC multiplied by the track length) are examined to compare behaviours of the Si and SiC devices as shown by the data in Figures 3.7(a) and (b). The total collected charge is determined by taking the integral of the current transients measured at the cathode contact for 100 ns after impact. For Si, Figure 3.7(a), the data show the dependence of collected charge on applied voltage, with lower values of Q_{dep} requiring higher bias conditions to trigger multiplication which is in line with data in the literature [55]. As can be observed

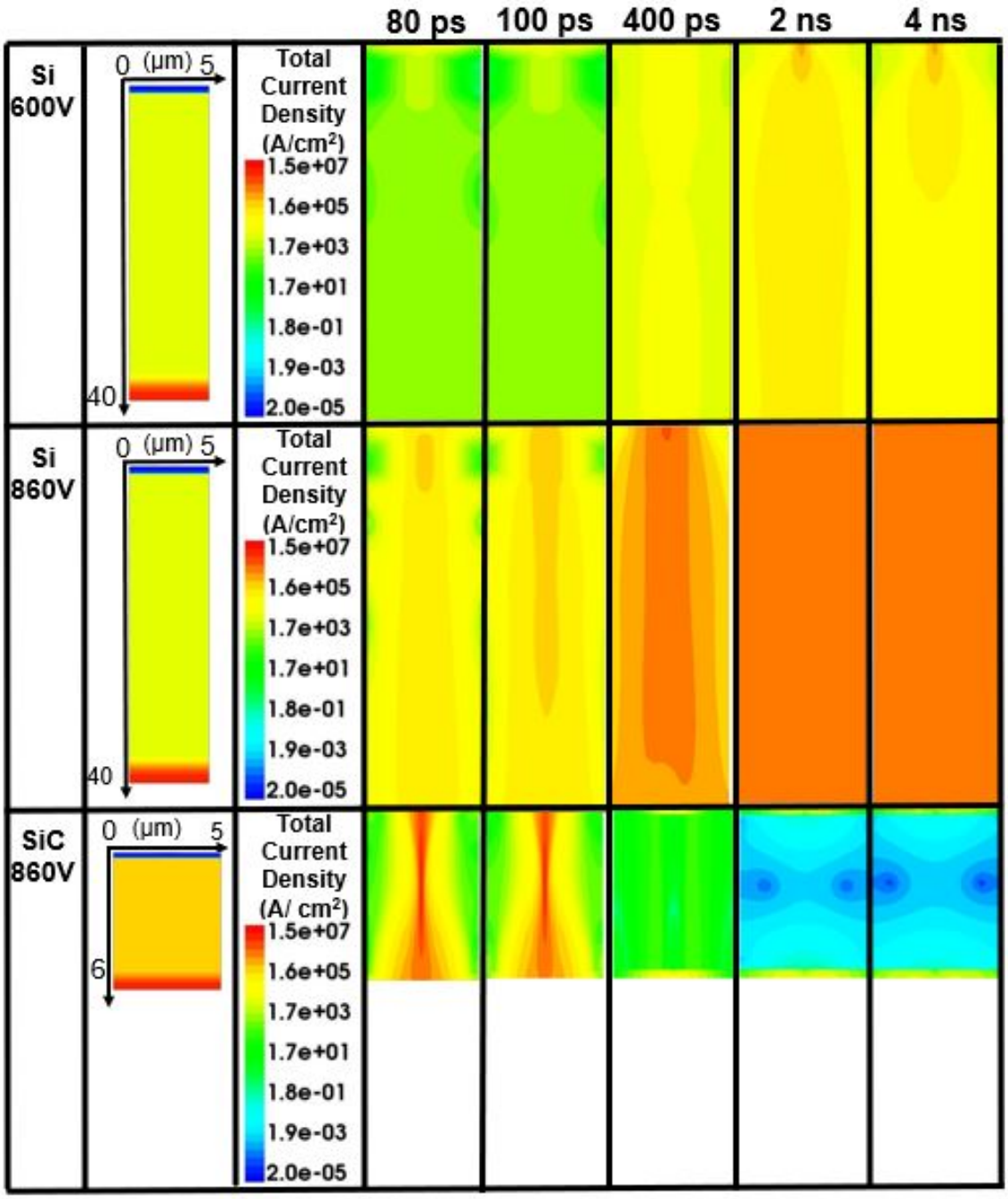


Figure 3.5: Internal device snapshots of Total Current Density at key intervals after initial heavy ion impact for Si (600 V and 860 V) and SiC (860 V).

from the data, collected charge exceeding 400 pC indicates failure of the device - the lowest collected charge value to result in device melting. The data show that the failure of the device can be observed below the breakdown voltage for heavy ion deposited charges as low as 0.006 pC (0.2% that of the silver ions commonly used in

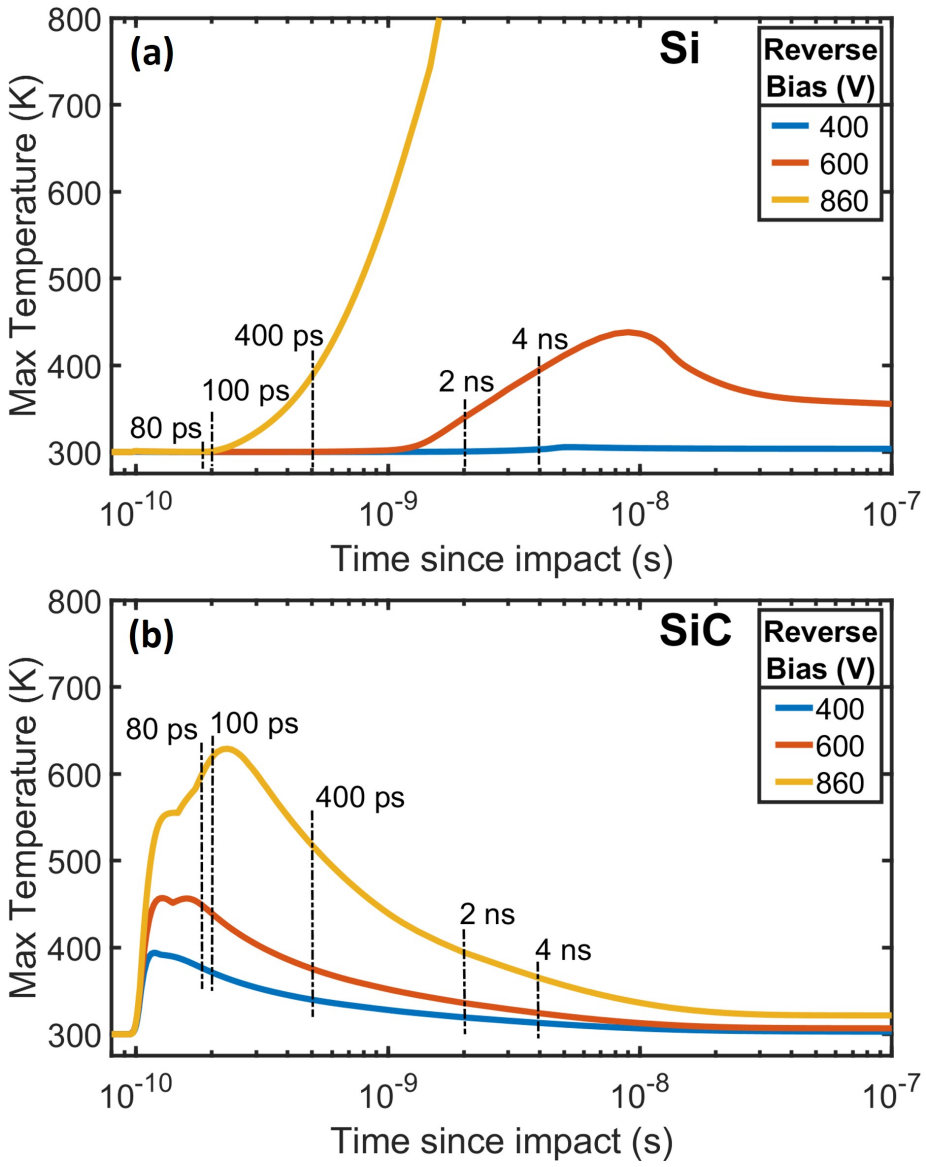


Figure 3.6: Ion-induced transient temperature for a heavy ion with 0.1002 pC/μm LET and 6.25 μm track length in (a) Si and (b) SiC.

SEE testing) when a reverse bias of 800 V is applied. As the value of Q_{dep} increases, the voltage for which failure is observed reduces, such that for Q_{dep} of 6.25 pC (which is equivalent to 300% that of a silver ion commonly used in SEE testing), breakdown occurs at ~60% of breakdown voltage. The data indicate that the failure of the Si device is due to the magnitude and local distribution of the internal electric field after the impact.

In SiC, it can be observed that a sharp jump in charge collected occurs at the breakdown voltage (as would be the case for no ionizing radiation) from Q_{dep} 0.006 pC

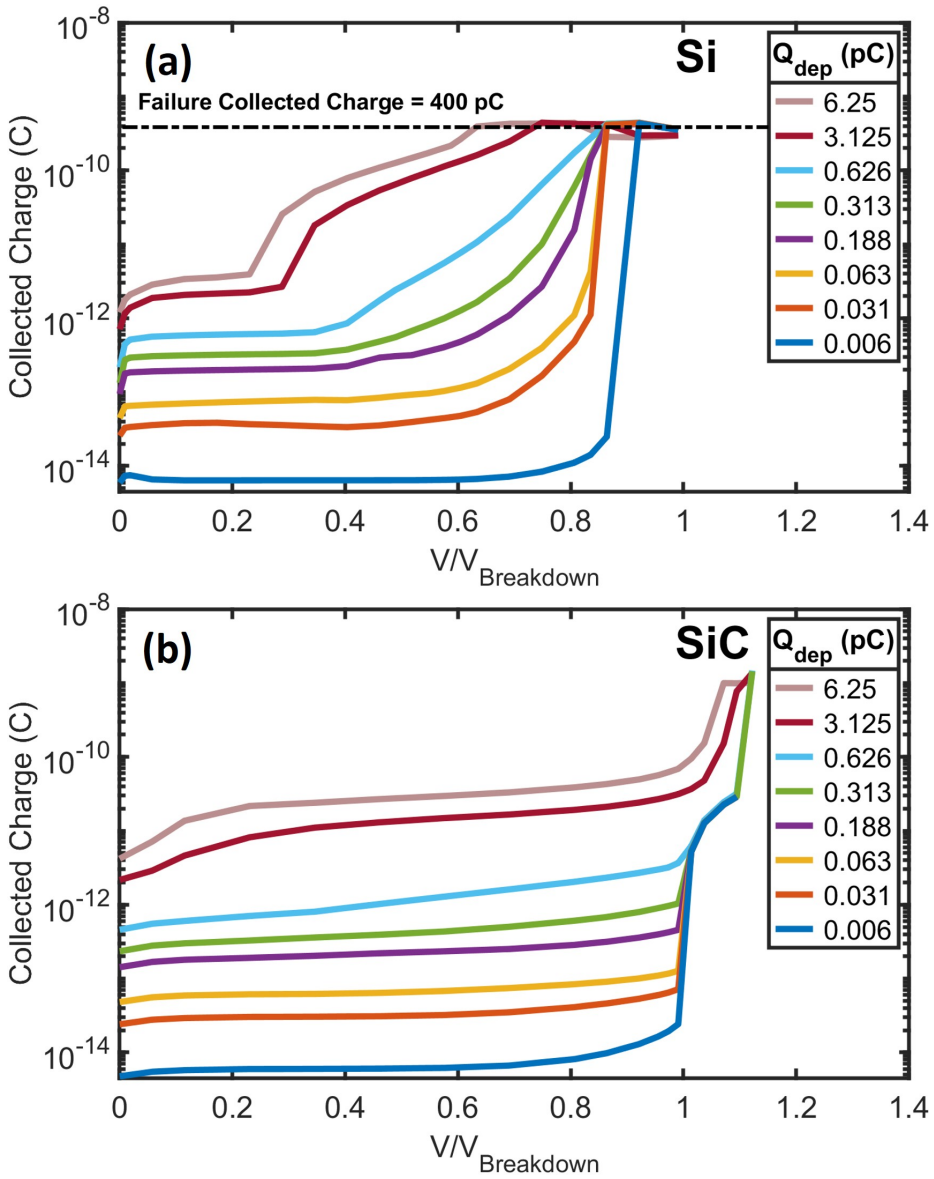


Figure 3.7: Collected Charge after heavy ion transient : (a) Si and (b) SiC.

to 0.626 pC. Hence, these simulations predict that SiC can operate at higher rated voltages even in the presence of a significant heavy ion impact. A failure collected charge is not observed in the data.

It is proposed that the difference in behaviour between the two materials is due to the difference in how the electric field profiles vary after the strike, as shown in Figure 3.3. Si shows significant enhancement of the electric field at the edges of the depletion region following the strike, as can be observed by the data in Figure 3.3(a), in contrast to the SiC data in Figure 3.3(b). To better understand this proposed effect,

the influence of deposited charge on the breakdown of devices is examined. It can be seen from the data in Figure 3.7 that collected charge increases with voltage due to charge multiplication. Therefore, in Figure 3.8, the voltage at which the different multiplication factors are observed as a function of deposited charge to allow for direct comparison between Si and SiC has been plotted. Here, M is the ratio of the charge collected to the charge deposited in the device for Si and SiC diodes. The data indicate the voltage for which a multiplication of M is achieved for a given heavy ion deposited charge. The ideal behaviour is that the lines would not show a dependence with the deposited charge, indicating that charge multiplication is insensitive to the incident radiation. It can be seen that this is largely the case for SiC, with decreasing voltage only evident for small multiplication values ($M = 2$ and 5) as the deposited charge increases. Further, it is observed that M increases with deposited charge at higher voltages, indicating the device is more robust to failure. For the Si device it can be observed that at higher deposited charge a lower applied reverse bias is required to result in the same value of M being achieved. This indicates that the maximum allowable reverse bias for the Si device to be resistant to all of the heavy ion conditions simulated is 61% of the breakdown voltage. In contrast, the SiC device does not demonstrate charge multiplication values of 10, 50 and 100 for reverse bias values below the breakdown voltages, even for high deposited charge values. Further, for the SiC device a 60% reduction in cosmic ray sensitivity to the highest energy heavy ion impact simulated is shown when the $M = 10$ line is considered due to the higher bias required to result in this multiplication in comparison to the Si device.

However, the data in Figure 3.8 show that for the $M = 2$ case at high levels of deposited charge, the Si device can operate at a higher reverse bias prior to resulting in the same charge multiplication value as for the SiC device. Here, the current transient for the SiC device is dominated by the shoot-through current which is generated by the heavy ion - alterations to circuit design will remedy this issue. This condition may be considered an extreme limit for the simulations and is therefore not a cause for concern.

In order to understand the spatial variation in device sensitivity to SEB further simulations focusing on the device-region specific response have been performed.

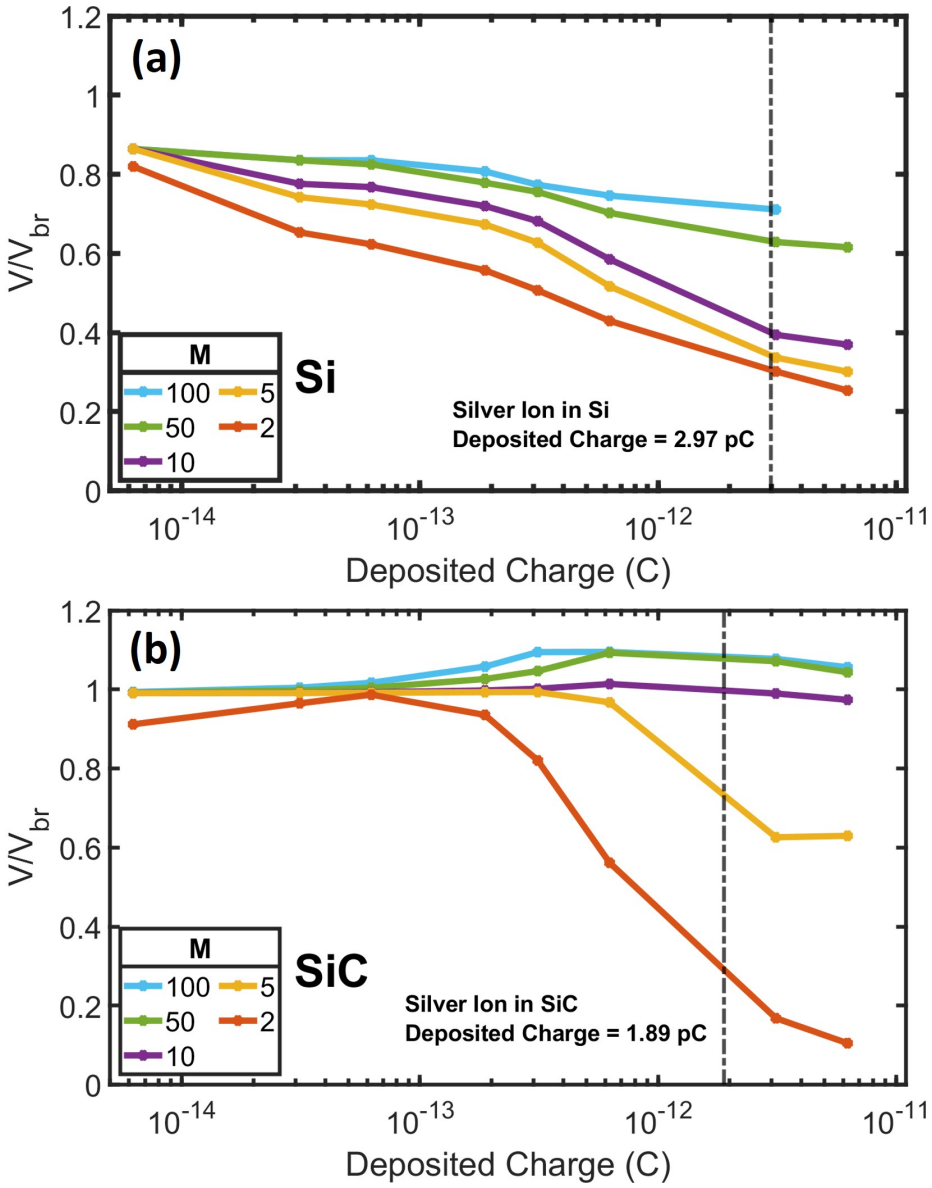


Figure 3.8: Charge multiplication after heavy ion transient : (a) Si and (b) SiC. The deposited charge from a Silver ion commonly used in SEE testing is displayed for both materials.

3.4 Highly localised Deposited Charge Simulation

Simulations have been performed where a highly localised region of charge has been deposited within the device and the response analysed - providing an insight into the contribution each region of the device provides towards the overall device response - examining the depth profile of the device sensitivity to SEB. These simulations have been performed at a number of locations spaced throughout the device depth (9 for

Si, 11 for SiC due to structural variations). Here, Silicon has again been used as a baseline comparison for the SiC device response. From this, an impression of the response to radiation of more complex structures can begin to be understood.

It has been shown that the device response to radiation is reliant on the internal electric field - with higher fields resulting in higher values of charge multiplication of the same magnitude of deposited charge. Here, the variation of this internal electric field with depth from the device surface has been studied by depositing charge at a number of key regions of interest within the device. As the heavy ion model generates a dense charge track which passes through multiple junctions and device regions of interest, this alternate method avoids this. For this reason, depositing charge in highly localised device regions identifies the contribution of each of these regions of interest to the overall radiation response of the device. To provide a direct comparison with the heavy ion simulations described earlier in this chapter, the same magnitude of charge is deposited in a smaller region.

3.5 Device Region Specific Response

The local charge deposition simulations have been performed with parameters summarised in Table 3.3. Two voltage conditions have been simulated for both the Si and the SiC devices, 600 V, a 70% industry standard derating and 860 V, 99% of the breakdown voltage. The eight different deposited charge values have also been simulated as they cover a wide range of potential interactions between a device in-situ whilst in operation.

Table 3.3: Parameters for the local charge deposition study.

Parameter	**Value**
Track Radius ω_0	0.05 μm
Track Length	1.0 μm
Horizontal Ion Striking Position from origin	2.5 μm
Initial Charge Generation Time T_0	100 ps

First, the 600 V Si case is examined, Figure 3.9(a), which is at an industry standard derating of 70%. SEB failure occurs at a number of conditions for the Si device with the lowest value of collected charge required to result in this failure at 340 pC. In

comparison to the standard heavy ion impact simulations, where deposited charge values of 6.25 pC and 3.125 pC resulted in the SEB failure of the device, where a region of the device exceeds the melting temperature of Silicon at 1650 K, here, the location of the deposited charge does play a role in the sensitivity of the device response.

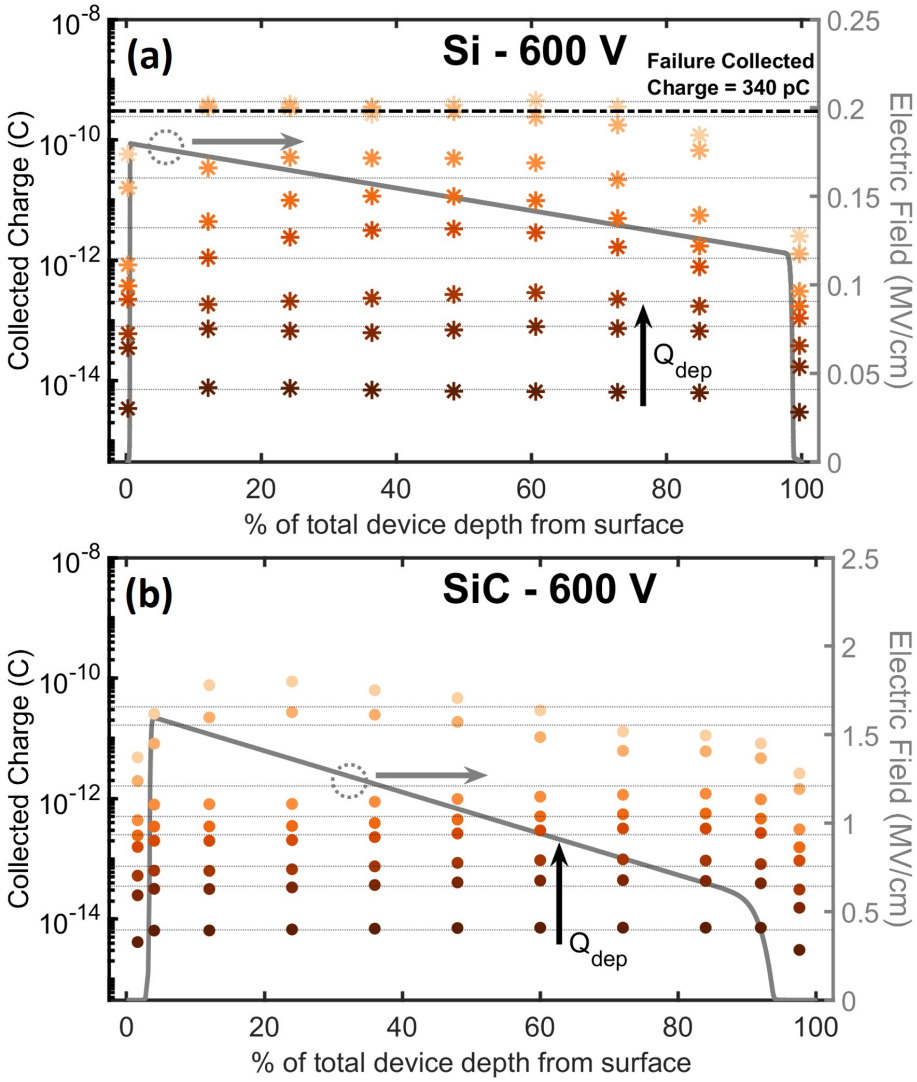


Figure 3.9: Collected charge for a range of local charge depositions from 0.006 pC (brown) to 6.25 pC (magnolia) in SiC at 600 V, a 70% industry standard derating. Corresponding pre-impact electric field profiles are shown as an underlay. Collected charge values from the corresponding traditional heavy ion impacts are shown as dashed lines ranging from 0.006 pC to 6.25 pC. Please note the electric field variation between the local charge depositi in figures.

For the Si device 600 V local charge deposition simulations, as shown by the data in Figure 3.9(a), reduced sensitivity is shown at the extremes of the device depth - near the top surface within 1% of the device depth and near the back surface of the device between 85% to 100%. A limited influence from the pre-strike electric field on the collected charge is shown. In comparison, for the 600 V SiC case, shown in Figure 3.9(b), no SEB failure is observed and a correlation between the pre-impact maximum electric field and the collected charge for Q_{dep} values of 6.25 pC and 3.125 pC is shown - indicating that charge deposition in regions of higher electric field result in higher values of collected charge. The maximum collected charge for a Q_{dep} value of 6.25 pC is shown at 24% of the total device depth from surface, at 88 pC which is 2.7 times that observed from the standard heavy ion impact simulations (33 pC). From this maximum, the collected charge decreases as the % of the total device depth increases to the lowest collected charge of 2.6 pC near the cathode contact of the device. The response of the SiC device is superior to that of a comparable Si device for local charge deposition at a 70% derating, however, SiC is not immune from failure.

Examining an increased bias condition of 860 V for SiC, Figure 3.10, SEB failure is observed over a number of impact locations. Any collected charge which exceeded 360 pC in this condition resulted in the SEB failure of the device, with a maximum temperature exceeding 3100 K. Similarly to the 600 V SiC case, Figure 3.9(b), a correlation between the pre-impact maximum electric field and the collected charge for Q_{dep} values of 6.25 pC and 3.125 pC is shown. At 4% of the total device depth from surface, an impact at the p^+/n- junction, a collected charge of 2400 pC is shown which is more than 30 times higher than the standard heavy ion impact for SiC at 860 V. The collected charge decreases with the increasing % of total device depth from surface from the maximum to the minimum at 98% of total device depth from surface, a value of 15 pC. The superiority of SiC is further shown through the lack of the inclusion of the 860 V Si data - all conditions excluding a handful of very low LET simulations at the extremes of the device, where the internal electric field is at its lowest, lead to melting of the device and SEB.

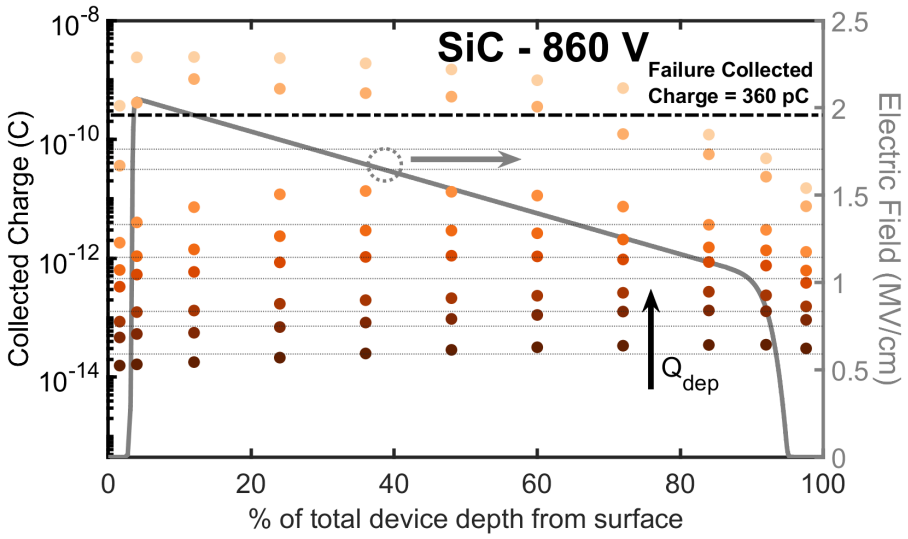


Figure 3.10: Collected charge for a range of local charge depositions from 0.006 pC (brown) to 6.25 pC (magnolia) in SiC at 860 V, 99% of the breakdown voltage. Corresponding pre-impact electric field profiles are shown as an underlay. Collected charge values from the corresponding traditional heavy ion impacts are shown as dashed lines ranging from 0.006 pC to 6.25 pC. Please note the electric field variation between the local charge deposition figures.

The variation in response to the different charge deposition methods, the standard heavy ion impact used in section 3.1 to section 3.3 and the highly concentrated local charge deposition used in this section, can be seen for SiC in Figure 3.11. The data have been calculated by taking the collected charge for the corresponding standard heavy ion impacts and then subtracting the collected charge from the highly concentrated charge deposition simulations. Here two charge deposition conditions and two device bias conditions have been considered, the 0.1002 and 1.0 pC/μm (0.626 pC and 6.25 pC deposited charge, denoted by + and • respectively) with 600 V and 860 V (70% and 99% voltage deratings, denoted by the black and red markers respectively). Figure 3.11(a) shows that for the lower deposited charge condition that a higher bias results in a large variation between the standard heavy ion impact and highly concentrated local charge deposition collected charge values - indicating the magnitude of the internal electric field in these regions. For the 600 V case all highly concentrated charge deposition simulation values return collected charge values below that of the standard heavy ion impact. At the extremes of the device a decrease in the % of collected charge to that of the standard heavy ion impact is observed with 73% and 81%

reductions for the impacts closest to the anode and cathode contacts respectively (2% and 98% of the total device depth from surface). As the % of the total device depth increases the % of collected charge variation reduces from the lowest, a 51% reduction, at a depth from surface of 4%, through to the highest closer to the cathode contact at a 25% reduction at a 84% device depth from surface. At a higher bias of 860 V there are low values of collected charge at the device extremes at a 51% reduction and a 65% reduction at total depths from surface of 2% and 98% respectively. As the % of the total device depth increases from the anode, a peak in the % collected charge variation occurs. At 36% of total device depth from the surface a 269% increase in the collected charge variation is observed - indicating the creation of extreme electric field peaks at the centre of the device which lead to enhanced impact ionization.

For a higher deposited charge in Figure 3.11(b) an extreme variation in the two collected charge values is shown. For the 600 V case a similar response to the 0.626 pC deposited charge simulations are shown. A decrease in the % of collected charge is observed at 85% and 75% reductions for the impacts closest to the anode and cathode contacts respectively (2% and 98% of the total device depth from surface). An increase in the collected charge is shown peaking at 166% at 24% of the total device depth from the surface. The magnitude of the this peak is amplified at a higher bias of 860 V. At a 12% depth from the device surface a 3430% increase in the collected charge is observed, resulting in device failure. For all device depths from surface between 12% to 98% the collected charge variation decreased towards that of the standard heavy ion simulation. From these, only impacts at 84%, 92% and 98% device depth from surface did not result in the catastrophic failure of the device - the same outcome as that of the standard heavy ion impact simulation at this value of deposited charge.

Highly localised charge deposition simulations have identified that the sensitivity of the SiC p–i–n device is highest close to the p^+/n- junction and 50% of the total device depth from surface. This is due to the combined effects of the internal electric field which at reverse bias of 860 V has a peak magnitude of 2.05 MV/cm (only 0.02 MV/cm below the critical breakdown electric field) and the additional modification of the electric field after highly localised charge deposition. A remedy to this sensitivity is device derating to 70% where no failures are observed over the range of charge depositions studied.

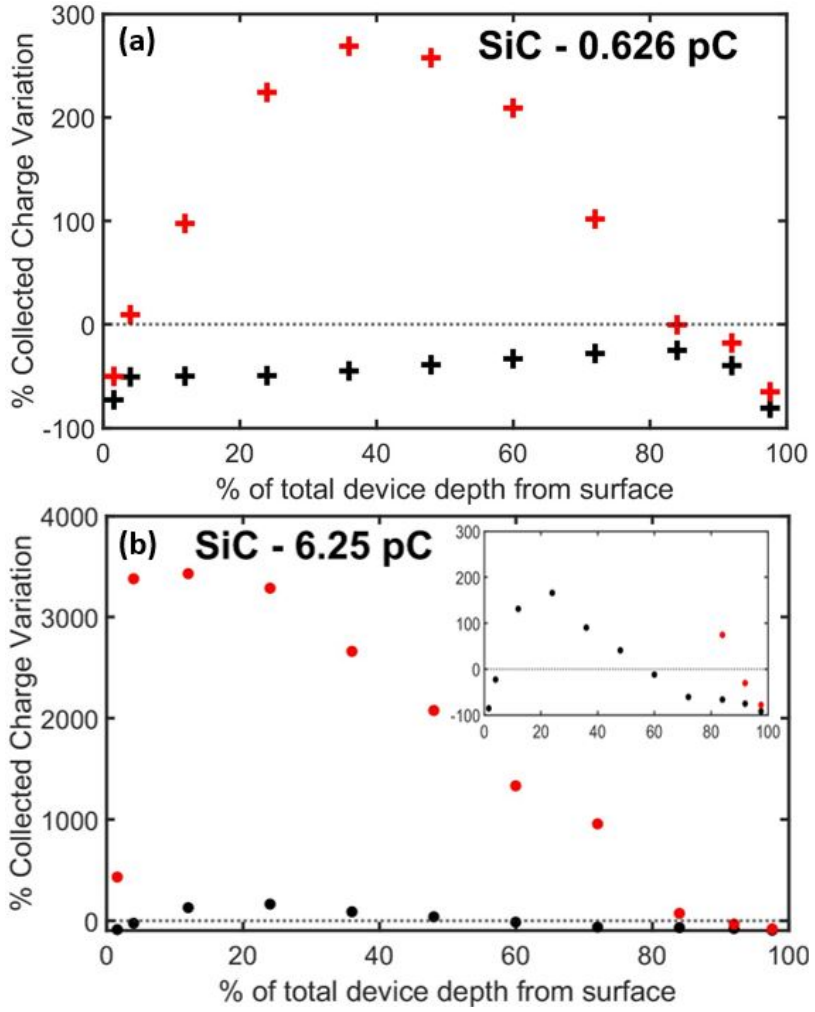


Figure 3.11: The percentage variation of collected charge between standard heavy ion simulations and local charge depositions for SiC at reverse bias of 600 V and 860 V (black and red markers respectively) for deposited charges of 0.626 pC and 6.25 pC (+ and •).

3.6 Conclusions

The radiation response of two materials key to the advancement of the future of the electrification of aircraft have been analysed through heavy ion simulations. It has been found that over a range of aerospace specific operating conditions that for deposited charge values equivalent to 300% of a silver ion commonly used in SEB testing that SiC does not undergo SEB for any bias applied up to 99% of the breakdown voltage. Si in comparison does have a much higher SEB sensitivity as lower deposited charge and bias values are required for the device to fail - with only

a deposited charge equivalent to 0.2% that of a silver ion required to cause device failure when a bias of 92% of the breakdown voltage is applied. Derating is therefore required if Si was to be used in aerospace applications.

Through highly localised charge deposition it has been identified that the internal electric field plays a crucial role on the SEB sensitivity. Correlation between the magnitude of the pre-impact electric field and the magnitude of collected charge was observed. SiC at a derating of 99% underwent SEB for charge deposition values of 300% and 150% that of a silver ion. However, at the industry standard derating of 70% of the breakdown voltage, where the magnitude of the peak electric field was reduced to 78% that of the original, no failures at these deposited charge values were observed.

In the quest to achieve a high reliability device against radiation, the combination of SiC with the JFET structure would seem to be the dream scenario. However, the SiC JFET sensitivity to radiation for aerospace specific applications is unknown. This is the focus of the following chapter.

4 Single Event Burnout Sensitivity of a SiC JFET

For the electrification of flight to become a reality, all components and systems of the next generation of electric and hybrid-electric aircraft need to be robust against SEB. The structures investigated in Chapter 3 provide insight to the 1D SEB sensitivity of devices. More complex 2D structures that are needed for power switching devices are pivotal in the realisation of these future aircraft concepts - ensuring high voltage operation which in turn provides high efficiencies. Having a clear knowledge of the limits of these switching devices under real-world conditions is imperative. Understanding of the JFET response to aerospace specific operating conditions is relatively unknown with the only data from Jean-Marie Lauenstein, the sole subject matter expert in SiC Wide Band Gap (WBG) Power Device Radiation Hardness Assurance at NASA [91]. For this reason, the focus of this chapter is to further the understanding of the SEB sensitivity of the SiC JFET through building on the findings of Chapter 3 via enhanced aerospace specific simulations. From this, key device SEB sensitive regions are to be identified and potential SEB hardening solutions outlined.

4.1 The Vertical JFET Structure

In order to understand the SEB sensitivity of a conventional vertical channel JFET (referred to as the VJFET from here on) structure through simulation, a suitable TCAD model is required. The structure of the model is shown in Figure 4.1, with parameters selected to match those of the real world device that was fabricated as part of the Innovate UK funded SiCTAA project. The vertical channel and drift region of the device are doped n-type at 5.25×10^{15} cm^{-3} with the gate doped p-type at 1.28×10^{19} cm^{-3}. The device source is located at the top of the image with the gate island a micron below, the drain of the device is at the bottom of the image, 15.325 μm from the top surface. The transfer characteristics and breakdown of the device are shown in Figure 4.2, at an ambient temperature of 300 K. These devices are designed to be operated near their blocking voltage limits in order to maximise their efficiency through a reduction in on-state losses. An optimal gate - source voltage of -60 V (with a 15% greater magnitude than the threshold voltage to accommodate for potential unwanted turn-on events) allowed for the largest breakdown voltage of

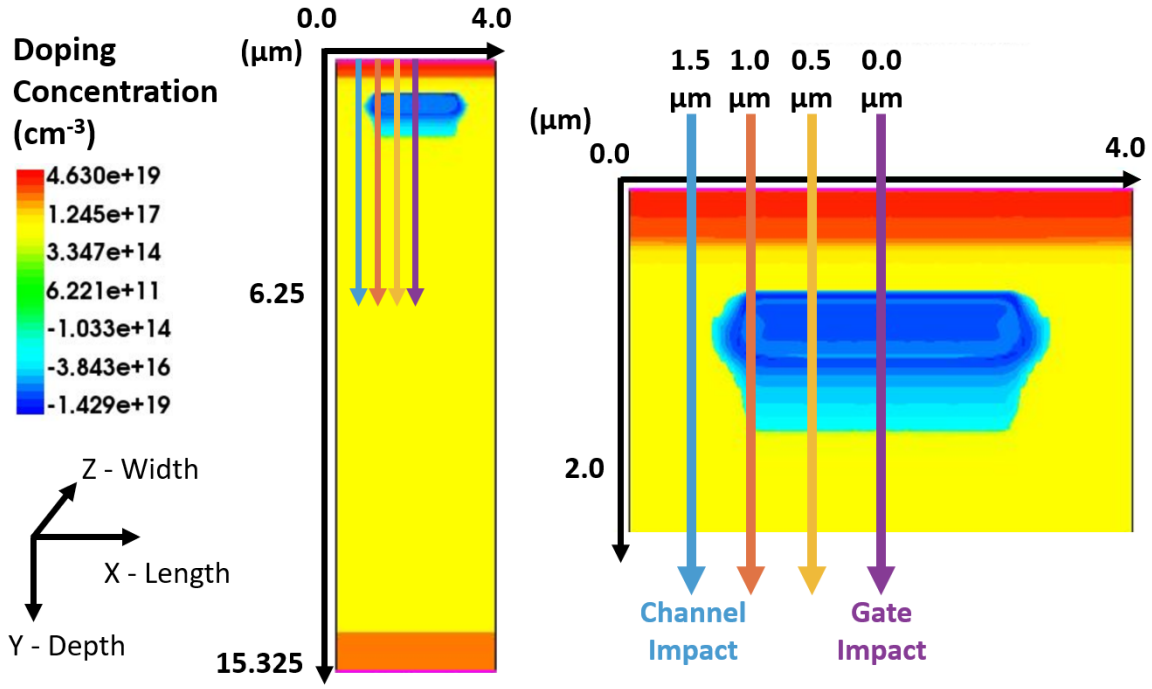


Figure 4.1: The VJFET with heavy ion impact locations indicated.

the device at 2430 V, which is in line with the analytical approximations for this structure.

As expected for a 2D structure the VJFET requires additional heavy ion impact locations in comparison to the study of the 1D power diodes in Chapter 3 in order to fully understand the device response. For this reason four different impact locations have been selected at different top surface locations between the centre of the channel (channel impact) and the centre of the gate (gate impact). A heavy ion track length of 6.25 μm has been selected to match that reported in Chapter 3 with LETs selected to also replicate real world aerospace specific operating conditions [104].

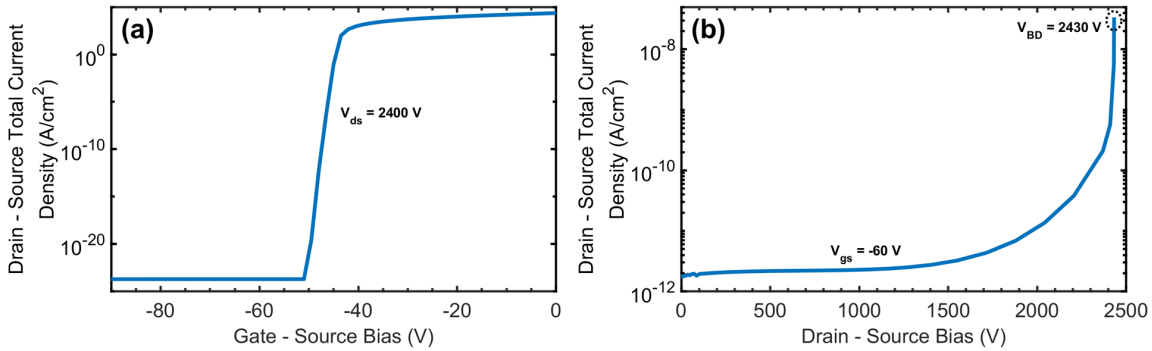


Figure 4.2: JFET transfer characteristics (a) and breakdown (b) both at 300 K.

A typical scenario (named here as aerospace specific scenario 1) highlights the variation in device response to impact location as shown by the data in Figure 4.3. Here an aerospace standard device derating of 40% of the breakdown voltage coupled with a heavy ion deposited charge of 300% of a silver ion commonly used in SEB experimental testing, shows three different device responses. The first of which is shown for impacts near the channel (denoted as 1.5 μm and 1.0 μm from the gate respectively) where the drain - source current returns to a current density of 10 μA/cm^2 - similar to that of the safe device responses described in Chapter 3. In this case, no SEB failure has occurred. The second response at a position denoted by 0.5 μm is the instantaneous failure of the device where the drain - source current density transient is not complete, rather, showing device melting due to the extreme current densities present. The third response is shown by the gate impact (0.0 μm from the gate) where the drain - source current density does not return to a safe value of less than 10 μA/cm^2 or undergoes an instantaneous failure, yet, the simulation concludes at a time of 0.1 μs with a current density above the safe value of 10 μA/cm^2. This has the potential for a shoot-through failure if this device were to be used in a real world circuit application.

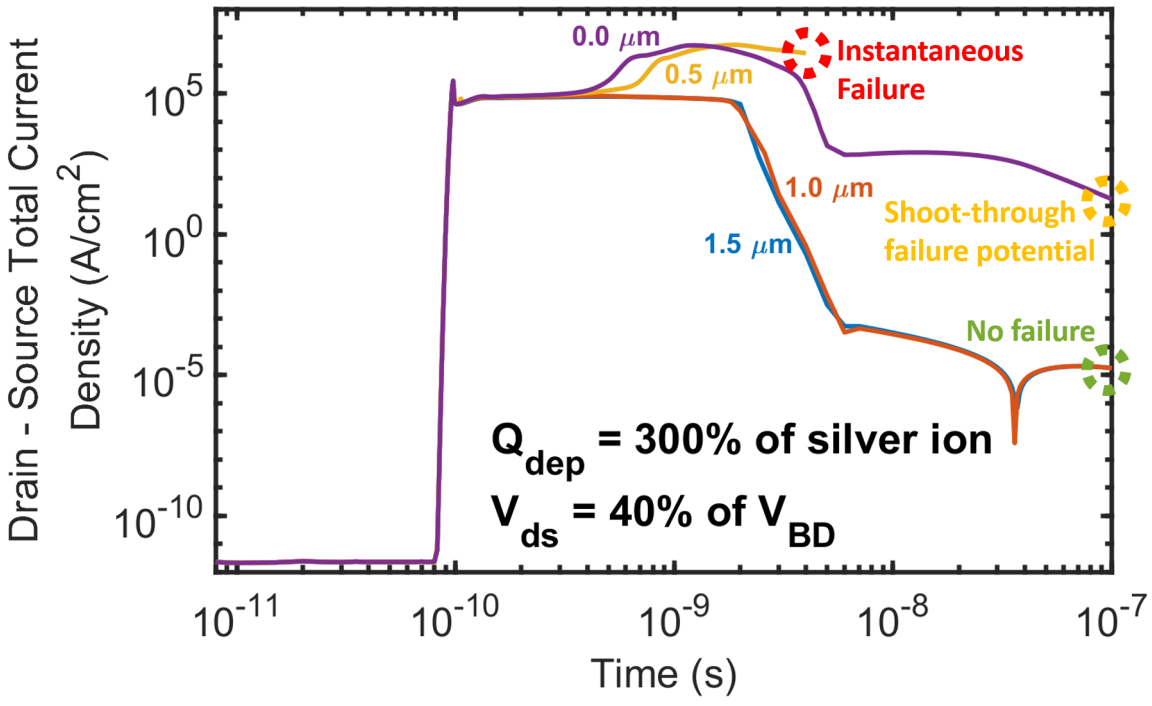


Figure 4.3: VJFET response to aerospace specific scenario 1 - a deposited charge equivalent to 300% that of a silver ion and a V_{ds} at 40% of breakdown voltage (1000 V) and a gate - source bias of -60 V.

A wide array of cosmic rays with a diverse range of energies bombard the earth and atmosphere every second. To gain an understanding of how the VJFET responds to this environment, further investigation into the range of deposited charges delivered to the simulated device, and their influence on device response, is required.

4.2 Charge Deposition Influence on Device Response

Aircraft traverse a range of altitudes on every flight - cosmic ray energies and fluxes are altitude and location dependent and it is therefore important that the VJFET is robust against any potential condition it is to be exposed to over its lifetime. In the Radiation Hardness Assurance community, where SEB sensitivity studies of devices are a feature, the silver ion is commonly used as a test to ensure the suitability of separate devices for use in aerospace. In both experimental and simulation studies the response of devices to a silver ion will determine whether the device is suitable for use on-board the aircraft. The VJFET with an industry standard derating of 70% is simulated for three different charge deposition conditions as shown by the data in Figure 4.4. For a deposited charge equivalent to 15% of a silver ion, which is considered to be quite substantial in the field, all 4 impact locations result in no failure of the device with drain - source current densities below 10 μA/cm^2 (as shown by the data in Figure 4.4(a)). Doubling the deposited charge to 30% of a silver ion, Figure 4.4(b), results in impact position dependent behaviours - instantaneous failure for channel impacts (1.5 μm and 1.0 μm from the gate) and no failures for the gate impacts (0.5 μm and 0.0 μm from the gate). For the channel impacts the maximum internal temperature reaches the sublimation temperature of SiC at 3100 K, leading to failure of the device - suggesting that for this condition that the gate impacts are more robust to the increased deposited charge. Increasing the deposited charge to 150% of a silver ion, as shown by the data in Figure 4.4(c), all four impact locations result in instantaneous failure. As the VJFET response to these deposited charge values resulted in failures, the device is not suitable for use on-board aircraft in its current state as a mission critical component. Channel impacts resulted in total device failure at lower deposited charge in comparison to gate impacts. For a 70% voltage derating there is potential for higher bias operating conditions to result in degradation of the device response. As discussed in Chapter 3, the internal electric field plays a key role in the outcome post charge deposition - and therefore was investigated further.

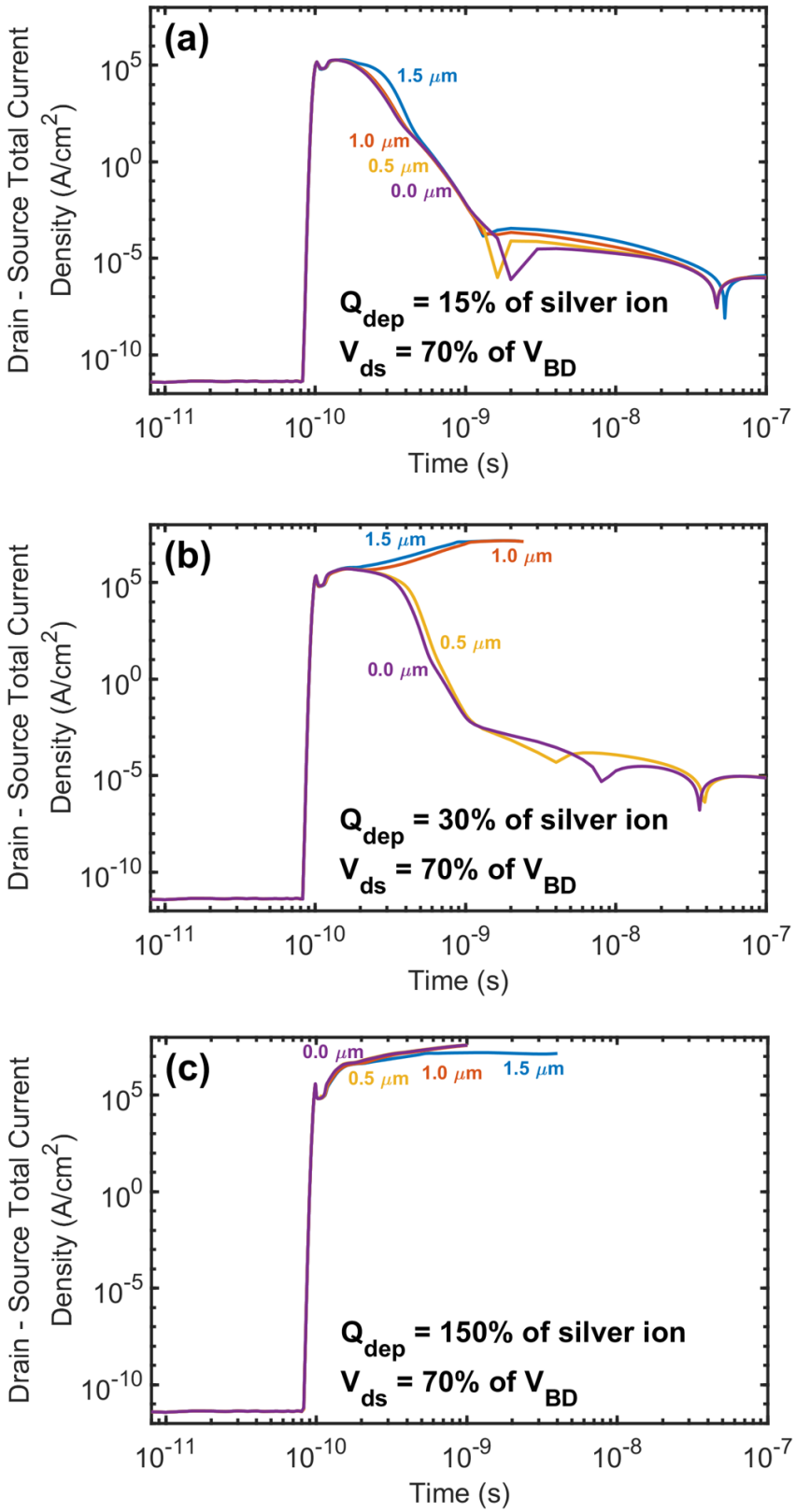


Figure 4.4: Charge deposition influence on the VJFET - 70% drain - source voltage derating with a gate - source bias of -60 V for three separate heavy ion deposited charges equivalent to 15% of a silver ion (a), 30% of a silver ion (b) and 150% of a silver ion (c).

4.3 Internal Electric Field Influence on Device Response

For SiC, the superlative critical electric field allows for its use in high voltage applications - however, this is a major challenge in terms of the SEB sensitivity. Generally, higher internal electric fields require lower deposited charges to result in the occurrence of SEB. Due to this, this section focuses on the internal electric field of the VJFET at three potential aerospace specific deratings, 99%, 70% and 40% of the breakdown voltage and the relation between device derating and the overall SEB sensitivity. The internal electric field profile of the VJFET can be seen for both the gate impact location, (a), and the channel impact location, (b), in the data in Figure 4.5. Taking into consideration the gate impact internal electric field profile, as shown by the data in Figure 4.5(a), it can be seen that the gate - source electric field peak, dip and peak shape which is created due to the location of the n^+ - p^+ source - gate junction, termed a trough feature from here on, occurs within the first 1.5 μm of the device depth. This trough feature is unchanged with the drain - source bias, it is instead dependent on the gate - source bias. From a device depth of 1.5 μm onwards, the variation in the electric field magnitude is shown, with the 99% derating generating an electric field peak of over 2.5 MV/cm, 0.5 MV/cm greater than the 70% derating and over 1.0 MV/cm greater than the 40% derating. This variation in electric field magnitude is shown through the entirety of the drift region of the device.

Taking into consideration the internal electric field profile within the channel, it can be seen from the data in Figure 4.5(b) that a reduction in derating does play a role on the magnitude of the electric field profile. As there is no source - gate p-n junction present, no trough feature is observed and instead for all deratings simulated the electric field profile grows to its maximum at around a device depth of 1.5 μm, which is level with the bottom of the gate and can be considered as the drain end of the channel. A similar trend to the gate impact location exists where the variation of the electric field magnitude between the different device deratings remains through the remainder of the device depth. When comparing the two impact locations the maximum electric field observed in the gate region is consistently 0.5 MV/cm greater than the comparable drain - source bias values for the channel impact case. With a critical electric field of $\sim$3 MV/cm (due to the drift region doping at 5.25×10^{16} cm^{-3}), and internal electric field values of within 10% of this for the pre-strike condition,

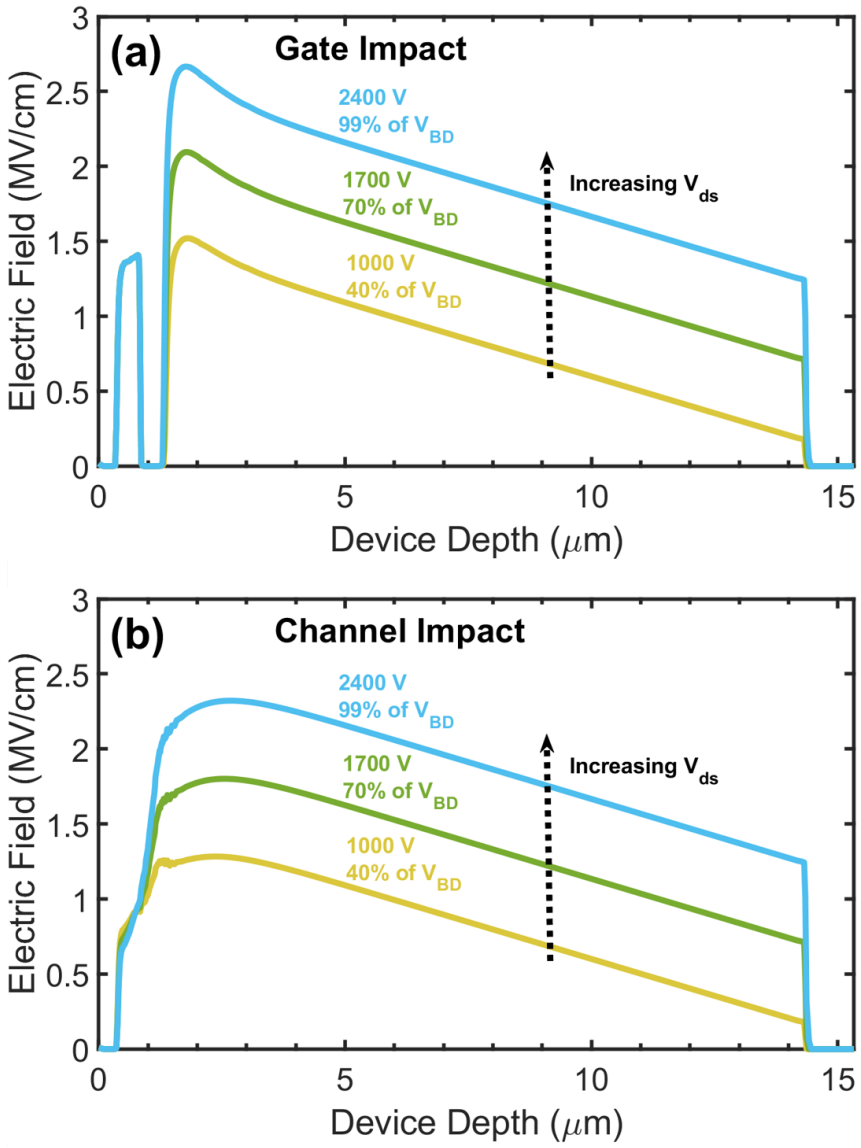


Figure 4.5: Pre-strike internal electric field y-cut profiles for the VJFET for a gate - source bias of -60 V and three separate drain - source deratings at 99%, 70% and 40% for the gate impact location (a), and the channel impact location (b).

coupled with potential electric field spiking post impact, it can be seen that at high deratings the possibility of SEB is increased in comparison to lower deratings.

The electric field y-cut profiles associated with these deratings are of importance when considering the device response in the following aerospace specific scenario - a fixed deposited charge equivalent to 30% of a silver ion for three separate deratings, 99%, 70% and 40% of the breakdown voltage, are shown by the data in Figure 4.6.

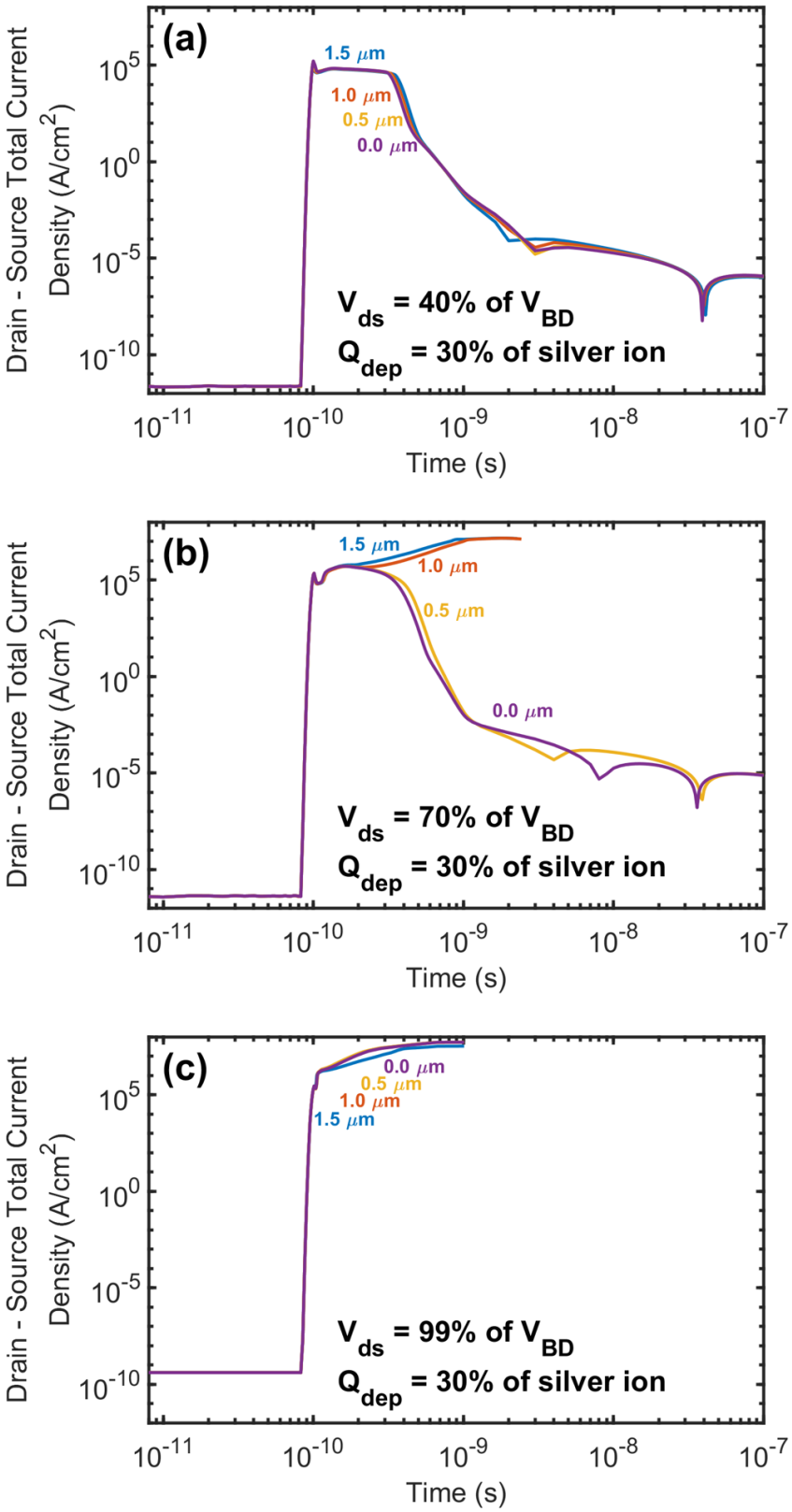


Figure 4.6: Drain - source bias influence on the VJFET, at a gate - source bias of -60 V, to a heavy ion impact with a deposited charge equivalent to 30% of a silver ion for a 40% derating, (a), a 70% derating, (b), and a 99% derating, (c).

For the lowest derating studied at 40%, it can be seen from the data in Figure 4.6(a) that no failures occur for the impact locations simulated following the outline in Figure 4.1. Increasing the derating to 70%, the channel impacts both result in instantaneous failure whereas the gate impacts both result in no failures as can be seen from the data in Figure 4.6(b). At the largest derating simulated of 99%, it can be seen that all impact locations investigated result in a device response of instantaneous failure as can be seen from the data in Figure 4.6(c). As mentioned previously, the higher internal electric fields result in an enhanced SEB sensitivity and this is seen in both the channel and gate impacts.

4.4 VJFET Single Event Burnout Sensitivity

The SEB sensitivity over a range of drain-source bias conditions for the VJFET is of importance in order to understand the overall performance of the device to an array of potential operating conditions relevant to aerospace. From this understanding, potential remedies to the device response can be identified and applied to reduced the overall device SEB sensitivity. Here, the VJFET has been simulated for a selected deposited charge equivalent to 30% of a silver ion with fixed gate - source bias of -60 V and a range of drain - source deratings up to 99% of the breakdown voltage for all four impact locations, as shown by the data in Figure 4.7. This deposited charge value has been selected as for all impact locations, variation in device response is observed in contrast to the higher deposited charges, equivalent to 300% of a silver ion, where failure of the device occurs at all bias levels studied. When investigating the SEB sensitivity of power devices through heavy ion studies, Soelkner [75] discussed two key features - the first being the sudden transition from a safe device response to a failed device which underwent SEB, being the sudden jump in collected charge for a small increase in derating - highlighting the sensitivity of carrier multiplication, and the second, which is the identification of the value of failure collected charge - the collected charge at the device terminals to result in the SEB failure of the device.

For the VJFET, the data in Figure 4.7 show both of these features detailed by Soelkner. The failure collected charge of 530 pC is identified as the minimum collected charge to induce SEB failure within the device. In contrast to the work of Soelkner the impact location of the heavy ion plays a role on the sensitivity of the

device response. It can be seen that the channel impact at 1.5 μm from the gate results in the highest device sensitivity as only a 60% derating is required to induce SEB. As the impact location moves towards the gate the data show that the SEB sensitivity reduces as higher deratings are required to induce SEB. The lowest sensitivity is observed for the gate impact where a derating of 99% results in SEB. It can be seen that the channel impacts are the weak link with regards to device SEB sensitivity in this vertical JFET structure.

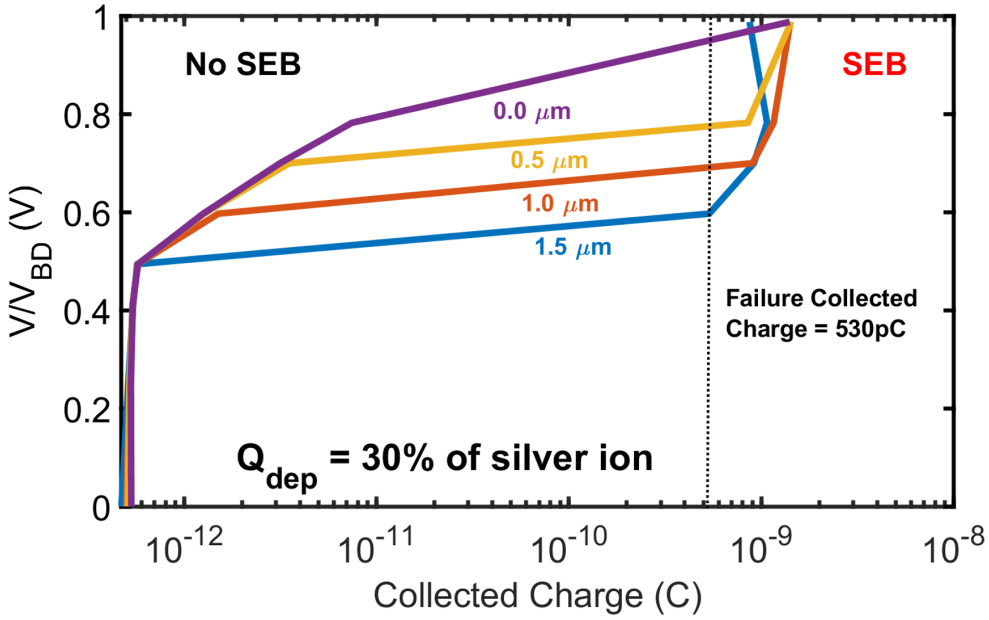


Figure 4.7: Single Event Burnout sensitivity of the VJFET for a selected deposited charge equivalent to 30% of a silver ion with fixed gate - source bias of -60 V and a range of drain - source deratings to 99% of the breakdown voltage for all four impact locations from 1.5 μm (channel impact) to 0.0 μm (gate impact).

From the data, it can be seen that the impacts in the gate region of the device are more sensitive to increases in deposited charge whereas the channel impacts are more sensitive to the drain - source bias. Additionally, in a real world situation it is unknown how and where the cosmic ray would impact the device and for this reason, to ensure safe operation of the VJFET, drain - source derating alone will not provide a sufficient SEB sensitivity reduction to enable operation in a high reliability aerospace environment. It is therefore important that other techniques are used to make this device robust against any potential aerospace condition it may be exposed to during its lifetime.

4.5 Biasing Technique to Reduce Single Event Burnout Sensitivity

Trade-offs are a key feature when considering the SEB sensitivity of devices - the balance between how robust a device is to SEB and its electrical performance. For all simulations reported in this chapter to this point a -60 V gate - source bias had been selected as this achieved the theoretical breakdown voltage for the device of 2430 V. However, if the SEB sensitivity of the device was to be prioritised over efficiency, a reduction in the gate - source bias is a possible technique that could be used to reduce the SEB sensitivity. If the maximum device derating was to be lowered, a lower gate - source bias could be used - this is shown by the data in Figure 4.8 for the VJFET. Here, aerospace specific specific deratings are shown from 2400 V, a 99% derating through to 1700 V, a 70% derating. From this, the different gate - source bias conditions required to block the channel can be observed. The reduction in bias conditions lead to a reduction of the device internal electric field - a feature which has the potential to reduce the amount of generated charge in the device through avalanche multiplication, as discussed in Chapter 3.

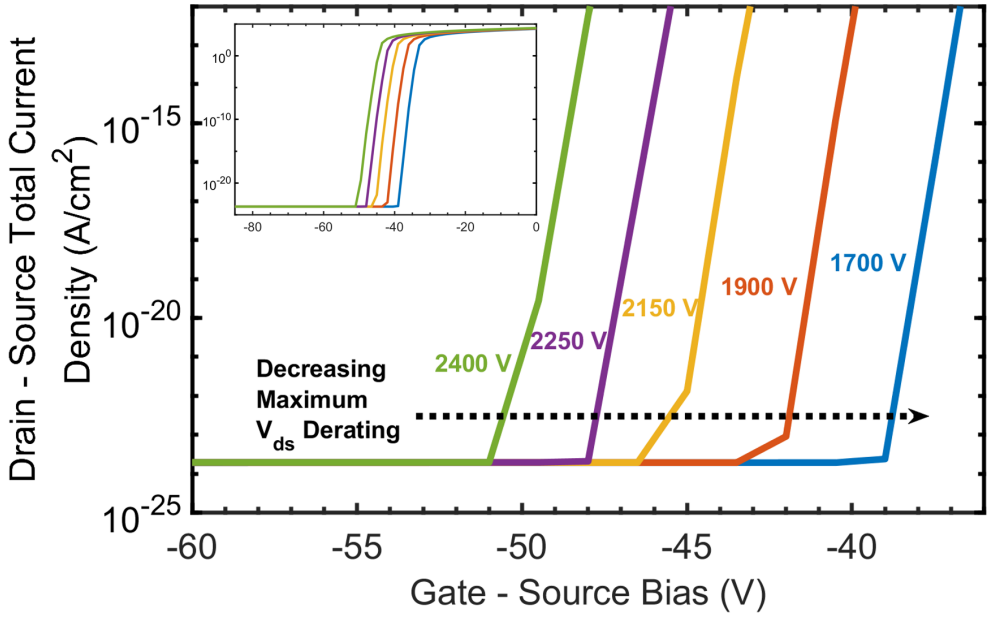


Figure 4.8: A close-up of the transfer characteristics of the VJFET for a range of aerospace specific deratings showing the suitable gate - source biases required to result in channel blocking. Inset shows the non-close-up plots.

A major additional benefit of reducing the gate - source electric field is that no further device development costs are involved and the adjustments can be made at a circuit level. To understand the suitability of these gate - source bias adjustments the simulation of the VJFET under one of the worst case situations, aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) has been performed.

The internal electric field of a device is of importance when considering its SEB sensitivity - the higher the electric field the higher the SEB sensitivity for impacts in that location. For the VJFET, the internal electric field profiles for the two impact locations of interest, the channel impact location (at 1.5 μm from the gate) and the gate impact location (at 0.0 μm from the gate) are shown in Figure 4.9. For the gate impact, Figure 4.9(a), it can be seen that the expected trough feature is evident as the device depth goes from the top surface, the source contact, through to the upper edge of the gate implant at a depth of 0.825 μm. The highest observed electric field peak is from the gate - source bias condition of -68 V at 1.6 MV/cm. To achieve a blocked channel for a drain - source derating of 70% (1700 V), a gate - source bias of -40 V is required. The benefit of this gate - source bias is that a trough feature electric field peak of 1.0 MV/cm is created - 0.4 MV/cm lower than that of the -60 V gate - source bias condition required to achieve the theoretical breakdown voltage of the device, therefore reducing the avalanche multiplication and the generated charge.

The variation in peak internal electric field for the channel impact case, as shown by the data in Figure 4.9(b), demonstrates the influence of the gate biasing conditions on the channel region of the device. When a high gate - source bias of -68 V is applied, a peak electric field at the edge of the source region is present of 0.9 MV/cm. Reducing this gate - source bias to -40 V results in a lowered peak of 0.5 MV/cm. For a 1D SiC structure subject to a heavy ion impact, the focus of Chapter 3, it was found that the internal electric field can increase in magnitude by up to 2.5 times its original value. With the critical electric field of SiC being $\sim$3 MV/cm, it can be seen that careful selection of the gate - source bias is crucial against the possibility of initiating SEB for all devices studied.

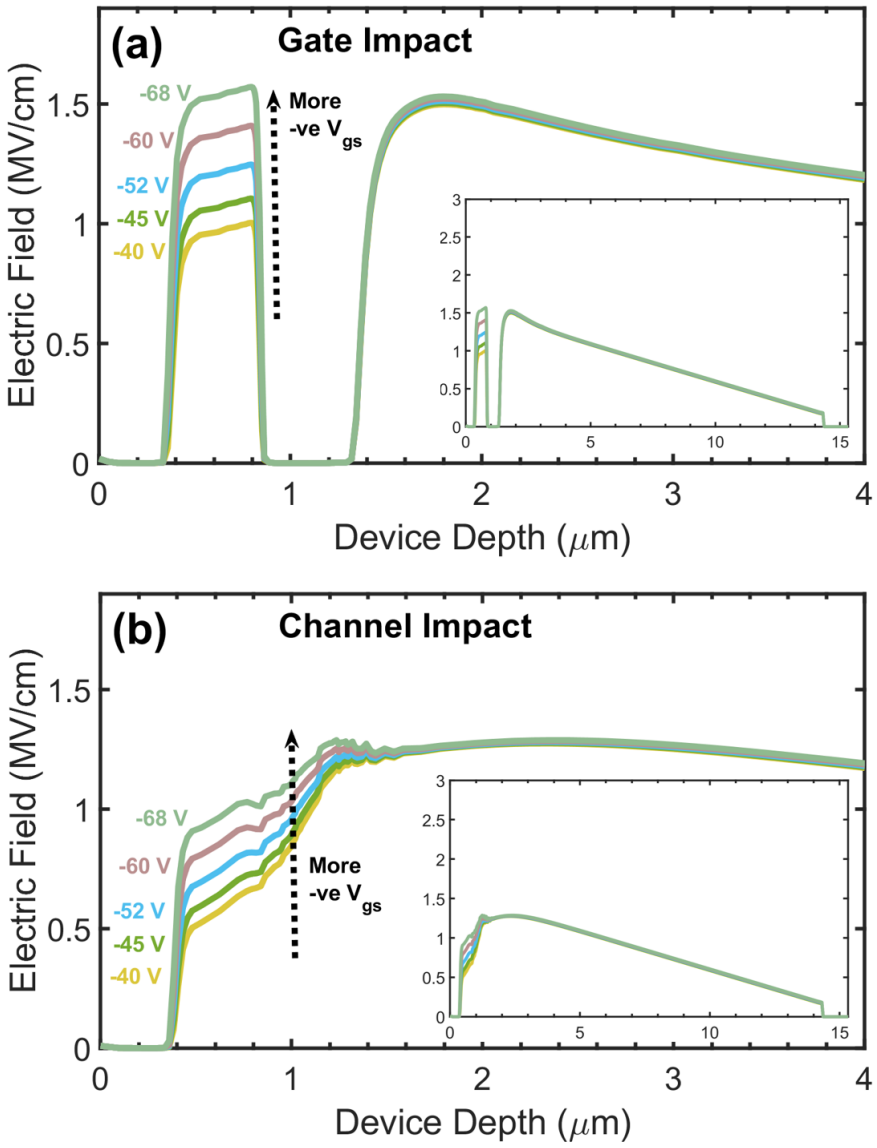


Figure 4.9: Close-up pre-strike internal electric field y-cut profiles for the VJFET with a drain - source derating of 40% (1000 V) for varied gate - source biases between -68 V and -40 V at an ambient temperature of 300 K for the gate impact, (a), and the channel impact, (b). Insets show the non-close-up plots.

In order to test the performance of these lowered gate - source bias conditions, the VJFET was subjected to one of the potential worst case conditions - aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion), as shown by the data in Figure 4.10.

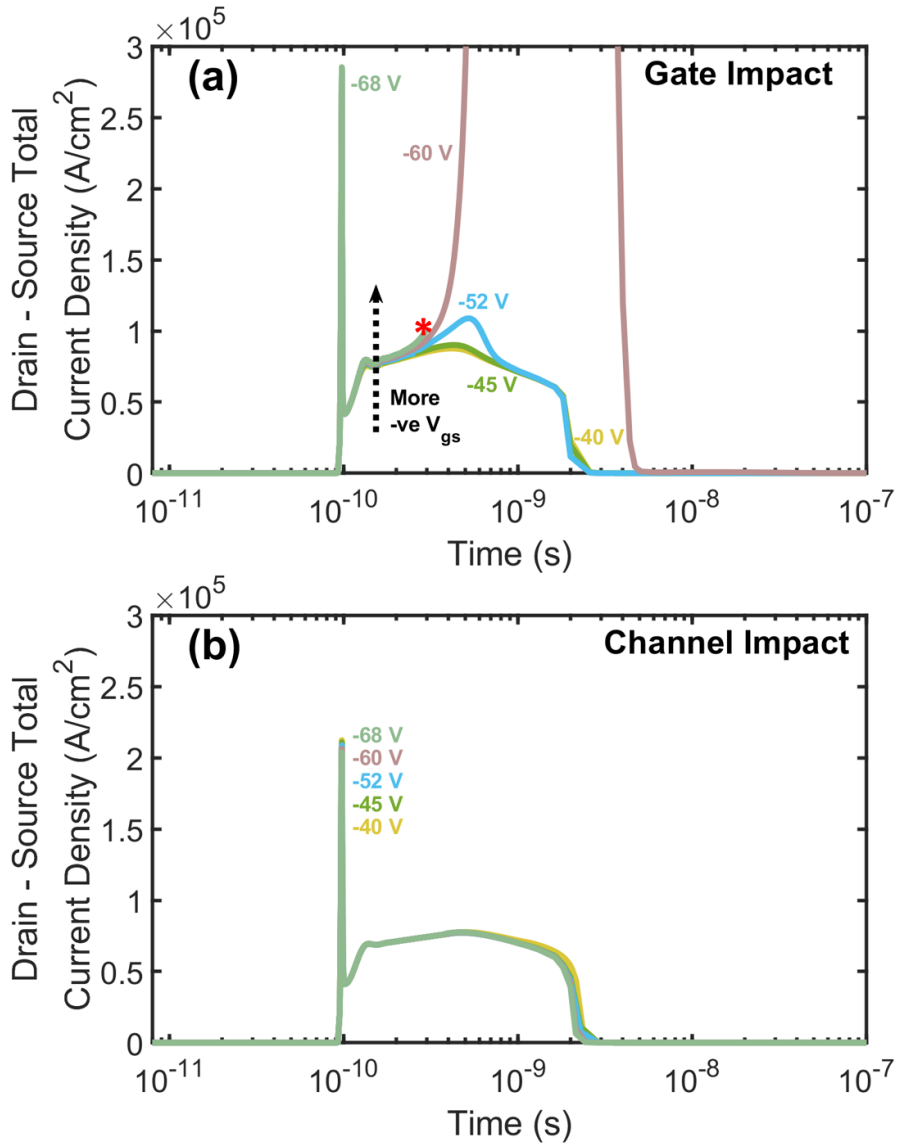


Figure 4.10: Drain - source total current density transient response of the VJFET to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source biases between -68 V and -40 V for the gate impact location, (a), and the channel impact location, (b). The * as shown in (a) indicates the occurrence of a SEB for the -68 V gate - source bias condition.

Considering the drain source current density transient response for the VJFET for the aerospace specific scenario 1 for the gate impact location, as shown by the data in Figure 4.10(a), at a gate - source bias of -68 V device failure is observed and SEB occurred within 300 ps (red asterisk) - the maximum lattice temperature has exceeded 3100 K. Reducing the bias to -60 V results in a large secondary current density peak

of 5 MA/cm^2 observed at 1 ns. Further, this transient does not return to the defined no failure condition of a current density of 10 μA/cm^2 or below, and therefore is classed as a potential shoot-through failure. However, as the gate - source bias is further reduced to -52 V, the device response results in a no failure case. Similarly for smaller values of gate - source bias the transient response of the device results in no failure indicating a device which is robust against SEB under this potential worst case scenario. The internal electric field has an influence on the device response for the gate impact condition - lowering this value reduces the SEB sensitivity of the device at a cost of a decrease in the maximum breakdown voltage.

Alternatively, for the channel impact location, as shown by the data in Figure 4.10(b), no change in device response is observed, all impacts at this location are safe to SEB. Therefore, when channel impacts are considered a reduction to the magnitude of the gate - source bias has no influence on the SEB sensitivity of the device, however, a reduction to the gate - source bias should still be considered for the overall device sensitivity as for gate impacts a reduction in SEB sensitivity is shown.

In order to understand the overall response of the VJFET to aerospace specific scenario 1, the gate - source total current density transient is now considered at gate - source biases between -68 V and -40 V for the gate impact location, as shown by the data in Figure 4.11. As a reduction in gate - source bias has no influence on the channel impacts, only the worst case channel impact condition is included, a gate - source bias of -68 V. Gate - source bias plays a key role on the response of the VJFET to aerospace specific scenario 1 - with device failure at -68 V, potential failure at -60 V and -52 V, and the non-occurrence of SEB at -45 V and -40 V. For the potential shoot-through failure condition of -60 V a peak gate - source current density of 13 MA/cm is observed, which is in contrast to those of the SEB safe -40 V gate and channel impacts where peak current densities of 4.3 MA/cm and 0.15 MA/cm are obtained respectively. For the -60 V gate - source bias case the magnitude and duration of the current density response is of concern. A notable secondary current peak can be observed after the initial heavy ion charge deposition spike for the -60 V and -52 V cases, indicating avalanche multiplication. As identified in Chapter 3, where the SiC 1D structure was susceptible to shoot-through and high temperature peaks, due to proximity of the anode and cathode, a similar feature is observed for the gate and source of the VJFET.

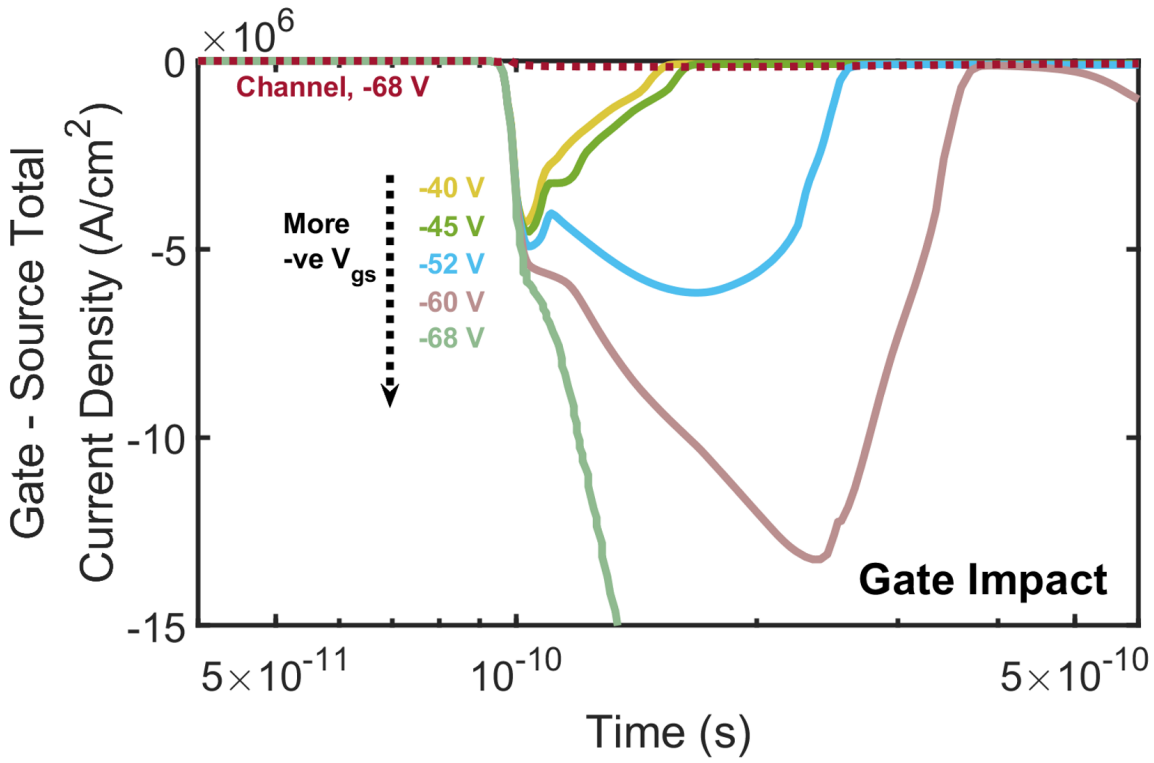


Figure 4.11: Gate - source total current density transient response of the VJFET to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source biases between -68 V and -40 V for the gate impact location, with the inclusion of the -68 V gate - source bias channel impact for reference (figure enlarged for clarity).

When a device undergoes an interaction with a cosmic ray, both the current transient response and the temperature response are key features which determine whether the device undergoes SEB. A sustained current density coupled with a spike in maximum temperature are the two main indicators of this failure. This maximum temperature analysis has been performed for the VJFET as shown by the data in Figure 4.12 for both the channel impact and gate impact locations for the device under aerospace specific scenario 1.

For the largest gate - source bias studied at -68 V, the sublimation of SiC occurs and SEB is induced as the maximum lattice temperature has exceeded 3100 K. At a lower gate - source bias of -60 V, it has already been noted that the current density transient response would likely result in a shoot-through failure - coupled with this is the expected high temperatures generated through these high current levels, as seen here with a peak maximum temperature of over 2500 K and a temperature of 2000 K

is observed 0.1 μs after the impact. This highlights the vulnerability of the device when it is operated under these conditions and the role the electric field between the gate and the source plays on the SEB sensitivity.

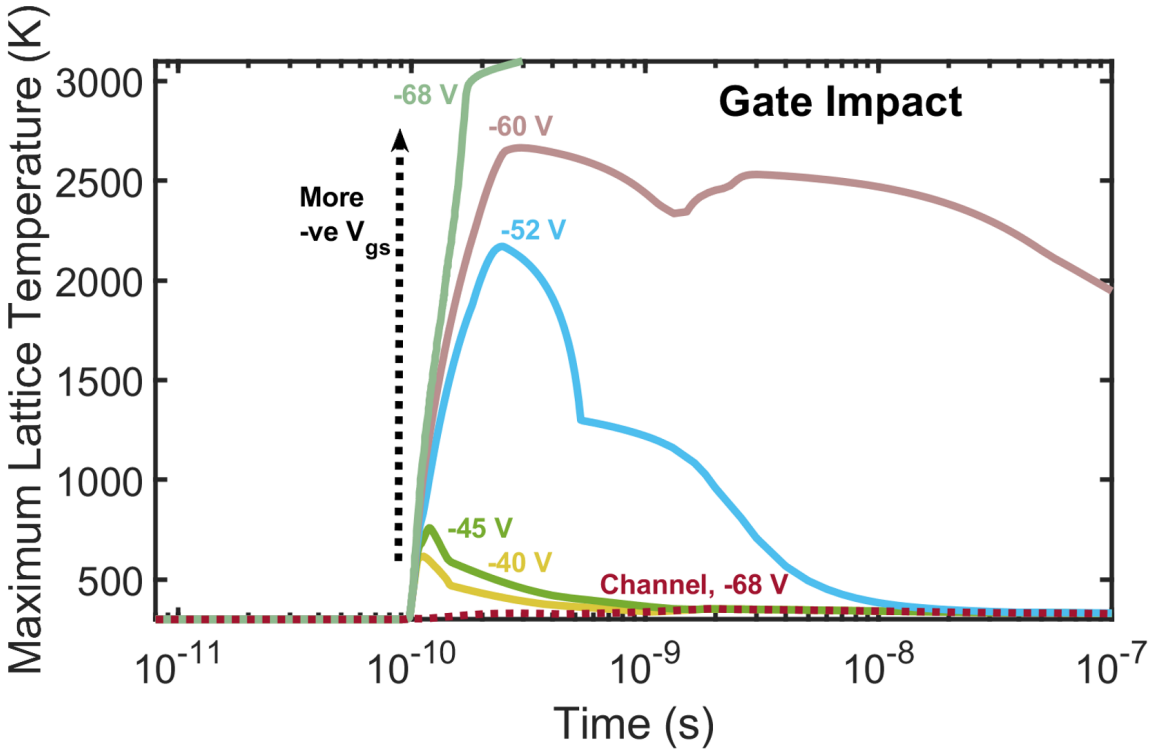


Figure 4.12: Maximum lattice temperature transient response of the VJFET to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source biases between -68 V and -40 V for the gate impact location with the inclusion of the worst case channel impact for reference.

If the gate - source bias is reduced below that of the optimal gate - source voltage of -60 V, a value with a 15% greater magnitude than the threshold voltage to accommodate for potential unwanted turn-on events, there is a reduction in maximum lattice temperature for the -52 V, -45 V and -40 V cases. To ensure a robust device against the aerospace specific scenario 1 a maximum gate - source bias of -45 V is permissible, this is due to the small time in which the maximum lattice temperature of the device exceeds those of the pre-strike condition of 300 K. For the channel impacts the minimal influence on transient response is shown here, with a maximum temperature increase of 30 K at the peak. At the lowest gate - source bias studied at -40 V, there

is a 20% reduction in peak lattice temperature observed in comparison to the -45 V case. The trade-off for this reduction in SEB sensitivity for the selection of a lower gate - source bias is that there is a reduction in the maximum drain - source derating that can be applied to the device.

It can be seen that by reducing the gate - source bias of the VJFET that its SEB sensitivity is reduced for the gate impacts only. However, in order to reduced the SEB sensitivity of the entire structure to cosmic ray impacts, an alternate technique is required. With limitations on possible device structure modifications, allowing only for gate vertical position to be shifted (as the channel width is to be maintained in order to achieve consistent threshold voltages). The modification of the device structure in this way is a feature that shall be investigated further in order to potentially reduced the SEB sensitivity of the device.

4.6 Structural Technique to Reduce Single Event Burnout Sensitivity

A common method to increase the breakdown voltage of a power device is to increase the separation between the junctions. This technique is proposed as a feature for a modified version of the VJFET in an attempt to reduced its SEB sensitivity. By increasing the gate - source separation the peak electric field within the surface region of the device, which has been shown to be instrumental in the overall device response to cosmic ray interaction earlier in this chapter, will be lowered, reducing the value of generated charge after ion impact. The standard source gate separation used in all simulations of this chapter to this point is at a value of 0.825 μm, which is identical to the physical device. This separation value is classed as a value of 100% of the original gate - source separation distance. To determine whether varying this separation results in a reduction in device SEB sensitivity, a range of gate - source separations have been simulated, from 100% of the original spacing through to 500% of the original spacing - the thicker layer is doped n-type at 10^{16} cm^{-3}, matching that of the original device. The pre-strike internal electric field profiles are important in order to understand their influence on the device response, these are shown for the modified VJFET for both the gate and channel impact locations in Figure 4.13. The influence of the modified structure spacing between the gate and source of the

device has on the internal electric field for the gate impact location can be seen Figure 4.13(a). Here, the trough feature, seen at a gate - source separation of 100%, with two sharp peaks with a maximum magnitude of 1.4 MV/cm evolves into a lower magnitude triangular shape as the separation of the gate and source increases - as shown at 500% separation where the peak electric field is 0.5 MV/cm.

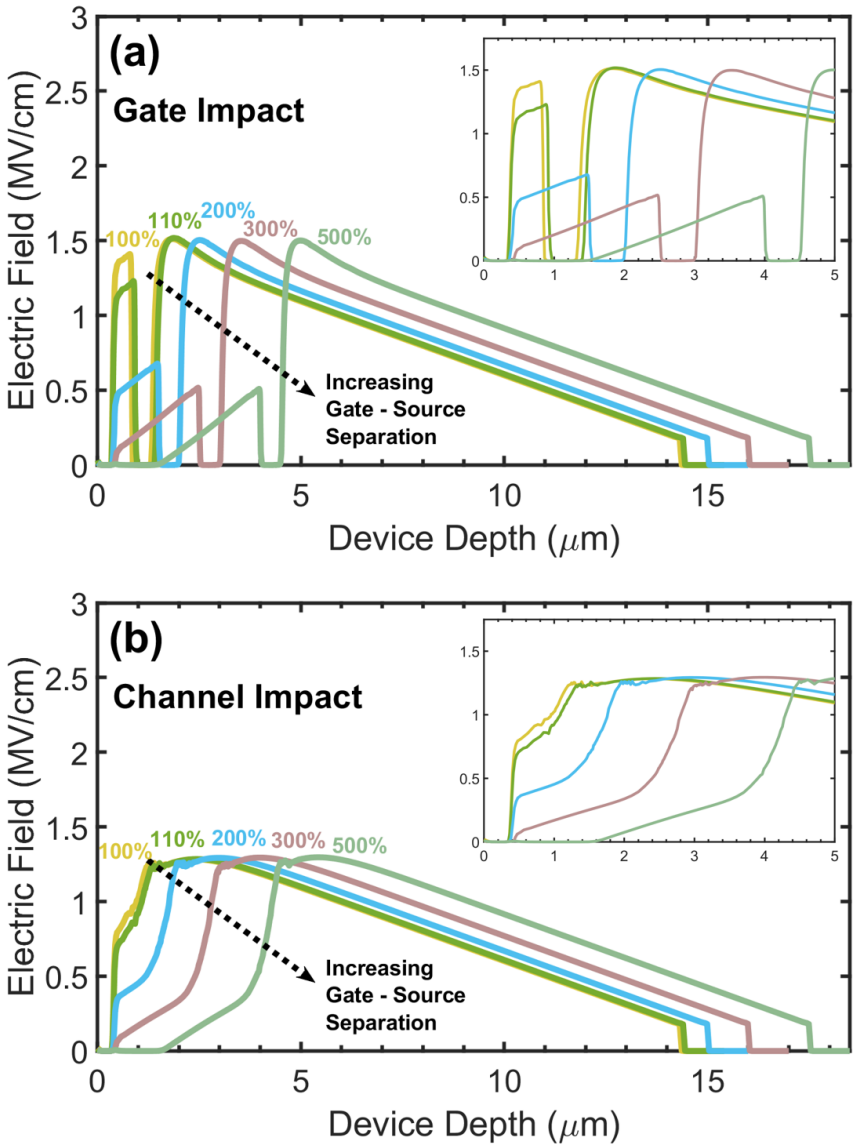


Figure 4.13: Pre-strike internal electric field y-cut profiles for the VJFET with a drain - source derating of 40% (1000 V) and a gate - source bias of -60 V at an ambient temperature of 300 K for varied gate - source separation values between 100% and 500% of the original device spacing for the gate impact location, (a), and the channel impact location, (b).

Due to limitations in the fabrication process used to realise these devices, the gate - drain separation is unable to be altered, and therefore in these simulations this separation has remained fixed. As increasing the gate - drain separation would only slightly reduced the magnitude of the electric field in the region of ion impact (the first 6.25 μm of device depth), little influence on the SEB sensitivity would be expected. From this, the electric field y-cut profile magnitude and distribution between the bottom of the gate region and the drain contact of the device is the same for all modified devices simulated.

Taking into consideration the channel impact location electric field y-cut profiles, as shown by the data in Figure 4.13(b), it can be seen that a similar trend of the increased gate - source separation results in a reduction in the magnitude of the electric field profile between the gate and the source. For both of the impact locations studied it is important to understand whether these modifications to the VJFET will result in a reduction in SEB sensitivity - both of these locations have been subjected to the aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) to enable a direct comparison with the previous simulations.

The transient responses in the drain - source current density to the aerospace specific scenario 1 are shown by the data in Figure 4.14 for ion impacts located at the gate (0.0 μm) and the channel (1.5 μm). For the gate impact location, the original gate - source separation resulted in the largest current density response out of all of the separations studied - a current peak of 5 MA/cm^2 at 1 ns and a current density above the no failure response mark of 10 μA/cm^2 at 0.1 μs - resulting in a potential shoot-through failure. As the value of gate - source separation is increased, the magnitude of the drain - source current density transient reduced, with the 110% separation case resulting in a no failure response - the same as all following separations studied. The channel impact location data indicate a trend between the gate - source separation and a reduction in the magnitude of the drain - source current transient response, as shown by the data in Figure 4.14(b). A no failure response is observed for the original gate - source separation denoted as (100%) and for all other separations studied. A feature to note when comparing the two separate impact locations is the similarity in the 500% gate - source spacing modification, here, the transient responses are similar in magnitude and duration, highlighting that the key region of interest when

attempting to reduce the SEB sensitivity of the device is the first few microns depth of the device between the source and the gate. In this region, not only does the electric field crowding at the edges of the gate influence the response to the gate impacts, but also the channel impacts.

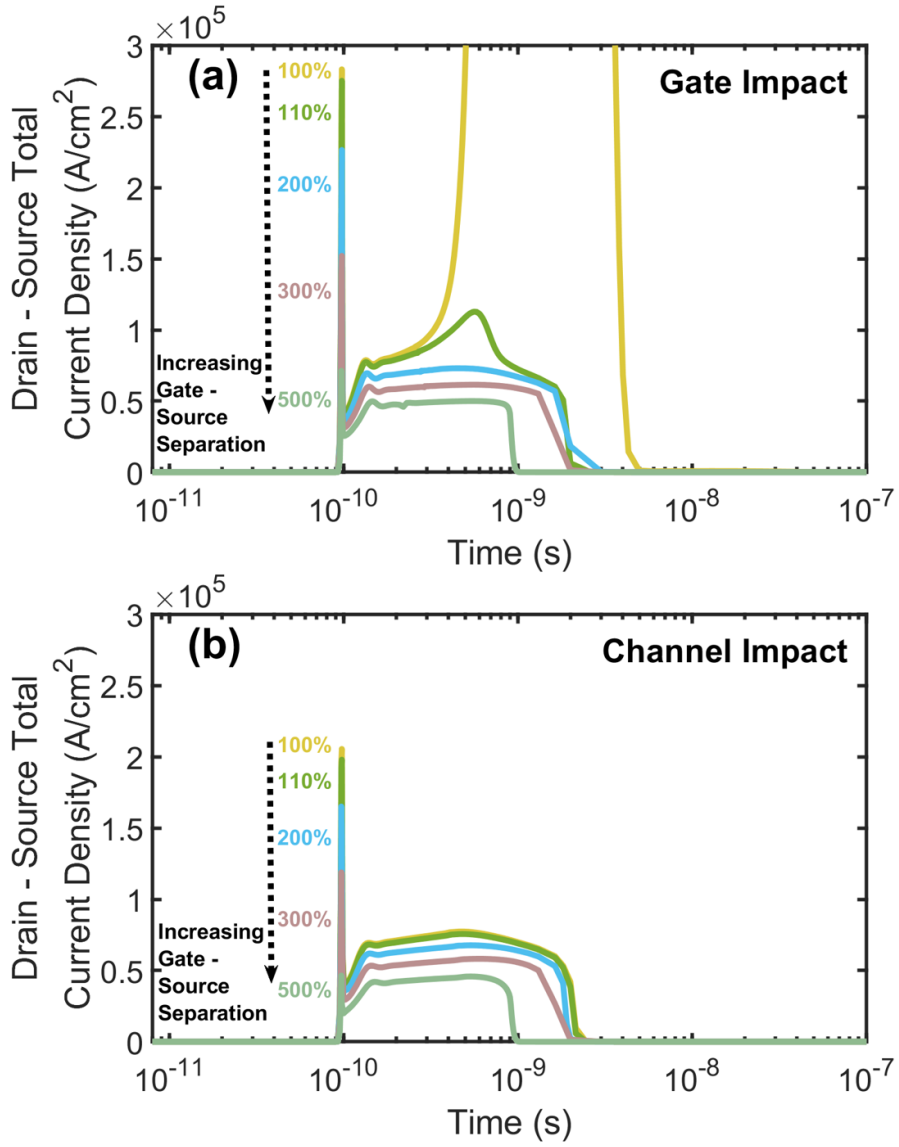


Figure 4.14: Drain - source total current density transient response of the VJFET with modified gate - source separation to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source separation values between 100% and 500% of the original device spacing for the gate impact location, (a), and the channel impact location, (b).

For the gate impact location it is of importance to understand the variation in gate - source total current density transient response to aerospace specific scenario 1 for the VJFET with modified gate - source separations. The data are shown in Figure 4.15. The secondary current peak, the region after the initial charge deposition from the heavy ion at 0.1 ns, is of particular interest. For the original device, denoted as the 100% case, a peak magnitude of 13 MA/cm^2 at 0.24 ns is observed which is in contrast to the 500% case where only a 4.5 MA/cm^2 peak at 0.15 ns is obtained, corresponding to a reduction of 65%. This feature relates to the magnitude of the internal electric field at the gate - source junction of the different VJFET structures, as shown by the data in Figure 4.13(a). The heavy ion studied in this work has a track length of 6.25 μm and the average magnitude of the electric field profiles up to this 6.25 μm point for the 100% gate - source separation VJFET is twice that of the 500% gate - source separation VJFET at 1 MV/cm and 0.5 MV/cm respectively.

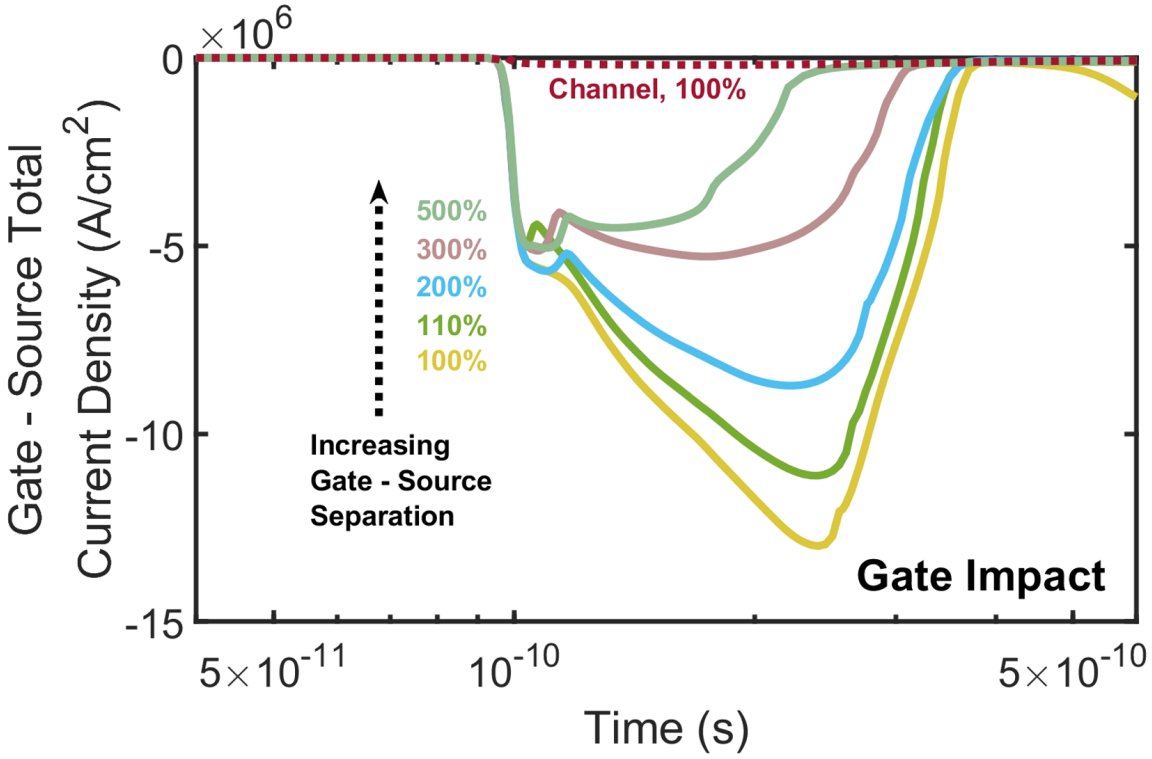


Figure 4.15: Gate - source total current density transient response of the VJFET, at a gate - source bias of -60 V, to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source separation values between 100% and 500% of the original device spacing for the gate impact location, with the inclusion of the worst case channel impact for reference (figure enlarged for clarity).

As discussed earlier in chapter 3, the pre-strike electric field magnitude can increase to up to 3 times this value a few ns after impact, leading to magnitudes which are comparable to the critical electric field of SiC at ∼3 MV/cm (due to the drift region doping at 5.25×10^{15} cm^{-3}). With peak electric field magnitudes of 1.4 MV/cm and 0.5 MV/cm for the original and 500% gate - source separation VJFETs respectively a decrease in peak electric field of 64% has resulted in a 99% reduction in peak drain - source current density between the two structures.

To understand the SEB sensitivity of the modified VJFET the maximum temperature transient response needs to be taken into consideration, as shown by the data in Figure 4.16.

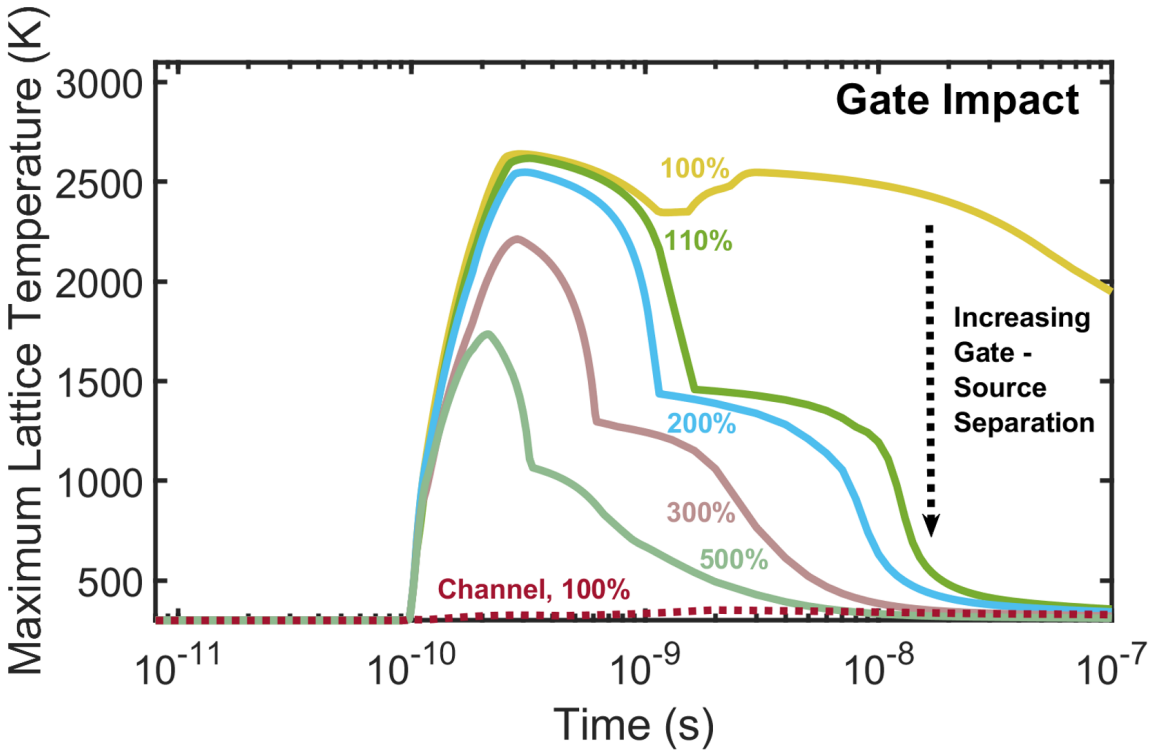


Figure 4.16: Maximum lattice temperature transient response of the VJFET with modified gate - source separation to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion) for varied gate - source separation values between 100% and 500% of the original device spacing for the gate impact location with the inclusion of the worst case channel impact for reference.

For the standard gate - source separation, high temperatures are observed in the vicinity of 2000 K for the duration of the simulation - which is to be expected from the previous current density transient response for this condition. As the gate - source separation increases, it can be seen that the maximum temperature within the device also decreases - in line with the reduction in the electric field magnitude. The channel worst case condition is included for reference (the original gate - source separation) - only a 50 K increase in maximum lattice temperature is observed, however, as the top of the gate is predominantly the region which generates the maximum device temperature, it is to be expected that when the heavy ion passes directly through this region, high temperatures are generated. Despite this, the 500% gate - source separation condition for the gate impact returns to the pre-strike maximum temperature less than 10 ns after the impact - resulting in a lower maximum temperature than that of the worst case channel impact. To harden the VJFET to this aerospace specific scenario, an increase in the gate - source separation to 500% of the original separation is suggested.

The RADHARD 500% gate - source separation VJFET structure has reduced SEB sensitivity in comparison to the original VJFET structure and the other device modifications studied, however, it is crucial that this device has suitable electrical characteristics to allow for its use in potential real world applications. The transfer characteristics and breakdown voltage for both the original and RADHARD 500% VJFET structures are shown by the data in Figure 4.17. The transfer characteristic data of Figure 4.17(a) show threshold voltages of -51 V and -29 V for the original and RADHARD 500% devices respectively. This feature is due to the pinch-off of the region between the gate - source in the RADHARD 500% device. This is a big advantage for the modified RADHARD 500% device as not only does this provide a lower threshold voltage, but short channel effects are also remedied whilst maintaining the same fabrication constraints through a reduction in the magnitude of the electric field at this critical region of the device.

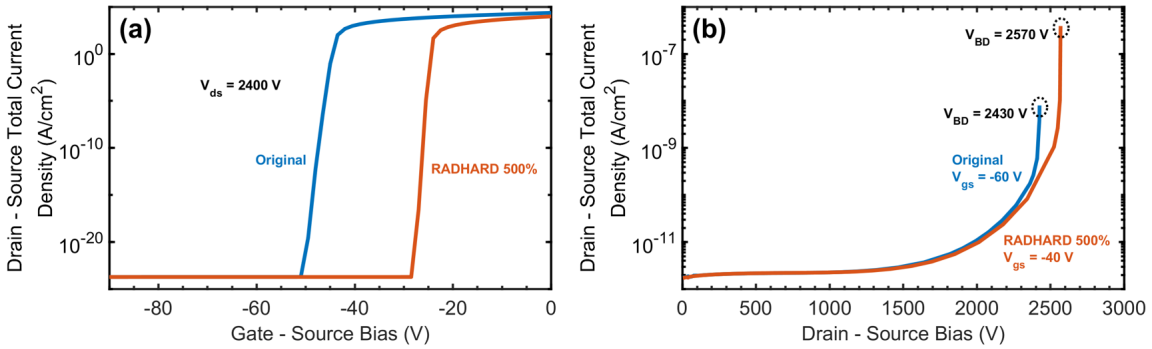


Figure 4.17: Transfer characteristics for both the original and RADHARD 500% gate - source separation VJFET structures (a), and respective breakdowns (b) both at 300 K.

The breakdown voltages of the two devices differ as shown by the data in Figure 4.17(b). Due to the Monte Carlo nature of the ion implantation used in the device creation some variation in breakdown characteristics are expected. In this study less than 1% variation in the breakdown voltage was identified through performing multiple simulation runs of the same original device process commands. The 6% increase of the RADHARD 500% gate - source separation VJFET breakdown voltage in comparison to the original device is due to the reduced magnitude of the electric field at the gate - source junction of the modified device, another beneficial feature of this structure.

To determine the optimum VJFET structure and operating conditions, a selection of the best performing cases studied, under the influence of aerospace specific scenario 1, are shown by the drain source total current density transient response data in Figure 4.18. Both the original VJFET structure and the RADHARD 500% structure, with the best performing gate - source bias condition at -40 V and the standard -60 V have all been considered. The RADHARD 500% device shows the best performance with both channel and gate impacts resulting in smallest transient duration with secondary current density transient peaks reaching only 0.05 MA/cm^2 and 0.045 MA/cm^2 for the gate and channel impacts respectively - 75% and 70% lower than the corresponding impacts for the original device.

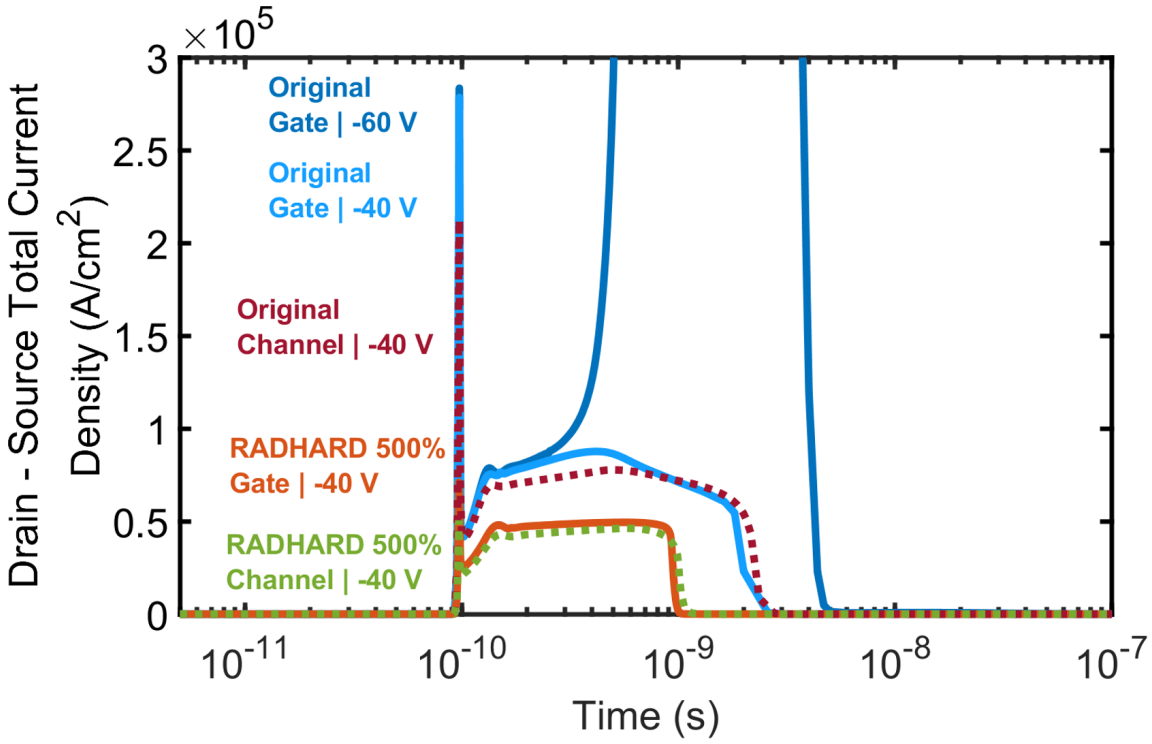


Figure 4.18: Drain - source total current density transient response of the original and RADHARD 500% gate - source separation VJFET structures to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion). Both gate and channel impact location data are included with either a gate - source bias of -60 V or -40 V used.

The gate - source current density transient response of the same selection of best performing cases studied are shown by the data in Figure 4.19. The key feature to note is the similarity in the response of the -40 V gate - source biased original and RADHARD 500% VJFETs when subjected to a gate impact. With a maximum peak of 4.3 MA/cm^2 and 4.4 MA/cm^2 for the original and RADHARD 500% gate impacts respectively and no indication of enhanced avalanche multiplication - as can be seen in the -60 V gate - source bias original VJFET gate impact - it shows that the gate - source current density response is dominated by the gate - source bias applied.

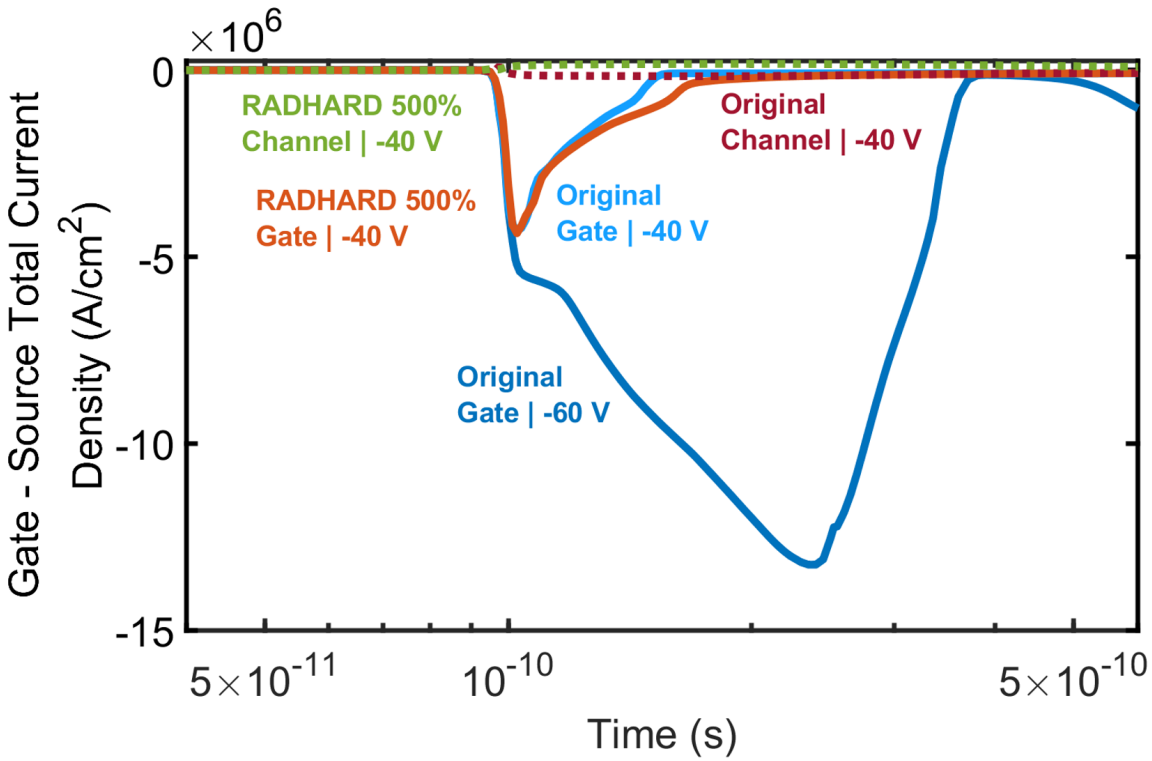


Figure 4.19: Gate - source total current density transient response of the original and RADHARD 500% gate - source separation VJFET structures to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion). Both gate and channel impact location data are included with either a gate - source bias of -60 V or -40 V used (figure enlarged for clarity).

The maximum lattice temperature is one of the main parameters used to identify the SEB sensitivity of a device, and the data shown in Figure 4.20 outline the performance of the best performing cases studied against aerospace specific scenario 1. In comparison to the original device gate and channel impacts at a gate - source bias of -40 V, the RADHARD 500% device provides a 7% reduction in the final maximum lattice temperature. The weak point of the VJFET, the gate impact location, highlights the importance of gate - source bias derating to reduce the SEB sensitivity. Under gate impact conditions both the modified RADHARD 500% and the original structure generated matching peak temperatures at 620 K at the instant of impact. This is in stark contrast to the original device at a -60 V gate - source bias with a peak temperature of 2650 K.

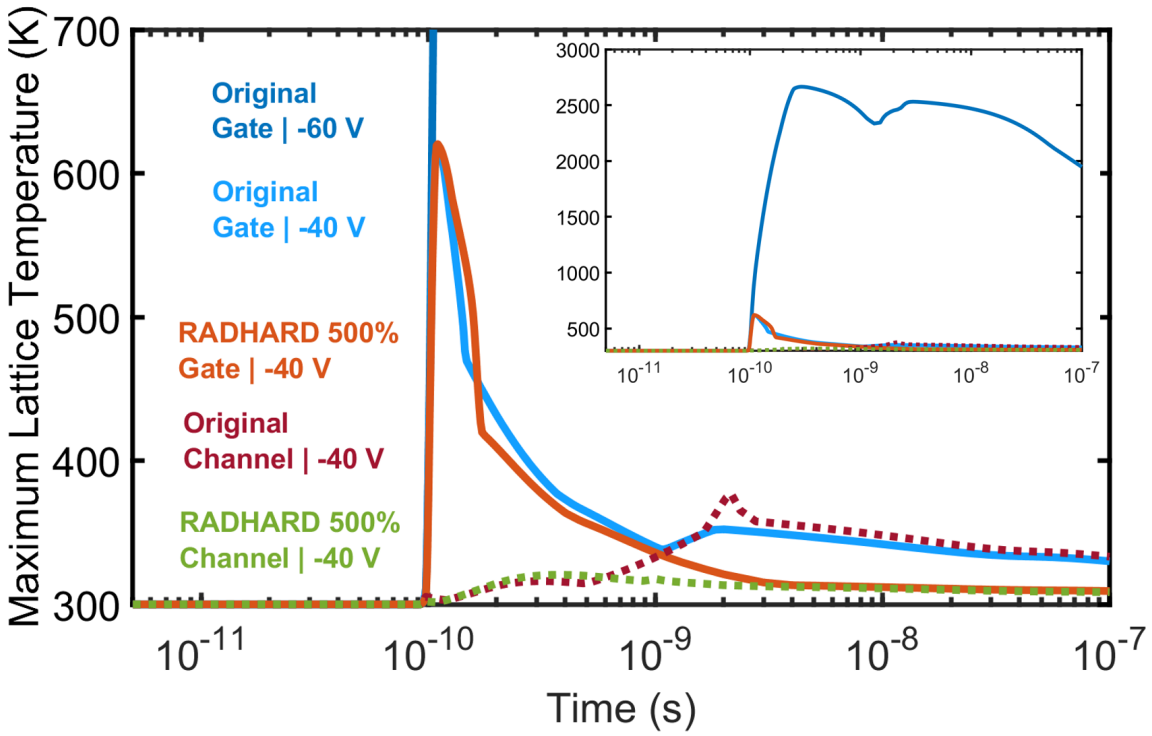


Figure 4.20: Maximum lattice temperature transient response of the original and RADHARD 500% gate - source separation VJFET structures to aerospace specific scenario 1 (1000 V drain - source bias, 40% derating, with a deposited charge equivalent to 300% of a silver ion). Both gate and channel impact location data are included with either a gate - source bias of -60 V or -40 V used.

4.7 Conclusions

Unlike the SiC power diode structure discussed in Chapter 3, which displayed a near ideal response to cosmic ray interaction requiring no derating to resist SEB, the 2D structure of the VJFET has the potential to fail at drain - source deratings at values as low as 40% - far below the industry standard derating of 70%. This is due to the gate region of the device and the influence this has on the internal electric field. Peak pre-strike internal electric field magnitudes of 1.5 MV/cm at the gate - source junction were observed for the 40% drain - source derating case. This, coupled with the knowledge that after impact the internal electric field can reach values 2.5 times that of the original pre-strike, it can be understood as to why large scale avalanche multiplication and SEB can occur.

To reduce the magnitude of the internal electric field between the gate and source

of the device a reduction in the applied gate - source bias was investigated. By lowering the original gate - source bias of -60 V to -40 V, for a drain - source bias derating of 40%, the peak internal electric field was reduced by 33% - from 1.5 MV/cm to 1.0 MV/cm. The lower gate - source bias case resulted in the avoidance of a potential shoot-through failure when subjected to a typical aerospace specific scenario, a deposited charge equivalent to 300% that of a silver ion. The trade-off, however, is the restriction in the maximum possible drain - source bias being limited to a derating of 70%.

An alternative radiation hardening strategy in the form of an increase in the VJFET gate - source separation, results in a reduction to the magnitude of the gate - source internal electric field. By increasing the gate - source separation of the original JFET by 4.0 μm a peak electric field reduction of 64% is observed which had resulted in a 99% reduction in peak drain - source current density between the two structures when subjected to a 40% drain - source bias derating and a deposited charge equivalent to 300% that of a silver ion used in SEB testing. Additional benefits of the increased gate - source separation device include the ability to mitigate short channel effects, an increase in breakdown voltage and a reduction in threshold voltage.

The alteration of the SEB sensitivity of the VJFET is limited to the techniques discussed due to the process of device fabrication. However, if a SEB hardened JFET was to be designed with major reductions to SEB sensitivity in comparison to the original VJFET, there would be a valid argument to produce this device despite the associated costs. As it has been shown in this chapter, structural modifications to the device can result in drastic reductions in SEB sensitivity - pushing these modifications further could lead to a device which could be a real game changer.

5 Single Event Burnout Sensitivity of a Bespoke Radiation Hardened SiC JFET

The radiation hardening of devices is a critical field where millions are invested in the development of structures which provide benefits in the response to radiation interaction. Building on the findings of Chapter 4, with the potential to make non - fabrication limited changes to the device, a new bespoke structure is considered - the lateral JFET (referred to as the LJFET from here on). This structure has been devised in order to further reduce the SEB sensitivity of a potential device which could be used as a like for like replacement in an aerospace application. The following chapter investigates the SEB sensitivity of this bespoke structure.

5.1 The Lateral JFET Structure

The structure of the LJFET builds on that of the vertical JFET - through the inclusion of an additional gate. Two channels are now created, one vertical and one lateral, allowing for greater current control in the device - which is thought to be of benefit when controlling the large SEB generated currents shown in the previous chapters. In the VJFET structure electrons flow directly from the source to the drain of the device, which is unlike that of the LJFET where the electrons have to flow from the source and past the gates, through both the lateral and vertical channels before reaching the drain, thus providing additional current control. The schematic of the LJFET is shown in Figure 5.1. This device consists of a top gate (top left p^+ region on schematic), a back gate (lower right p^+ region), a source (top right n^+ region) and a drain (bottom n^+ region). Doping concentrations, and device dimensions have all been selected to emulate the real world version of this device. As with the VJFET of Chapter 4, in order for the device to conduct, a drain - source bias is applied. For this normally on structure a negative bias is applied to the gates in order to pinch off the channel and block conduction when required. The transfer characteristics and breakdown voltage of the device are shown by the data in Figure 5.2. Due to the mission critical nature of this device when used as a component in a potential power system for an aerospace application, it is imperative that the channel is fully blocked

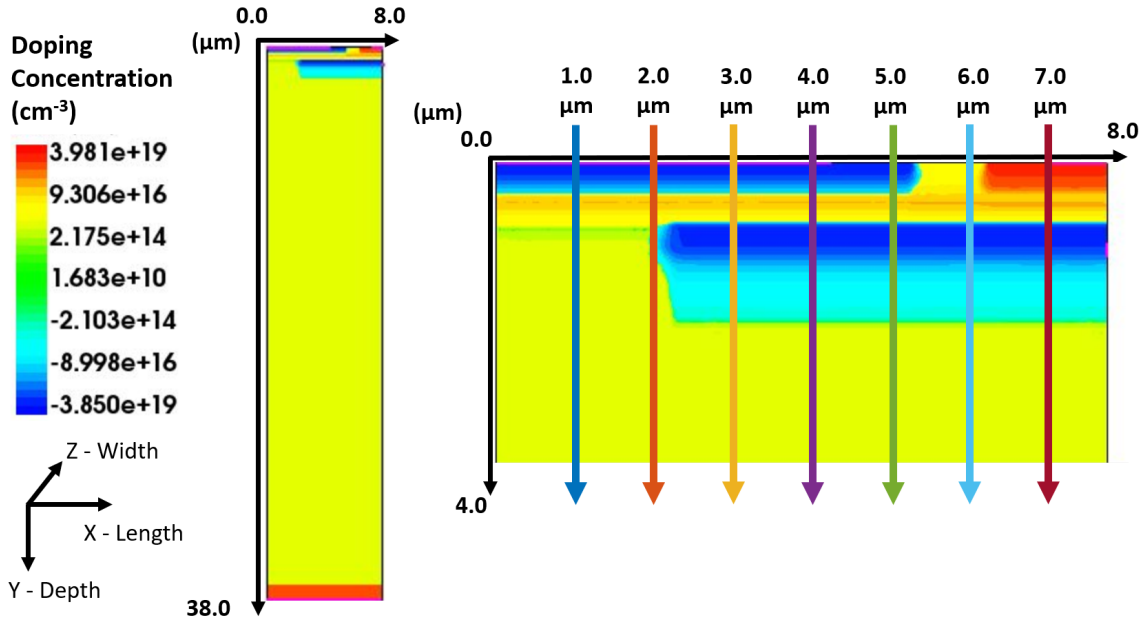


Figure 5.1: The LJFET with heavy ion impact locations indicated.

when needed. When a 99% drain - source derating is applied to the device, the gate - source threshold voltage is -6 V, as shown by the data in Figure 5.2(a). For this reason a gate source bias of -15 V has been selected, as this would match the real world precautions that would be made to protect the device against the potential impact transient spikes would have on the system.

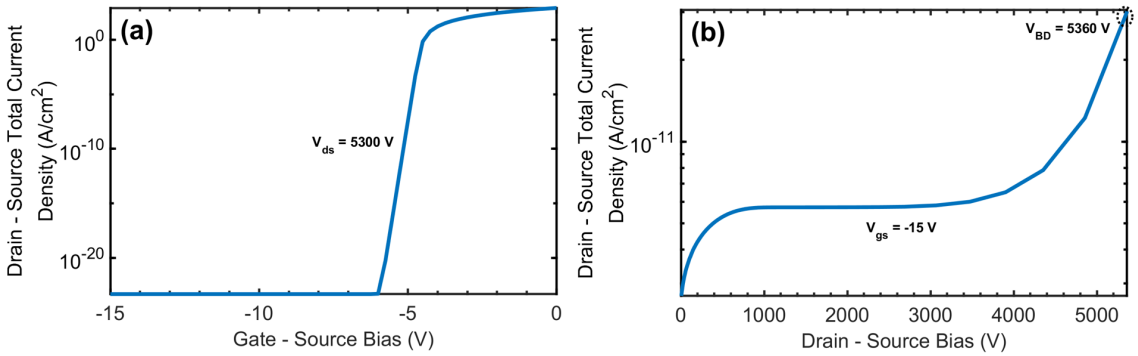


Figure 5.2: LJFET transfer characteristics, (a), and breakdown, (b), both at 300 K.

Due to the structural variations between the VJFET and the LJFET the breakdown voltages differ. The larger drift region of the LJFET, 30 μm greater than that of the VJFET, results in a breakdown voltage of 5360 V when a gate - source bias of -15 V is applied, as shown by the data in Figure 5.2(b).

To gain an understanding of the structural influence on device response to heavy ion impact, 7 different impact locations across the top surface of the device have been simulated - they are shown by the schematic in Figure 5.1. The impact locations have a 1 μm separation and the length of the heavy ion path, at 6.25 μm, matches that of standard heavy ion simulations performed in both Chapter 3 and Chapter 4 - to aid comparison between the structures studied. The LJFET incorporates structural features from both the p–i–n diode from Chapter 3 and the VJFET from Chapter 4. The 1 μm impact location cuts through the top gate, p^+ doping, and part of the drift region, n^- doping, of the LJFET only - similar to the p–i–n diode of Chapter 3. The 7 μm impact location cuts through the source, n^+ doping, back gate, p^+ doping, and part of the drift region, n^- doping, of the LJFET - similar to the gate impacts of the VJFET in Chapter 4. From the findings of the previous chapters it is predicted that a higher SEB sensitivity will be observed at the 7 μm impact location as the larger magnitude of the electric field in this region resulted in a lower bias to failure for a given heavy ion deposited charge.

5.2 Structural Influence on Device Radiation Response

The key difference between the LJFET and the VJFET is the addition of a top gate. Two channels are created within the LJFET and for this reason a number of unique regions within the device are present, which are of interest when considering the SEB sensitivity. To provide a representation of potential real world operating conditions the LJFET is now studied at a 70% drain - source derating, the industry standard, with a heavy ion deposited charge equivalent to 30% that of a silver ion commonly used in SEB testing - for 7 different impact locations across the top surface of the device. The transient response of the top gate is examined first, as shown by the data in Figure 5.3. For all impact locations studied an initial transient current density peak is observed at the instant of heavy ion impact. A trend in the magnitude of these peaks exist, with the largest peaks observed at the device edges (1 μm and 7 μm impacts). For the impacts between 1 μm and 5 μm, current is flowing from the top gate to the source - the opposite is true for the remaining impacts of 6 μm and 7 μm where current flows from the source to the top gate. The variation in behaviours centre around the top gate - source separation, as shown by the schematic in Figure 5.1. After the initial impact from the heavy ion all current density transients

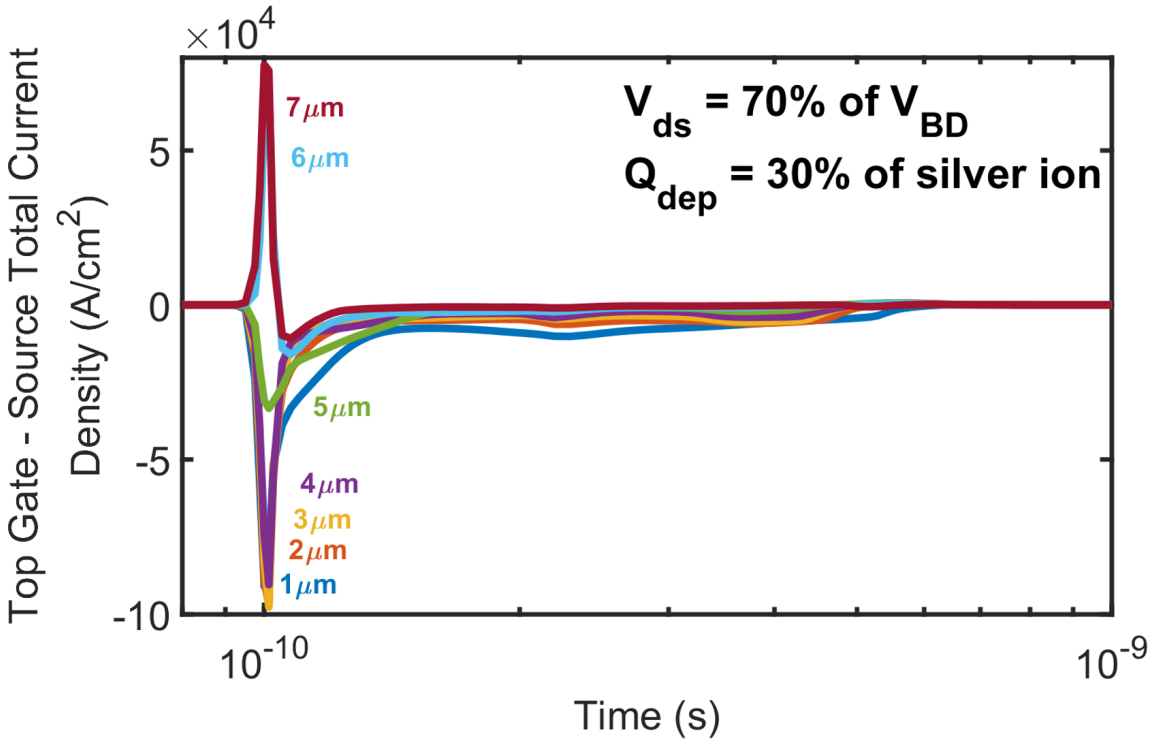


Figure 5.3: Top gate - source total current density transient response of the LJFET to a 3800 V drain - source bias, 70% derating, with a deposited charge equivalent to 30% of a silver ion whilst at a gate - source bias of -15 V for a number of top surface impact locations - as shown by the data in Figure 5.1. Please note that this figure has been cropped to show the region of interest.

decay and return to their pre-strike conditions within a nanosecond. No secondary current spikes are observed for any of the impact locations indicating the lack of SEB occurrence here.

It is important that the back gate response of the LJFET to heavy ion impact is considered - the corresponding data for all 7 impact locations are shown in Figure 5.4. The impacts on the left hand side of the top gate - source lateral separation, from 1 μm to 5 μm, show a positive current from the back gate to the source. This is unlike the behaviour of the 6 μm and 7 μm impacts where current flows from the source to the back gate. The response of the back gate is opposite to that of the top gate for all impact locations studied. Despite the variation in peak current densities generated by the heavy ion at the instant of impact, the following response of all impact locations is similar, with a decay in magnitude and a return to pre-strike conditions within a nanosecond after impact, matching that of the top gate response.

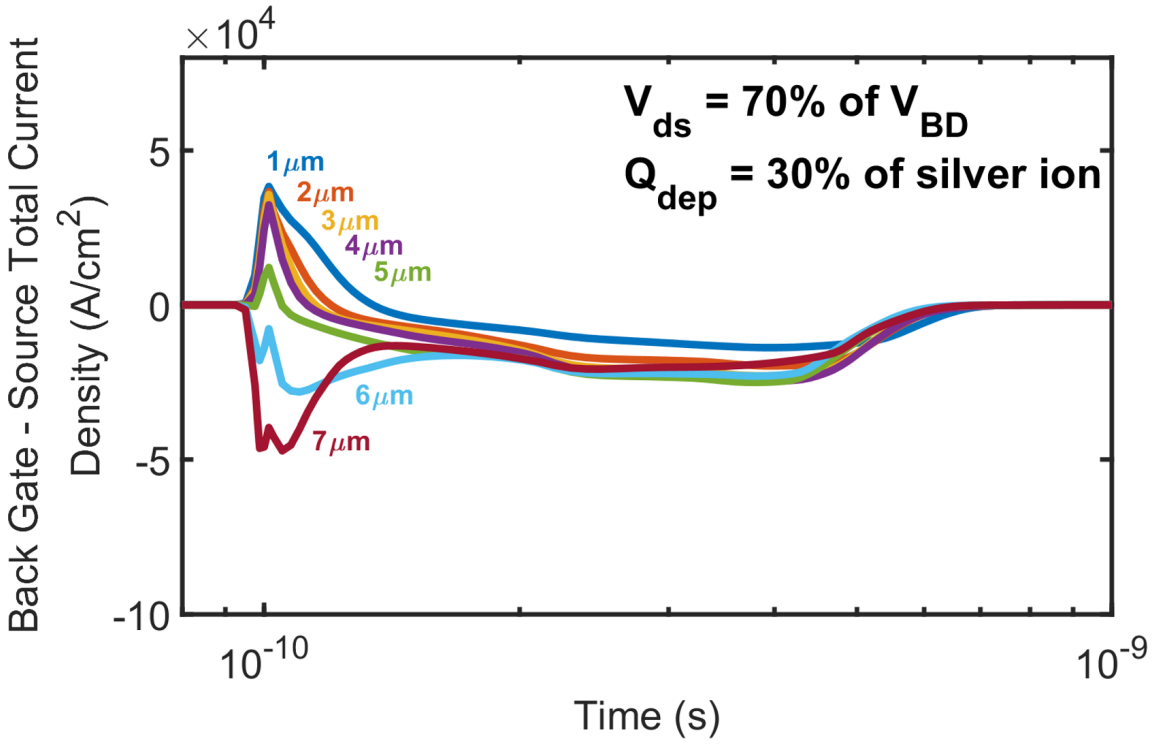


Figure 5.4: Back gate - source total current density transient response of the LJFET to a 3800 V drain - source bias, 70% derating, with a deposited charge equivalent to 30% of a silver ion whilst at a gate - source bias of -15 V for a number of top surface impact locations.

It is also important to understand the radiation response of the LJFET drain - data are shown for all heavy ion impact locations Figure 5.5. At the instant of impact the heavy ion generated current peaks of all 7 impacts have similar magnitudes at $\sim$0.04 MA/cm^2, with matching directions of current flow from source to drain. Despite the variation in the transient profile for all impact locations, each returned to the pre-strike condition within a nanosecond after impact, which again is a similar feature to the top gate and back gate transient responses. No impact location shows a higher level of SEB sensitivity - indicating that there are no weak points of the LJFET to heavy ion impact. This is unlike the behaviour of the VJFET studied in Chapter 4 where heavy ion impacts at the gate region of the device resulted in a higher sensitivity to SEB in comparison to channel impacts - which was understood to be due the higher magnitude of the electric field in these locations.

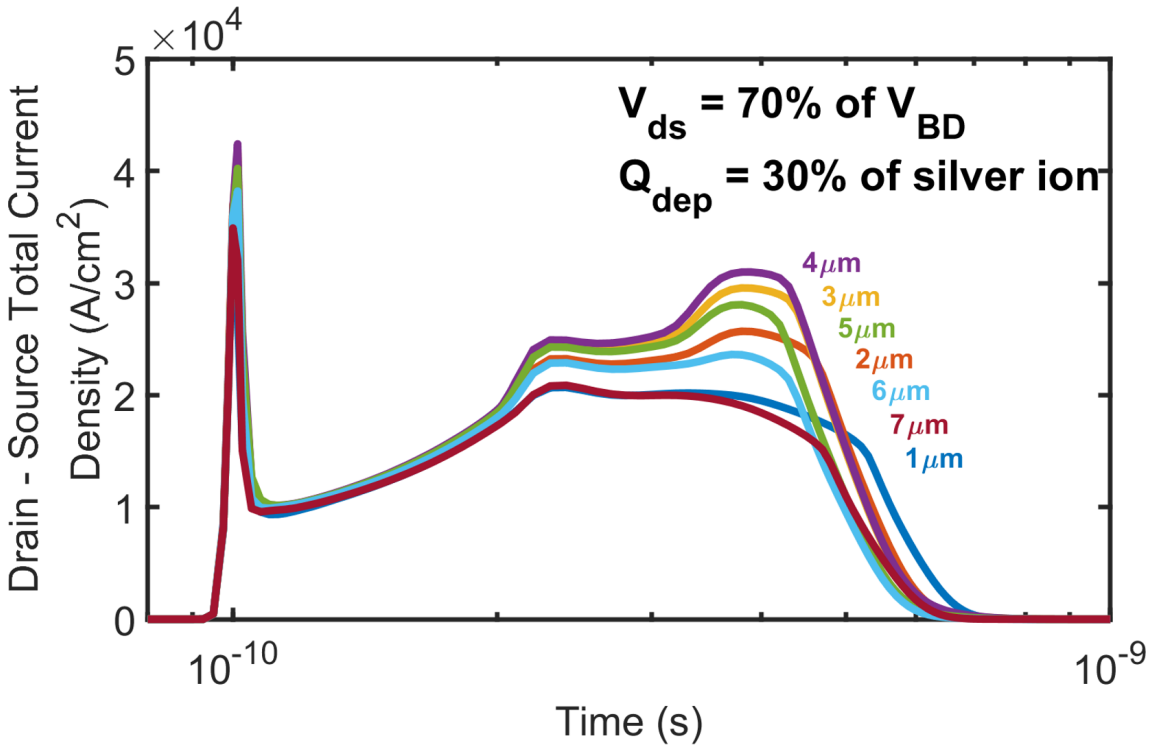


Figure 5.5: Drain - source total current density transient response of the LJFET to a 3800 V drain - source bias, 70% derating, with a deposited charge equivalent to 30% of a silver ion whilst at a gate - source bias of -15 V for a number of top surface impact locations.

The maximum lattice temperature is the key parameter in the determination of the SEB sensitivity of a device - with the occurrence of SEB being device melting after heavy ion impact. The temperature response of the LJFET is now considered for all 7 impact locations studied, as shown by the data in Figure 5.6. At the instant of heavy ion impact the peak temperatures of all 7 impact locations are within a range of 5 K, with the lowest temperature observed at 306 K for the 7 μm impact and the highest at 311 K for the 4 μm impact. The simulations all conclude at at time of 0.1 microseconds, and at this point the maximum lattice temperatures of all impact cases are within a 1 K range - highlighting the lack of structural influence on radiation response. In comparison to the VJFET when simulated to matching conditions, a drain - source bias derating of 70% and a heavy ion deposited charge of 30% that of a silver ion commonly used in SEB testing, the device underwent SEB when channel impacts were considered - SEB did not occur for the gate impacts. The LJFET shows superior resistance to SEB under these conditions - due to the inclusion of the top

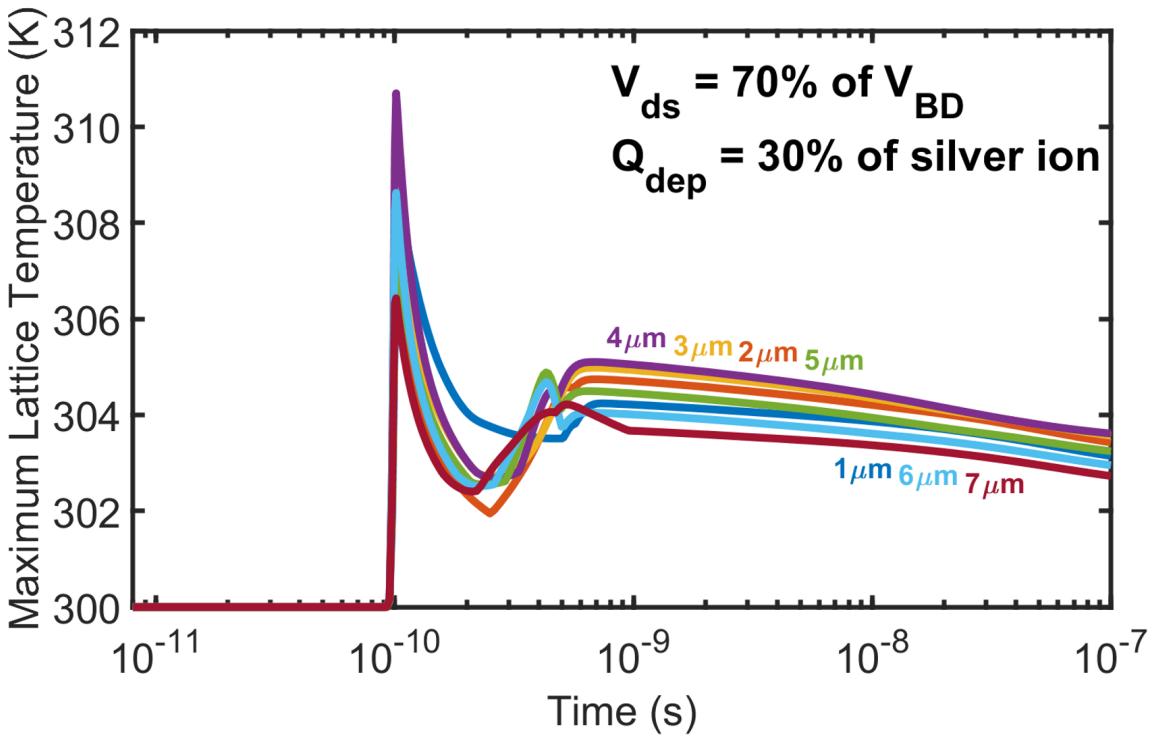


Figure 5.6: Maximum lattice temperature transient response of the LJFET to a 3800 V drain - source bias, 70% derating, with a deposited charge equivalent to 30% of a silver ion whilst at a gate - source bias of -15 V for a number of top surface impact locations.

gate and additional channel, which in turn controls the SEB generated current.

The LJFET can withstand heavy ion impacts to a potential real world scenario at a drain - source derating of 70% and a charge deposition of 30% that of a silver ion. It is therefore important that the SEB sensitivity limits of this device are identified. Through simulation at an increased bias derating the deposited charge to induce SEB can be pinpointed. A drain - source derating of 99% is now used. Additionally, to further understand the role the device structure plays on the overall response to heavy ion impact, two impact locations at the edges of the device are considered, the 1 μm and 6 μm cases. The 1 μm impact resembles that of the simulation of p–i–n device in Chapter 3, whereas the 6 μm case is novel to the LJFET in that the impact passes through through the top of the device and the back gate without going through the source. The drain - source total current density transient response of the LJFET for the 1 μm and 6 μm impact locations at a 99% drain source derating for the SEB occurrence transition point are shown by the data Figure 5.7. For a deposited charge value of 6% that of a silver ion, both impact locations do not undergo SEB, as shown

by the data in Figure 5.7(a). The drain - source total current densities of the 1 μm and 6 μm cases both peak at 0.015 MA/cm^2 at the instant of heavy ion impact, 0.1 ns. Both transient responses decay to the pre-strike values within a nanosecond after impact.

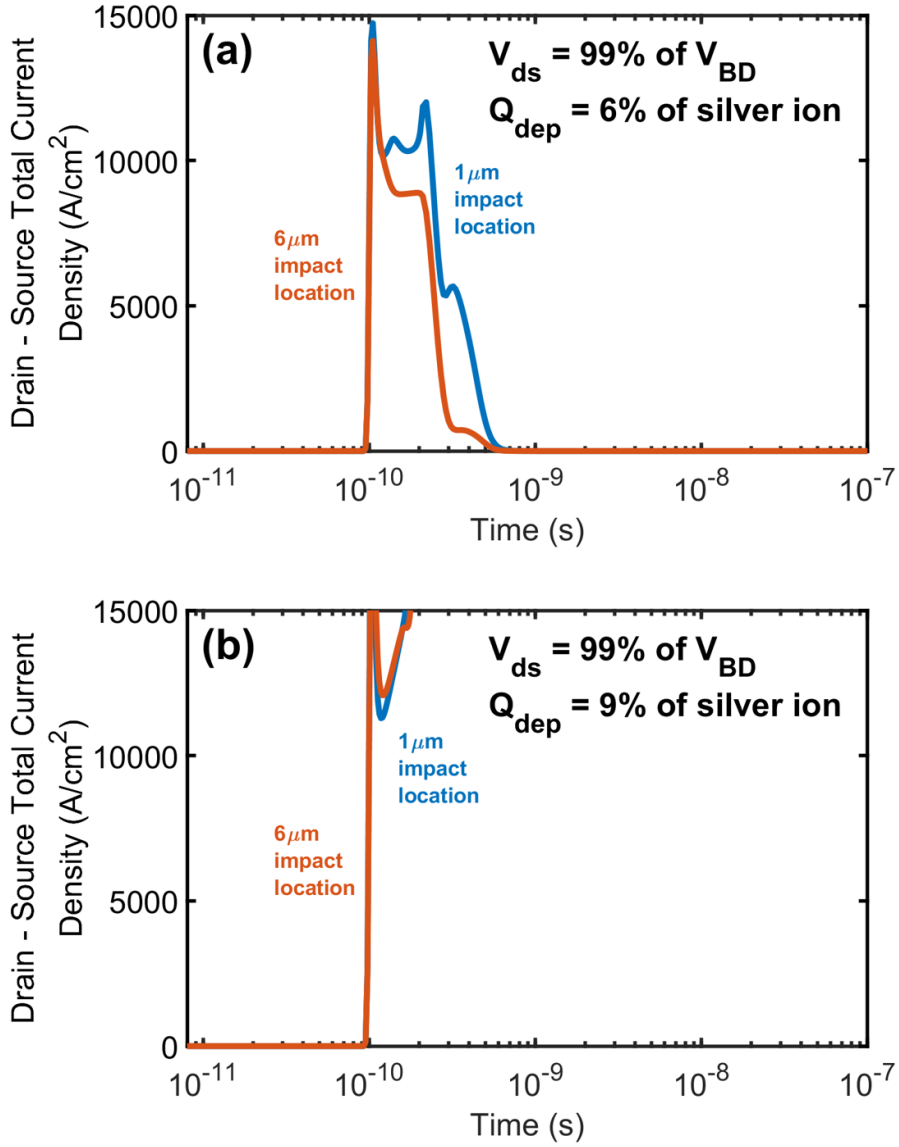


Figure 5.7: Drain - source total current density transient response of the LJFET to two heavy ion impacts on either edge of the device, at 1 μm and 6 μm, for a 5300 V drain - source bias, 99% derating, a gate - source bias of -15 V with a deposited charge equivalent to 6% of a silver ion, (a), and 9% of a silver ion (b).

At a higher deposited charge SEB is observed for both impact cases, as shown by the data in Figure 5.8(b). For a deposited charge value equivalent to 9% that of a silver ion commonly used in SEB testing, the initial heavy ion induced drain - source current density peaks reach a magnitude of 0.015 MA/cm^2 - matching that of the 6% silver ion simulations. However, within 0.1 ns these current densities spike to over 20 MA/cm^2 (not shown in the figure). This response is characteristic of the occurrence of SEB.

The maximum lattice temperature provides a clear indication of either the occurrence or non-occurrence of SEB, and for this reason the transient response of the LJFET to both the 1 μm and 6 μm heavy ion impact cases are shown by the data in Figure 5.8.

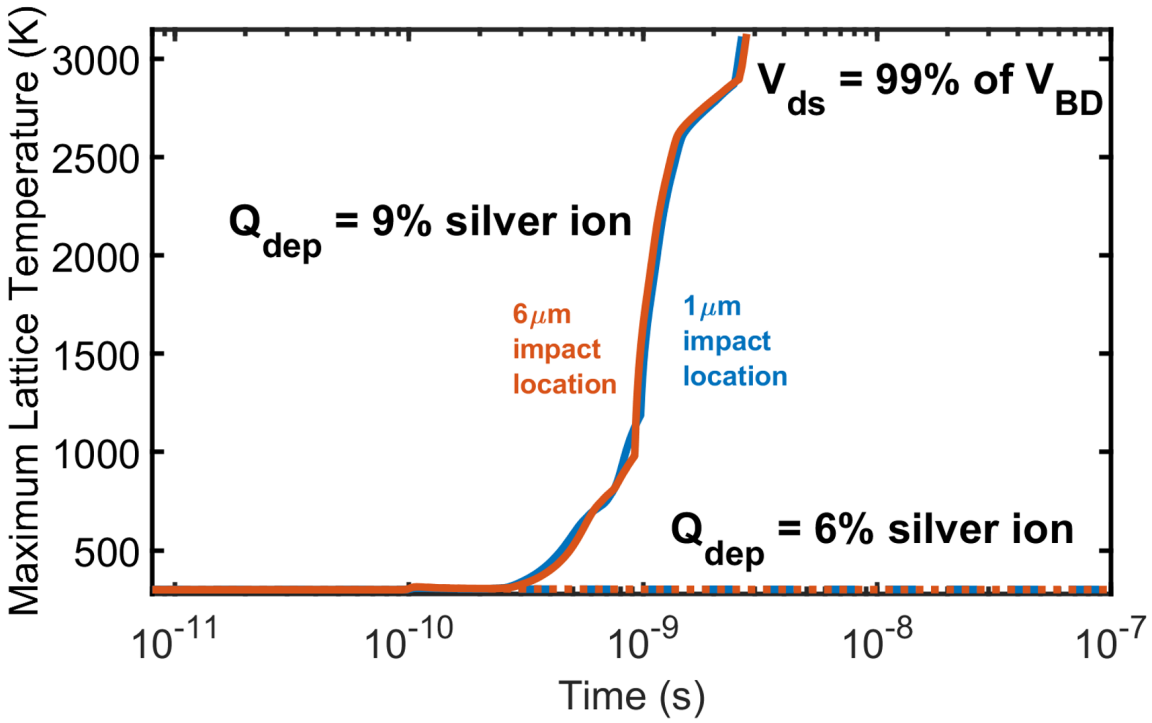


Figure 5.8: Maximum lattice temperature transient response of LJFET to two heavy ion impacts on either edge of the device, at 1 μm and 6 μm, for a 5300 V drain - source bias, 99% derating, and a gate - source bias of -15 V. Data for two deposited charges are shown which are equivalent to 6% and 9% that of a silver ion commonly used in SEB testing.

This data reinforces the fail or no-fail nature of these two deposited charges applied, with the 6% silver ion resulting in temperatures which return to pre-strike conditions of 300 K, and the 9% silver ion resulting in the SEB failure of the device for both impact locations studied with temperatures reaching 3100 K - the quoted sublimation temperature of SiC. As both the 1 μm and 6 μm heavy ion impacts result in matching responses at either the 6% silver ion deposited charge, where both don't undergo SEB, or the 9% silver ion deposited charge, where both do undergo SEB, it is noted that regardless of top surface impact location on the LJFET, the response will be dictated by bias and deposited charge - similar to the findings reported in Chapter 3 for the p–i–n diode.

To examine the occurrence of SEB in the LJFET in more detail, key internal device snapshots are compared to identify the variation in response for the two deposited charge values studied, the 6% and 9% silver ion deposited charges - corresponding to the non-SEB and SEB cases respectively. As it has been found that impact location on the top surface of the LJFET plays no role in the SEB sensitivity, an impact location of 3 μm has been selected as it is at the centre of the device. Snapshots of the total current density transient response of the LJFET at a drain - source derating of 99%, a gate - source bias of -15 V and deposited charges of 6% and 9% that of a silver ion are shown in Figure 5.9. As has been described earlier in this section, the occurrence or non-occurrence of SEB is indicated within the first nanosecond after heavy ion impact. For this reason snapshots at pre-strike, 100 ps, 200 ps, 600 ps and 800 ps post-strike have all been selected. Additionally, as the variation in SEB response occurs at the top of the device where the gates and source of the device are present, only this part of the LJFET is shown which matches the close-up shown in Figure 5.1. As expected the pre-strike snapshots match as they are at the same bias deratings. A variation in response is apparent 100 ps post-strike - the 9% silver ion case shows the beginnings of source to back gate shoot-through, something which is not observed in the 6% silver ion case. In the 9% silver ion case at 200 ps post-strike, a higher density current density region has formed between the source and back gate at a value of $\sim$5 MA/cm^2. At this instant for the 6% case an elevated current density between the back gate and the drain of the device is created at a value of $\sim$0.05 MA/cm^2.

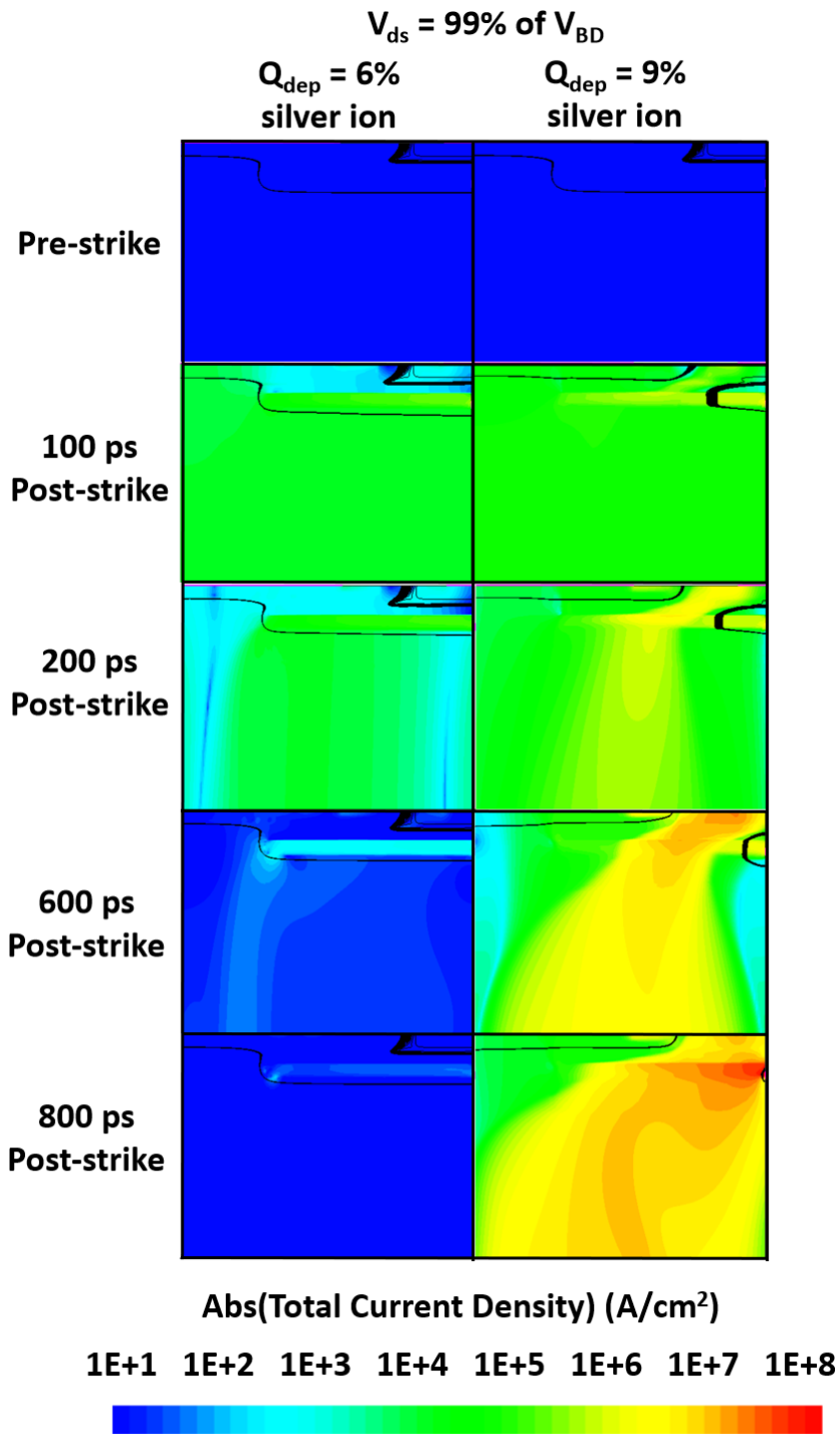


Figure 5.9: Key structure snapshots of the total current density transient response of the LJFET at 5300 V drain - source bias, 99% derating, and -15 V gate - source bias for a 3 μm heavy ion impact with deposited charge values equivalent to 6% and 9% that of a silver ion commonly used in SEB testing. Black lines correspond to the electrostatic potential. Please note that these snapshots are comparable to that of the close-up of the LJFET as shown in Figure 5.1.

Moving to 600 ps after impact, it can be seen on the 9% silver ion case that the back gate to source short has expanded and developed into a higher density short between the source and drain - this happens at the same time as the 6% silver ion case returns to pre-strike conditions. At 800 ps after impact the 6% silver ion case has not undergone SEB whilst the 9% silver ion continues to generate a source to drain short with peak current densities above 50 MA/cm^2 - at this stage lattice temperatures rise to ∼1100 K and SEB is imminent.

Despite the superior radiation response of the LJFET to that of the VJFET, there is still potential room for improvement in the performance of the LJFET. This can be achieved through further reduction to SEB sensitivity by removing the heavy ion induced source to drain short. The following section focuses on a potential method to alter the SEB sensitivity through modifications to the LJFET back gate.

5.3 Back Gate Modification to Adjust Single Event Burnout Sensitivity

As identified in the previous section, SEB occurred in the LJFET through a short of the source and drain through the back gate. To make this device more robust against SEB a potential modification is suggested - a reduction in the magnitude of the ion implantation of the back gate p^+ well to increase its resistance and potentially reduced the currents generated from the heavy ion impact. An impact location of 7 μm is considered as this is the condition in which the greatest improvement in device response is expected for these modifications. Y-cut profiles of the aluminium active concentration for the 7 μm impact location of both the original and the modified back gate devices are shown by the data in Figure 5.10. The high concentration region at a depth from the top surface of ∼1 μm is of key importance. Here the modified back gate ion implantation dose has been dropped to 20% that of the original. Variation in the aluminium active concentrations can be seen at a depth from top surface of ∼1.5 μm - this is not of concern due to its low magnitudes - this feature is due to the Monte Carlo nature of the ion implantation through simulation.

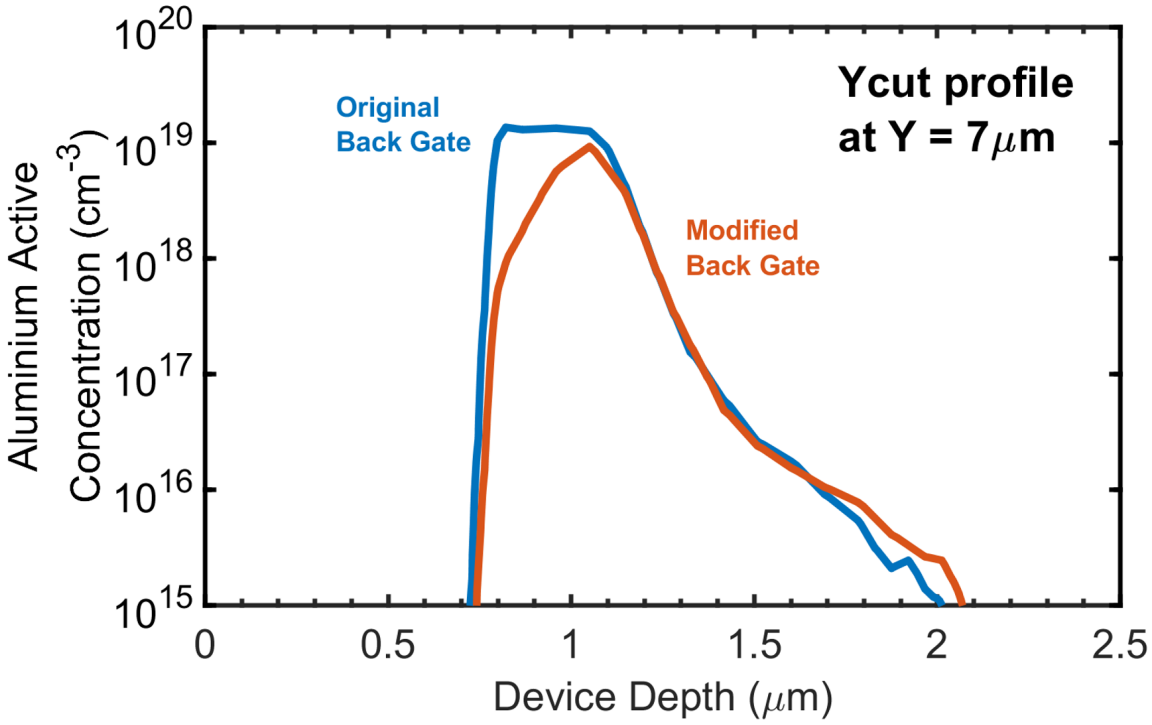


Figure 5.10: Aluminium active concentration y-cut profiles at a top surface impact location of 7 μm, for both original and modified back gate versions of the LJFET. Please note that only the region of interest is shown.

To identify whether the modified back gate provides a reduction to the SEB sensitivity of the LJFET, the 99% drain - source derating coupled with the deposited charge values equivalent to 6% and 9% of a silver ion commonly used in SEB testing have been studied with data shown in Figure 5.11. For the original structure the 6% silver ion does not result in SEB whereas the 9% silver ion does. The modified gate LJFET shows a matching response, with no failure when subjected to a 6% silver ion deposited charge and the occurrence of SEB when a 9% silver ion impacts the device. Rather than reducing the SEB sensitivity, the modified gate has enhanced sensitivity requiring a shorter time period to induce the failure in comparison to the original LJFET. Hence this method is not a viable option to reduce the SEB sensitivity of the LJFET. If the acceptor concentration of the back gate of the modified LJFET was to be lowered further the threshold voltage of the device would be changed - this device would no longer be a like-for-like replacement of the original. Alternatively, raising the acceptor concentration is not possible as the value in the original LJFET is at the upper limit possible with current technology.

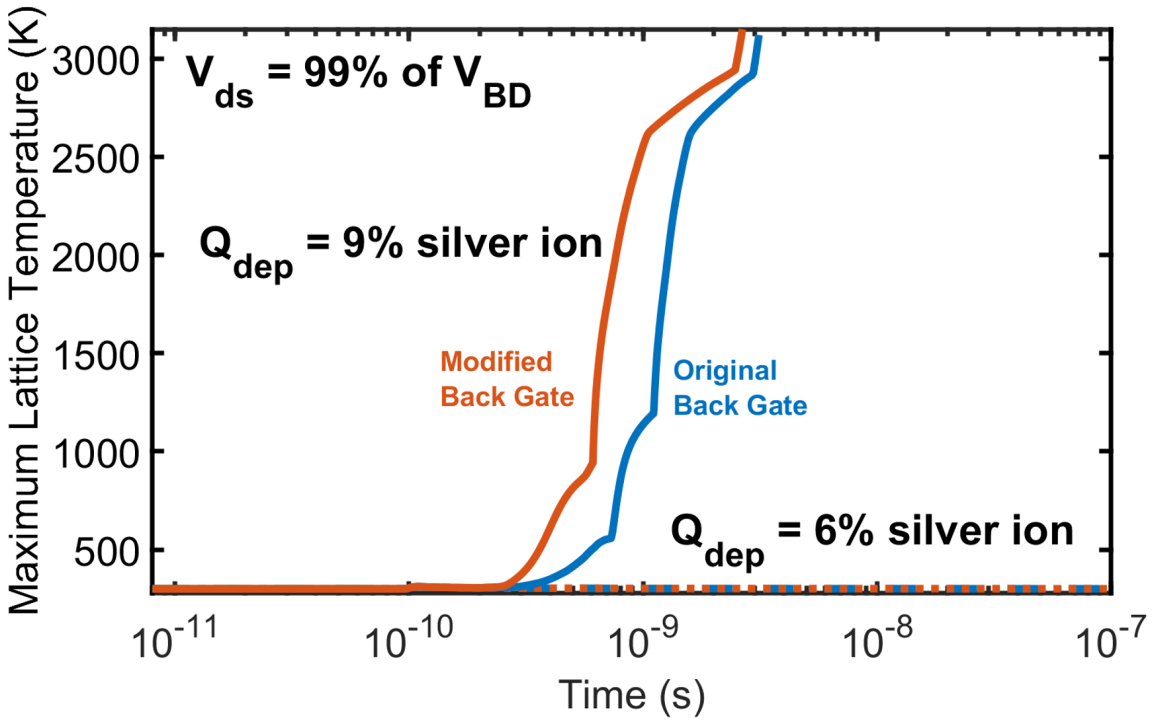


Figure 5.11: Maximum lattice temperature transient response of the original and modified back gate versions of the LJFET at 5300 V drain - source bias, 99% derating, and -15 V gate - source bias for a 7 μm top surface heavy ion impact location with deposited charge values equivalent to 6% and 9% that of a silver ion.

Previously when investigating methods to reduce the SEB sensitivity of the VJFET, two were identified. The first was in relation to the operating conditions of the device. By reducing the applied gate - source bias the magnitude of the internal electric field between the gate and source of the device was reduced. This did have limitations, mainly through reducing the maximum drain - source bias that could be applied prior to breakdown. The second method was a modification to the device structure through increasing the gate - source separation, which also reduced the internal electric field between the gate and the source. For the LJFET there is no option to reduce the gate - source bias as it is already at the real world limit of -15 V. For this reason, the variation of the LJFET gate - source separation is investigated further in the following section.

5.4 Radiation Hardened LJFET through Electric Field Suppression

The VJFET of Chapter 4 was radiation hardened through modification of the gate - source separation where an in increase in the spacing between the gate and source lowered the magnitude of the electric field in that region, in turn reducing the value of the SEB generated current. A similar method is to be applied to the LJFET in an attempt to reduce its SEB sensitivity. For the original LJFET the distance between the back gate and source, termed the back gate source thickness T_{BGS}, was set at 0.82 μm. Four modified versions of the LJFET, which have incorporated additional regrowth (with doping at 10^{16} cm^{-3}) on top of the original structure have been studied - the structures of the modified devices are shown by the schematic of Figure 5.12. The maximum additional regrowth of the modified structures have been set to +500% (+4.1 μm) that of the original T_{BGS}. Burying the gates at depths lower than this becomes unpractical and is not compatible with silicon carbide process capabilities.

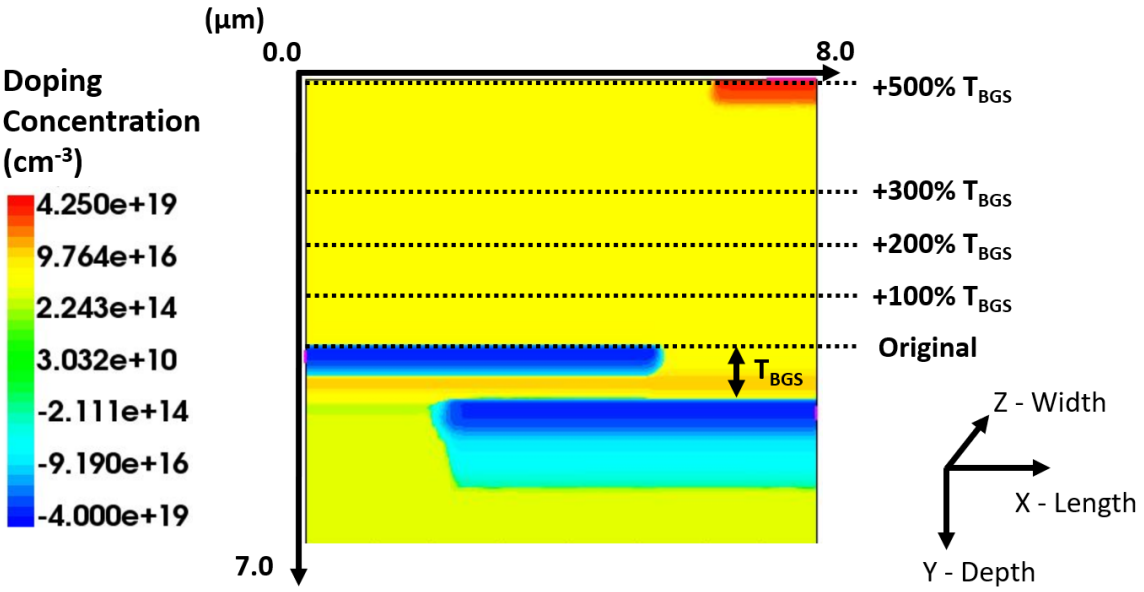


Figure 5.12: The LJFET with 5 different gate - source separations indicated in terms of the original thickness between the back gate of the device and the source, T$_{BGS}$.

It is important that the modified LJFET structures can be used as like-for-like replacements to the original LJFET by having matching electrical behaviours. The transfer characteristics and breakdown voltage of the original and the +500% T_{BGS} modified LJFETs are shown by the data in Figure 5.13. The transfer characteristics of the two devices match as do the breakdown voltages - enabling the modified structure to be used in a real world application without the need for additional system modification.

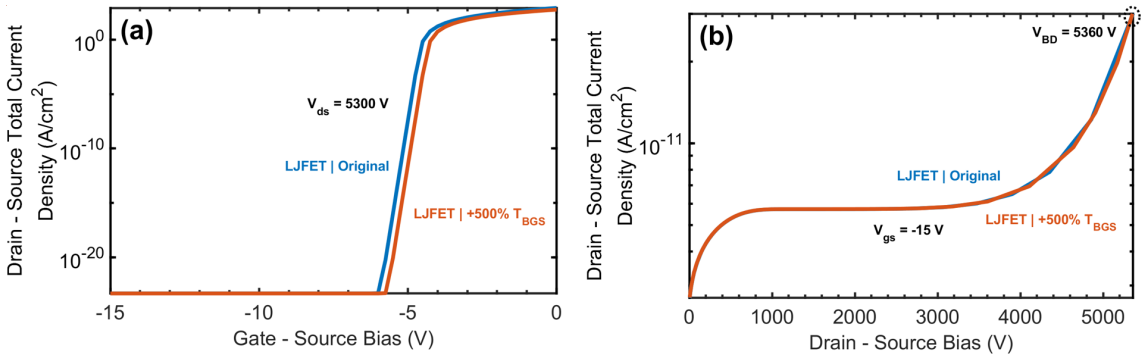


Figure 5.13: The original and +500% T_{BGS} modified LJFET transfer characteristics, (a), and breakdowns, (b), both at 300 K.

Understanding of the internal electric field of the original LJFET and modifications are of paramount importance when considering the respective SEB sensitivity. If a cosmic ray was to impact LJFET and pass through a region of high electric field there is an increased possibility of avalanche multiplication, and in turn, increased SEB sensitivity. Real-world scenarios need to be considered. It is also of importance that a direct comparison can be made between the structures studied in Chapter 4, the VJFET and its modifications, where a focus was placed on both the 40% drain - source bias derating with deposited charge equivalent to 300% that of a silver ion commonly used in SEB testing, and also the 70% drain - source bias derating commonly used in industry. For this reason the pre-strike internal electric field y-cut profiles, at a top surface impact location of 3 μm, of the LJFET and modified variations at two device drain - source deratings of 40% and 70% are shown by the data in Figure 5.14.

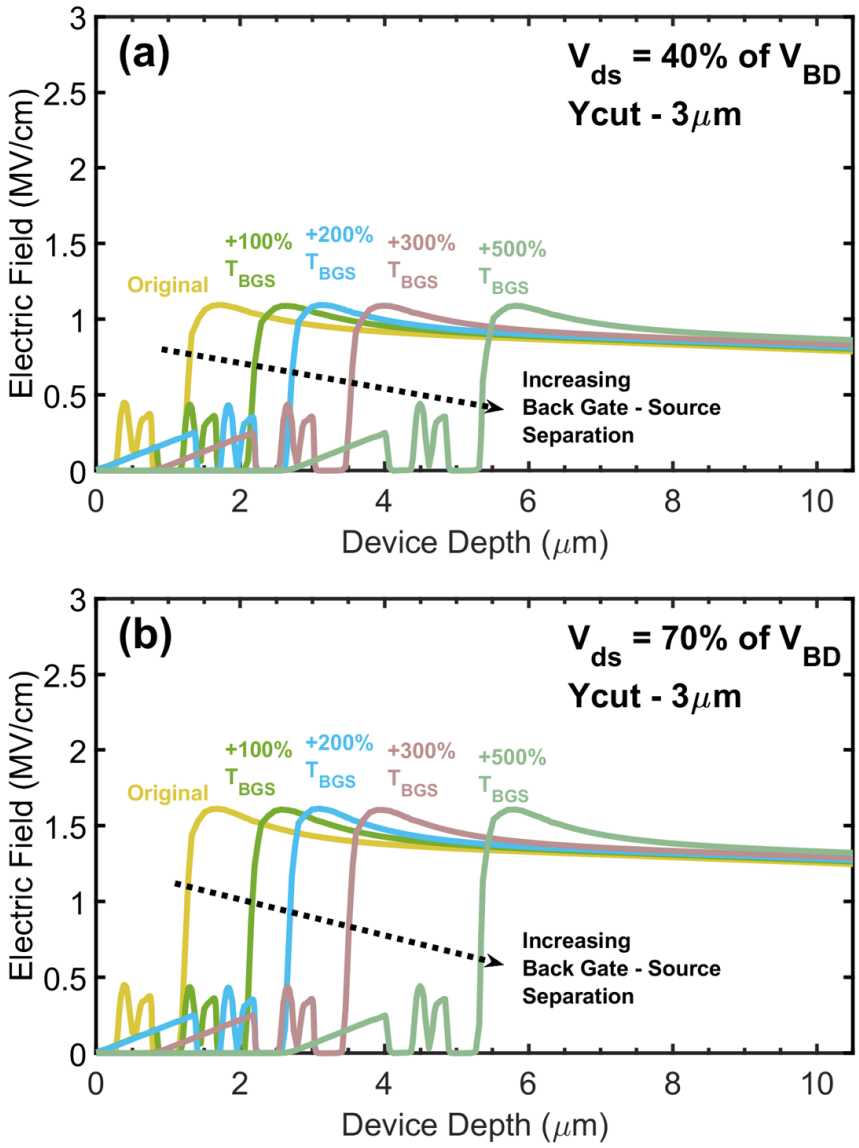


Figure 5.14: Pre-strike internal electric field y-cut profiles at a top surface location of 3 μm for the original LJFET and modifications at a gate - source bias of -15 V, with a drain - source derating of 40%, (a), and the industry standard derating of 70%, (b).

The y-cut profile of the LJFET and modifications at a drain - source derating of 40% are shown by the data in Figure 5.14(a). The electric field peak for the original LJFET exists at a depth from top surface of 1 μm. Between the top surface of the device and this peak a region of low electric field magnitude is present, a feature which is present for all devices studied. As the back gate to source separation increases the location of the peak electric field is shifted further from the top surface of the device to the last peak value of the +500% T_{BGS} modification at 5.5 μm. The benefit of the

+500% T_{BGS} modification over the original LJFET is that there is a larger region of low electric field prior to the peak at the back gate. At an industry standard drain - source derating of 70% similar characteristics are observed to that of the 40% derating case, however, at elevated electric field, as shown by the data in Figure 5.14(b). For this drain - source derating of 70% the electric fields peak at 1.6 MV/cm for all devices studied - a fraction of the critical electric field of SiC at ∼3 MV/cm. With respect to this, a key finding of Chapter 3 was that after heavy ion impact on the p–i–n structures studied, the internal electric fields increase by up to 2.5 times their pre-strike value - a feature that could potentially induce SEB for the LJFET.

Two real world scenarios are considered for the original LJFET and the modifications - a drain - source deratings of 40% and a drain - source derating of 70%, with both experiencing a deposited charge equivalent to 300% that of a silver ion commonly used in SEB testing, with the former matching the conditions of aerospace specific scenario 1 discussed in Chapter 4. A key parameter used to identify the SEB sensitivity of a device is the maximum temperature generated from the ion impact, with SiC sublimation indicating the occurrence of SEB.

The maximum lattice temperature transient response of the devices studied to these scenarios are shown by the data in Figure 5.15. The first scenario of a drain - source derating of 40% and a deposited charge of 300% that of a silver ion, shall now be considered, as shown by the data in Figure 5.15(a). Peak temperatures of all devices studied range between 322 K for the original LJFET to 306 K for the +500% T_{BGS} modification - highlighting the influence of the low electric field region present in the latter. Neither the original LJFET or any of the modifications undergo SEB for this scenario. The maximum lattice temperature responses of the original LJFET and modifications to the second scenario - a drain - source derating of 70%, the industry standard, with a deposited charge of 300% that of a silver ion commonly used in SEB testing, are shown by the data in Figure 5.15(b). Contrasting behaviours are observed with the original, +100% T_{BGS}, +200% T_{BGS} and +300% T_{BGS} devices all undergoing SEB as their peak temperatures exceeded the sublimation temperature of SiC at 3100 K. The +500% T_{BGS} device did not undergo SEB where a peak temperature of 313 K was obtained - largely due to the low magnitude electric field region between the top surface of this device and the back gate, limiting the potential of avalanche multiplication after heavy ion impact.

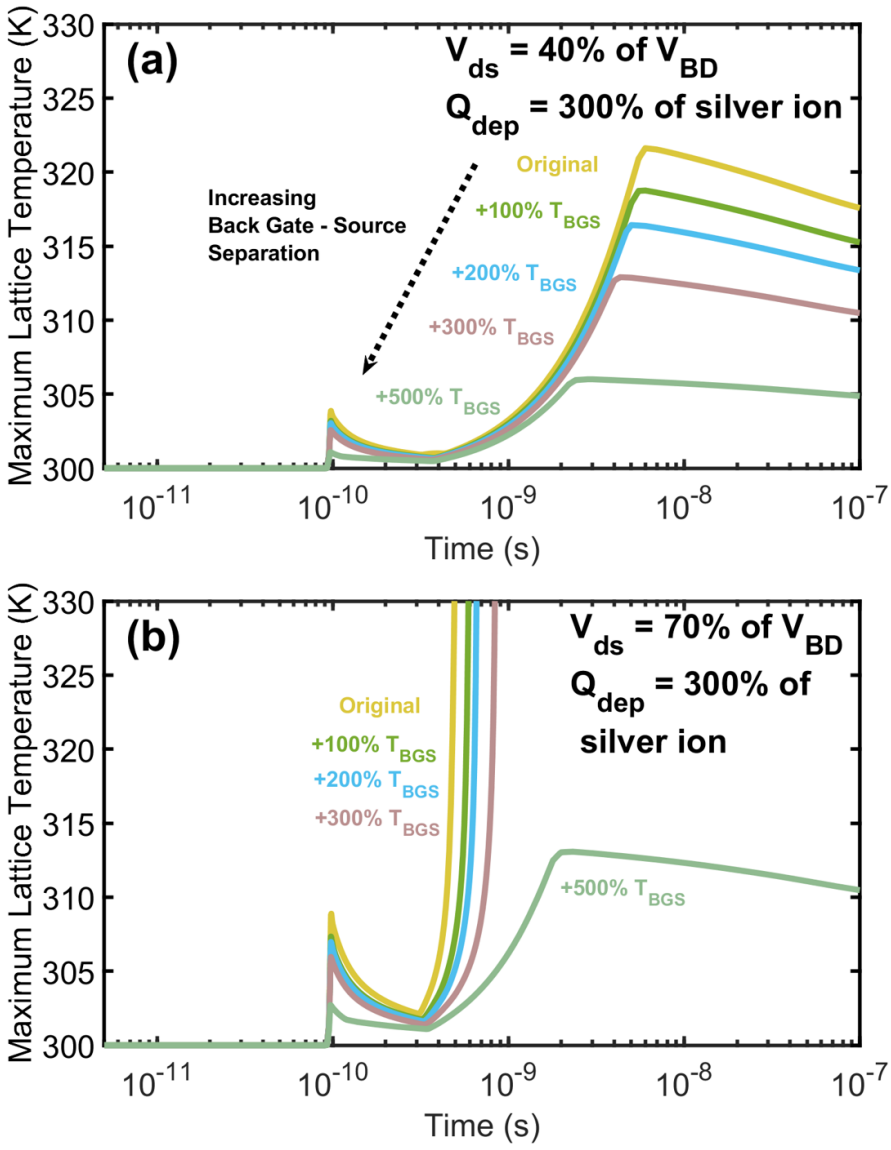


Figure 5.15: Maximum lattice temperature transient response for the original LJFET and modifications for a heavy ion deposited charge equivalent to 300% of a silver ion with an impact location at a top surface position of 3 μm, a gate - source bias of -15 V, with a drain - source derating of 40%, (a), and the industry standard derating of 70%, (b).

5.5 Single Event Burnout Sensitivity of JFET Structures

To this point a number of devices have been considered as radiation hardened alternatives to the original VJFET structure of Chapter 4. All modifications have focused on manipulating the internal electric field of the respective devices whilst maintaining standard electrical characteristics. The focus of this section is to understand which de-

vice provides the best overall performance. The original VJFET and LJFET devices are considered with their best case radiation hardened options, the RADHARD 500% VJFET and the +500% T_{BGS} LJFET. The maximum lattice temperature transient response of these devices to aerospace specific scenario 1, a drain - source derating of 40% and a deposited charge equivalent to 300% that of a silver ion commonly used in SEB testing, are shown by the data in Figure 5.16.

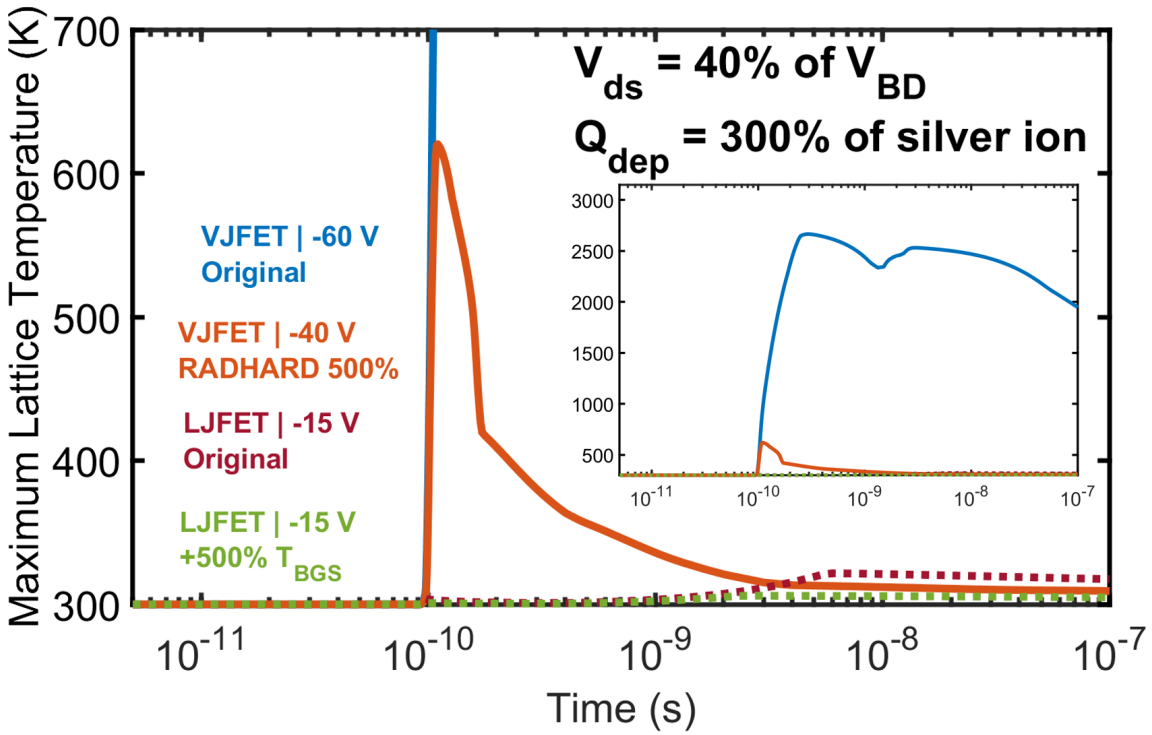


Figure 5.16: Maximum lattice temperature transient response of the original VJFET and LJFET with radiation hardened models for a heavy ion deposited charge equivalent to 300% of a silver ion with a drain - source derating of 40%, referred to as aerospace specific scenario 1. Gate - source bias conditions are shown.

The worst case impact locations have been selected for this comparison, with gate impacts being used for the VJFET and a top surface impact location of 3 μm for the LJFET. The original VJFET with a -60 V gate - source bias has the worst performance with a peak temperature of 2670 K and a final transient temperature of 1950 K. The modified version of the device, the RADHARD 500% VJFET, has a gate - source separation equal to 500% that of the original device. Additionally, a lower gate - source bias is used - resulting in a peak temperature of 620 K and a final transient temperature of 309 K. The sharp initial temperature spike which is present

for both of the VJFET devices is not observed for either of the LJFETs. The original LJFET has a peak temperature of 322 K and a final transient temperature of 318 K. The +500% T_{BGS} LJFET which has an additional regrowth of 500% that of the back gate - source separation has a peak temperature of 306 K and a final transient temperature of 305 K. Despite the marginal final transient temperature benefit the RADHARD 500% VJFET at a gate - source bias of -40 V over the LJFETs, it is felt that the LJFET which lacks the initial peak maximum temperature spike is the device of choice when the SEB sensitivity is concerned.

5.6 Conclusions

When operated under potential real world conditions, a bespoke SiC JFET (LJFET) has resulted in a reduced radiation response to that of devices studied previously. When subject to the same aerospace specific scenario of a drain - source bias derating of 40% and a deposited charge equivalent to 300% that of a silver ion used in SEB testing, the LJFET, which incorporated both a vertical and a lateral channel to counteract the SEB generated currents, showed no variation in top surface impact sensitivity unlike that of the VJFET of Chapter 4. The peak temperature for the LJFET under this scenario was 322 K, 2340 K less than that of the VJFET. This variation is due to the internal electric field of the LJFET which contains a region of low electric field below 0.5 MV/cm where the VJFET has a peak of 1.5 MV/cm. Combined with the knowledge from Chapter 3 that after impact the internal electric field of the devices studied can reach values 2.5 times that of the original pre-strike, the reduced SEB sensitivity of the LJFET can be understood.

Methods to further reduce the radiation response of the LJFET have been successful. The suppression of the internal electric field of the device through modification of the back gate - source separation resulted in devices with lower SEB sensitivity. Through the inclusion of an additional 4.2 μm of regrowth between the gate and source, the modified device could withstand harsher radiation conditions, due to the creation of an extended low electric field region below a magnitude of 0.5 MV/cm, 30% that of the original, for the entirety of the additional regrowth region. The modified LJFET at an industry standard drain - source derating is robust against all heavy ion deposited charge conditions studied, up to and including 300% that of a silver ion.

As the design of this bespoke structure allows it to be a like-for-like replacement to that of the device studied in Chapter 4, coupled with its reduced SEB sensitivity, the LJFET is seen as the device of choice for future aerospace applications.

6 Conclusions

The first objective of this research was to determine the suitability of materials key to the advancement of the future of the electrification of aircraft. Both Si and SiC were investigated due to their electrical characteristics. To avoid the potential influence 2D structures could have had on the studies of the material sensitivity, 1D SiC and Si p–i–n diodes were the devices of choice. Through the use of heavy ion simulations, both devices were subjected to an array of aerospace specific scenarios, and their responses were analysed. For deposited charges up to the equivalent of 300% that of a silver ion commonly used in SEB testing and reverse bias deratings of 99% of the breakdown voltage, the SiC device did not undergo SEB. Si on the other hand had a much higher SEB sensitivity, requiring much lower bias and deposited charge values to fail - a deposited charge equivalent to 0.2% that of a silver ion resulted in the failure of the device when a bias of 92% of the breakdown voltage was applied. It is noted that derating of the Si device was needed in order for it to be used for aerospace applications.

When analysing the transient response of the internal electric field after heavy ion impact for both SiC and Si for a bias derating equal to 70% of the breakdown and a deposited charge equivalent to 30% that of a silver ion, it was observed that the internal electric field could reach magnitudes 2.5 times that of the pre-strike. For Si with a peak pre-strike electric field of 0.18 MV/cm and a critical electric field 0.24 MV/cm, and SiC with a peak pre-strike electric field at 1.6 MV/cm with a critical electric field of 2.07 MV/cm, it can be understood as to why large scale avalanche multiplication and SEB could occur.

The importance of the internal electric field on device failure was highlighted through highly localised charge deposition where correlation between the magnitude of the pre-impact electric field and the magnitude of collected charge was observed for both Si and SiC. At a reverse bias derating of 99% of the breakdown voltage SiC underwent SEB for charge deposition values of 300% and 150% that of a silver ion. However, when this was reduced to an industry standard derating of 70% of the breakdown voltage, the magnitude of the peak electric field was reduced to 78% that of the original - no failures at these deposited charge values were observed.

The second main objective of this research was to understand the SEB sensitivity of a potentially unbeatable SiC JFET structure - with SiC having the favourable material response in comparison to Si, and the JFET with its known total dose ruggedness. However, with very limited published research on the topic, the response of the SiC JFET to radiation was the next focus.

It was found that unlike the SiC p–i–n structure, which displayed a near ideal response to cosmic ray impacts requiring no reduction in derating to resist the occurrence of SEB, the Vertical JFET, the 2D JFET of choice due to its similarities to a real-world sponsor owned structure, had the potential to fail at drain - source bias deratings as low as 40% that of breakdown. A derating which was far below the industry standard of 70%. This feature was due to the gate region of the device and the resulting influence it had on the internal electric field. For the 40% drain - source bias derating peak pre-strike internal electric field magnitudes of 1.5 MV/cm at the gate - source junction were observed. With the knowledge that the post-impact internal electric field can rise to 2.5 times that of the pre-strike, it is now known as to why this bias derating resulted in failure when the device was subjected to a deposited charge equivalent to 300% that of a silver ion.

Methods to reduce the magnitude of the internal electric field were identified, the first being a bias technique. By lowering the original gate - source bias of -60 V to -40 V, for a drain - source bias derating of 40%, the peak internal electric field was reduced by 33% - from 1.5 MV/cm to 1.0 MV/cm. When subjected to a deposited charge of 300% that of a silver ion the lower gate - source bias condition did not result in a potential shoot-through failure of the device, whereas, the original -60 V condition did. A trade-off of this method is the restriction in the maximum possible drain - source bias being limited to a derating of 70% when the lower gate - source bias is selected for use.

An alternative method to the biasing technique is a radiation hardening strategy in the form of an increase in the VJFET gate - source separation, this results in a reduction to the magnitude of the gate - source internal electric field. The modified structure when subjected to an aerospace specific scenario of a drain - source bias derating of 40% of the breakdown with a deposited charge equivalent to 300% that of a silver ion, had an electric field reduction of 64%, which resulted in a 99% reduction

in peak drain - source current density in comparison to that of the original structure. Additional benefits of the increased gate - source separation device include the ability to mitigate short channel effects, an increase in breakdown voltage and a reduction in threshold voltage.

The alteration of the SEB sensitivity of the VJFET is limited to the techniques discussed due to the process of device fabrication. However, the third main objective of this research was to understand the SEB sensitivity of a bespoke JFET, designed specifically to be robust against radiation. The SiC LJFET was investigated.

The structure of the LJFET incorporated both a vertical and a lateral channel and provided an extra element of current control in comparison to the VJFET to counteract the SEB generated currents. When subjected to the same aerospace specific scenario as the VJFET, 40% drain - source derating and deposited charge equivalent to 300% that of a silver ion, the LJFET did not undergo SEB. Under this scenario the peak temperature of the LJFET was 322 K, 2340 K less than that of the VJFET under the same conditions. This was due to the nature of the LJFET internal electric field. The LJFET contains a region of low electric field below 0.5 MV/cm whereas the VJFET at this point has a peak of 1.5 MV/cm. Due to the heavy ion impacts in this work penetrating only the top 6.25 μm of the device, this feature of the LJFET is crucial in terms of its SEB sensitivity.

Methods to reduced the radiation response of the LJFET further have been successful. Through suppression of the internal electric field of the device via modification of the back gate - source separation devices with lower SEB sensitivity were created. Through the inclusion of an additional 4.2 μm of regrowth between the gate and source, the modified device could withstand harsher radiation conditions, due to the creation of an extended low electric field region below a magnitude of 0.5 MV/cm, 30% that of the original, for the entirety of the additional regrowth region. The modified LJFET at an industry standard drain - source derating is robust against all heavy ion deposited charge conditions studied, up to and including 300% that of a silver ion commonly used in SEB testing.

As the design of this bespoke structure allows it to be a like-for-like replacement to that of the device studied in Chapter 4, coupled with its reduced SEB sensitivity, the LJFET is seen as the device of choice for future aerospace applications.

6.1 Future Work

With the global need to achieve carbon free flight by 2040 the findings of this research are of paramount importance. Additionally, flying taxis and personal air mobility could be a possibility by as early as 2025 if legislation permits, however, the ownership, running and certification of these vehicles will all rely on achieving higher levels of reliability then would currently be deemed possible. By using the techniques outlined in this work, a significant reduction in the inevitable failure rates of current SiC power devices would be realised, in turn, providing major commercial and safety advantages. Potential steps could be taken to apply this work and further its impact - the first stage is through data validation.

Two methods that are used for the determination of SEEs in power devices are heavy ion testing and pulsed laser testing. Heavy ion testing requires the use of an ion beam facility in order to perform the required analysis. The associated travel and equipment use costs make this method less feasible than pulsed laser testing. Pulsed laser testing can be performed with relative low cost in the lab with results that have been shown to agree with those produced by the heavy ion testing method [116]. Benefits of using the pulsed laser technique include the combined features of the lack of exponential attenuation of the optical pulse, facilitating carrier injection throughout the device and the quadratic dependence on laser pulse intensity, highly localized to the high intensity region near the focus of the beam - allowing charge injection at any depth of the device. This technique will probe the high e-field regions within the SiC device.

An alternative method of validation offers an added level of realism to the data through cosmic ray equivalent irradiation tests - by observing SEB sensitivity of devices in real world radiation conditions via high-altitude testing at the likes of the Jungfraujoch Research Station in Switzerland. At 12000 ft above sea level, this facility allows for the analysis of device performance in conditions nearing those of flight.

Manufacture of the radiation hardened devices outlined in Chapters 4 and 5 of this work will enable comparative testing to be performed against the original baseline devices. Further, similar tests to these radiation hardened devices as were performed on the originals in this work will allow for validation of these modifications. Once

these validations have been made, the creation of a SEB predictive simulation model could be performed, allowing for the identification of device SEB sensitivity during the device design stages. Further, through the use of this model, bespoke SEB robust devices can be conceptualized prior to manufacture.

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