Graphene Hall Sensors for Harsh Environment Current Sensing

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For Agnes and Clarence

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Abstract

Development of electronic devices which are capable of operating in harsh environments is a key enabler in the aerospace industry's move towards the More Electric Aircraft (MEA). The superlative material and electronic properties of graphene have generated significant interest in the development of next generation electronic devices. The use of graphene for development of highly sensitive graphene Hall effect sensors for use in power electronics modules is investigated, however it is found that conventional lithographic processing contaminates the surface of the graphene film often resulting in degradation of these properties.

A novel approach to fabricating high yield, reproducible graphene devices through the use of a Cu sacrificial layer is described. The use of such a sacrificial layer is studied and compared to conventional lithographic processing (no sacrificial layer), fabrication with an Al sacrificial layer (a method commonly used by graphene manufacturers) and commercial graphene sensors fabricated by the manufacturer of the CVD graphene films used in this study. Surface analysis in the form of Atomic Force Microscopy (AFM) and Raman spectroscopy is utilised, showing that graphene devices fabricated using a Cu sacrificial layer significantly reduces defect density over that of devices fabricated using both no sacrificial layer and Al sacrificial layer suggesting a reduction in surface doping of 60 % over devices fabricated with no sacrificial layer. Height profiles of AFM images taken across devices additionally exhibit reduced surface roughness (8.8±0.20 nm) in comparison to the average RMS surface roughness of 16±0.60 nm and 17±0.40 nm observed across devices fabricated using no sacrificial layer and Al sacrificial layer respectively. Electrical characteristics additionally show that the use of a Cu sacrificial layer not only offers improved device sensitivity, carrier mobility and reduced carrier

density but device yield is increased from 12 % to 82 % with variability in characteristics reduced from 40 % to 10 %. The graphene sensors developed using a Cu sacrificial layer are further optimised through external biasing in order to shift the Fermi level of the graphene towards the charge neutrality point, resulting in an increase in current related sensitivity of 165±16.5 V/AT observed in un-gated devices to 972±19.0 V/AT at the Dirac point.

Both high temperature and AC characteristics of devices are presented in order to examine the suitability of the graphene sensors for the desired application. Device characteristics taken up to 473 K are shown to exhibit a gaussian trend with temperature, largely attributed to evaporation of moisture absorbed to the surface either during processing or device storage. External gate biasing to reduce this effect is demonstrated with a reduction in the thermal coefficient of sensitivity from $4.5\pm0.18\times10^3$ ppm/K to $0.50\pm0.025\times10^3$ ppm/K observed when $V_G > V_{DIRAC}$. Devices still however exhibit a small gaussian trend with temperature. Vacuum annealing of devices show that this gaussian trend can be removed with characteristics post anneal exhibiting a linear trend with temperature and a significantly reduced thermal coefficient of just $0.27\pm0.014\times10^3$ ppm/K. It is summarised that in order to successfully implement devices with a linear temperature dependance and reduced thermal coefficient, appropriate packaging needs to be developed in order to protect the surface of the graphene film post anneal. AC characteristics up to 250 kHz are analysed with devices having an observed cut off frequency of 200 kHz. This cut off is thought to be an inherent limitation of the test setup however this bandwidth is still a significant increase on the 120 kHz limit observed in commercial semiconducting Hall sensors.

Finally, the analysis of SiC JFETs is presented and utilised to develop a representative LTSpice model. The JFET SPICE modelling is shown with the simulated output characteristics shown to be within 9.0 % of those extracted from functional devices, comparable to the variability seen in characteristics of manufactured devices ($\sim$ 10 %). LTSpice modelling is used to develop both the input and output circuitry that forms the final Hall sensor system made up of the input current bias, the PWM signal of which the Hall sensor will detect, buffering and differential amplification of the output signal and finally level shifting and filtering.

Statement of Copyright

Contents

List of Publications

1. **A.Peters**, S.Turvey, A.B.Horsfall, "High temperature graphene sensors for harsh environment current sensing," *Proceedings of IEEE Sensors Conference*, Montreal, p. 1-4, (2019).

2. M.I.Idris, M.H.Weng, **A.Peters**, R.J.Siddall, N.J.Townsend, N.G.Wright, A.B.Horsfall, "Positive flatband voltage shift in phosphorus doped SiO_2/N-type 4H-SiC MOS capacitors under high field electron injection," *Journal of Physics D: Applied Physics*, vol. 52, (2019).

3. H.K.Chan, N.G.Wood, K.V.Vassilevski, N.G.Wright, **A.Peters**, A.B.Horsfall, "Silicon carbide based instrumentation amplifiers for extreme applications," *Proceedings of IEEE Sensors Conference*, Bushan, p. 5-8, (2015).

4. **A.Peters**, J.P.E.Gausden, T.Hallam, I.Amit, A.B.Horsfall, "Enhancing the yield of high performance graphene devices through the use of a Cu sacrificial layer", (In progress).

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List of Abbreviations

AC	Alternating Current
AFM	Atomic Force Microscopy
AMR	Anisotropic Magnetoresistance
APS	Ammonium Persulphate
APU	Auxiliary Power Unit
BE	Binding Energy
BHF	Buffered Oxide
BJT	Bipolar Junction Transistor
CMRR	Common Mode Rejection Ratio
CVD	Chemical Vapour Deposition
DC	Direct Current
DOS	Density of States
ECS	Environmental Control System
ETM	Emerging Technologies and Materials
FET	Field Effect Transistor
FWHM	Full Width Half Maximum
GFET	Graphene Field Effect Transistor

GHS	Graphene Hall Sensor
GMR	Giant Magnetoresistance
ICAO	International Civil Aviation Organisation
JFET	Junction Field Effect Transistor
LPF	Low Pass Filter
MEA	More Electric Aircraft
MOS	Metal Oxide Semiconductor
PMMA	PolyMethylMethAcrylate
PWM	Pulse Width Modulated
RAT	Ram Air Turbine
RF	Radio Frequency
RIE	Reactive Ion Etching
RMS	Root Mean Square
RRCS	Rolls-Royce Control Systems
RTA	Rapid Thermal Annealing
SLG	Single Layer Graphene
SPICE	Simulation Programme with Integrated Circuit Emphasis
TLM	Transfer Length Method
TMAH	Tetramethylammonium Hydroxide
VDP	Van Der Pauw
WBG	Wide Band Gap
WF	Work Function
2DEG	2D Electron Gas

Chapter 1

Introduction

Air passenger traffic has increased at an annual rate of 9.0 % since the 1960's [1], however with this increase in air traffic comes an increase in CO_2 emissions, accounting for 2.0 % of the world's CO_2 emissions today [2]. This is reflected in the data presented by the International Civil Aviation Organisation (ICAO) in Figure 1.1 which show both the historical and forecasted civil air passenger traffic growth from 1995 to 2040.

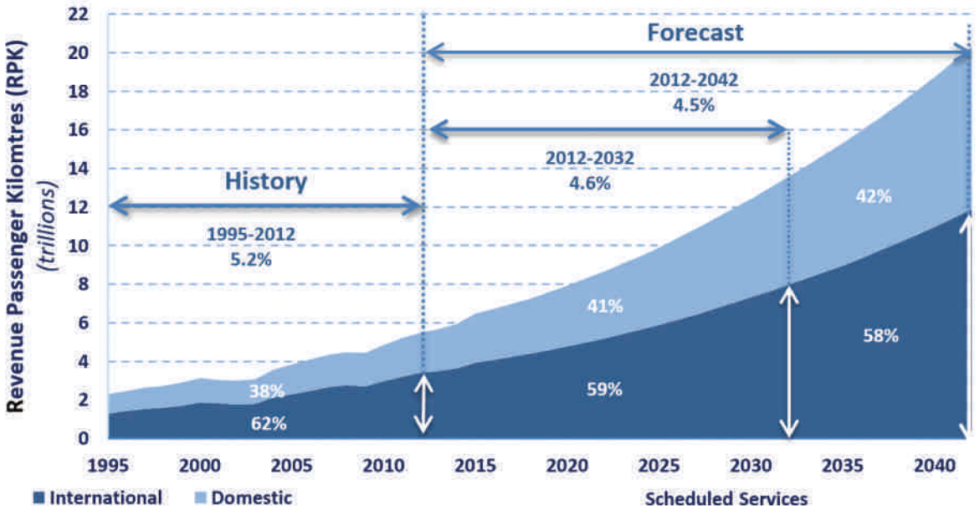


Figure 1.1: International Civil Aviation Organisation (ICAO) historical and forecasted civil air passenger traffic from 1995 to 2040. *Image taken from [3].*

As a result, both the aircraft operators and the aerospace industry are required to offer continuous improvements in safety, capability, and availability while reducing

costs, noise and CO_2 emissions. To meet these expectations, aerospace systems are undergoing a long-term transition from using mechanical, hydraulic and pneumatic power systems toward globally optimised electrical systems. It is noted that these forecasts were made pre COVID-19 and the civil aerospace industry may take up to five years to recover to the flying levels seen in early 2020. It has however accelerated the need for more efficient, electric aircraft with UK aviation committing to net zero carbon emissions by 2050 [4]. This premise forms the main motivation for the work carried out in this thesis.

1.1 Evolution of Aircraft Systems

Prior to modern day jet engines, all secondary power on an aircraft was generated manually through the use of a pulley system [5]. This type of aircraft was used throughout WWII, however the growth in size and weight beyond this point rendered them inefficient and paved the way toward aircraft with assisted secondary power systems. The idea of jet propulsion was first patented by René Lorin in 1913 however these systems were never manufactured due to the immaturity of the technology at the time. In 1930 Frank Whittle patented the first gas turbine jet engine but it wasn't until eleven years later until the engine completed its first successful flight [6].

Present day aircraft systems convert fuel into power, the majority of which is used for propulsion with the remaining power split between four secondary power systems [7]:

- **Pneumatic power -** This is obtained from high pressure air drawn from the engines compressors and is used to supply power to the Environmental Control System (ECS) and aircraft anti-icing systems. Pneumatic power can also be obtained from the Auxiliary Power Unit (APU) to provide starting of the main engines.
- **Hydraulic power -** This is generated by a hydraulic pump and used to drive actuation systems for flight control including landing gear deployment and braking.

- **Electrical power -** This is obtained from the main generator which is coupled to engines in the aircraft. This is used to provide cabin power when the aircraft is stationary, lighting and emergency power during flight.
- **Mechanical power -** This is taken from the main engine drive shafts and transferred via mechanical gearboxes from the engines to the hydraulic pumps.

The complexity of these systems has led to reduced efficiency over time and with the continued demand for lighter, more fuel efficient systems the focus has shifted towards all-electric systems. Advances in power electronics have made the realisation of all-electric systems more feasible in recent times. This would however require a shift towards all secondary power on an aircraft being run through electrical systems in a single step and as such a more gradual approach is preferred. This is often referred to as the More Electric Aircraft (MEA) wherein new electrical systems will be adopted individually with both hydraulic and pneumatic systems remaining as backup. As technology advances this may result in the complete removal of all non-electric systems from the aircraft however recent advancements into sustainable fuel options, such as that of hydrogen powered aircraft [8], may allow for a more hybrid solution.

1.2 More Electric Aircraft

The MEA is a hybrid solution towards the electrification of aircraft systems, replacing the three individually optimised systems previously described (electric, hydraulic and pneumatic) with one globally optimised electrical system. The schematic in Figure 1.2 offers a comparison between the conventional aircraft system and that of the proposed MEA. The Ram Air Turbine (RAT) and Environmental Control System (ECS) present in conventional aircraft have been removed in favour a new Auxiliary Power Unit (APU) design which encompasses electrically driven compressors, heater and cooler units to pressurise and condition the air in aircraft cabins. These systems are intended to drastically reduce the CO_2 and noise levels from that of conventional aircraft.

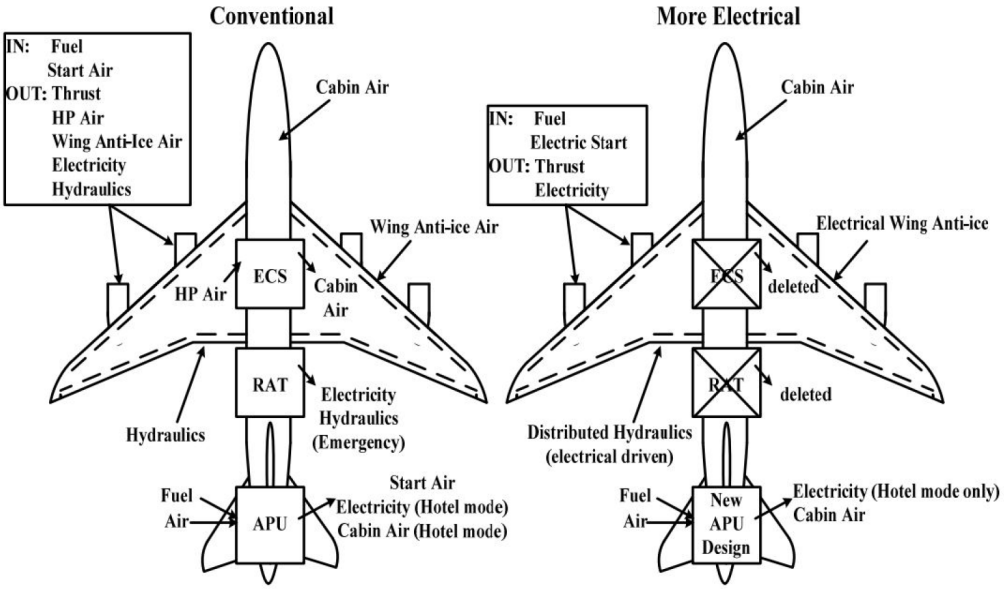


Figure 1.2: Conventional aircraft system (left) showing the location of the Ram Air Turbine (RAT), Environmental Control System (ECS) and Auxiliary Power Unit (APU) and More Electric Aircraft system (right) showing the removal of the RAT and ACS in favour of a new APU design. *Image taken from [9].*

In a conventional aircraft system the RAT provides the aircraft with hydraulic power and the ECS provides air supply and cabin pressurisation. Air supply at this stage typically comes from bleed air taken from a compressor stage in the engine. Removal of such systems may require electrical systems to operate in a more extreme environment than previously. Increased reliability is therefore critical with the move to the MEA and with this comes an inherent need for electronic devices which are capable of operating in harsher environments, particularly with the plan to remove the accessory gearbox from aircraft engines to improve efficiency. A magnetic field sensing solution is required for a number of applications, namely position and speed sensing in electrical machines as well as over current protection in power electronics modules. This thesis will focus on the development of such a sensor suitable for aerospace applications.

1.3 Challenges for High Temperature Electronic Systems

The development of high power semiconductor electronics capable of operating at temperatures beyond the 125°C limit placed on conventional Silicon electronics [10] without additional cooling systems would be advantageous to not only the aerospace industry but additionally that of the automotive and energy industry. Presently in aircraft systems when the environmental temperature is too high for the electronics used to control systems that reside in hotter areas of the engine they are either housed in a cooler area of the engine (typically around the side of the engine fan cowl) or require active cooling which is pumped from elsewhere in the aircraft [11]. This necessitates the use of additional overheads in the form of more connectors and long cables adding additional weight and complexity to the system. This additional wiring has the potential for increasing failure rates and in the past there have been aerospace tragedies linked to degradation of overhead wiring, most notably that of the Swissair Flight 111 in Nova Scotia in 1998 [12].

It is clear that given the drive to further increase the amount of electronics in aircraft systems, a more practical solution is required. Wide bandgap (WBG) semiconductors such as GaN and SiC are the leading contenders for such applications. The majority of research is currently aimed towards SiC based devices for operation in the high ambient temperature range, due to reduced defect density in the material in comparison to that of GaN. There remain practical challenges with the material, most notably the high defect density which can lead to high leakage currents which can be significant when developing high power devices leading to junction breakdown. Appropriate packaging solutions also present an additional limitation on the operating temperature of these devices, with the stress and oxidation of the materials used in packaging solutions restricting the temperature operation to < 600°C. Nevertheless there have been significant advancements in WBG semiconductor technologies in recent years with companies such as Wolfspeed offering SiC MOS solutions in the range of 3.3 kV, allowing for the development of higher power systems [13].

An additional contender for high temperature electronics in recent years is that of graphene, with the intrinsic carrier density shown to be an order of magnitude less sensitive to temperature than that of silicon [14]. This is critical with the main factor behind the degradation of conventional semiconducting materials is the dramatic increase in intrinsic carrier density with temperature. Whilst a significant amount of research has been in reported in the development of graphene devices, the technology remains relatively immature in terms of real world device applications. The majority of the research thus far has also pertained to the room temperature and cryogenic applications of the material however there remains significant scope for applications in higher temperature, harsh environments.

1.4 Thesis Outline

This thesis consists of 6 chapters, the first of which is this introduction. Chapter 2 includes a brief background review of present current sensing techniques and their limitations within harsh environment applications. The idea of utilising graphene based devices to overcome these limitations is presented alongside a brief overview of graphene's structural and electronic properties leading to the challenges in fabricating functional electronic devices. Finally, some common analysis methods used throughout the thesis are discussed, particularly Raman spectroscopy of graphene and electrical characterisation techniques.

Chapter 3 presents the challenges encountered in fabricating graphene devices using standard lithographic techniques. The use of a Cu sacrificial layer to reduce contamination during photolithography and increase the repeatability of results is analysed and compared to alternative metal sacrificial layers and devices fabricated using no sacrificial layers using techniques such as Raman and Atomic Force Microscopy (AFM). Electrical characteristics are also extracted and compared against commercial graphene Hall sensors as well as these fabrication techniques. Optimisation of these characteristics through external gate biasing is demonstrated with results also allowing for analysis of the Dirac point and how it is representative of the quality of the graphene surface. Finally the obstacles to successfully

package graphene devices most notably attempts to wire bond to the contacts are discussed.

Chapter 4 evaluates the performance and stability of graphene device characteristics at elevated temperature and at a bandwidth beyond the 120 kHz limit of present day commercial devices. The high temperature characteristics of graphene devices up to 200°C are presented with the influence of external gate biasing on the thermal stability of graphene devices also examined. In addition to the external biasing, the influence of the external environment on the high temperature performance is discussed with recommendations as to how this can be optimised in future device iterations. AC measurements of graphene devices up to 200 kHz are analysed with the limitations of the external measurement system on these characteristics also described.

The SiC based circuitry which are designed to integrate with both the input and output interface of the graphene hall sensors are shown in chapter 5. The characteristics of the SiC JFETs which form the basis of this circuitry are analysed and used to form a representative LTSpice model for use in circuit designs. Both the current source to be used at the sensor input and the optional output signal conditioning circuitry, namely SiC JFET based amplifiers, level shifters and filtering are simulated in LTSpice to examine the performance of a fully integrated Hall effect system using both un-gated sensors and those biased at the Dirac point.

Finally, chapter 6 offers a summary of the work presented in this thesis and identifies areas for additional development if this work were to be taken forward in the future.

Chapter 2

Literature Review

2.1 Introduction

The ability to monitor current flow is critical to a wide variety of electrical and electronic systems, each with unique performance requirements such as bandwidth, temperature stability, reliability and cost. One such application is that of power electronics, with monitoring of current flow required for both protection and closed loop current-mode control of converters. Many power electronics applications require devices to operate at high switching speeds ($>$ 100 kHz) and high temperature ($>$ 150°C). This precludes the use of many present day devices due to thermal instability and low bandwidth operation. The main scope of this project is to design sensors capable of monitoring current flow in SiC power electronic converters operating in an aerospace environment, requiring the devices to be stable at high temperature and sampling high switching speeds.

Specifically, SiC switch mode inverters operate with a fundamental frequency in the order of 10–60 kHz. In order for a sensor to accurately detect current in such a system it needs to be capable of operating at ten times this bandwidth (in the order of MHz) due to Nyquist theorem [15]. According to Nyquist theorem in order to adequately reproduce a signal it should be sampled at a rate that is at least two times the highest frequency, with the Nyquist frequency given by Equation 2.1:

$$f_s \geq 2f_c \tag{2.1}$$

where f_s is the Nyquist frequency in kHz and f_c the carrier frequency of the signal in kHz.

Whilst this stipulates that the sample frequency need only be two times the highest frequency in order to reproduce a signal, this typically only reproduces the fundamental frequency of the signal. A Pulse Width Modulated (PWM) signal is made up of several harmonics with the fifth harmonic being approximately ten times that of the fundamental frequency. As such in order to accurately reproduce the full signal, sensors must be capable of operating at a frequency of 100–600 kHz. Comparatively, current semiconducting devices available marketed at high frequency current sensing operate up to a bandwidth of 120 kHz [16]. This makes them unsuitable for the detection of the high frequency current signals which will be generated in the SiC power modules.

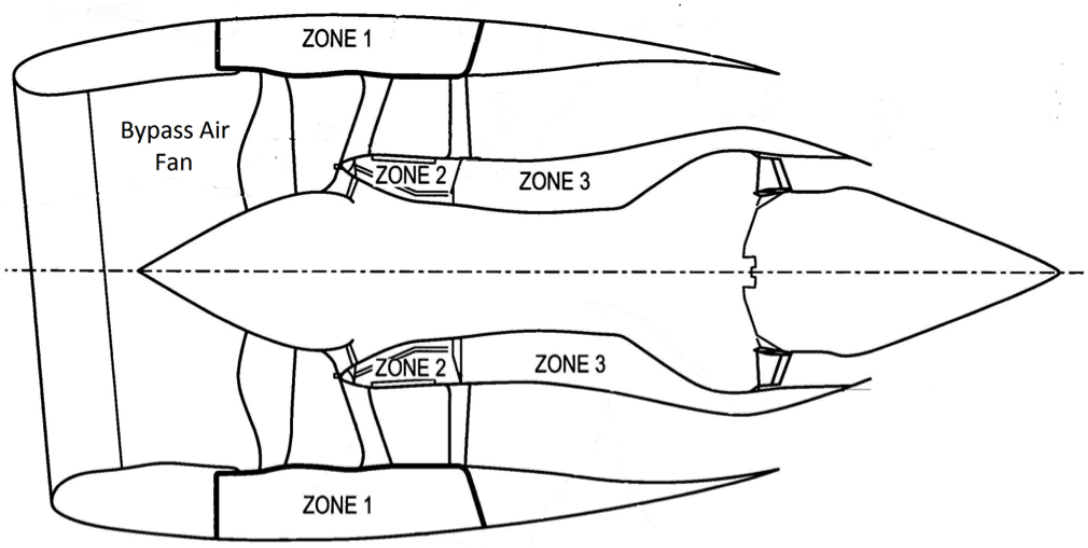


Figure 2.1: Schematic diagram showing the main zones where electronics are housed around the outside of a three shaft gas turbine engine; Zone 1(the area under the fan cowl doors), Zone 2 (the area under the core fairings) and Zone 3 (the area under the thrust reverser). *Image taken from [17].*

In addition to high frequency operation, environmental conditions also need to be considered. The sensors that are to be developed under this project are required for implementation in power module demonstrators where the operating environment

temperature ranges from 200-300°C [17]. Thermal stability is therefore critical to applications in this area, something which presently limits current sensing in this application. These environmental requirements stem from the location of the electronics within the typical three shaft gas turbine engine which is currently divided into zones as can be seen in Figure 2.1. There are three main zones which can be seen; Zone 1 (the area under the fan cowl doors), Zone 2 (the area under the core fairings) and Zone 3 (the area under the thrust reverser).

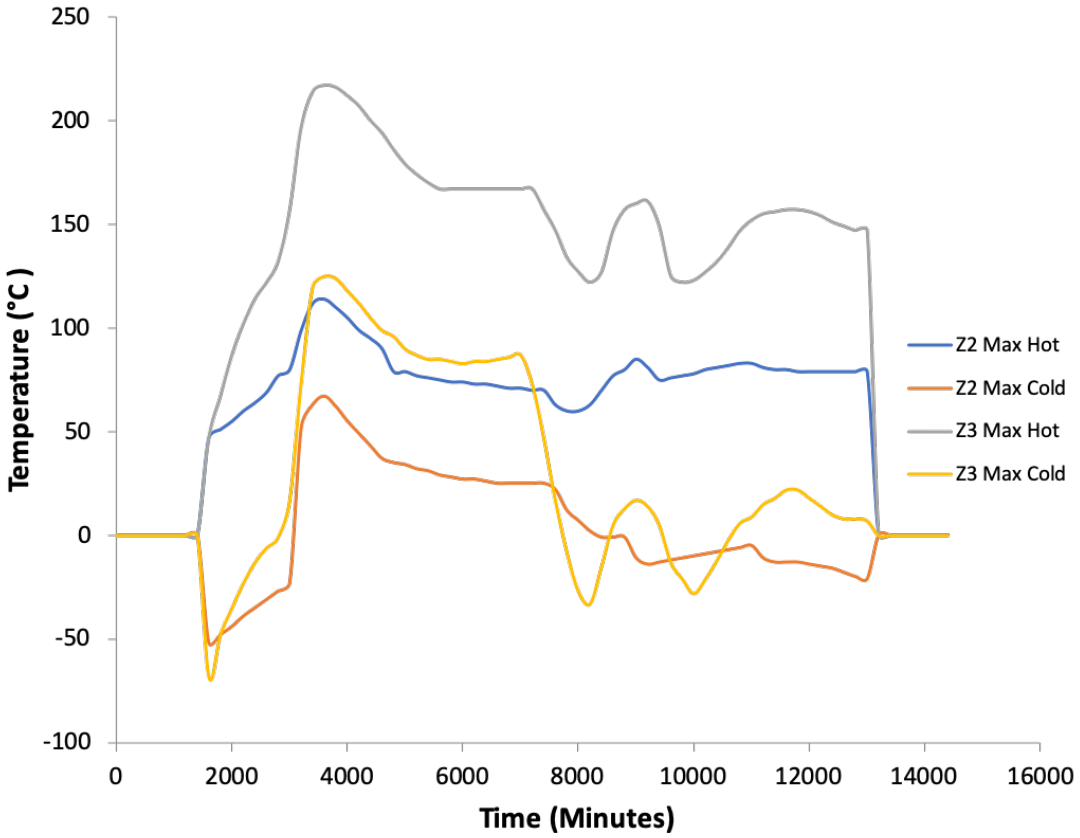


Figure 2.2: Measured temperatures in Zone 2 and Zone 3 of a Trent 700 test flight over time. *Image taken from [17].*

Presently, the electronics in an aircraft engine are located in Zone 1 where access is easy and it is isolated from the high temperatures generated during the combustion process in the core of the engine. The temperature range in this region is relatively benign allowing for the use of conventional Si electronics. This area however causes aerodynamic drag and subsequently reduces efficiency. As the aerospace industry move towards more efficient and environmentally friendly aircraft this region is to be slimmed down, requiring electronics to be moved into zones closer to the

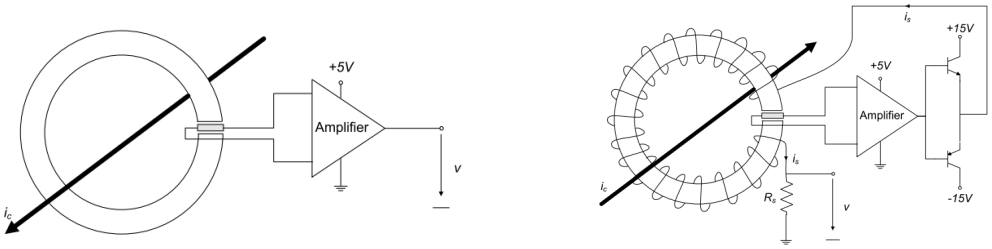
engine core (also known as core mounted electronics). Whilst previous studies have shown that the temperatures generated in Zone 2 are benign enough for electronics to be mounted in, it is not presently considered suitable due to the difficulty in accessing this area of the engine. Zone 3 is seen as the most accessible region for core mounted electronics however the maximum temperature ranges from 200-300°C. The measured temperatures in Zone 2 and Zone 3 from Trent 700 flight test data can be seen in Figure 2.2.

It is also important to consider that whilst the work presented in this thesis focuses on Hall sensors for use in power electronic converters there also exists applications for position and speed control within electrical machines. This is particularly important with the move to MEA as a variety of applications exist where future engine designs will have electrical machines mounted close to the engine core where they will be subjected to higher operating temperatures as discussed in Chapter 1. These electrical machines require both sensors for positional and speed control and also integration of a drive system which will require development of higher temperature electronics. In order to provide a suitable solution to these issues it is important to first consider the limitations of present current sensing techniques under the environmental conditions discussed in this section.

2.2 Current Sensing Techniques

The most fundamental technique for current sensing is the application of Ohm's law in the form of shunt resistors, with the voltage drop across the resistor being directly proportional to the flow of current. A significant drawback of this type of current sensing is that the shunt resistor is electrically connected between the measured current and sense circuit leading to high power losses of the order of I^2R (where I is the current flow in Amps and R the resistance in Ohms). Alternatively, there exists a group of current sensors based on Faraday's law of induction which allow for electrical isolation between the measured current and the output signal, namely Rogowski coils and current transformers [18]. The Rogowski coil is essentially a toroid of material which is placed around a conductor - the AC field

that is produced by the current induces a voltage in the coil which is proportional to the rate of change of the current [19]. These sensors are therefore unable to detect currents that generate static electric fields although it is possible to place the coil in a system with an open-loop magnetic field sensor to provide information on DC currents [20]. Finally, the most common group of current sensors, known as magnetic field sensors which have the ability to detect both static and dynamic magnetic fields, making them the most attractive prospect for the purpose of this study.



(a) **(b)**

Figure 2.3: Schematic representation of a magnetic field sensor in a) Open-loop configuration of a magnetic field sensor, with the output voltage (V) being taken directly from the sensor output after amplification and b) Closed-loop configuration of a magnetic field sensor, utilising a secondary winding to compensate the flux to zero. The output of the magnetic field sensor is used as an error signal and the current through the secondary winding, I_s, is used to determine the magnitude of the current through the conductor (I_c). *Image taken from [21].*

Magnetic field sensors commonly come in two different configurations; closed-loop and open-loop. Closed-loop configuration is typically preferred due to higher accuracy and sensitivity [21], with thermal drift also being significantly lower than sensors connected in open-loop configuration [22]. Figures 2.3a and 2.3b show example schematics of a magnetic sensor connected in open-loop and closed-loop configuration respectively. In closed-loop technology, the output is used to correct any error in the system arising from magnetisation losses. This is achieved by feeding back the output signal to a comparison via the sensor with a reference point. Any error between the output and reference is used by the control software to change the system input to correct for this error. This can sometimes be used to reduce any thermal drift present in the system and increase the linearity of the

output. The most commonly used types of magnetic field sensors are anisotropic magnetoresistance (AMR), giant magnetoresistance (GMR) and Hall effect sensors. Both AMR and GMR utilise structures wherein the resistance varies as a function of applied magnetic field, however they suffer from high thermal drift and non-linearity which requires compensation often through the use of a Wheatstone bridge [23]. These devices are also highly sensitive to external magnetic fields and exhibit significant hysteresis behaviour. This thesis will focus solely on the development of Hall effect sensors due to the low power dissipation and ability to measure over a higher current range [21, 24].

2.2.1 Hall Sensors

Hall sensors are electrically isolated devices that can be used to detect magnetic fields. They can additionally be used as current sensors through field detection by inferring the current flow. The Hall element itself typically consists of a thin sheet of conductive material, which when placed in a magnetic field, induces a voltage perpendicular to both the magnetic field and the direction of current flow. When a perpendicular magnetic field is present, a Lorentz force is exerted on the electrons. This disturbs the current distribution which results in a potential difference, known as the Hall voltage, across the output. A schematic of a typical Hall element is shown in Figure 2.4.

The Hall voltage generated at the output can be described by Equation 2.2

$$V_H = \frac{BI}{net} \tag{2.2}$$

where B is the magnetic flux density in Tesla, I the current flow through the Hall element in Amps, n the bulk carrier density in cm^{-3}, e the electronic charge (1.6×10^{-19} C) and t the thickness of the Hall element in cm.

The current related sensitivity of Hall effect sensors is derived from Equation 2.2 and can be described as the ratio of the output voltage to the factor of the magnetic field and input current bias as in Equation 2.3. This term is also commonly referred to as the Hall coefficient which is denoted as R_H.

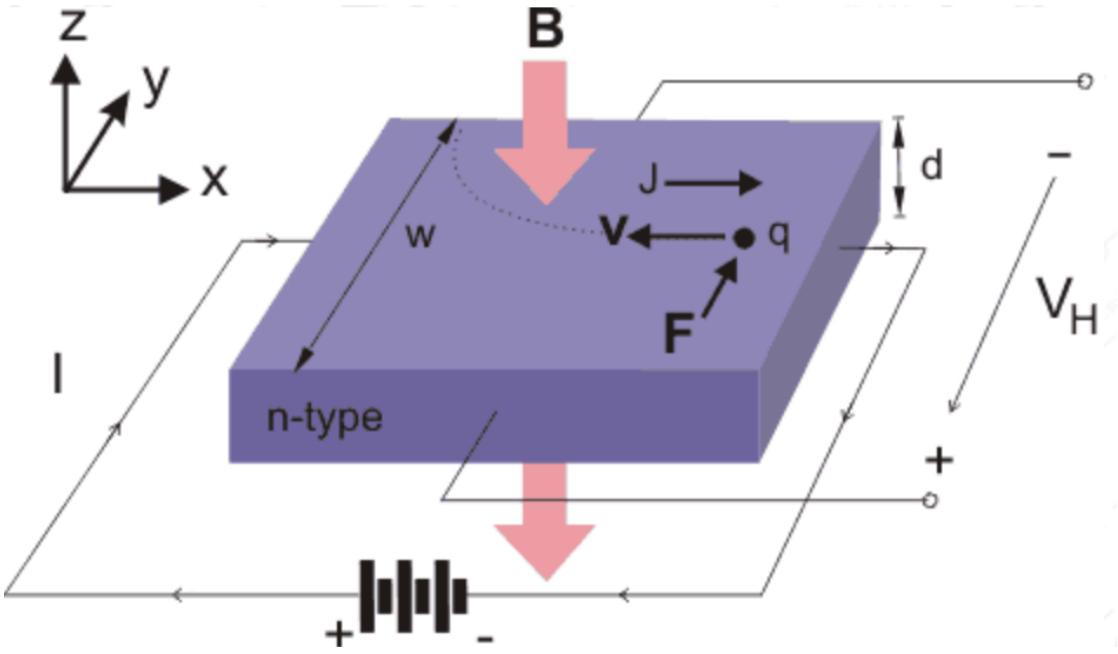


Figure 2.4: Schematic diagram of Hall effect through a conductive material showing direction of current and magnetic field. *Image taken from [25].*

$$S_I = \frac{V_H}{BI} = \frac{1}{ne} \tag{2.3}$$

The most commonly used semiconducting materials for Hall elements are InSb, InAs and GaAs due to their high carrier mobility and low bulk carrier density in comparison to alternate semiconductor materials such as Si. The low carrier density allows for increased resolution at the output according to Equation 2.2 whereas high carrier mobility allows for maximisation of current flow with low power dissipation and ultimately faster switching speeds - crucial in AC field applications [26]. The bandgap of these materials however leads to high thermal instability of material properties due to bandgap narrowing at high temperatures. The bandgap as a function of temperature can be described by Equation 2.4 [27]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{2.4}$$

where $E_g(0)$ is the bandgap at 0 K in eV, α and β are material dependant constants and T the temperature in Kelvin.

The intrinsic carrier density in a semiconductor is dependant on the bandgap of the material according to Equation 2.5.

$$n_i = \sqrt{N_C N_V}\exp\left(-\frac{E_g}{2kT}\right) \tag{2.5}$$

where N_C is the effective density of states in the conduction band in cm^{-3}, N_V the effective density of states in the valence band in cm^{-3} and k the Boltzmann's constant (1.38×10^{-23} JK^{-1}).

It can be seen from Equation 2.5 that $n_i \propto exp\left(-\frac{E_g}{2kT}\right)$. By combining Equations 2.4 and 2.5, the increase in temperature results in a larger exponent value. This means that a combination of the bandgap narrowing and thermal instability results in an increase in intrinsic carrier concentration and ultimately leads to a reduction in device sensitivity with increasing temperature. This thermal instability is even more dominant in materials such as InSb which exhibit a higher device sensitivity, meaning that ultimately in device terms there is a trade-off between highly sensitive devices and thermal drift. It would be pertinent to think that the use of a metallic conductor could provide a solution to this problem, however the Hall effect in metals is significantly lower than in semiconductors. This can be attributed to the fact that the concentration of conduction electrons in metals is around five orders of magnitude higher than in intrinsic semiconductors and as such the electrons in a metal have a significantly lower drift velocity [28]. Electrons with a low drift velocity experience a weaker Lorentz force and as such a lower Hall output is produced.

An alternative that is sometimes utilised to reduce this thermal drift and maximise sensitivity is to use two dimensional electron gas (2DEG) layers [29–31]. The principle of these devices is to confine the electrons in a 2D quantum well layer through the use of two parallel layers of wider bandgap semiconductors, called spacer layers. This spacer layer results in increased carrier mobility by separating the ionised donor atoms from the quantum well. As the thickness of this spacer layer controls the amount of charge trapped in the quantum well, this layer also determines the current sensitivity of the device - the thinner the spacer layer is, the lower the carrier concentration. GaAs/GaAlAs structures have yielded devices

with sensitivity of 1200 V/AT and a temperature coefficient of -1000 ppm/K [32]. Through the use of an InGaAs spacer layer, devices with sensitivity of 900 V/AT and a temperature coefficient of -433 ppm/K have been achieved [29]. Whilst these devices demonstrate a lower magnetic sensitivity, the temperature coefficient is significantly reduced, providing a more suitable device for applications where operation over a wide temperature range is required. However, these device structures are complex requiring the formation of III-V semiconductor heterojunctions [33, 34].

The surge of interest into 2D materials however provides a similar and perhaps more practical solution. Graphene in particular is of interest due to its high carrier mobility, ambipolar operation, low carrier density and atomically thin channel layer. The main origin of thermal instability in conventional Hall devices is fluctuations in intrinsic carrier density which dominates the device sensitivity. This often results in either additional circuitry being required to reduce the thermal instability or the use of devices with a larger active region to reduce the impact of the external temperature. The superlative electronic properties of graphene at temperatures that range between room and cryogenic temperatures have been the subject of a significant number of reports in the literature [35–38]. The low sheet carrier concentration, coupled with high carrier saturation velocity [39] that results from the linear dispersion relation and the thickness of a single atomic layer make graphene the leading candidate for the realisation of high sensitivity, high bandwidth Hall effect sensors.

In addition to the superlative material properties, the potential to directly grow graphene on to the surface of a SiC wafer facilitates the monolithic integration of the Hall device with SiC based signal conditioning circuitry, which is typically required due to the low-level output of Hall devices. The characteristics of ohmic contacts on graphene for temperatures above room temperature have been reported previously [40, 41], however the behaviour of graphene-based devices at high temperatures has not been reported widely. Studies have shown that due to the unique band structure, the intrinsic carrier concentration of graphene is significantly less sensitive to variations in temperature than that in technologically relevant semiconductors such as Si or GaAs [42]. Combining this temperature

invariance with the ability to monolithically integrate graphene with SiC makes graphene an attractive prospect for the realisation of highly sensitive, thermally stable Hall sensors. This is particularly crucial to this study due to the harsh environments that devices are required to operate in, with SiC being a well known material for the realisation of transistors for applications that require high temperature operation and high switching speeds [43, 44]. The switch mode inverters of which the Hall devices are designed to detect current flow through utilise SiC switching devices and as such the ability to fabricate graphene Hall devices on a SiC substrate is important for integration with these systems.

2.3 Graphene

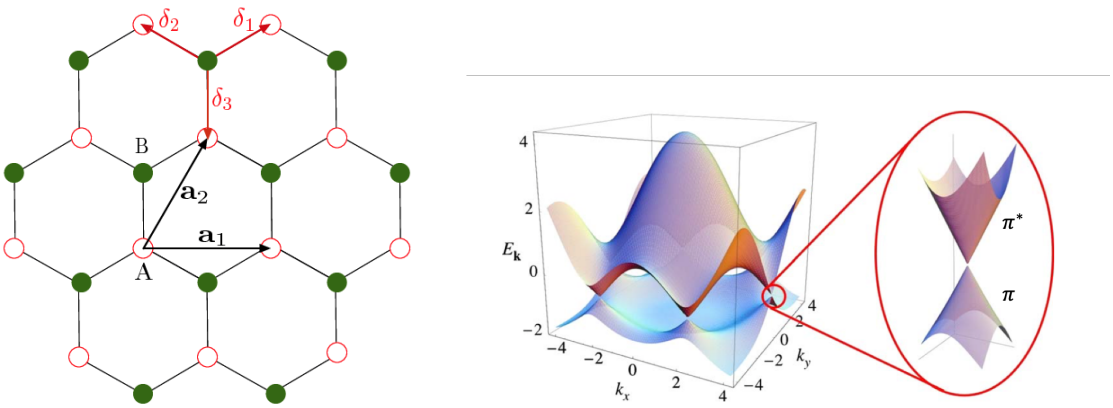
The seminal isolation of graphene in 2004 by Novoselov and Geim [38] created enormous research interest in the realisation of graphene devices. Much of this interest can be attributed to the reported exceptional electronic properties of graphene such as high carrier mobility (of up to 200,000 $cm^2V^{-1}s^{-1}$) [45], high thermal conductivity (5000 WmK^{-1}) [46] and low sheet carrier density (10^{11}-10^{13} cm^{-2}) [47]. Initially, it was thought the exceptionally high carrier mobility would allow for ultimately thin field effect transistors capable of operating at significantly higher switching speeds than present technology, however the zero bandgap of graphene and ambipolar behaviour of charge carriers has limited this. This however does not preclude its use in alternative device applications, particularly that of sensors, with graphene's unique combination of physical properties allowing it to be exploited across a variety of sensing applications such as optical sensors, chemical sensors and magnetic field sensors [48].

The majority of the experimental work reported in this thesis utilises monolayer graphene, also known as single layer graphene (SLG). SLG is a single layer of sp^2 bonded carbon atoms in which each carbon atom is covalently bonded to three nearest neighbouring atoms in the plane with a C-C distance of 0.142 nm to form a hexagonal lattice structure. A representation of this hexagonal lattice structure is shown in Figure 2.5a.

2.3.1 Electronic Structure

Many of the exceptional properties of graphene can be attributed to the aforementioned hexagonal lattice structure, in which two carbon atoms A and B form a single unit cell of the lattice structure. Each carbon atom has 4 valence electrons in the outer shell, 3 of which are tightly bonded to neighbouring carbon atoms by σ bonds. The remaining electron oscillates up and down perpendicular to the graphene plane and produces a p_x orbital (where x is the direction perpendicular to the plane of atoms), which gives rise to graphene's electronic properties. The p_x orbital overlaps with the p_x orbital of a neighbouring carbon atom to form

π-bonds. These π-bonds hybridise together to form delocalised electron π-bands - resulting in the π band structure shown in Figure 2.5b.



(a) **(b)**

Figure 2.5: Schematic diagrams of a) the hexagonal lattice structure of graphene, showing distance between carbon atoms [49] and b) the electronic band structure of graphene, showing the Dirac point where the conduction and valence bands meet (inset). *Image taken from [35].*

Figure 2.5b shows that the upper conduction (π^*) band and lower valence (π) band meet. This is commonly known as the Dirac point (E_D) due to the relativistic behaviour displayed by electrons at this point. For pristine, undoped graphene the Fermi level (E_F) is located at the Dirac point, where the valence and conduction bands touch with no bandgap opening - as can be seen in the band structure of single layer graphene in Figure 2.6. This means that graphene is effectively a zero-bandgap semiconductor and is often described as being a semi-metal [50]. At the Dirac point, charge carriers exhibit relativistic behaviour resulting in the high mobility values often exhibited in pristine graphene [45]. Electronic dispersion around the Dirac point is linear with the electronic structure of graphene being described by the relativistic Hamiltonian: $H = \nu_F \sigma \hbar k$ [51] where ν_F is the fermi velocity, σ a spinor-like wave function, $\hbar$ Planck's constant and k the electron wave vector.

However in practice, the Fermi level of graphene is often shifted away from the Dirac point due to doping of the graphene film. This Fermi level can however be shifted back towards the Dirac point by applying an external gate bias to the

graphene film - in device terms, this allows for control over the charge carrier density by applying an external gate bias. Relating this back to Hall sensors - operating the device at a bias point where the carrier density is lowest maximises the Hall coefficient as can be observed from Equation 2.3. This can be seen from the data in Figure 2.7, which show the Hall coefficient as a function of external gate bias. This corresponds to Equation 2.2 which stipulates that the output of a Hall sensor is inversely proportional to the charge carrier density. The data show that as the applied gate bias is increased, the Hall coefficient is increased to a maximum point and beyond this point the coefficient is reduced again.

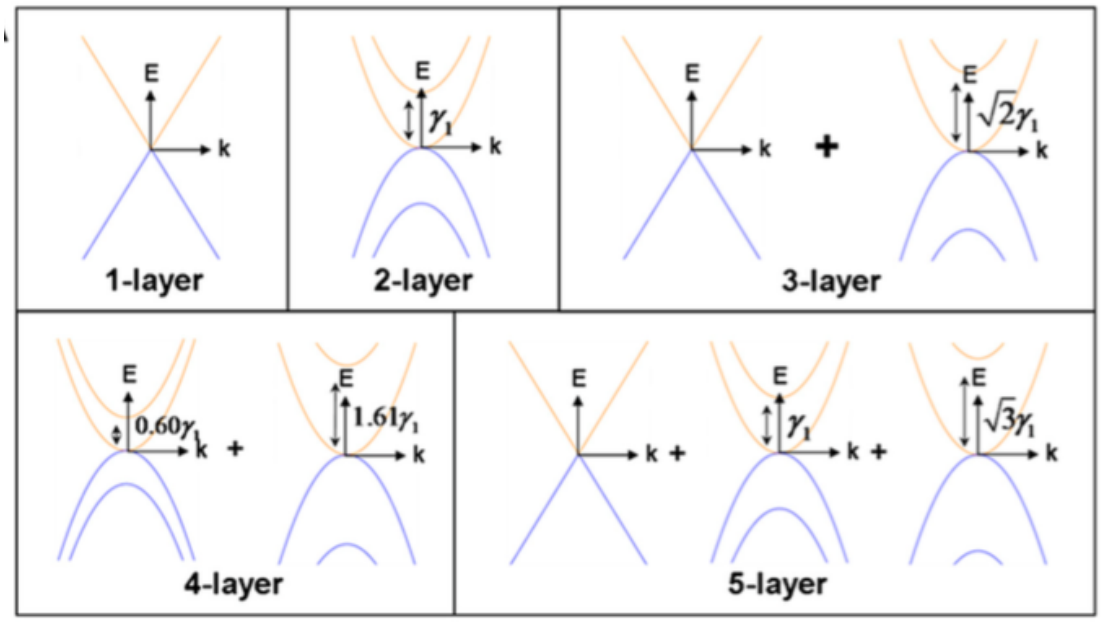


Figure 2.6: Evolution of graphene band structure structure from single layer to multi layer graphene (up to five layers) showing the energy spacing of the hyperbolic bands, γ, as the number of layers are increased. *Image taken from [52].*

Increasing the graphene thickness results in a dramatic shift in the electronic properties described above. The data in Figure 2.6 show that as the number of graphene layers increases, two π-bands are added to the existing band structure for each additional layer. As the thickness increases from bi-layer to few layer graphene the band structure is dependant on both the number of layers and the stacking sequence. The influence of E_D over the electronic properties is reduced as the number of layers is increased. This can be observed in the data shown in Figure 2.7 with a significantly smaller magnitude of Hall coefficient shown around the

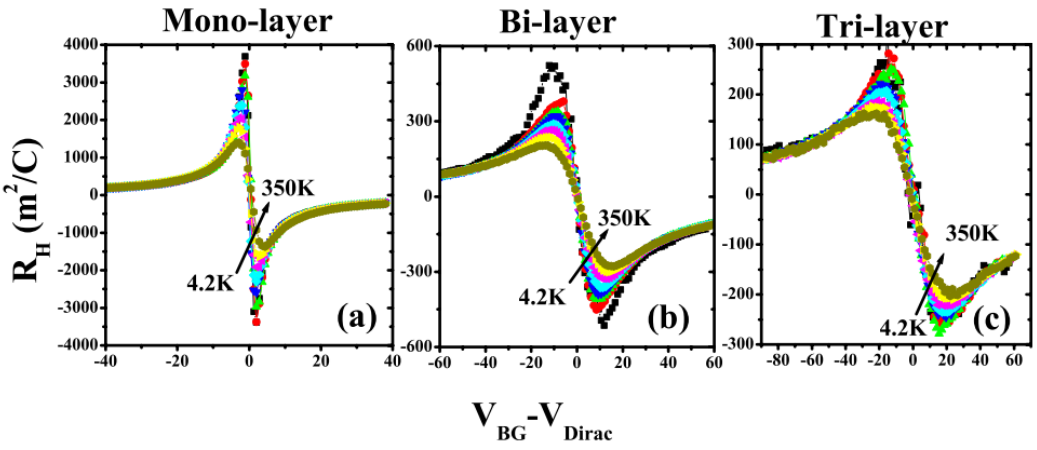


Figure 2.7: Hall coefficient as a function of gate bias in monolayer, bi-layer and tri-layer graphene. *Image taken from [53].*

Dirac point as the number of graphene layers is increased. The data show that the increase from monolayer to bi-layer graphene results in a reduction in Hall coefficient from 4000 m^2C^{-1} to approximately 500 m^2C^{-1} around the Dirac point and even further to just 300 m^2C^{-1} in tri-layer graphene demonstrating the importance of controllability of the graphene growth during synthesis.

2.3.2 Graphene Synthesis

Graphene synthesis is now relatively advanced, with techniques having matured significantly since it was first mechanically exfoliated in 2004 [38]. Chemical vapour deposition is the most popular of these methods for large scale production due to the low cost and high quality of the graphene film - comparatively shown in Figure 2.8 alongside alternative synthesis techniques. Epitaxially grown graphene also remains popular for electronics applications due to simpler processing methods and integration with existing SiC based devices [54, 55]. The majority of work in this thesis utilises CVD grown graphene transferred to a Si/SiO_2 substrate, additional work has been carried out with both CVD graphene transferred to a SiC substrate and graphene epitaxially grown on a SiC substrate to allow for both comparison of behaviours and further development of high temperature properties.

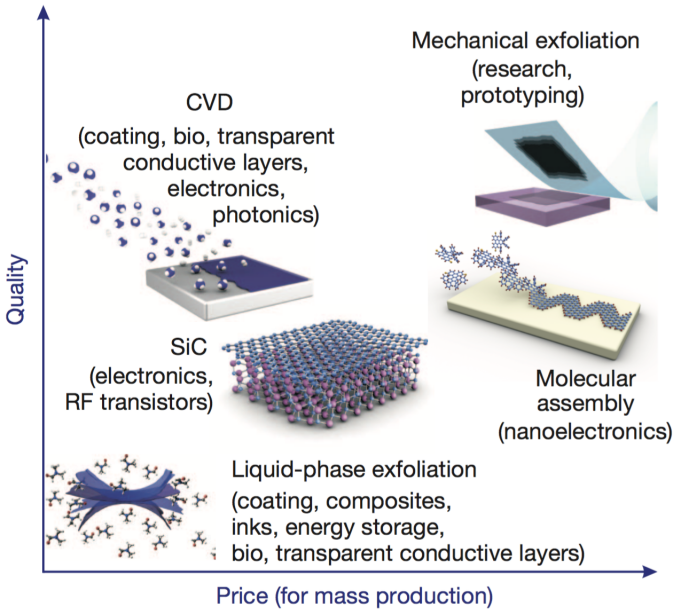


Figure 2.8: Development of graphene synthesis techniques and their suitability for mass production. *Image taken from [37].*

Mechanical Exfoliation

This conceptually simple technique consists of repeatedly peeling graphene layers from graphite crystals through the use of adhesive tape. Whilst this method has been largely responsible for the surge of graphene research, the flakes isolated from this technique are typically small in size (<10 μm) [38, 56], inconsistent and irregularly shaped. Figure 2.9 shows a digital image of a mechanically exfoliated graphene flake. It can be seen that whilst this flake is larger than average, there are folds and tears in the film and the shape of the film is irregular. As such, this synthesis method is not suitable for large yield applications - although the quality of exfoliated graphene flakes remains significantly better than other growth methods, with mobilities in excess of 200,000 $cm^2V^{-1}s^{-1}$ reported in suspended flakes [55] and up to 20,000 $cm^2V^{-1}s^{-1}$ in unsuspended graphene films [45]. The high quality and inexpensive nature of mechanically exfoliated graphene makes it a popular choice for research and prototype devices, however as this study will focus on industrial applications devices fabricated in this thesis will use graphene synthesised by alternative methods.

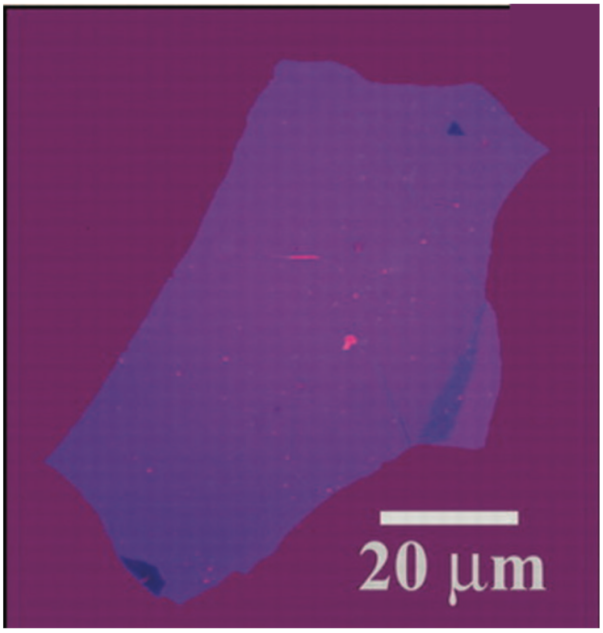


Figure 2.9: Digital image of mechanically exfoliated graphene. *Image taken from [38].*

Chemical Vapour Deposition

Chemical Vapour Deposition (CVD) growth of graphene is a technique which has seen significant developments in recent years, with graphene having been grown by CVD from carbon containing gases on a catalytic metal surface. Graphene growth has been demonstrated on a wide variety of metals including, Fe, Ru, Co, Rh, Ir, Ni, Pd, Pt, Cu and Au [54]. To date Cu and Ni have provided the most success, with growth on these substrates first being reported in 2008 and 2009 respectively [57,58]. For metals with high carbon solubility such as Ni, the carbon diffuses into the substrate as it is heated at a rate directly corresponding to the solubility. As the substrate is cooled, dissolved carbon segregates to the surface to form graphene sheets. This type of growth mechanism leads to highly inhomogeneous graphene layers, with very little control over thickness and uniformity.

CVD growth on a Cu surface is favoured as it is self mediating due to the low C solubility in Cu (<0.0001 % at 1000°C [59]), meaning graphene can only form by direct decomposition of the C containing gas on the Cu surface, with the growth limited to one monolayer.

The typical CVD growth process on a Cu foil involves annealing of the Cu foil in

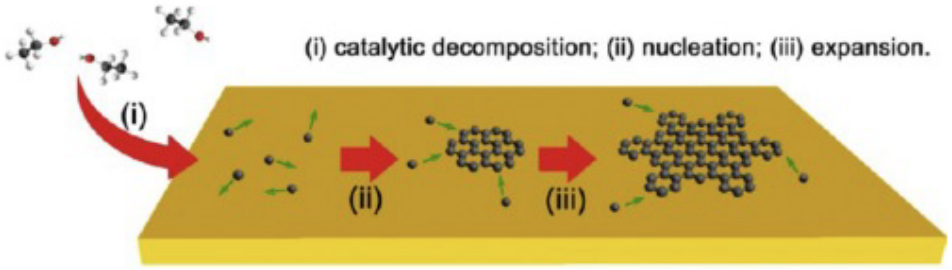


Figure 2.10: Schematic of CVD graphene growth on Cu foil. *Image taken from [60].*

an Ar/H_2 atmosphere to remove any impurities on the surface and increase the Cu grain size followed by introduction of a hydrocarbon source such as methane in to the gas flow and subsequent annealing at around 1000°C, which leads to the graphene formation. This growth method can be seen illustrated in Figure 2.10, showing that the carbon atoms nucleate after catalytic decomposition of hydrocarbons resulting in expansion of nuclei into large graphene domains. Mobilities of up to 100,000 $cm^2V^{-1}s^{-1}$ have been achieved on as grown CVD graphene films [61], however as this growth method is performed on a conductive substrate, transfer of the graphene film to an insulating substrate such as SiO_2 is required for electronic device applications. This in turn has an impact on the electronic properties of the graphene film. Transfer is typically performed using a PMMA resist which contaminates the graphene surface with resist residues, therefore further annealing is required to clean the graphene film once transferred [62]. The transfer process also leads to an increased likelihood of cracking or damage to the film meaning that as-transferred CVD has reduced quality over the as-grown film [63, 64].

Epitaxial Graphene

Graphitisation of hexagonal SiC was first reported in 1961 [65] during high temperature annealing. During annealing, the top layers of the SiC crystals undergo thermal decomposition, the Si atoms desorb and the remaining carbon atoms on the surface rearrange and re-band to form epitaxial graphene layers. Growth on the Si- face produces uniform coverage on a wafer scale whereas growth on the C- face exhibits faster growth kinetics making thickness control difficult. As such

epitaxial graphene is typically grown on the Si- face however this is not without its own challenges. An unwanted buffer layer forms at low temperature between the graphene layer and substrate, this buffer layer introduces further scattering sites often caused by the additional phonons present, resulting in decreasing carrier mobility [55]. A schematic diagram of this epitaxial graphene growth process is shown in Figure 2.11. It is possible to remove this buffer layer through the process of hydrogen intercalation between the buffer layer and the SiC substrate. This is achieved by heating in a hydrogen atmosphere at high temperatures resulting in the hydrogen atoms saturating the upper Silicon bonds which are bound to the buffer layer ultimately resulting in the conversion of the buffer layer to quasi-free standing (QFS) graphene [66].

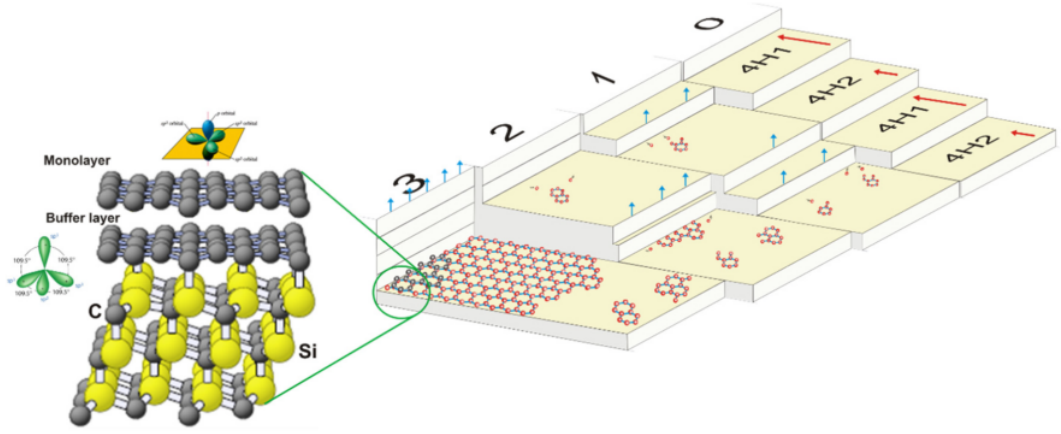


Figure 2.11: Schematic of epitaxial graphene growth via sublimation method on Si-face of SiC. *Image taken from [67].*

Epitaxial graphene on SiC is particularly attractive to this project as it can be grown directly on SiC substrates, removing the need for transfer to other insulating materials. Whilst the majority of the work carried out in this thesis utilises CVD grown graphene on a SiO_2/Si substrate for initial development of fabrication processes due to low cost of manufacturing and wide scale availability, the intention is to transfer this process to epitaxially grown graphene when implemented in real world applications. This will ultimately allow for the development of a monolithically integrated current sensing solution capable of operating in the required environmental conditions.

2.3.3 Hall Effect in Graphene

As previously stated the high carrier mobility, low carrier density and atomically thin layer make graphene Hall sensors (GHS) an attractive prospect. Besides the obvious advantages of maximising the sensitivity of devices and ultimately the magnitude of the output, minimising the need for additional output circuitry such as amplification there are additional advantages related to the 2D nature of the material. Most notable of these is the negligible planar Hall effect exhibited in GHS. Planar Hall effect is a phenomena that occurs when magnetic fields which are in line and not perpendicular to the plane of the sensors generates a signal at the sensor output [68]. This occurs due to the three dimensional nature of existing Hall effect sensors and results in a parasitic voltage, reducing the sensor accuracy. However this effect is negated in GHS due to the two dimensional, atomically thin layer. This gives a more reliable output signal and removes the need for circuitry to separate the true signal from the parasitic voltage.

GHS also exhibit extremely low noise [69] which combined with the high sensitivity allows for improved resolution over that of commercial Hall sensors. This means that GHS can detect magnetic fields in the region of <100 nT [70] in comparison to fields in the region of 10-100 μT [71] for commercial Hall sensors. The minimum detectable magnetic field for a Hall effect sensor can be described by Equation 2.6:

$$B_{Min} = \frac{\sqrt{4k_B T R_s \Delta f}}{R_H I} \tag{2.6}$$

where k_B is the Boltzmann constant (1.38×10^{-23} JK^{-1}), T the temperature in Kelvin, R_s the series resistance in $\Omega/\square$, Δf is the change in frequency in Hz, R_H the Hall coefficient in m^{2}C^{-1} and I the bias current in Amps.

It can be seen from this equation that the increased field resolution stems from the low noise exhibited in graphene, with the noise spectral density of thermal noise being described by Equation 2.7:

$$S_V = 4k_B T R \tag{2.7}$$

Additionally the high mobility of graphene devices allows for operation over an increased bandwidth over the 120 kHz currently imposed by commercial devices in addition to faster response times. Whilst it is clear that graphene has the potential to overcome many of the limitations exhibited in bulk semiconducting Hall sensors there remains numerous challenges with regards to fabricating graphene devices which will be discussed further in the following section.

2.4 Graphene Device Challenges

Whilst the seminal graphene paper of Novoseleov and Geim [38] created a lot of interest surrounding the potential of graphene to push the boundaries of existing semiconductor technology, there still remain a number of significant challenges to overcome for the technology to be commercially viable. Many of these roadblocks pertain to methods surrounding device fabrication, patterning and the production of high quality, scalable graphene processes. The lack of bandgap is also a considerable issue for some device types such as transistors, the majority of which require both p-type and n-type carriers in order to switch devices off. This precludes their use in applications where a high on/off ratio is required such as logic devices [72]. Studies into engineering a bandgap in graphene have been undertaken, most notably the method of substrate induced bandgap opening [73]. There are also a number of other methods such as the formation of graphene nanoribbons and biasing of bilayer graphene [74]. Many of these techniques are however still limited, with a significant amount of development required in order to be suitable for real-world applications. Nevertheless, successful graphene field-effect transistors (GFETs) have been demonstrated in the literature despite the low on/off ratio [75, 76]. Figure 2.12 shows the typical structure of a GFET designed to operate at high frequencies.

Rather fortuitously, whilst the zero bandgap of graphene limits its use a transistor, it significantly enhances its use as a sensor over alternative materials. Graphene has been demonstrated as a suitable material for use in magnetic sensing in particular, with high carrier mobility, atomically thin channel layer, low carrier con-

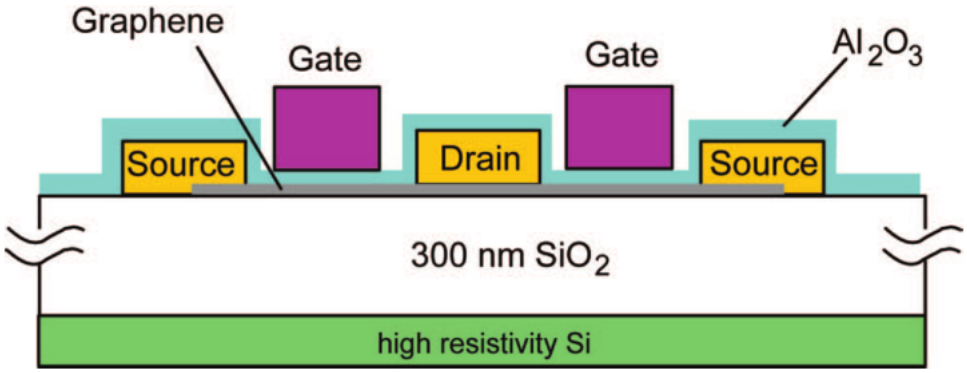


Figure 2.12: Schematic cross section of a graphene field-effect transistor designed for gigahertz frequency operation. *Image taken from [77].*

centration and the previously discussed weak temperature dependence which has hindered commercial Hall effect devices [22]. The atomically thin layer of the graphene channel means that the current related sensitivity is inversely proportional to sheet carrier density, according to Equation 2.8. The voltage related sensitivity in a graphene Hall effect device can be given by Equation 2.9.

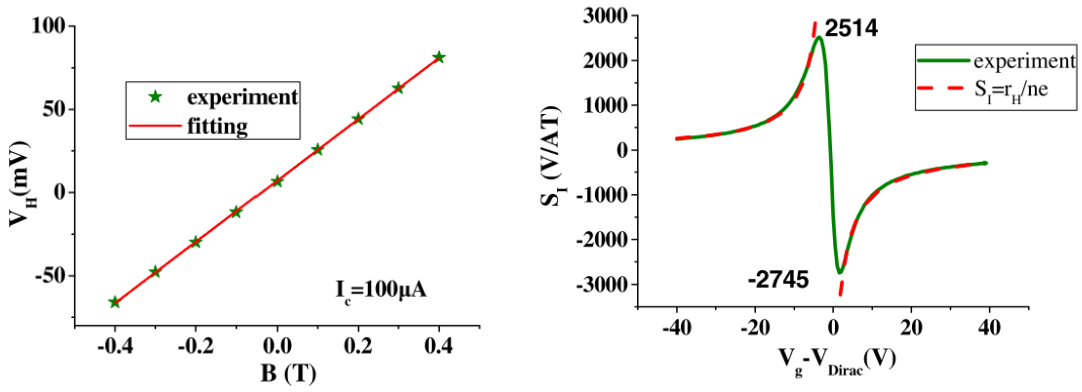
$$S_I = \frac{1}{n_{2D}e} = \frac{V_H}{BI} \tag{2.8}$$

where n_{2D} is sheet carrier density in cm^{-2}, e the electronic charge (1.6×10^{-19} C), V_H the Hall voltage in Volts, B the magnetic flux density in Tesla and I the current through the Hall sensor in Amps.

$$S_V = \frac{\mu W}{L} = \frac{V_H}{B} \tag{2.9}$$

where μ is carrier mobility in $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, W the width of the active channel layer in cm and L the length of the active channel layer in cm.

The data in Figure 2.13 show the variation in Hall sensitivity of a CVD graphene sensor fabricated on a back gated SiO_2 substrate reported by Chen *et al.* [78]. Figure 2.13a shows the output of devices without a gate bias applied, whereas Figure 2.13b shows the current related sensitivity of devices as a function of applied gate bias, with the Dirac point evident at a gate bias of approximately -5.0 V. It can be seen that these devices achieve a sensitivity of up to 2514 V/AT at the Dirac



(a) (b)

Figure 2.13: Output of a typical CVD graphene Hall element showing a) Hall voltage as a function of magnetic field for ungated devices and b) current related sensitivity as a function of gate bias for gated devices. *Image taken from [78].*

point, exceeding that achieved by commercially available InSb devices by 57 % ($\sim$ 1600 V/AT) [21] and even that of 2DEG devices reported in literature (500-1000 V/AT) [29, 33, 79]. In addition to the high current related sensitivity of the graphene film, the material also lends itself to applications in areas where present day devices are limited. Of particular interest in this study are the applications where high frequency operation is required (such as monitoring of current flow in power electronic converters that are subject to high switching speeds) and also where sensors are subjected to high temperatures (the typical temperature range in the desired engine zone is 200-300°C).

Despite the success with initial research in these areas there still remains a number of challenges in fabrication of reliable, reproducible graphene devices suitable for real world applications. The most prominent of these issues encountered in this study were both surface preparation and patterning of devices - this is due to the amount of solvents typically used in these processes. One popular method to reliably pattern graphene devices is that of electron-beam lithography. The process is similar to that of standard photo lithography however the use of an electron-beam to pattern the film requires a more sophisticated lithographic set up and as such makes scaling up difficult. There is also very low throughput due

to the time taken to complete the process [80]. The complexity of these issues are further discussed in the following sections.

2.4.1 Influence of Metal Contact and Substrate Choice on Material Properties

The sensitivity of graphene to the external environment means that any material with which it comes into contact has a deleterious impact on the electronic properties, including metal contacts and insulating substrate. Inevitably in order to achieve functional electronic devices both metal contacts and an insulating substrate are required and as such it is fundamental to understand the origin of this degradation in order to reduce the impact on the material properties and hence device performance. Initially considering metal contacts, it is important to understand the electrical characteristics of the metal-graphene interface. The energy band diagrams of metal-semiconductor, metal-metal and metal-graphene interfaces are shown in Figure 2.14.

When a metal comes into contact with a semiconductor there is a flow of charge from high energy states to low energy states, until the Fermi levels (E_F) are balanced on both sides of the junction under thermal equilibrium. This forms a Schottky barrier (ϕ_B=ϕ_M-χ) at the interface where ϕ_M is the work function of the metal and χ is the electron affinity of the semiconductor. Band-bending occurs due to the lower carrier density in the semiconductor, resulting in the formation of a depletion layer of width W_{dp}. In contrast, the metal-metal interface is shown to have no potential barrier although there remains a transfer in charge through the metal-metal interface to cancel out the difference in work functions, the small redistribution of the electron cloud screens this potential difference due to the large carrier density. This screening length is typically very small at just a fraction of a nm and can be expressed as λ=$[4\pi N(E_F)]^{-\frac{1}{2}}$ where $N(E_F)$ is the density of states (DOS) at the Fermi level, resulting in a sharp change in the vacuum level at the metal-metal interface [81] as can be seen in Figure 2.14b.

Considering the metal-graphene interface shown in Figure 2.14c, it is remarkably

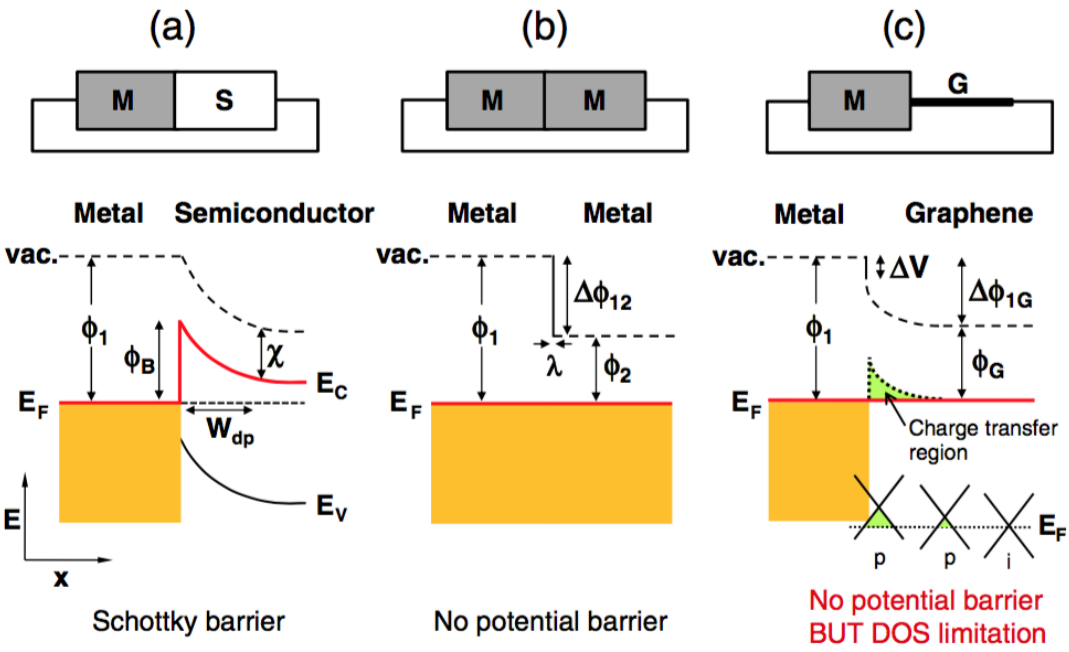


Figure 2.14: Energy band diagrams for a) metal-semiconductor interface b) metal-metal interface and c) metal-graphene interface. The location of the Fermi level (E_F), conduction bands (E_C), valence bands (E_V) are shown. Schottky barrier height (ϕ_B), depletion region width (W_{dp}) and electron affinity (χ) are also denoted in these diagrams. It can be seen that whilst the metal-graphene interface has no potential barrier it is limited by the density of states at the Fermi energy. *Image taken from [81].*

similar to that of the metal-metal interface largely due to the lack of bandgap in graphene. A small charge transfer at the metal-graphene interface occurs, which results in a significant shift in the position of E_F. This charge transfer decreases away from the interface. A dipole layer is formed at the interface as a result of this charge transfer, the potential difference of which is expressed as ΔV and is dependant on the strength of the metal-graphene interaction. Charge transfer alongside Pauli's repulsive interaction [82] cause metal contacts to dope the graphene, the magnitude and type of which is dependant on the metal work function in comparison to that of graphene. As such it is crucial to understand how specific metals interact with the graphene interface in order to determine the most suitable contact choice, taking into consideration both low contact resistance and reduced charge transfer doping.

The interaction of a metal contact with the graphene surface can be split into two

categories: physisorbed metals and chemisorbed metals [82, 83]. Physisorbtion refers to metals that are weakly bonded to the carbon atoms of the graphene, whereas chemisorbed metals are chemically bonded to the atoms in the graphene film. This strong bonding means that the probability of charge carriers crossing the metal-graphene interface is significantly higher for chemisorbed metals, however the magnitude and direction of doping is dependant on the difference between the metal and graphene work function. Adsorbtion of charge carriers results in a shifting of the Fermi energy: an upwards shift means that the graphene film has been doped with electrons from the metal contact, whereas a downwards shift indicates hole doping.

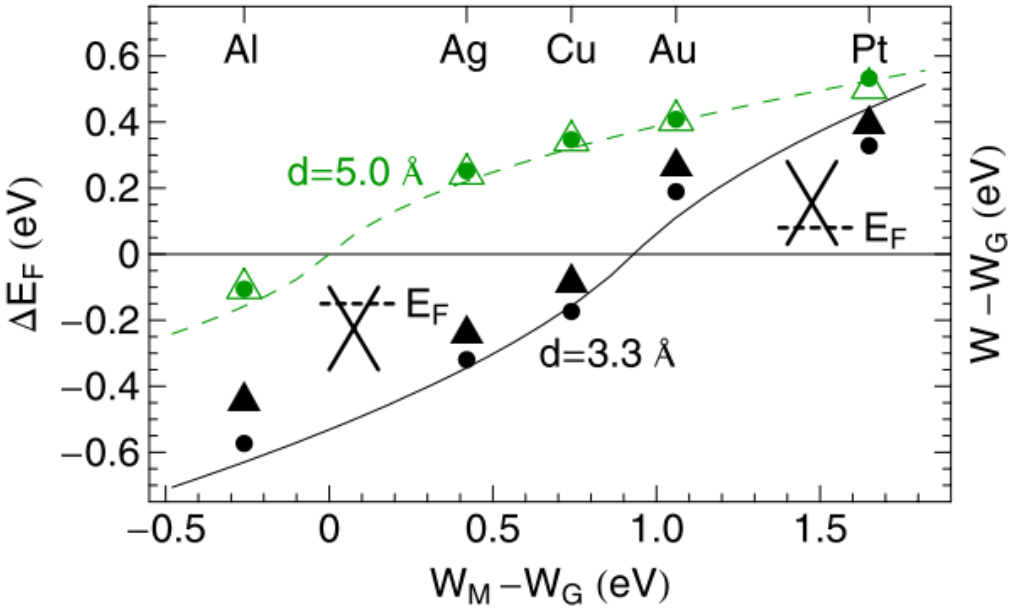


Figure 2.15: Shift in Fermi energy as a function of metal-graphene work function difference (dots) and change in graphene work function as a function of metal-graphene work function difference (triangles) for two different seperations, d, between the metal and graphene surface. *Image taken from [84].*

The shifts in Fermi levels for physisorbed metals Al, Ag, Cu, Au and Pt are shown in Figure 2.15 with Al, Ag and Cu shown to n-type dope the graphene whereas Au and Pt are p-type. Whilst these metals preserve the characteristic electronic structure of graphene, unlike chemisorbed metals such as Co, Ni and Pd, the Fermi level is still shifted away from the graphene Dirac point, resulting in either n-type or p-type doping. Many metallisation schemes however use a combination

of a chemisorbed metal to bond the metal contact to the graphene followed by a capping layer using a physisorbed metal. Practically there needs to be a trade-off between metal contacts that disturb the electronic structure of graphene the least and those that offer low contact resistance. As such it is pertinent to consider the study of contact resistance on graphene devices alongside these results.

Previous studies have found that despite the strong interaction of Ni with graphene, a strong charge transfer occurs at the Ni-graphene interface without causing a significant disturbance to graphene's electronic structure [85]. As Ni has a higher work function than graphene it causes the Fermi level to shift below the Dirac point and dopes the graphene film p-type, this in turn results in a considerable increase in the DOS at the graphene Fermi level which alongside the small contact separation results in a low contact resistance. Comparing this to contact resistance extracted for alternative metallisation schemes, as shown in Table 2.1, it can be seen that metals with a large work function difference between the metal and the graphene typically result in a lower contact resistance although this isn't the case for Pd and Pt. Observed contact resistance values however do not take into consideration other factors such as resist contamination at the interface which would contribute to the high contact resistance values seen for Pd and Pt in Table 2.1. In addition to the low contact resistance, Ni is also shown to have a low lattice mismatch of just 1.2 % and is in fact the closest matched interface to graphene of all the transition metals. As such 5 nm thick Ni contacts were used throughout this study with a 100 nm Au capping layer to prevent oxidation and enable probing for electrical characterisation.

In addition, the insulating substrate onto which the graphene is transferred can also dope the graphene film with the level of doping dependant on how strongly the substrate interacts with the graphene [86]. This is particularly prevalent when graphene is epitaxially grown on the Si- face of SiC, with the doping effects such that this method is commonly used to engineer a bandgap in graphene [73]. This is largely due to the interaction between the graphene and the substrate causing a breakdown of the A and B lattice sub-symmetry. This breakdown is caused by the formation of a buffer layer between the substrate and epitaxial layer which reduces the carrier mobility [87, 88]. As this buffer layer is only present when the material

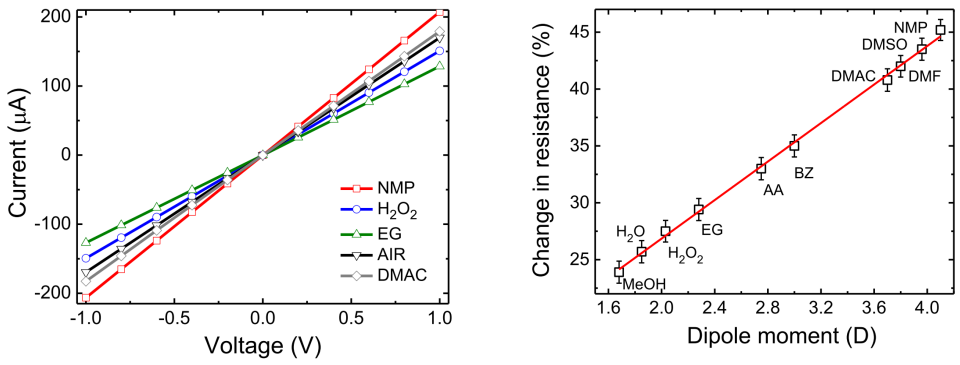
Table 2.1: Work function (WF), binding energy (B.E), Diffusion energy barrier (E_{Diff}), effective metal-graphene distance (d_{M-C}) and lattice mismatch of metals commonly use to contact graphene. *Image taken from [85].*

Contact metal	WF (eV)	B.E (eV)	E_{Diff} (eV)	d_{M-C} (Å)	Lattice mismatch (%)	R_C (kΩ.µm)
Al	4.28	0.97	0.11	3.65	N/A	N/A
Ti	4.33	1.70	0.59	2.18	3.7	12.0±0.1
Cr	4.50	0.18	0.006	2.36	3.3	4.1±0.52
Ni	5.35	1.51	0.22	2.11	1.2	0.22±0.1
Au	5.47	0.09	0.006	3.62	1.6	1.32±0.2
Pd	5.60	1.06	0.03	2.79	3.2	3.60±0.3
Pt	5.70	1.56	0.17	3.59	2.5	2.80±0.2

is grown on the Si-face the mobility of graphene grown on C-face is significantly higher. The thickness of graphene grown on C-face, as previously mentioned, is not controllable and as such it is not feasible for reproducible large scale graphene growth, meaning in order to improve the electronic properties of epitaxial graphene on SiC, other methods have to be employed. These include removal of the buffer layer through the use of hydrogen intercalation [89, 90] and transferral of CVD grown graphene to a SiC substrate.

2.4.2 Interaction with Organic Solvents

Graphene is particularly sensitive to environmental factors such as organic solvents, lithographic resists and ambient air, causing unintentional doping of the graphene film. These contaminants also introduce external scattering sites to the graphene surface which reduce carrier mobility and increase electron concentration through charge transfer doping. This sensitivity is particularly evident when examining studies into the use of graphene for chemical and gas sensing applications. Hill *et al.* explored the suitability of graphene for chemical sensing, stipulating that it offers the best surface to volume ratio of any material in that every atom in the graphene layer is exclusively a surface atom [48].



(a) **(b)**

Figure 2.16: Response of epitaxial chemiresistor sensor to analyte vapours showing a) change in current-voltage characteristics and b) change in resistance as a function of vapour dipole moment. *Image taken from [85].*

Nagareddy demonstrated the use of epitaxial graphene as a chemiresistor sensor. Chemiresistor sensors exhibit a change in electrical resistance when exposed to analyte vapours [85]. The devices in this case consist of an epitaxially grown graphene film in a van-der-pauw test structure which is then exposed to varying analyte vapours, the electrical properties are then extracted to see if any shift is observed. Figure 2.16 shows the response of these sensors when they are exposed to varying analyte vapours. Initially considering the current-voltage characteristics shown in Figure 2.16a, they exhibit an obvious shift in resistance when exposed to analyte vapours, this is also evident in Figure 2.16b where the resistance is shown to change dependant on the dipole moment of the vapour. This change is due to adsorption of the vapour to the graphene surface which can shift the intrinsic carrier density and lead to n-type or p-type doping of the film.

Whilst this surface adsorption is advantageous for chemical sensing applications it can be detrimental to the performance of electrical sensors such as the ones fabricated in this study. This presents a significant challenge when processing graphene devices, with the use of organic solvents present in many standard fabrication processes particularly lithographic patterning and surface cleaning. Thermal annealing has been used as an alternative to a standard solvent clean for the removal of organic contaminants. Studies have shown that resist residues can act as external scattering sites and thus degrade the transport properties of the

graphene film [91, 92]. This is particularly problematic in monolayer graphene as the atoms are all exposed directly to impurities [93]. Therefore achieving clean graphene surfaces is critical to the fabrication of graphene devices, particularly those to be used for sensing applications. The thermal effects on graphene devices however are not fully understood. Whilst annealing above 300°C in vacuum is widely accepted to eliminate resist residues on the graphene surface [94, 95] it simultaneously brings graphene into close contact with the insulating substrate and increases the electrostatic interaction. This leads to doping of the graphene film and degradation of electrical properties [96]. The effects of thermal annealing temperature on the Dirac point and key electrical properties can be seen from the data in Figure 2.17.

Prior to annealing a back gate voltage of 48 V is required to obtain Dirac point operation due to doping from both the substrate and PMMA used during processing. This Dirac point is shifted towards 0 V after annealing at 100°C and 200°C which could be interpreted as removal of adsorbants on the graphene surface. This correlates with the electron and hole mobilities both increasing with annealing temperature up until 200°C. Beyond 200°C the Dirac voltage is shown to shift away from 0 V, with decreasing mobility. At an annealing temperature of 300°C electrical properties are still significantly improved over characteristics before annealing however annealing at 400°C is shown to cause serious degradation of the carrier mobility linked to heavy doping of the graphene surface. Conversely, the AFM images shown in Figure 2.17c show that the cleanest graphene surfaces are achieved at annealing temperatures of 300°C and 400°C with the AFM profiles at these temperatures showing a smoother surface. It is evident from these results that optimal electrical performance does not necessarily correspond with the cleanest graphene surfaces. As thermal annealing can also lead to damage of the graphene film, it is therefore when fabricating devices in this study to reduce the contact with organic solvents and resist residues to allow for optimum device performance.

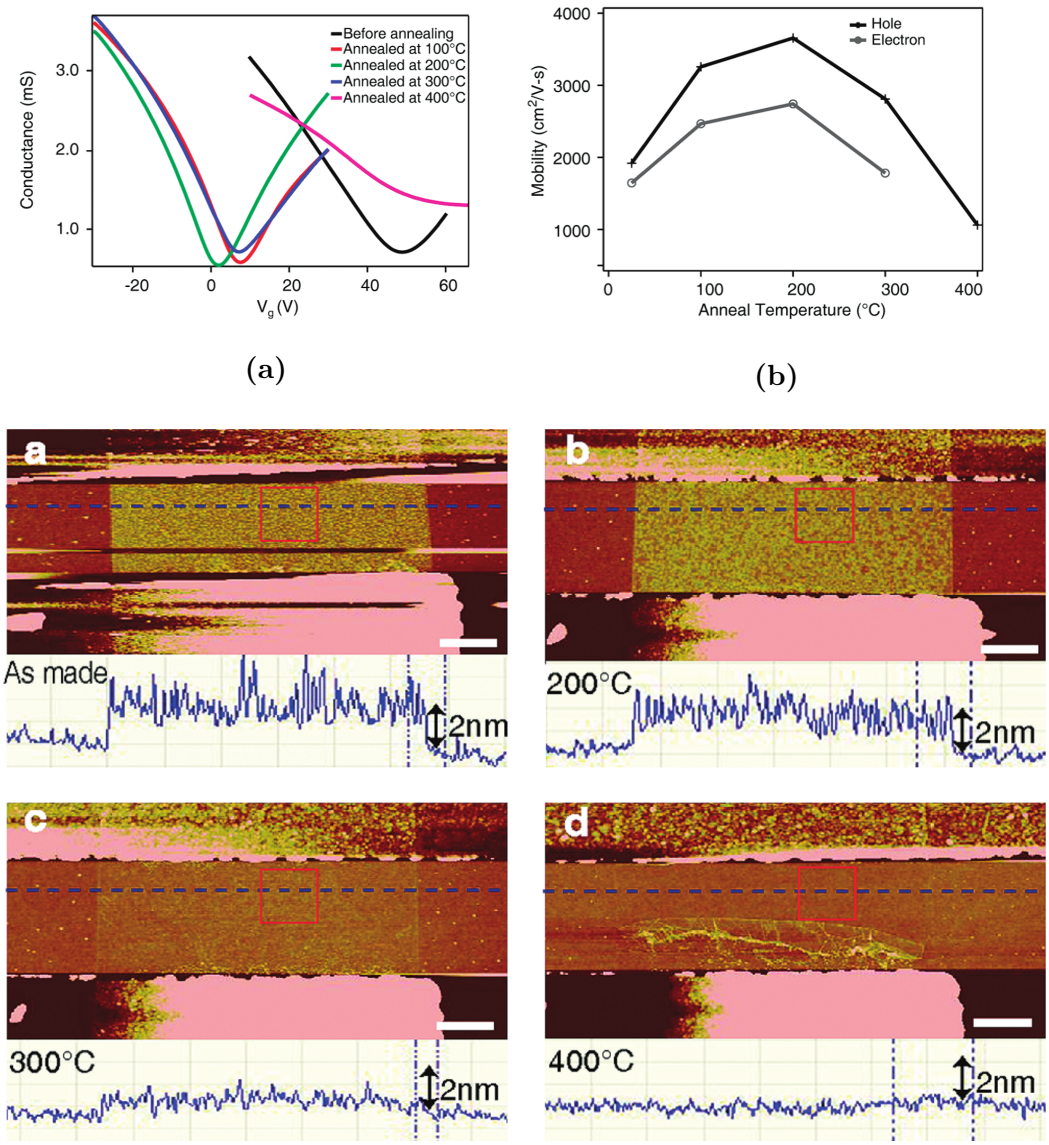


Figure 2.17: Effects of thermal annealing temperature on a) conductance as a function of gate voltage, b) hole and electron mobility and c) changes in graphene surface quality with increasing annealing temperature. *Image taken from [96].*

2.4.3 Suitability as a Material for High Temperature Devices

One of the limitations with present day semiconducting Hall devices is the large thermal instability due to narrowing of the energy gap with increasing temperature, ultimately resulting in an increase in intrinsic carrier density. Monolayer

graphene is a zero bandgap material, meaning thermal instability due to bandgap narrowing does not occur. This of great importance when considering the design of Hall sensor with device sensitivity being inversely proportional to carrier density, as can be seen in Equation 2.2. Studies have shown that the intrinsic carrier concentration in graphene is an order of magnitude less sensitive to temperature than that of traditional semiconductors [14]. Limited studies have been carried out into thermal effects in terms of device applications, however studies have determined that thermally generated carrier density can be described using [97]:

$$n_{th} = \frac{\pi}{6}\left(\frac{k_B T}{\hbar \nu_F}\right)^2 \tag{2.10}$$

where k_B is Boltzmann constant (1.38×10^{-23} JK^{-1}), T the temperature in Kelvin, $\hbar$ the reduced Planck's constant (1.05×10^{-34} Js^{-1}) and ν_F the Fermi velocity in ms^{-1}.

The carrier density in graphene is directly linked to the Fermi level by Equation 2.11 [14]:

$$n = \left(\frac{E_F}{\hbar \nu_F}\right)^2 /\pi \tag{2.11}$$

This relationship shows that an increase in Fermi level results in an increase in carrier density and vice versa. Therefore, when the Fermi level sits at the Dirac point the carrier density will be at a minimum, however when performing high temperature measurements the thermally generated carrier density also needs to be taken into consideration. Equation 2.10 predicts that for a device operating at the Dirac point, the thermally generated carrier density is zero however in a practical device this is not the case.

Banadaki *et al.* have demonstrated a GFET for high temperature sensing applications with a temperature coefficient of resistance of 3150 ppmK^{-1} [98]. These devices consist of a single graphene layer on a SiO_2/Si substrate, similar to devices fabricated in this study, however the intended application requires these GFETs to be highly sensitive to changes in temperature. A schematic of these GFETs is shown in Figure 2.18a. The intrinsic carrier density as a function of gate bias

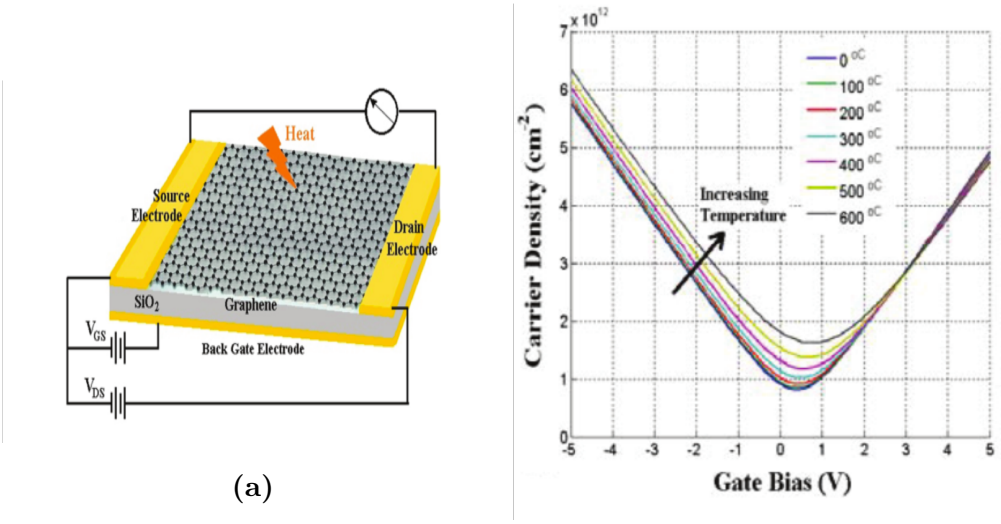


Figure 2.18: GFET temperature sensor a) schematic and b) intrinsic carrier density as a function of gate voltage with increasing temperature. *Image taken from [98].*

with increasing temperature is subsequently shown in Figure 2.18b. It can be seen from these results that for a gate bias of 2 V and above the thermal coefficient of the carrier density is significantly reduced with thermal instability becoming almost negligible at a gate bias of 3.0 V. This suggests that the thermal coefficient of graphene devices can be uniquely controlled through tuning of the gate bias which is particularly advantageous to this study where a low thermal coefficient is critical to device operation.

In addition to low thermal drift, the material also needs to be thermally conductive in order for the device to be able to withstand high temperatures. Graphene has been found to have outstanding thermal properties, with a thermal conductivity as high as 5300 $Wm^{-1}K^{-1}$ for single layer graphene [46]. This far exceeds that of diamond which has a thermal conductivity of up to 2200 $Wm^{-1}K^{-1}$ and is the best known bulk thermal conductor. Combining this with the ability to grow graphene on a SiC substrate makes it a valid option for current sensing in high temperature environments, particularly as the majority of existing high temperature electronic devices are SiC based.

2.5 Integration with Silicon Carbide Switching Devices

The low-level output exhibited in Hall effect sensors typically requires amplification in order to provide a useable signal. Whilst the advances in graphene fabrication should allow for development of Hall effect devices with improved resolution and sensitivity and therefore a reduction in output signal conditioning, some circuitry may still be required. Due to the system requirements previously described such as high temperature operation and high switching speeds, the semiconductor material used to design this amplification also needs to be carefully considered. Advances in SiC technology for applications in high temperature and high power applications [99] make it an obvious contender. This has additional advantages due to the ability of graphene to be grown epitaxially on SiC allowing for monolithic integration of graphene sensors with interfacing circuitry. In order to fully understand how the implementation of SiC devices into developing this circuitry, the fundamental properties of SiC must first be considered.

2.5.1 SiC Physical and Electrical Properties

SiC is a compound semiconductor that consists of Si and C atoms covalently bonded to form a SiC crystal [100]. This strong chemical bonding gives the material very high hardness, chemical inertness and high thermal conductivity [101]. SiC exhibits a wide bandgap (2.3–3.3 eV), the exact value of which is polytype dependant, high critical electric field strength and high saturation drift velocity and as such it is commonly used for high power, high temperature and high frequency electronics applications [102, 103]. Each Si atom is covalently bonded to four neighbouring C atoms in a tetrahedal structure, and vice versa. These tetrahedral structures are bonded together in a hexagonal structure (in the case of 4H-SiC and 6H-SiC) and a cubic structure for 3C-SiC, shown in Figure 2.19. The bulk structure of SiC is then formed by stacking of these hexagonal layers allowing for the material to adopt different crystal structures, known as polytypism [104]. The most commercially available of these polytypes are 3C-SiC, 4H-SiC and 6H-

SiC, where H represents hexagonal and C cubic, the lattice structures of which are shown in Figure 2.19, where A, B and C are the potentially occupied sites in a hexagonal close- packed structure. Two layers cannot successively occupy the same site (i.e. the next layer on top of an 'A' must be either 'B' or 'C' sites). For most materials only one stacking structure is usually stable however, SiC crystallises in more than 200 known polytypes.

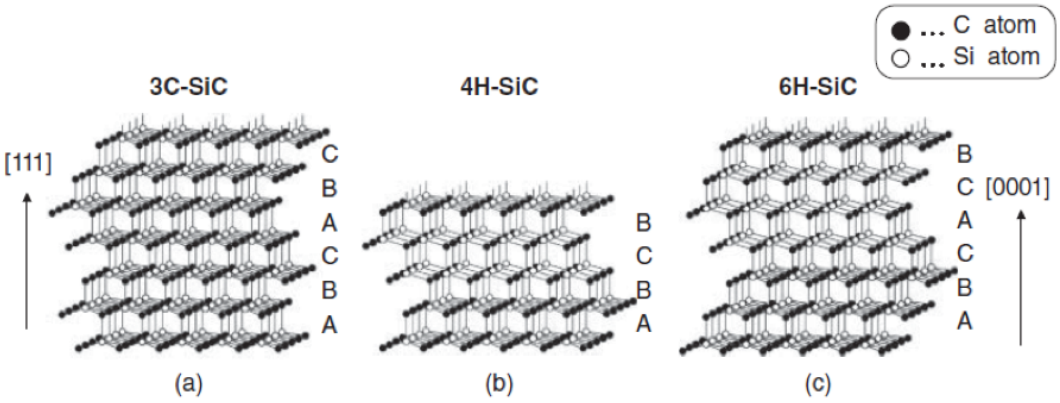


Figure 2.19: Lattice structure of 3C-SiC, 4H-SiC and 6H-SiC. *Image taken from [105].*

The stability of SiC polytypes is strongly temperature dependant [106]. As such, 3C-SiC has proven to be unstable and is transformed into hexagonal polytypes at very high temperatures (1900-2000°C) [107]. This makes it difficult to grow 3C-SiC ingots at a sensible growth rate, nevertheless it remains a popular choice due to its ability to be grown heteroepitaxially on Si substrates [108]. 2H-SiC is also unstable at high temperatures and as such 4H-SiC and 6H-SiC polytypes are the most popular where high temperature application is required. The majority of the work in this thesis focusses on 4H-SiC.

The electrical properties of the most commonly used SiC polytypes are summarised in Table 2.2, with Si properties also shown as a comparison. Similar to Si, all polytypes of SiC have an indirect bandstructure however SiC has a significantly larger bandgap (2.2-3.2 eV) in comparison to Si 1.12 eV. SiC has a high thermal conductivity and an intrinsic carrier concentration which is ∼16 orders of magnitude lower than that of Si, allowing for significantly higher operating temperatures. The intrinsic carrier concentration suggests a maximum operating temperature of 800°C [109] there is however a practical limit of approximately 500°C in or-

der for a SiC device to operate reliably [110]. The high critical electric field of 2.2 MV/cm also makes it suitable for use in power electronics applications. These superior properties make SiC the material of choice in electronic circuits for use in extreme environments such as in aerospace, energy production and industrial automation [111].

Table 2.2: Electrical properties of SiC and Si at 300 K. [105].

Property	Si	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV) at 300 K	1.12	2.36	3.26	3.02
Critical Electric Field (V/cm)	3.0×10^5	1.4×10^6	2.2×10^6	1.7×10^6
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	1.5	3.3-4.9	3.3-4.9	3.3-4.9
Electron Saturated Drift Velocity (cms^{-1})	1.0×10^7	2.0×10^7	2.2×10^7	1.9×10^7
Electron Mobility ($cm^2V^{-1}s^{-1}$)	1500	800	900	400
Hole Mobility ($cm^2V^{-1}s^{-1}$)	450	320	120	90
Relative Dielectric Constant	11.9	9.72	9.76	9.66

2.5.2 SiC Based Differential Amplifiers

The low-level output voltage of Hall sensors means an amplification stage is essential in order to extract useable information. Due to the system requirements, SiC devices were found to be suitable for this application due to their ability to withstand high temperatures in addition to the simplicity of integrating graphene technology with SiC.

Silicon based differential amplifiers typically use device types such as Bipolar Junction Transistors (BJT's) and MOSFETs. However when fabricated in SiC these device types suffer from a number of limitations with MOSFETs suffering from an unstable threshold voltage due to poor gate oxide quality, restricting maximum operating temperatures to less than 300°C [112]. Silicon-on-insulator (SOI) technology, whilst enabling the development of high temperature electronics, has an effective limit of 300°C. Bipolar transistors have been shown to have a low input impedance in comparison to FET devices. SiC MESFETS with 500 hours of continuous operation at 500°C have been demonstrated however the devices suffer

from high gate leakage at these temperatures due to the low barrier height of the Schottky barrier gate [113].

Junction Field Effect Transistors (JFETs) offer a viable solution to the intrinsic limitations of other commonly used device types such as those previously discussed, with the lack of gate oxide layer resulting in greater threshold voltage stability and reduction of intrinsic noise. Stable long term operation of SiC JFETs has been demonstrated at 500°C with less than 1.0 % shift in threshold voltage [114].

Differential amplifiers designed using SiC JFETs have been reported in the literature, most notably by Patil *et al.* [115]. They demonstrate the use of 6H-SiC JFETS to construct differential pairs, operating at temperatures of up to 450°C.

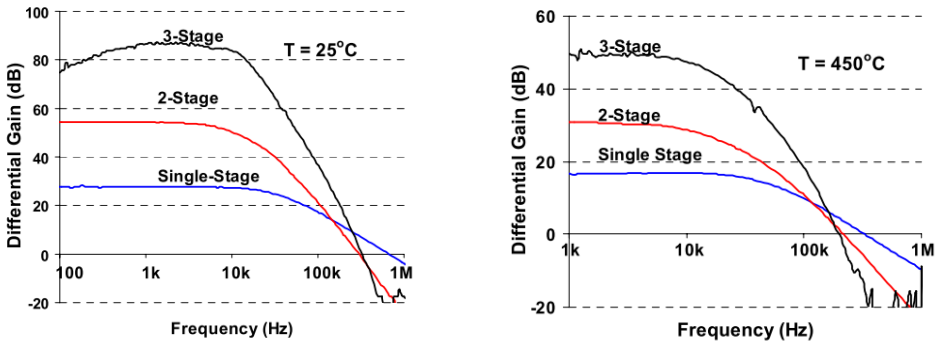


Figure 2.20: Differential gain of multi-stage differential amplifier at a) 25°C and b) 450°C. *Image taken from [115].*

Figure 2.20 shows the differential gain of these amplifiers at both room temperature and 450°C. They are shown to exhibit a three-stage differential gain of up to 87 dB at room temperature, with this reducing to 50 dB at 450°C. These devices are constructed using differential pairs with external biasing and passive load - the voltage gain is shown to be higher when this is switched to active load. Typically, active load amplifiers have minimal shift in DC gain with temperature suggesting they are suited to high temperature applications. The transfer characteristics in Figure 2.21 show a significant mismatch between the differential pairs resulting in offset voltage shift of up to 2.0 V at high temperatures.

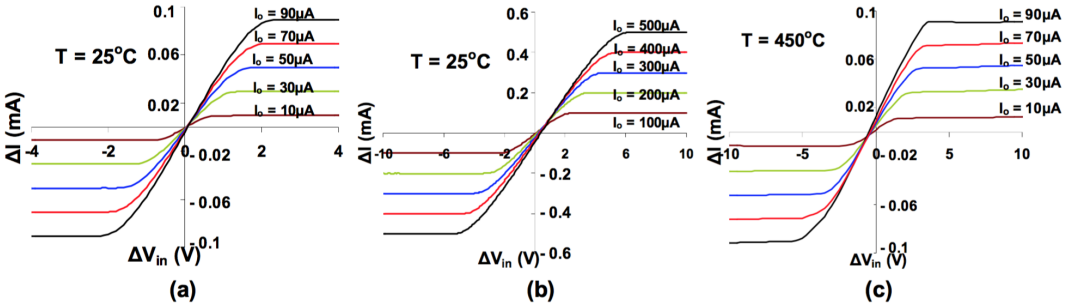


Figure 2.21: DC transfer characteristics of differential pairs for varying bias currents at both 25°C and 450°C. *Image taken from [115].*

SiC JFET based operational amplifiers have been demonstrated with an open loop gain of up to 67 dB and a threshold voltage shift of 0.5 V [116]. A two-stage fully monolithic differential amplifier with gain of 69 dB at 576°C has been shown in [115]. Monolithic integration is advantageous as it allows for differential amplifiers to be easily interfaced with various sensor types and also allows for a number of applications where space optimisation is essential.

Low frequency $1/f$ noise in devices can be evaluated by measuring the spectral density and extracting the Hooge parameter of the device at various frequencies. Values of the Hooge parameter typically vary between different semiconductor devices, with values of 2.0×10^{-3} observed in p-n junction diodes [117] and values of 1.0×10^{-8} observed in BJT's [118]. Lower values of Hooge parameter suggest very high degree of structural quality for the channel material and a rather small contribution of the contacts in the total noise of the device [119]. SiC JFETs with Hooge parameter of $\sim10^{-5}$ were observed at temperatures above 300°C [119]. At present there are two models to explain the origin of low frequency noise and analyse noise data: the carrier density fluctuation model and the mobility fluctuation model. Carrier density attributes the origin of noise to random trapping and de-trapping of free carriers by traps that have a set distribution of time constants. These distributions can arise naturally at the semiconductor-oxide interface from spatially uniform distribution of tunnelling depths to the trapping sites [120]. Comparatively, the mobility model attributes noise to spontaneous mobility fluctuation due to scattering of carriers.

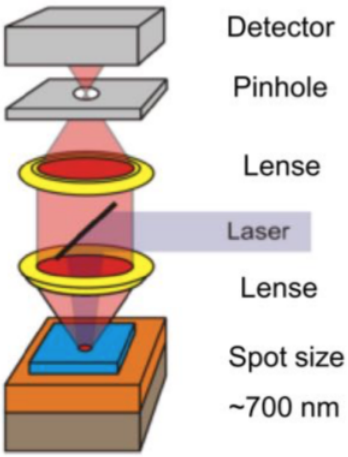
2.6 Graphene Analysis Techniques

Surface analysis techniques are vital to understanding how the graphene film is affected by different processing techniques and thus give a vital insight into how to optimise the process and ultimately the electronic properties.

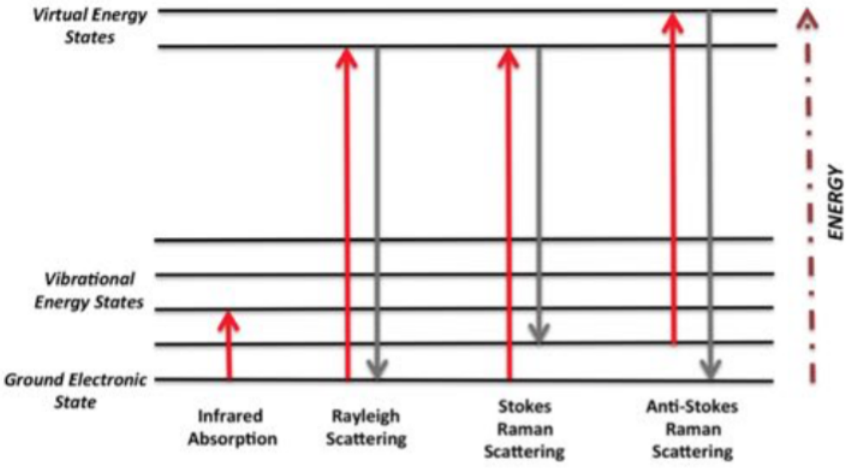
2.6.1 Raman Spectroscopy of Graphene

Raman spectroscopy is a vibrational spectroscopy technique based on the inelastic scattering of monochromatic light which can provide both chemical and structural information. A typical experimental system of a Raman setup is shown in Figure 2.22a. The scattering of photons upon generation by a monochromatic laser is being observed. The interaction of these scattered photons promotes the molecule to a virtual energy state before it is de-excited and returns to its original energy state. Elastic scattering, also known as Rayleigh scattering is the most common. This occurs when the molecule relaxes and returns to its original energy level, with the emitted photon having the same energy as the incident photon. Inelastic scattering, which we are more interested in this case, is much less common and occurs when the emitted photon has a differing energy to that of the incident photon. This results in an energetic gain or loss, with a shift in wavelength also being observed. There are two types of inelastic scattering - Stokes and anti-Stokes. Stokes scattering occurs when a molecule is promoted from its ground state to a higher energy state due to the absorption of energy, with the photon now having less energy than initially, resulting in a shift to a longer wavelength (also known as red-shift). Anti-Stokes occurs when a molecule occupies an excited state and is demoted to the ground due to transfer of energy from the molecule to a photon. This results in a higher energy photon which is shifted to a shorter wavelength (also known as blue-shift). An energy diagram showing these transitions is demonstrated in Figure 2.22b.

Raman spectroscopy is widely utilised as a versatile technique to characterise both electronic and mechanical properties in graphene, such as number of graphene layers, doping levels and defect density. The Raman spectra for both pristine



(a)

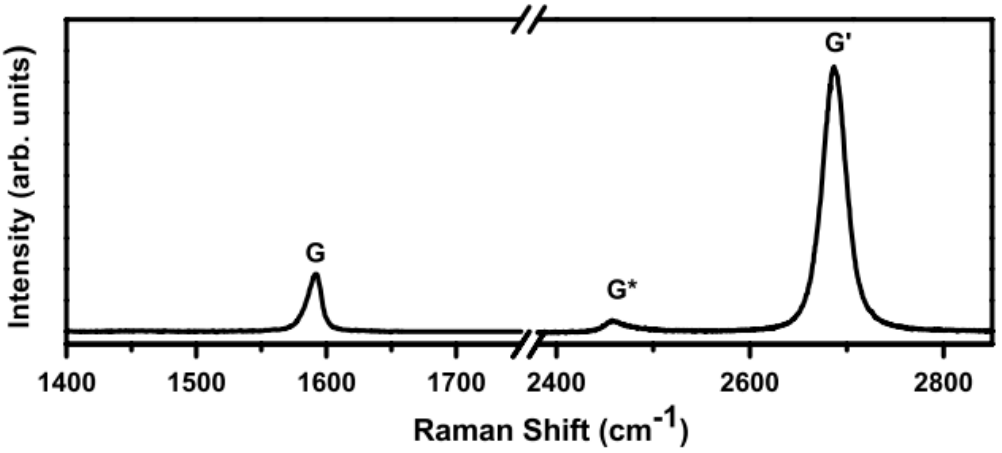


(b)

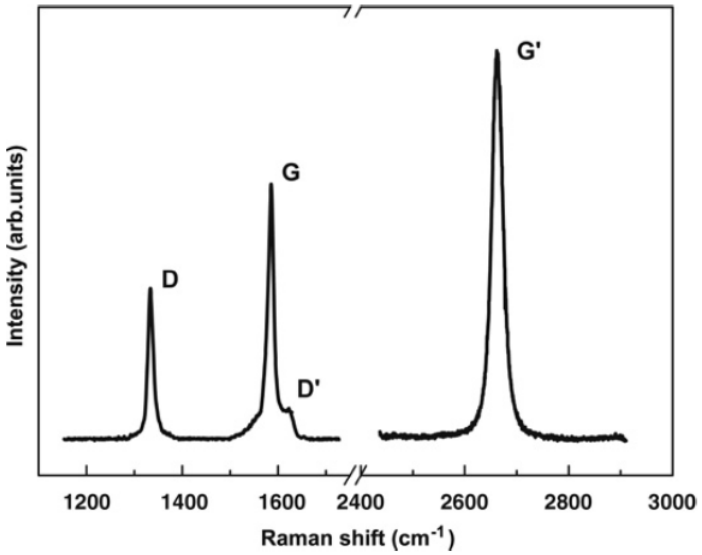
Figure 2.22: a) Typical Raman spectroscopy setup and b) energy level diagram showing stokes, anti-stokes and Rayleigh scattering. *Images taken from [85] and [121] respectively.*

graphene and disordered graphene is shown in Figure 2.23. Initially considering the Raman spectra of pristine graphene shown in Figure 2.23a it can be seen that there is a G' peak (more commonly referred to as the 2D peak) present at $\sim$2690 cm^{-1} and a G peak at $\sim$1590 cm^{-1}. The Raman spectra for disordered graphene in Figure 2.23b is shown to have additional D and D' peaks at around 1350 cm^{-1} and 1620 cm^{-1} respectively which is commonly attributed to defects present in the graphene film. As such, this factor can be used as a tool to estimate defect density by calculating the D/G peak ratio. For pristine graphene this ratio

will be close to 0 and will show an increase with the presence of defects in the film.



(a)



(b)

Figure 2.23: Raman spectra of a) pristine graphene and b) disordered graphene. *Image taken from [122].*

Many studies reported in the literature have shown that monitoring of the 2D peak intensity can be utilised as a tool for thickness determination of graphene films. The 2D/G ratio alone however can not be used as an accurate determination of graphene thickness, with numerous studies showing that this ratio is also dependant on the electron and hole concentration. Das *et al.* showed that as the graphene film is doped and Fermi level shifted - the 2D/G ratio is reduced from

the maximum value that occurs at the charge neutrality point [123]. At the charge neutrality point the 2D/G ratio is at a maxima with the hole and electron doping at a minimum shifting the ratio lower, hence a low 2D/G may not necessarily be as a result of bi-layer graphene, so it is important to consider this factor alongside the full-width at half maximum (FWHM) when determining the thickness of a graphene film.

Ferrari *et al.* [124] showed that peak intensity and FWHM are dependant on the number of graphene layers. This is demonstrated in Figure 2.24 with bi-layer graphene shown to have a broader and blue-shifted 2D peak than that of monolayer graphene.

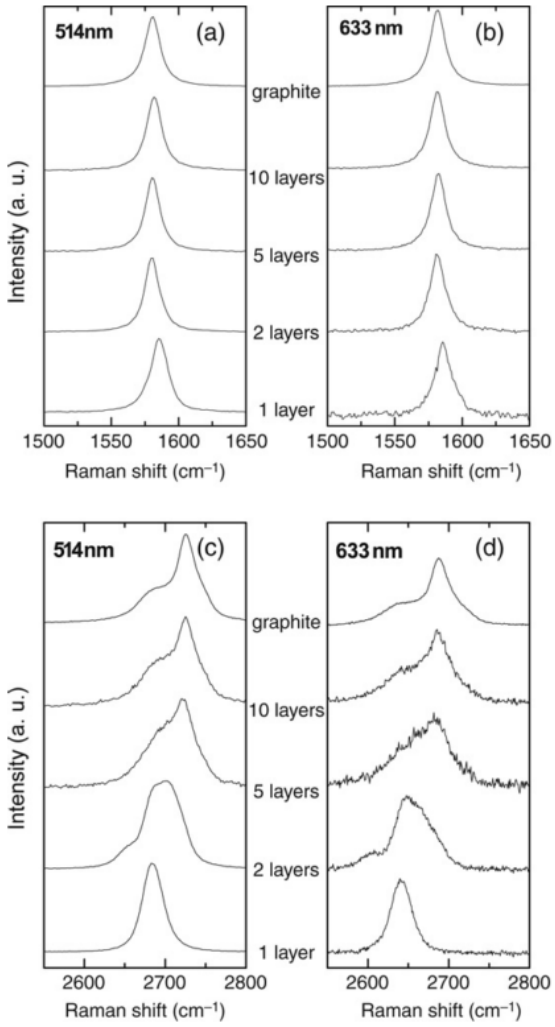


Figure 2.24: Evolution of G (images a and b) and 2D (images c and d) bands with increasing graphene layers for 514 nm and 633 nm excitations. *Image taken from [124].*

The results from Raman scattering experiments are reported throughout this thesis as an assessment of surface quality and to determine the impact different fabrication techniques have on the quality of the graphene surface.

2.6.2 Electrical Characterisation

Van der Pauw and Hall Measurements

Four-probe measurements were performed using a van der Pauw configuration in order to minimise the contribution of metal contacts to extracted sheet resistance values that is often seen in standard two-probe measurements. An optical micrograph of a typical Hall cross used for such measurements is shown in Figure 2.25a.

(a) **(b)**

Figure 2.25: Hall cross used for Van Der Pauw images with a) showing an optical image of fabricated structures and b) showing a schematic cross-section.

Resistance is determined by passing a current between adjacent contacts (A to B) and measuring the resulting voltage drop across the opposing adjacent contacts (C to D). The resistance is therefore defined as:

$$R_{AB,CD} = \frac{V_{CD}}{I_{AB}} \tag{2.12}$$

By carrying out additional measurements between other contact edges $R_{CD,AB}$, $R_{AC,BD}$ and $R_{BD,AC}$, an average of resistance can be taken to provide more accurate measurements.

Hall measurement is a critical tool in electrical characterisation, allowing for extraction of key parameters including carrier mobility and sheet carrier density. As

the graphene in this project is intended for use as a Hall sensors, these measurements are also crucial for determining key performance metrics such as the current related sensitivity (S_I), absolute sensitivity (S_A) and offset equivalent magnetic field (B_{off}). The Hall effect occurs when a current is passed between opposing contacts of a conducting material, with the resulting voltage measured between the adjacent contacts. When a magnetic field is applied perpendicular to the direction of current flow a Lorentz force is exerted on the charge carriers resulting in an accumulation of charge carriers at the edge of the conductor. This results in a potential difference being generated perpendicular to both the current flow and magnetic field, commonly known as the Hall voltage (V_H). The Hall voltage is defined as:

$$V_H = \frac{R_H B I}{t} \tag{2.13}$$

where R_H is the Hall coefficient in cm^3C^{-1}, B the magnetic field in Tesla, I the current in Amps and t the thickness of the conductive film in cm. The Hall coefficient is further defined by:

$$R_H = \frac{1}{ne} \tag{2.14}$$

where n is the carrier density in cm^{-3} and e the charge of a proton (1.6×10^{-19} C).

In 2D materials such as graphene, sheet carrier density is used as opposed to 3D carrier density and as such Equation 2.13 can be amended to the following:

$$V_H = R_H B I \tag{2.15}$$

The carrier density in Equation 2.14 is subsequently the sheet carrier density as opposed to bulk and measured in cm^{-2} with Hall coefficient reduced to cm^2C^{-1}. Hall mobility is subsequently determined using Equation 3.6:

$$\mu_H = \frac{R_H}{R_{SH}} \tag{2.16}$$

where R_H is the Hall coefficient in cm^2C^{-1} and R_{SH} the sheet resistance in $\Omega/\square$.

When analysing Hall cross performance in terms of a magnetic sensor, the sensitivity of the Hall voltage to magnetic field for a given bias current is often used as the benchmark for sensor performance. This is most commonly referred to as the current related sensitivity which can be determined using Equation 2.17:

$$S_I = \frac{V_H}{BI} \tag{2.17}$$

where V_H is the Hall voltage generated at the sensor output in Volts, B the magnetic field in Tesla and I the bias current in Amps.

Equation 2.17 forms the basis for analysis of the graphene Hall sensor performance in subsequent sections and will be used to extract a number of critical parameters including the sheet carrier density and the carrier mobility.

2.6.3 Calculation of Errors

Throughout this thesis accuracy of numerical values is determined through calculation of the standard error of the mean.

The mean of the data can be calculated according to Equation 2.18:

$$\bar{x} = \frac{\sum x_i}{n} \tag{2.18}$$

where x_i is each individual data value and n the sample size.

The standard deviation of a data set can subsequently be calculated according to Equation 2.19:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n} (x_i - \bar{x})}{n-1}} \tag{2.19}$$

Finally the standard error of the mean is calculated according to Equation 2.20:

$$\sigma_{\bar{x}} = \frac{\sigma}{\sqrt{n}} \tag{2.20}$$

Numerical values throughout this thesis are subsequently quoted in the format shown in Equation 2.21:

$$\bar{x} \pm \sigma_{\bar{x}} \tag{2.21}$$

2.7 Summary

The requirement for sensors capable of operating at higher temperature and higher frequency than is presently available as the aerospace industry moves towards the MEA is identified with the limitations of present current sensing techniques also discussed. The suitability of graphene to overcome these limitations and enable development of highly sensitive Hall effect devices is discussed alongside developments in graphene synthesis techniques. Challenges within graphene device processing is also discussed, namely the influence of organic solvents and metal contacts on the electronic and transport properties of graphene. The limited theoretical studies into graphene's potential use as a high temperature material is also presented, the basis of which forms a key part of this study. As well as the sensors, SiC based amplifiers are discussed, the development of which would allow for monolithic integration of graphene Hall sensors with SiC circuitry in high temperature power electronic applications due to the ability to epitaxially synthesise graphene on SiC. Finally, analysis techniques that are used throughout this thesis are discussed in depth with particularly focus on how they are applied to analysing graphene films and devices.

Chapter 3

Optimisation of Graphene Device Processing

3.1 Introduction

The exceptional material and electronic properties of graphene have been well documented, with an increase of interest in developing devices including high speed FETs [38, 125], chemical sensors and high frequency amplifiers [77, 126]. Many of these properties however are true only of pristine, uncontaminated graphene. Generally, the electronic properties of graphene are degraded due to a number of limiting factors such as contaminants on the surface, choice of substrate and overall quality of the graphene layer. Device fabrication by standard lithography exposes the hydrophobic graphene surface to organic resist residues which can not be removed using standard solvents. These residues can act as external scattering sites on the surface which degrade the transport properties [96]. Annealing is often used to remove residues and restore the graphene surface, however residues will still remain in areas covered by metal contacts. As such, development of fabrication techniques that reduce contamination and damage of the graphene film are critical for the realisation of high performance graphene devices with a high yield.

Due to the sensitivity of the graphene surface to any material with which it comes into contact, the choice of substrate is also inherently critical to device perfor-

mance. Interaction between the graphene film and substrate results in charge transfer doping from adsorption of atoms or molecules on the substrate surface. This alters the transport properties of the graphene including carrier type and concentration [86]. For example, SiO_2 substrates which are typically used for transferred CVD graphene introduce external scattering sites from trapped charges and low energy surface phonons, both mechanisms which are known to degrade device performance [127].

This chapter reports the difficulties encountered in fabricating graphene devices due to the issues described above and develop methods for both optimisation of these processes and device characteristics.

3.2 Fabrication of Devices Through The Use of a Copper Sacrificial Layer

Standard lithographic processing typically used in device fabrication presents a number of challenges when applied to graphene. Photoresist residues contaminate the graphene surface, resulting in the degradation of electronic properties and ultimately poor device performance. Additionally, the low surface adhesion results in graphene detachment from the substrate when using standard solvents including tetramethylammonium hydroxide (TMAH), a common ingredient in photoresist developers. This generally results in a low device yield and significant variability in device performance across the wafer. E-beam lithography is a popular technique to minimise sample contact with organic solvents, however it has low throughput and as such is not scalable for high volume, wafer scale manufacturing of devices [128, 129]. Figure 3.1 shows optical micrographs of graphene films patterned using standard lithographic processing, with the graphene film exhibiting signs of wrinkling and detachment from the substrate. This is particularly evident in the right hand image with the lighter blue area shown being the graphene film which is only partially covering the desired pattern. The left hand image also shows areas of residue on the un-patterned areas of the substrate which is residue of graphene

film which has detached from the patterned areas and been deposited on other regions of the wafer.

One solution to reduce this issue is to deposit a metal sacrificial layer onto the graphene surface prior to exposure to any organic contaminants. Ni has been proposed as a suitable metal [130] however the Ni-Gr interface is based on a chemisorption reaction (rather than a physisorption interaction) and as such forms a nickel carbide which disturbs the electronic structure of the graphene film in the area underneath the metallised region [131]. This in turn leads to the degradation of the electronic and transport properties which are fundamental to achieving optimal device characteristics. Al is also a popular choice of metal sacrificial layer and is in fact recommended by many CVD graphene suppliers as part of their fabrication processes. Whilst the use of Al does reduce detachment in comparison to conventional fabrication methods, Al is etched by TMAH based developers [132] and as such the graphene film is not fully protected with partial detachment still occurring at the edges of the desired pattern, resulting in a degradation of the electronic properties. In order to identify a suitable alternative, the interaction of metals when in contact with the graphene film needs to be considered.

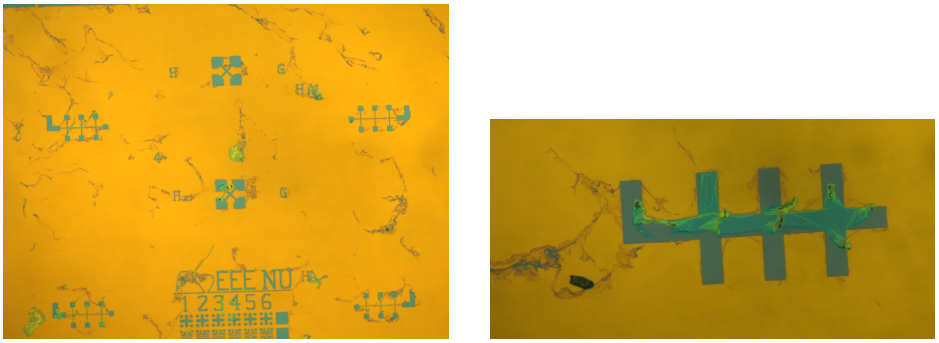


Figure 3.1: Optical micrographs of devices fabricated using no sacrificial layer.

The data in Table 3.1 show the work function of different metals and the work function of graphene when in contact with these metals. Changes in the graphene work function when in contact with the metal film results in charge transfer and unintentional doping of the graphene layer [84] and as such it is important to choose a metal which causes a reduced shift in work function in order to preserve the electronic properties of the graphene film. Of the metals listed, Cu results in the smallest shift in graphene work function, $\Delta\ W_G = -0.08$ eV. Studies reported

Table 3.1: Work function of metals (W_M), work function of graphene (W_G) when in contact with different metals that are suitable for use as a sacrificial layer and the shift in graphene work function ΔW_G when in contact with these metals. [84].

	Gr	Ni	Cu	Al	Au
W_M (eV)		5.01	5.22	4.08	5.54
W_G (eV)	4.48	3.66	4.40	4.04	4.74
ΔW_G (eV)	0	-0.82	-0.08	-0.44	+0.26

in the literature for the growth of CVD graphene on a Cu catalyst demonstrates that Cu has a sufficiently small enough interaction with the graphene film and the solubility of carbon in copper is low [133, 134].

There have been several studies into the behaviour of the Cu-Gr interface, as this is a fundamental consideration for the Chemical Vapour Deposition (CVD) growth of graphene on a Cu film. Previous studies have shown that Cu is a favourable catalyst for this process, because of the low carbon solubility and lack of a chemical based interaction with the graphene surface. Additionally, the chemicals used to chemically remove excess copper during the wet transfer processes, including ammonium persulphate (APS), have been shown to cause little or no damage to the material and electronic properties of the graphene film [135, 136]. Considering these factors, a hypothesis that a thin Cu film deposited on the graphene surface would make a more suitable metal sacrificial layer in comparison to either Al or Ni was developed.

Nine commercial CVD graphene samples on SiO_2/Si substrate were used in this study, to enable the direct comparison of three fabrication approaches - no sacrificial layer, Al sacrificial layer and Cu sacrificial layer. Twelve eight-terminal Hall structures of varying width, six identical Van der Pauw structures and four TLM structures were fabricated onto each sample to enable the extraction of the electronic material properties. For the fabrication processes that utilised a sacrificial metal layer, a 50 nm metal film was deposited onto the surface of the graphene using e-beam evaporation. Subsequently, conventional photolithography

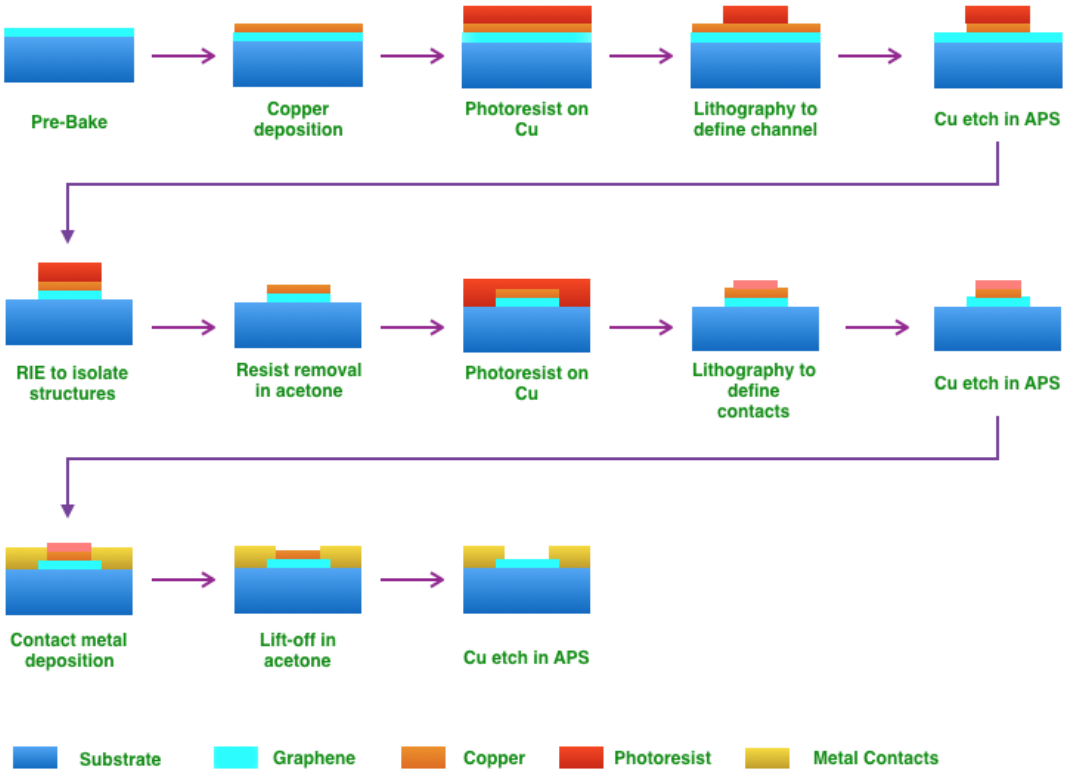


Figure 3.2: Device fabrication process steps using Cu sacrificial layer.

patterning using S1813 positive resist was performed to define the physical dimensions of the graphene channels. The unwanted metal film was then etched using a 0.1M solution of APS for Cu and TMAH for Al, followed by a Reactive Ion Etch (RIE) process to remove the excess graphene. The residual photoresist was then removed using acetone. A second photolithography step was then performed to define windows for the deposition of the metal contacts to the graphene. After the removal of the unwanted metal film using APS and TMAH, deposition of Ni/Au (5 nm/100 nm) films were performed using e–beam evaporation, prior to lift off to define the pattern in warm acetone. The metal film protecting the surface of the graphene in the active device was subsequently removed. A schematic representation of the process flow using a Cu sacrificial layer is shown in Figure 3.2. For devices fabricated using no sacrificial layer steps 2, 5, 10 and 13 are not involved in the process.

3.2.1 AFM Analysis

Atomic Force Microscopy (AFM) measurements of the graphene surface were obtained using a Park AFM system operating in non-contact mode. The measurements were taken across each of the nine wafers with the largest flake on each sample that allowed for a full 10 μm$\times$10 μm image to be captured to enable a direct comparison between the surface morphology of the different fabrication methods. Images shown in this section are representative of those taken across each of the nine wafers. The errors calculated for numerical values are taken from the standard deviation of values taken across each of the nine samples, with five measurements taken per a sample. Typical topographic images of the as received graphene films are shown in Figure 3.3a. It can be seen from the image the existence of residue on the graphene film, which can be observed as the bright areas. These are likely to originate from the transfer of the graphene film to the SiO_2/Si substrate by the commercial supplier of the graphene film. This is an issue commonly seen in CVD graphene when a wet transfer process is employed [137]. The image also shows that the film has the appearance of being continuous over the length scale investigated here, which agrees with the typical domain size for commercial CVD grown graphene, which is typically 20 μm. The average RMS surface roughness across the as received films is 2.5$\pm$0.50 nm. The images in Figures 3.3b - 3.3d show the topography of the surfaces for samples fabricated using conventional fabrication methods, Al sacrificial layer and Cu sacrificial layer respectively.

Considering the surface topology for the samples fabricated using no sacrificial layer, it can be seen that the majority of the graphene film has detached from the substrate, as the image shows large areas where the surface is dominated by SiO_2. The bottom right of the image in Figure 3.3b shows evidence of graphene which has remained on the sample and it shows an increase in RMS roughness of the graphene to 16$\pm$0.60 nm. This represents an increase in roughness of over 500 % in comparison to the as received films. Figure 3.3c show the AFM topography of samples fabricated using an Al sacrificial layer. It can be seen that whilst this layer has reduced detachment of the graphene film, it has folded in some regions, which results in a non-continuous film. The AFM images show significant residue on the

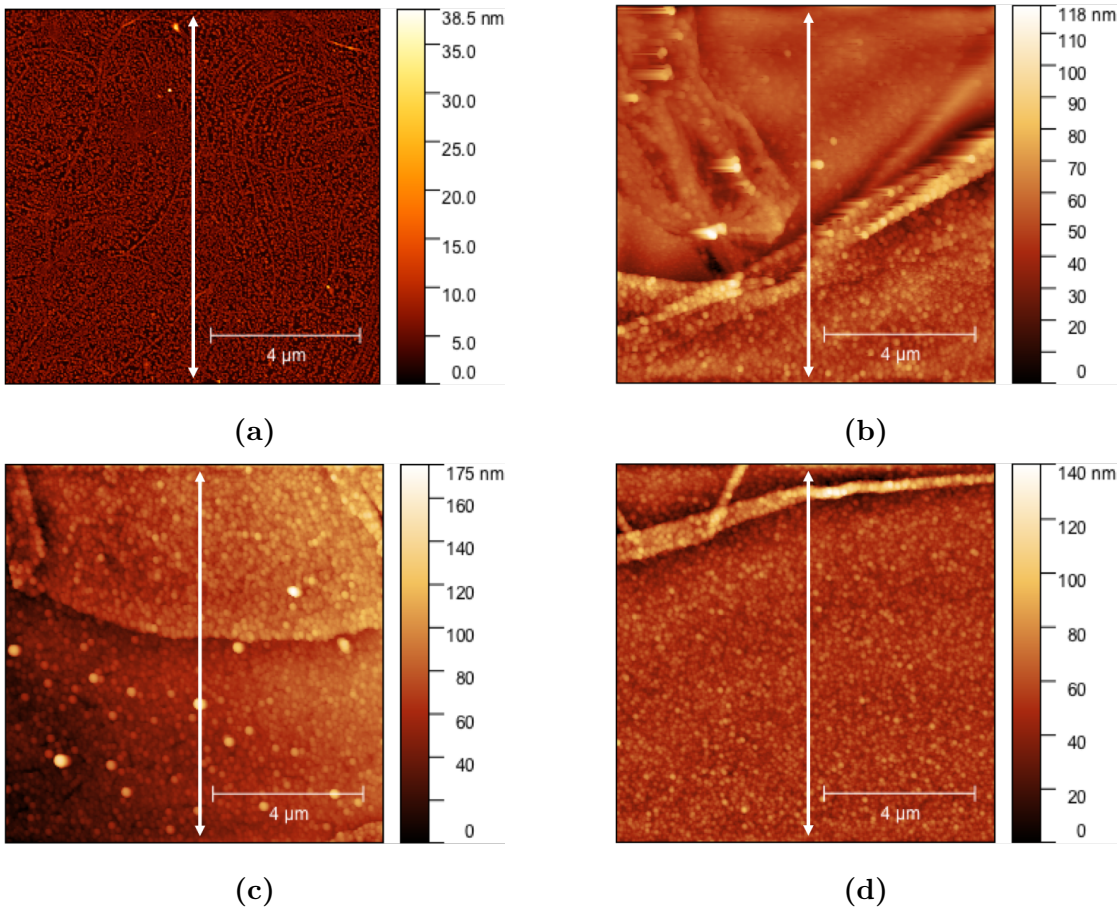


Figure 3.3: 10 μm×10 μm AFM topography of a) as received graphene films b) graphene films processed with no sacrificial layer c) Al sacrificial layer and d) Cu sacrificial layer. The white arrows indicate the region the line scans shown in Figure 3.4 were taken.

surface, as evidenced by the high concentration of bright features, suggesting that the Al layer has not been completely removed by the TMAH etch process. The average RMS surface roughness of the films processed using the Al sacrificial layer is found to be 17±0.40 nm, a significant increase over the as received film and an increase of 12 % over the samples fabricated using conventional lithography without a sacrificial layer.

In contrast, the samples fabricated using a Cu sacrificial layer have an average surface roughness of 8.8±0.20 nm, which is a significant reduction in comparison to the values reported for the no sacrificial layer and Al sacrificial layer techniques. The topography of the sample surface can be seen in Figure 3.3d, with the film shown to be mostly continuous. There is still some minor cracking present in

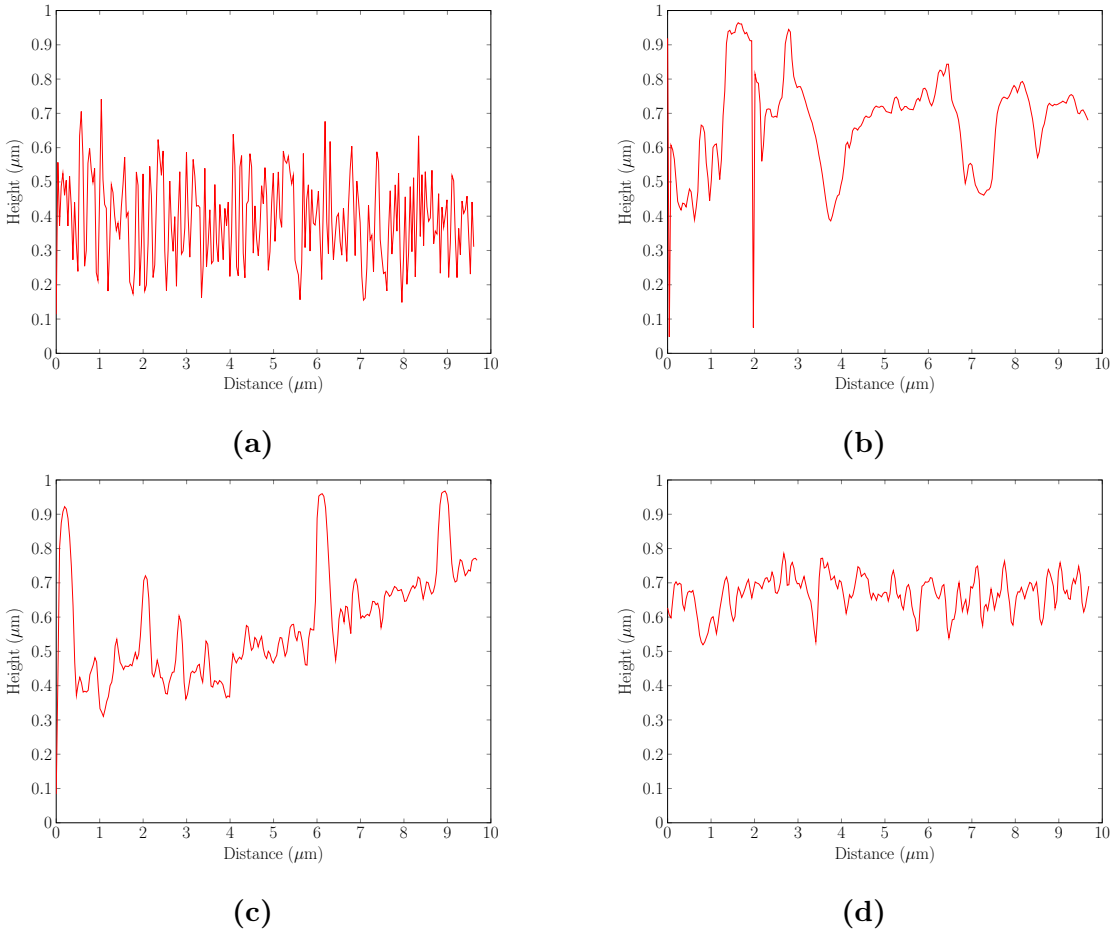


Figure 3.4: Height profile of a) as received graphene films, b) graphene films processed with no sacrificial layer, c) Al sacrificial layer and d) Cu sacrificial layer. Line scans were taken from the region denoted by the white arrows in Figure 3.3.

the graphene film in the upper left portion of the image, however there is no detachment of the film from the substrate. The low density of bright features on the surface of the graphene film indicates that there is little copper or resist based residues remaining on the graphene film after the removal of the copper sacrificial layer.

The corresponding height profiles of the AFM images seen in Figure 3.3 are shown in Figure 3.4. The data show the variation in height along a line across a 10 μm wide area of the continuous graphene films. Considering the height profile for the as received graphene films, shown in Figure 3.4a, it can be seen that the height profile is consistent across the measured area. A significant roughness can however be observed as evidenced by the repetitive change in measured height between 0.20 μm and 0.70 μm, with a short lateral displacement period. In contrast,

the height profile of graphene films fabricated using no sacrificial layer and an Al sacrificial layer, shown in Figures 3.4b and 3.4c respectively, exhibit an overall trend in the height profile along the line of measurement. This trend is not observed in the underlying SiO_2 film in either case, so the observed behaviour must arise from the graphene film, rather than the substrate. This trend may have arisen due to a number of factors, which include tears in the graphene film, a large number of residues on the surface or non-uniform removal of the metal sacrificial layer. Finally, the height profile of samples fabricated using Cu sacrificial layer is shown in Figure 3.4d. It can be observed from the data that the sample shows a significant reduction in the variability of height along the 10 μm line in comparison to those fabricated with no sacrificial layer and Al sacrificial layer. Taking this into account alongside the reduced RMS surface roughness previously described, suggests that the use of a Cu sacrificial layer results in a graphene film with a smoother surface and continuous layer in comparison to alternative methods.

It is further hypothesised that the increased surface roughness exhibited across the Cu sacrificial layer samples in comparison to as received is a result of the influence of the observed area of cracking in the upper left of the film. As such surface roughness measurements were repeated across a smaller 5.0 μm area of graphene film resulting in a reduced average surface roughness of 3.3$\pm$0.40 nm. This is significantly reduced from the previous value of 8.8$\pm$0.20 nm and is comparable to that of the as received graphene film at 2.5$\pm$0.50 nm. This data corresponds to that evidenced in the height profiles which suggests that as received graphene films and those fabricated with a Cu sacrificial quality have comparable surface quality and roughness.

3.2.2 Raman Spectroscopy

In addition to chemical contaminants observed on the surface during AFM analysis, exposure to the chemicals required for device fabrication can result in structural damage to the graphene film. As such, it is advantageous to be able to measure the mechanical strain in the graphene film using techniques such as Raman spectroscopy, which also allow the mapping of the strain distribution across a film.

The ability to measure the mechanical strain alongside chemical composition of the surface enables the determination as to whether shift in Raman characteristics is due to mechanical strain in the graphene film or doping of the surface. The most prominent features of the Raman spectra for graphene are the G peak, observed at 1580 cm^{-1} and the 2D peak at 2670 cm^{-1}. The Raman spectra of disordered graphene exhibit additional D and D' peaks at approximately 1350 cm^{-1} and 1620 cm^{-1} respectively. The concentration of defects in the graphene film can be determined by analysing the ratio of the intensities of the D and G peaks, the D/G peak ratio. The intensity of the D peak is known to increase with defect density. In addition, the ratio of the 2D to G peak intensities can be analysed to determine the number of graphene layers, whilst any shifts in these peaks can be used to extract the doping of the graphene film from contaminants on the surface. Similar to the AFM images shown in Section 3.2.1, the Raman spectra shown in this section are representative of those taken across each of the nine wafers. The errors calculated for numerical values are taken from the standard deviation of values taken across each of the nine samples, with five measurements taken per a sample.

The data in Figure 3.5 show the Raman spectra of the graphene films as received and after device fabrication. Initially considering the spectra of the as received films, it can be seen that the characteristic 2D and G peaks are present at 2690 cm^{-1} and 1593 cm^{-1} respectively, similar to those observed in CVD graphene films [122]. The 2D/G peak ratio of 1.1$\pm$0.10 is lower than expected for high quality monolayer graphene. In general, the intensity of the 2D peak has a higher amplitude for monolayer graphene, with values of the 2D/G ratio in excess of 2.0 typically observed in CVD graphene [122]. The spectra show evidence of an additional D peak which is located at 1350 cm^{-1}, which is indicative of defects or impurities on the graphene surface. These impurities likely originate from the wet transfer processes commonly used to transfer the CVD grown graphene film from a catalytic metal to an insulating substrate. This process generally involves the use of organic chemicals, such as PMMA, to support the graphene film during the transfer [138].

Lorentzian fitting was applied to the D peaks of the spectra, as is common prac-

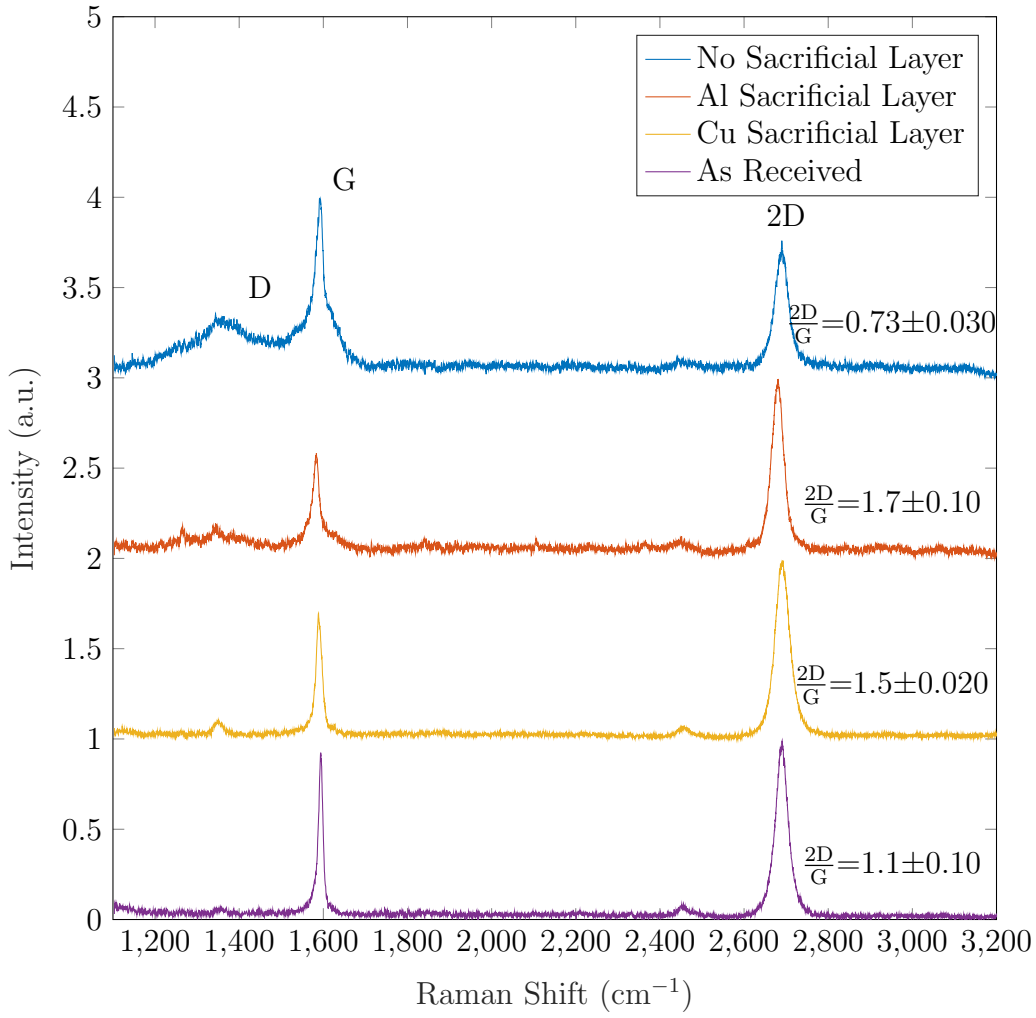


Figure 3.5: Raman spectra of as received films (purple trace), devices fabricated using conventional lithography (red trace), Al sacrificial layer (yellow trace) and Cu sacrificial layer (blue trace). Spectra have been offset on the y-axis with all spectra having been normalised and baseline removed.

tice with graphene Raman spectra [139–141]. These are shown in Figure 3.6 to enable a direct comparison between the data sets to examine the influence of the different fabrication techniques on the defect density. Initially comparing Figures 3.6a and 3.6b, the D peak intensity extracted from this data is found to be approximately 12±0.12 for as received samples and 97±0.43 for devices fabricated using no sacrificial layer, resulting in an increase in D/G ratio from 0.03±0.002 for the as received films, to 0.2±0.01 for devices processed using no sacrificial layer. This significant increase in the D/G ratio indicates that fabrication has introduced further defects in the graphene film, likely due to the fact that when no sacrificial layer

is used, photoresist comes into direct contact with the graphene film. This results in organic contaminants on the surface that remain after the use of acetone for photoresist removal. These contaminants introduce external scattering sites into the graphene film, which are expected to increase the transfer doping of the film and reduce the carrier mobility [91]. Additionally, it can be seen that the G peak has been red shifted from 1593 cm^{-1} in the as received film to 1591 cm^{-1}. This red shift typically occurs due to uniaxial strain in the graphene layer [142]. The origin of uniaxial strain in the sample processed using conventional photolithography is likely to be physical tears in the graphene film, resulting in the weakening of carbon bonds [143].

The Raman spectra for the graphene processed using a Cu sacrificial layer show a decrease in the D peak intensity in comparison to those processed using no sacrificial layer, resulting in a D/G ratio of just 0.07±0.004. In contrast, the D peak intensity for the samples that were fabricated using an Al sacrificial layer has increased to 148±0.930, giving a D/G ratio of 0.22±0.010, similar to that of samples fabricated using no sacrificial layer. This high D/G ratio can be interpreted as an increased defect density in the graphene, indicating that an Al sacrificial layer either doesn't provide sufficient protection against resist contaminants or the Al layer is introducing defects to the surface, which correlates with the AFM data presented in the previous section. The data in Figure 3.6c also show the existence of a further peak, located at around 1260 cm^{-1}, which is only present in samples fabricated using an Al sacrificial layer. Whilst it has not been possible to identify the chemical composition of this peak from reports in the literature, it is highly likely that this originates from residual Al based species that are chemically bound to the graphene surface, most likely at defects [144].

The data show that the use of a Cu sacrificial layer significantly reduces the concentration of defects and contaminants on the graphene surface, with a D/G ratio of 0.07±0.004 which is comparable to that of the as received graphene, which was previously extracted as 0.03±0.002. This suggests that unlike the Al sacrificial layer, Cu protects the surface from organic contaminants as a result of the photolithography process and that the ammonium persulphate etch process results

in negligible Cu residue on the graphene film at the conclusion of the fabrication process.

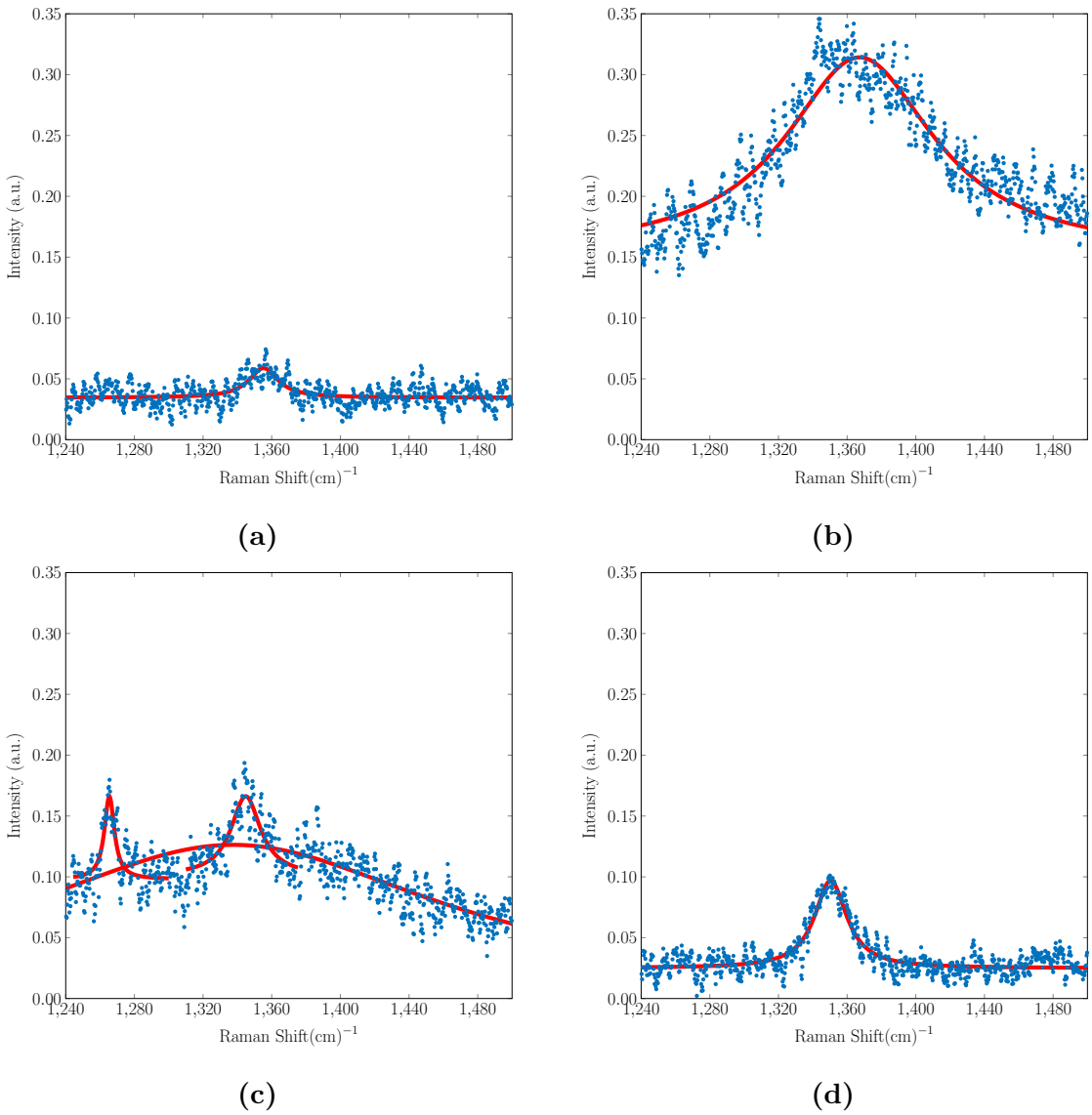


Figure 3.6: Isolated D peak intensity of a) as received films, b) devices fabricated with no sacrificial layer, c) Al sacrificial layer and d) Cu sacrificial layer.

The ratio of the 2D peak to G peak intensities is often used as a parameter to determine the number of graphene layers, with values in excess of 1 often being obtained for monolayer graphene films [145]. However it is also dependant on surface doping and as such can not be used as a definitive method. Nevertheless the FWHM of the 2D peak and shift of the centroid can be used to give a more complete picture of both the number of layers in the graphene and of the surface doping. The 2D/G ratio for the samples processed with an Al sacrificial layer is found to be

1.7±0.10, whilst for the Cu based samples it is 1.5±0.020. For samples fabricated with no sacrificial layer this is found to be reduced to a value of 0.73±0.030. The reduction in 2D/G peak ratio is therefore unexpected, however studies into Raman spectroscopic characterisation of graphene have found that the 2D/G ratio is also dependant on doping of the graphene layer by the substrate or surface contaminants. Previous reports in the literature have identified that for this reason it can be difficult to accurately determine the number of graphene layers when the film has been deposited on or transferred to an insulating substrate [143].

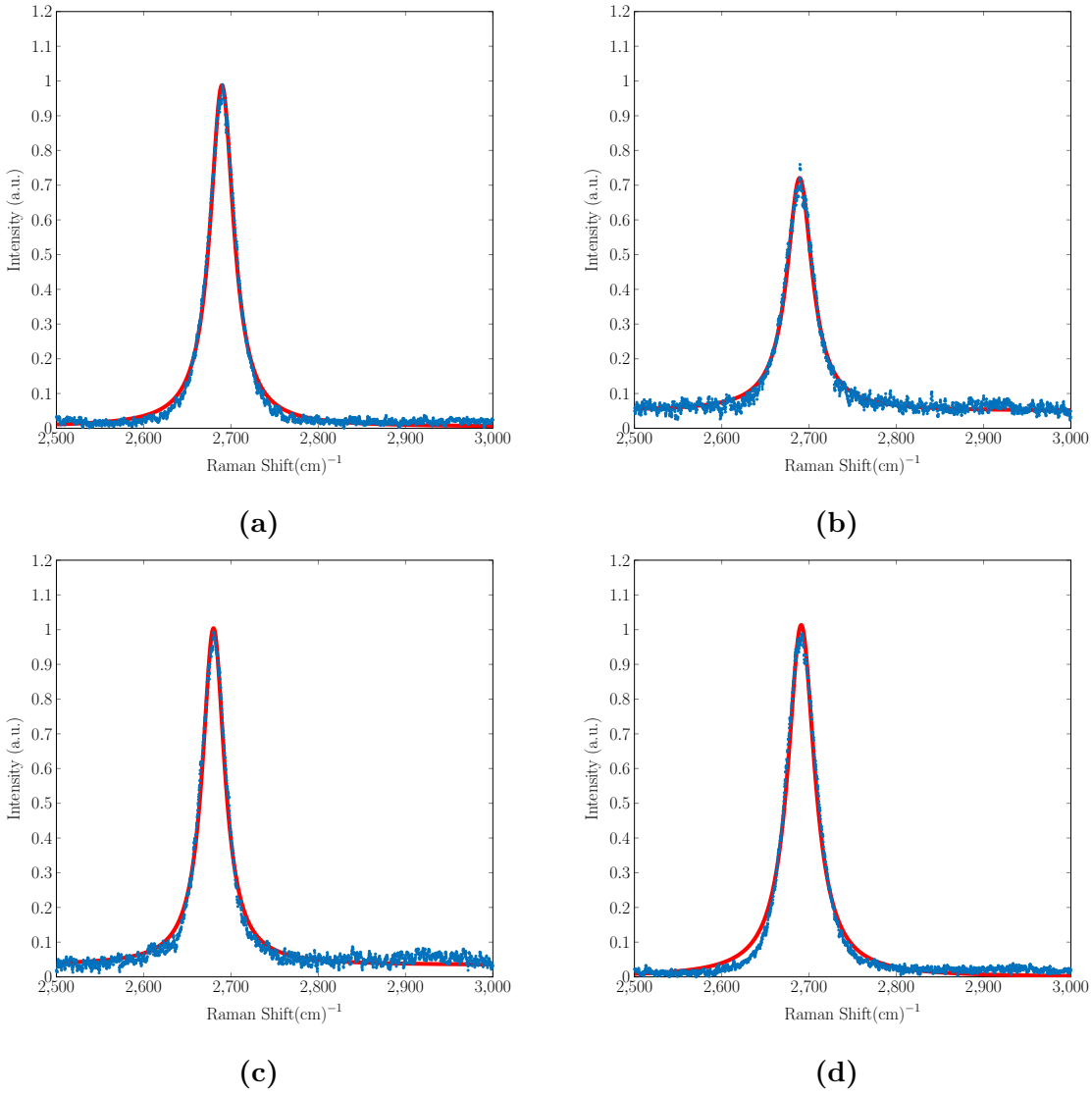


Figure 3.7: Isolated 2D peak intensity of a) as received films, b) devices fabricated with no sacrificial layer, c) Al sacrificial layer and d) Cu sacrificial layer.

Das *et al.* presented data which showed the impact of hole and electron doping on the 2D/G ratio, the result of which is shown in Figure 3.8. Correlating the

extracted shifts in 2D/G ratio to this data it is possible to estimate the shift in sheet dopant concentration. Using the 2D/G ratio of as received films (1.1±0.10) as a starting point, it is estimated that when using no sacrificial layer the carrier concentration is shifted by approximately 1.5×10^{13} cm^{-2} however it is unknown if the dopant type is n or p. This shift is reduced to approximately 1.0×10^{13} cm^{-2} when using an Al sacrificial layer and even further to 0.6×10^{13} cm^{-2} when using a Cu sacrificial layer. This suggests that the use of a Cu sacrificial layer reduces doping of the surface by approximately 60 % in comparison to devices fabricated using no sacrificial layer.

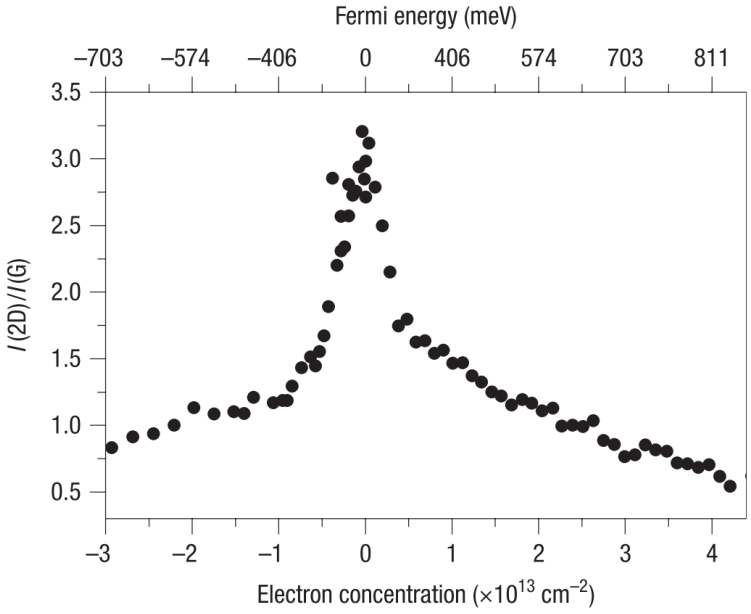


Figure 3.8: The influence of hole and electron doping on the 2D and G peak intensity of graphene films. *Image taken from [123].*

As the 2D/G ratio is heavily influenced by doping in the graphene film, the FWHM of the the 2D peaks can also be extracted in order to accurately determine the number of graphene layers. This metric has been shown to increase by a factor of two when the graphene transitions from single to bilayer [124]. The isolated 2D peak intensities are shown in Figure 3.7 with the FWHM of the peaks subsequently extracted from these data. The extracted FWHM for the as received graphene yields a value of 37.1±0.310 cm^{-1}. For graphene devices fabricated using standard lithography this value increases to 39.3±0.370 cm^{-1}, for Al sacrificial

layer it is 34.3±0.0300 cm^{-1} and for Cu sacrificial layer it remains the same at 37.6±0.0300 cm^{-1}. This suggests that the number of layers remains consistent across samples, with the variation in 2D/G ratio likely due to doping effects.

3.2.3 Electrical Characterisation

Electrical characterisation of devices was performed using a Keithley 4200 parameter analyser. In addition to fabricated devices, commercial devices purchased from the same graphene manufacturer were also characterised to allow for comparison of how the critical electronic properties of devices fabricated in this study compare with those of commercially available devices. All electrical measurements carried out in this section were performed across 20 devices on each of the nine wafers with five measurements taken per a device. For calculation of errors, numerical values taken from devices considered to be none functioning i.e. no electrical conduction between measured terminals were excluded. Two-terminal measurements were performed to determine the variation in sheet resistance of the graphene with process conditions on two-terminal test structures, the schematic of which is shown in Figure 3.9.

Figure 3.9: Schematic diagram of two terminal test structures with the blue area representing the graphene structure and gold representing the contacts.

The resulting current-voltage characteristics are shown in Figure 3.10. For devices fabricated using conventional lithography it can be seen that the channel is highly resistive in comparison to that of pristine graphene which typically has resistance values in the region of 100-200 $\Omega/\square$ [146]. This is likely due to contaminants on the surface and the non-continuous graphene film. Comparatively, devices fabricated using Al and Cu sacrificial layers have a significantly reduced resistance, although the I-V characteristics of the Al devices are shown to be non linear. This could be due to residues on the surface unintentionally doping the graphene layer [147, 148] or an unusually high contact resistance which is common in graphene devices fabricated using optical lithography [149].

This unintentional doping of the graphene layer is supported by the Raman spec-

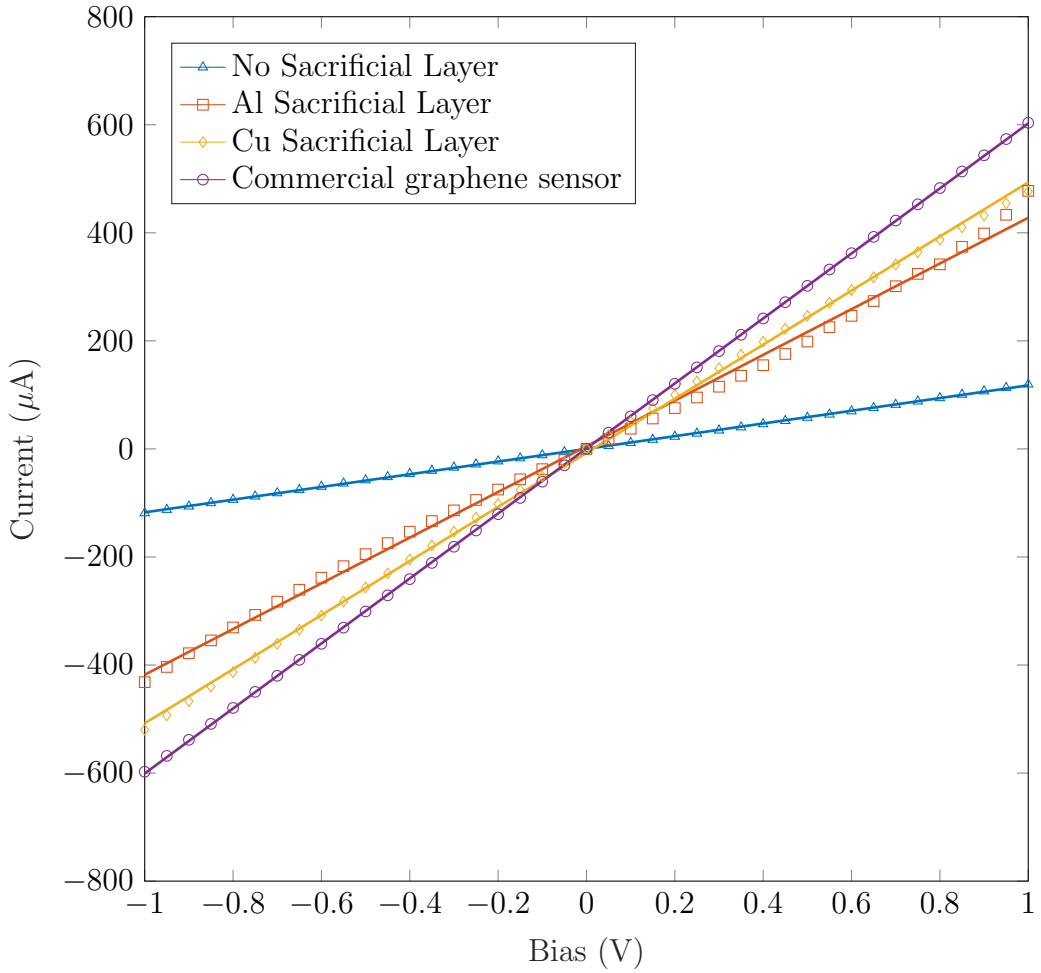


Figure 3.10: I-V characteristics of 4 terminal Hall structures of as received commercial devices, those fabricated using no sacrificial layer, Al sacrificial layer and Cu sacrificial layer. Linear fitting of data points is also exhibited in order to determine the linearity of the I-V characteristics.

troscopy results shown in Figure 3.5, with the increased defect density observed with the Al device results correlating with the suggestion that there is residue present on the graphene surface. Two terminal measurements alone however are not an accurate method for determining the sheet resistance across the graphene film as these measurements do not remove the influence of the contact resistance, with the total resistance given by Equation 3.1 [150]:

$$R_T = R_{Gr} + 2R_C \tag{3.1}$$

where R_{Gr} is the resistance of the graphene path of conduction between the two contacts shown in Figure 3.9 in Ohms and R_C the contact resistance in Ohms.

The Transfer Length Method (TLM) is a two probe technique which is commonly used to extract the contact resistance, sheet resistance and the transfer length characteristics of metal interfaces. A TLM test structure consists of a series of metal electrodes patterned in a resistor network, as can be seen in Figure 3.11a. These electrodes are separated by a varying channel length, L_{CH}, with the width (W) and length (L) of each contact remaining fixed. The total resistance is then measured between all adjacent metal contacts and can be described by Equation 3.2 [150].

$$R_T = R_{Sh}\left(\frac{L_{Ch}}{W}\right) + 2R_C \tag{3.2}$$

where R_{Sh} is the sheet resistance of the graphene film in $\Omega/\square$, L_{Ch} the channel length in μm and W the contact width in μm.

By plotting the measured total resistance as a function of the channel length, both R_C and R_{Sh} can be extracted from the resulting linear fit of the experimental data. An example of such a plot is shown in Figure 3.11. It can be seen that R_{Sh} can be extracted from the slope of the linear fit whilst R_C can be extracted from the y-intercept. However this method relies on the assumption that the sheet resistance underneath the contact is equal to that between contacts. In graphene this is not the case with carrier concentration in the film underneath the contact typically dependant on the type of contact metal used. This can lead to a different density of states underneath the metal contact in comparison to that of the channel areas resulting in a significant variation in sheet resistance [151]. This often results in non linear behaviour and low repeatability of measurements meaning an accurate value of sheet and contact resistance is difficult to quantify using this method.

TLM measurements were initially carried out on samples using both no sacrificial layer and Al sacrificial layer, however due to the low yield and damage to the TLM structures that occurred during processing, a representative dataset was unable to be extracted. TLM measurements shown were therefore extracted from samples

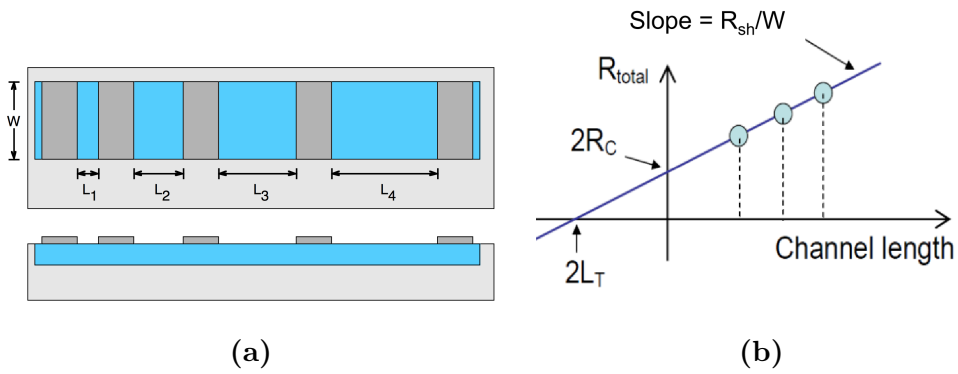


Figure 3.11: a) Schematic diagram of a typical TLM test structure and b) TLM plot of total resistance as a function of channel length. *Image taken from [85].*

fabricated using a Cu sacrificial layer only with measurements not consistent across each structure. As such the data set presented is represented of a single device only. These results however show the difficulty of using TLM structures to isolate the contact and sheet resistance in 2D materials. The data in Figure 3.12 show the resulting TLM plot from measurements on Cu sacrificial layer devices. The non-linearity of the extracted total resistance as a function of channel length is evident from these results. In addition to the issues with TLM measurements in 2D materials described previously, such as the different density of states underneath the contact area, the non-uniform quality of the graphene layer across the channel described in previous sections can also contribute to this non-linearity.

Nonetheless by excluding the data point at 40 μm as an outlier there is a linear region present between 20 μm to 45 μm which allows for extraction of contact resistance and sheet resistance. Extrapolation of this line gives a value of 29 Ω for contact resistance and 1.63 k$\Omega/\square$ for the sheet resistance. Initially, the sheet resistance value extracted appears accurate however the contact resistance value extracted from this is lower than expected although it has been seen to be achieved in Ni electrodes on graphene previously [151]. The small number of data points available for extrapolation in the linear region however makes it difficult to assess the validity of these results. This also represents an issue when it comes to reproducibility of results, with extracted values varying significantly across a wafer.

Due to the difficulties encountered in separating the contact resistance from sheet

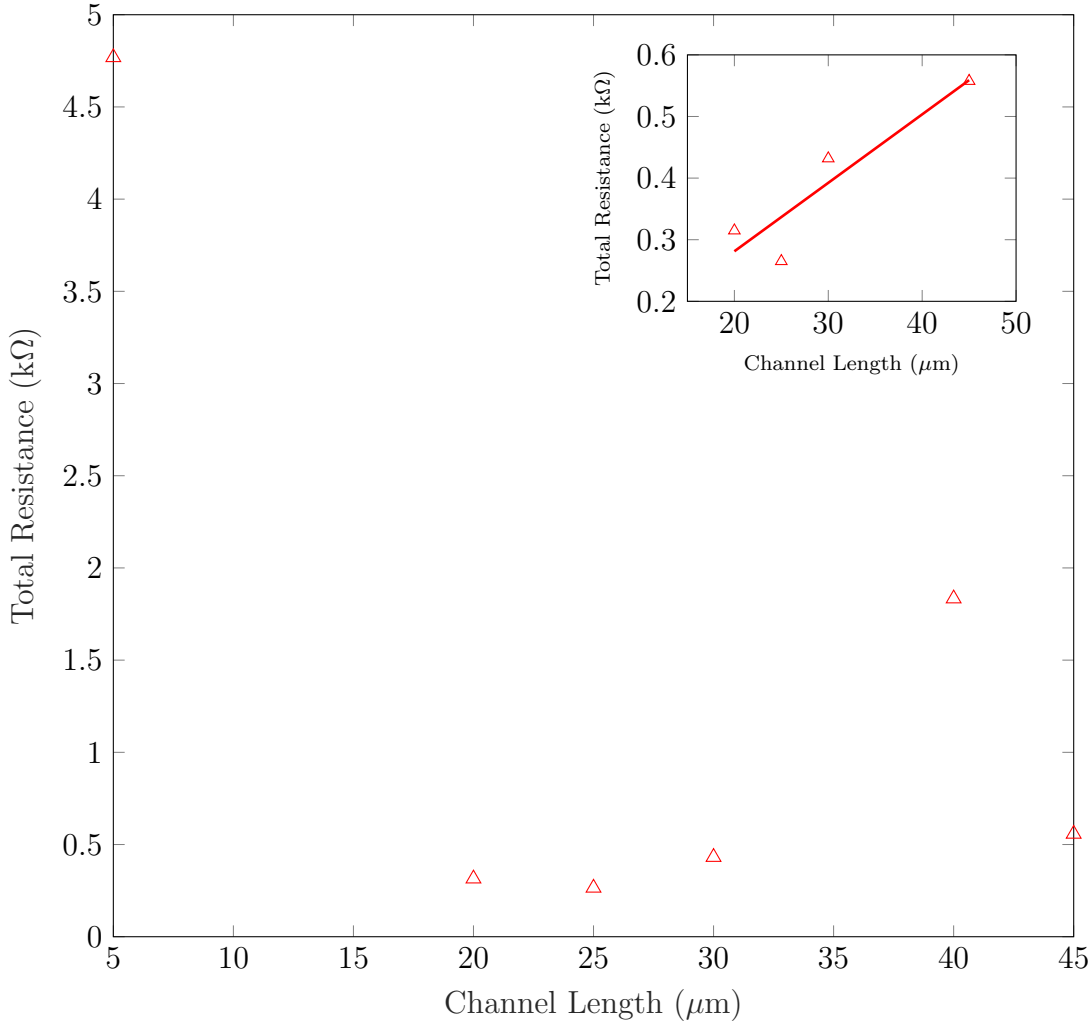


Figure 3.12: TLM plot of devices fabricated using a Cu sacrificial layer showing total resistance as a function of channel length with the linear region shown inset.

resistance, van der Pauw (VDP) structures were employed to extract sheet resistance values. Whilst this doesn't allow for separation of contact resistance from the sheet resistance, this method minimises the influence of metal contacts to the measured resistance value allowing for a more accurate determination of overall sheet resistance and any electrical parameters extracted. The resulting sheet resistances extracted using this method are summarised in Table 3.2 in the following section.

Hall Effect Measurements

Hall measurements were performed on fabricated devices in order to extract critical electrical parameters including sheet carrier density and carrier mobility. They also give a good indication of how the sensor performs in comparison to commercial devices. Schematic diagrams of the hall structures used to perform these measurements are shown in Figure 3.13.

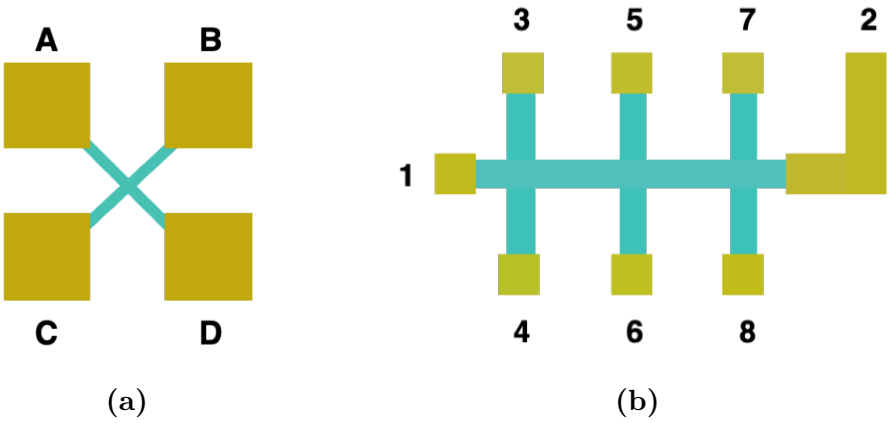


Figure 3.13: Schematic diagrams of a) four terminal Hall structures and b) eight terminal Hall structures used in this study with the blue areas representing the graphene structures and the gold areas representing the metal contacts.

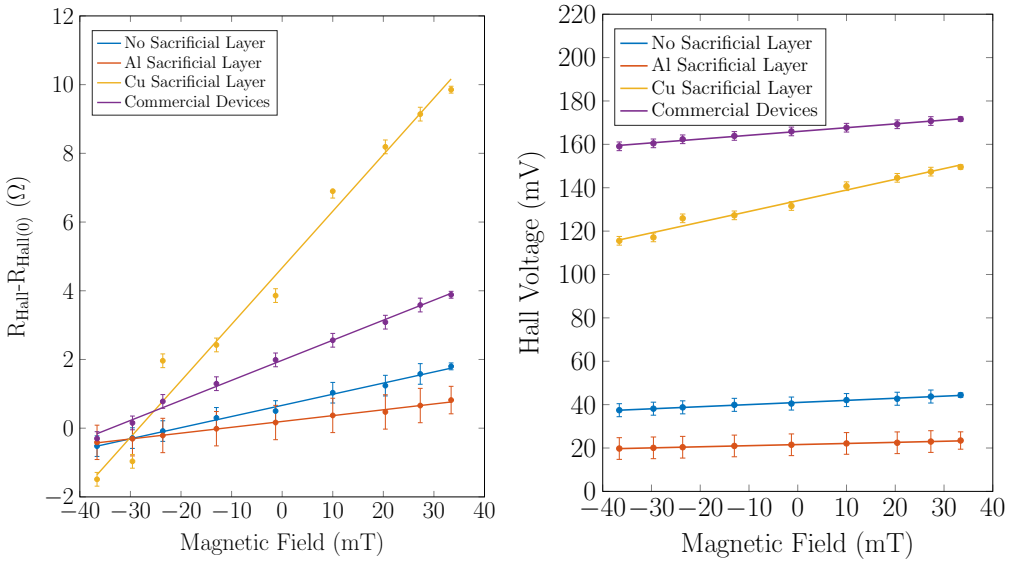
The data in Figure 3.14a show the normalised Hall resistance (R_{Hall}-$R_{Hall(0)}$) as a function of magnetic field for devices fabricated using no sacrificial layer, Al sacrificial layer and Cu sacrificial layer with a fixed current of 3 mA. The sensors are shown to demonstrate highly linear behaviour with an R^2 value of > 0.99, comparable to graphene devices reported in the literature and even that of commercially available devices [152]. The Hall resistance is normalised as a function of the Hall resistance at zero field to demonstrate the impact of offset shifting on device characteristics, with devices fabricated using a Cu sacrificial layer showing the highest offset shifting. Offset shifting at zero applied field is the potential difference exhibited in the graphene film with electric current flow in the absence of an external magnetic field. This offset is undesirable as it limits the ability of the sensor to detect low magnetic fields. The current related sensitivity can additionally be extracted from the gradient of Figure 3.14b which show the Hall

voltage as a function of magnetic field. It is defined as the ratio of the Hall voltage to the multiple of magnetic field and current bias, given in Equation 3.3:

$$S_I = \frac{V_H}{BI} \tag{3.3}$$

As shown by the data in Figure 3.14b, devices fabricated using both no sacrificial layer and an Al sacrificial layer are shown to exhibit a similar magnitude of response in the region of 20–40 mV, although devices fabricated using no sacrificial layer have increased current related sensitivity (32.4±6.40 V/AT in comparison to 17.0±5.90 V/AT for devices fabricated using an Al sacrificial layer). Comparatively, devices fabricated using a Cu sacrificial layer exhibit a significantly increased magnitude of response, with a current related sensitivity of 165±16.5 V/AT. Extracted current related sensitivities for devices fabricated using the Cu sacrificial layer are also shown to be increased over that of commercially available CVD graphene devices tested in this study (58.0±8.70 V/AT) although they still remain lower than that of graphene devices previously reported in the literature [78, 153, 154]. These devices have reported sensitivities of >1000 V/AT however this is largely due to external biasing of the graphene film to allow for Dirac point operation. As such it is expected that through external gate biasing the sensitivity limit of devices fabricated in this study can be explored further. Comparatively, Hall effect devices available commercially are typically limited to sensitivities of <100 V/AT [155].

Offset shifting at zero applied field is exhibited in Figure 3.14b, most notably in devices fabricated with no sacrificial layer with an offset voltage of approximately 39±1.2 mV, reduced to 21±0.63 mV when using an Al sacrificial layer. However this is increased to 120±2.60 mV when using a Cu sacrificial layer and even further to 160±1.80 mV for commercial devices. This could be attributed to the increased current related sensitivity exhibited in these devices. As such it is important to use these parameters to extract the offset equivalent magnetic field for a more accurate comparison of device performance. The offset equivalent magnetic field, defined as the ratio of offset voltage to absolute sensitivity can be determined using:



(a) **(b)**

Figure 3.14: Hall effect measurements showing a) Hall resistance normalised by the offset and b) Hall voltage as a function of magnetic field with a fixed current bias of 3 mA for commercial devices, devices fabricated using no sacrificial layer, Cu sacrificial layer and Al sacrificial layer. Linear fitting of data points is also exhibited in order to determine the linearity of the Hall voltage as a function of magnetic field.

$$S_A = \frac{V_H}{B} \tag{3.4}$$

$$B_{off} = \frac{V_{off}}{S_A} \tag{3.5}$$

where B_{off} is the offset equivalent magnetic field in Tesla, V_{off} the offset voltage in Volts and S_A the absolute sensitivity of the Hall structure in V/T.

This is a critical parameter to consider as reducing the offset equivalent magnetic field leads to improvements in device sensitivity and reproducibility of results [156]. This yields values of 0.4±0.01 T for devices fabricated using no sacrificial layer and Al sacrificial layer. Both fabrication methods are shown to be comparable with regards to magnetic field offset, with the result uncertainty being too large to determine whether devices with lower current related sensitivity (those fabricated using Al sacrificial layer) do in fact exhibit a larger offset equivalent magnetic field.

In order to investigate this further, samples fabricated using a Cu sacrificial layer also need to be taken into account.

The offset equivalent magnetic field is found to be reduced by approximately 50 % to 0.2±0.01 T for samples fabricated using a Cu sacrificial layer despite having a larger offset voltage, largely due to the higher current related sensitivity. Commercial devices however exhibit an anomalously high offset magnetic field of 0.9±0.02 T. The origin of this offset is not evidentially clear however it is often described in literature as being a direct result of contact misalignment [157]. In order to investigate this further it is pertinent to consider other critical electronic properties of the fabricated graphene films. These can also be extracted from the data in Figure 3.14a with the resultant parameters shown in Table 3.2.

Both the sheet carrier density and carrier mobility can be further extracted from Figure 3.14b according to Equations 3.6 and 3.7:

$$\mu = \frac{R_H}{R_{SH}} \tag{3.6}$$

where R_H is the Hall coefficient described in Section 2.6.2 in m^2/C^{-1} which can be extracted by converting the current related sensitivity from mks to cgs units ($\times 10^4$) and R_{SH} the sheet resistance in $\Omega/\square$.

$$R_H = \frac{1}{ne} \tag{3.7}$$

where e is the charge of a proton (1.6×10^{-19} C^{-1}).

These data are summarised in Table 3.2 alongside the sheet resistance data extracted using the VDP method described previously. A key trend which can be seen from these data is that higher carrier mobility and reduced sheet carrier density results in an increase in the current related sensitivity of devices. The sheet resistance is also reduced in devices with higher current related sensitivity. It can be seen that this occurs when devices are fabricated using a Cu sacrificial layer. The reduced carrier mobility exhibited when fabricating devices with no sacrificial layer and an Al sacrificial layer suggests that these processes have introduced scattering sites into the graphene film, limiting mobility.

Table 3.2: Electrical properties of as received commercial devices and those fabricated using no sacrificial layer, Al sacrificial layer and Cu sacrificial layer extracted from the data in Figure 3.14a

	R_{SH} ($\Omega/\square$)	n_s (cm^{-2})	S_I (V/AT)	μ ($cm^2V^{-1}s^{-1}$)	Yield %
No sacrificial layer	$1.1\pm0.22\times10^3$	$1.9\pm0.38\times10^{13}$	32.4 ± 6.40	$1.2\pm0.24\times10^3$	12
Al sacrificial layer	$1.3\pm0.46\times10^3$	$7.0\pm2.5\times10^{13}$	17.0 ± 5.90	$1.0\pm0.36\times10^3$	25
Cu sacrificial layer	$0.80\pm0.10\times10^3$	$3.8\pm0.38\times10^{12}$	165 ± 16.5	$2.1\pm0.23\times10^3$	82
Commercial devices	$1.2\pm0.18\times10^3$	$1.0\pm0.15\times10^{13}$	58.0 ± 8.70	$1.3\pm0.19\times10^3$	75

Remarkably, fabrication of devices through the use of a Cu sacrificial layer is shown to provide not only an improvement in electrical characteristics over those fabricated with no sacrificial layer and Al sacrificial layer but over those fabricated commercially. The most notable difference in results is the dramatic increase in device yield when using a Cu sacrificial layer - increasing from just 12 % when using no sacrificial layer to 82 %. This is particularly advantageous in the use of wafer scale processing as it significantly reduces cost of the final sensor. The use of an Al sacrificial layer does slightly increase yield, relative to devices fabricated with no sacrificial layer, to approximately 25 % however this is still not high enough for wafer scale processing using this technique viable. It should be noted that, in this study a working device is defined as a Hall sensor that produces a potential difference across two terminals when a current bias is applied to the adjacent terminals and is also responsive to changes in magnetic field.

In addition to the significant increase in yield, a critical parameter to consider when fabricating devices is the reproducibility. In graphene processing this is a particular issue due to the sensitivity of the graphene film to contaminants introduced during lithographic processing. The variability of devices fabricated has been quantified by extracting the sheet resistance of devices across each 1 cm$\times$1 cm die. The data in Figure 3.15 show a box and whisker plot of device sheet resistances for devices fabricated using Cu sacrificial layer, Al sacrificial layer and no sacrificial layer. From these data it can be seen that devices fabricated using Al sacrificial layer exhibit the largest variability (approximately 40 % spread) in characteristics across a wafer whereas the variability across Cu sacrificial layer devices

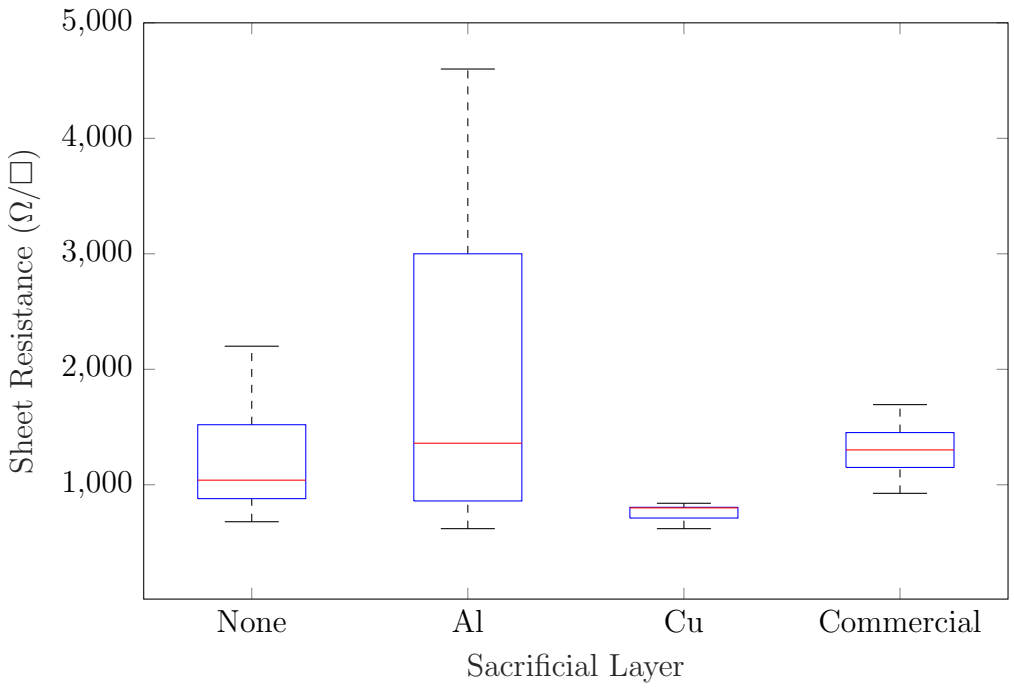


Figure 3.15: Variability of sheet resistance across a wafer for devices fabricated using no sacrificial layer, Al sacrificial layer, Cu sacrificial layer and as received commercial devices.

is significantly reduced to as low as 10 %. The variability of devices fabricated using a Cu sacrificial layer is also shown to be slightly reduced to over that of commercially available graphene devices which exhibit a spread in characteristics of 15 %. This corresponds to the data previously shown that use of a Cu sacrificial layer improves protection of the surface during fabrication and reduces the introduction of dopants during these processes.

Overall both the surface analysis and electrical characterisation of graphene devices fabricated in this section strongly suggest that the use of a Cu sacrificial layer offers improved surface quality of the graphene film and enhances the electrical characteristics of the final device. Whilst devices fabricated using a Cu sacrificial layer are found to be comparable to that of commercially available bulk semiconductor and graphene devices, the current related sensitivity and mobilities observed remain lower than that of some graphene devices described in literature. Many of these devices however utilise external gate biasing for Dirac point operation, a concept which will be explored in the following section.

3.3 Dirac Point Operation of Graphene Devices

Graphene's band structure leads to many of the exceptional properties described previously, with a key area of interest being the K and K' points at which the conduction and valence bands meet (also commonly referred to as the π and π^* bands). The point at which these meet is more commonly known as the Dirac point, named due to the relativistic behaviour of charge carriers at this point. Ideally the Fermi level would sit at this point, however many of the fabrication methods described previously result in unintentional doping of the graphene, which leads to shifting of the Fermi level away from this point. It is however possible to apply a bias through a separate gate contact in graphene devices in order to shift the Fermi level back towards the Dirac point. This ultimately allows for control over the sheet carrier density in the graphene sheet. This is particularly advantageous with regards to Hall sensing as reduction in sheet carrier density allows for optimisation of device sensitivity which can also be individually tuned for each device. The Dirac point is typically found by measuring conductivity as a function of gate bias - the point at which the conductivity is lowest is known as the Dirac voltage (i.e. the bias that needs to be applied to shift the Fermi level to the Dirac point). For pristine graphene at 0 K this point lies at a bias of 0 V as there will have been no shifting in the position of the Fermi level which sits at the point where the conduction and valence bands meet (as in the upper diagram in Figure 3.16). As such, the shift in Dirac voltage can also be used as a metric to determine the impact of fabrication and synthesis methods on the unintentional charge density in the graphene film as well as being used as a tool for optimising electronic and transport properties.

The Dirac point of both fabricated devices and commercial graphene devices were extracted by applying a fixed voltage bias between the two contacts and applying a voltage sweep to the back gate contact. The subsequent current flow between the drain and source contacts is plotted as a function of gate bias, as shown in Figure 3.17. The gate bias at which the drain current reaches a minimum corresponds to the Dirac point of the graphene film. For as received commercial devices this

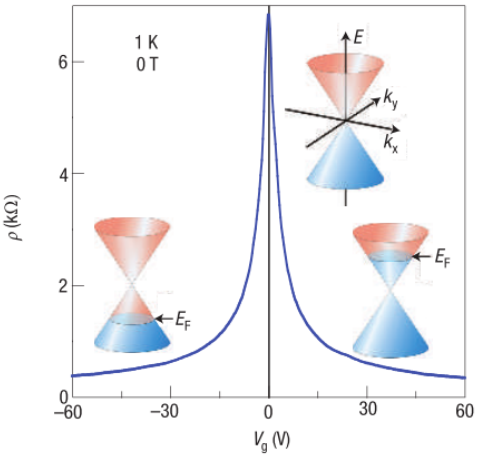


Figure 3.16: Change in resistivity with changing gate voltage with the representative shift in Fermi level shown in the insetted diagrams. *Image taken from [129].*

is shown to be at 38±1.0 V, and for devices fabricated using Cu sacrificial layer method this is shown to be at 39±1.0 V.

The comparable Dirac point suggests that devices fabricated utilising a Cu sacrificial layer do not appear to cause further contamination to the graphene surface in comparison to commercial devices produced by the manufacturer of the graphene film. This bias is however a significant shift from the 0 V Dirac point observed in pristine graphene. There are a number of points to consider as to the origin of this shift. Firstly, damage caused to the graphene film during the growth and wet transfer process from growth catalyst to substrate. This is a strong possibility given the comparable Dirac point values observed between the two fabrication methods. Secondly, the oxide layer between the substrate and graphene film acts as an insulating barrier and thus the true biasing point may be closer to neutral than observed. This is due to the fact that the applied gate voltage, V_{GS}=V_{OX}+V_C where V_{OX} and V_C are the voltage drop across the oxide layer and semiconductor respectively [158]. The voltage drop across the oxide layer can be further described as V_{OX}=E_{OX}/t_{OX} where E_{OX} is the electric field in the oxide and t_{OX} the oxide thickness.

Whilst the shifting of the Dirac point away from the 0 V bias region is often cited as an assessment of surface doping, the width of the Dirac point peak has also been used as a comparative factor to assess the quality of the graphene layer.

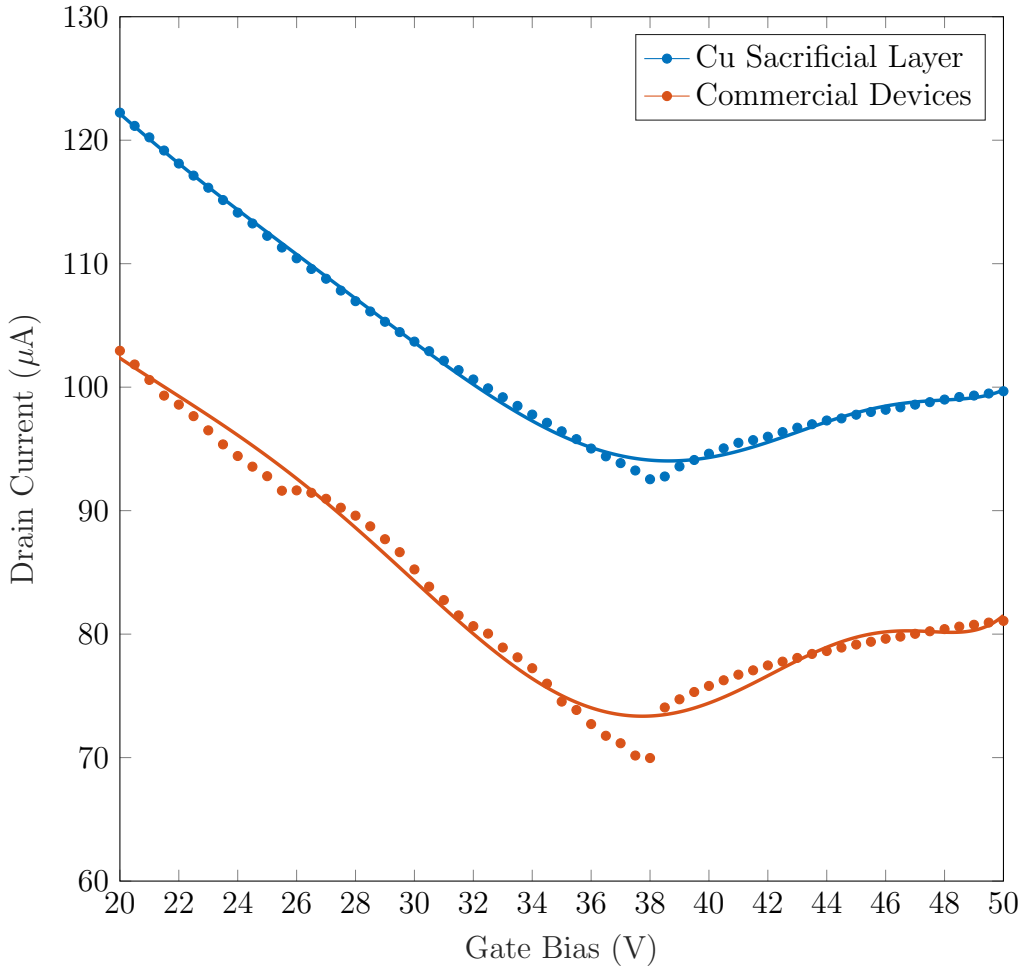
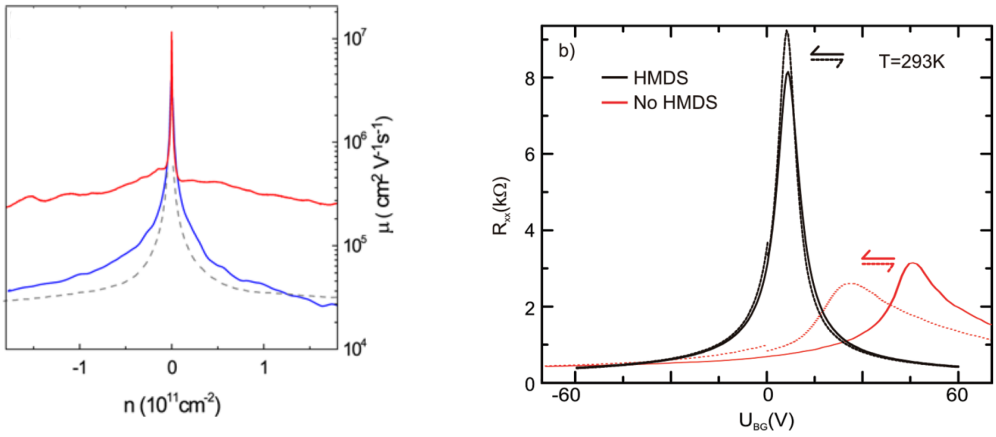


Figure 3.17: Drain current as a function of gate bias for devices fabricated using a Cu sacrificial layer and as received commercial devices. Polynomial curve fitting was applied for extraction of the Dirac point.

Bolotin *et al.* observed a reduction in the width of the Dirac point by a factor of 20 upon current-induced heating to a width of just 2.0×10^{10} cm^{-2} reflecting a vast improvement in graphene surface quality [45]. The data from this study can be observed in Figure 3.18a showing device resistivity as a function of gate voltage before and after current annealing (current-induced heating of the graphene film to anneal the film). It is hypothesised that this reduction in Dirac point width stems from changes in charge inhomogeneity in the sample.

Additionally Lafkioti *et al.* observed a reduction in hysteresis around the Dirac point when using a hydrophobic substrate underneath the graphene film, attributed to a reduction in dipolar adsorbates between the substrate and graphene surface [159]. The data shown in Figure 3.18 indicate that analysis of both the



(a) **(b)**

Figure 3.18: Impact of surface quality on width and hysteresis of Dirac curve with a) Resistivity as a function of gate voltage for devices prior to (blue) and after (red) current annealing and b) Hall resistance as a function of gate voltage for graphene on hexamethyldisilazane (HMDS) (black) and graphene on Si/SiO_2 (red) shown. *Images taken from [45] and [159] respectively.*

width of the extracted Dirac point and any hysteresis will allow a more complete determination of the quality of the graphene layers.

Hysteresis measurements were carried out on devices fabricated using no sacrificial layer, Al sacrificial layer, Cu sacrificial layer and commercially fabricated devices. These data were extracted by performing a forward gate sweep from 0 V to 50 V and a reverse gate sweep from 50 V to 0 V using a scan rate of 0.20 Vs^{-1}. The resulting data are shown in Figure 3.19. The Dirac point is not as prominent on these sweeps owing to gate biasing carried out without the use of an Ohmic contact on the underside of the substrate. As such it is difficult to accurately estimate the width of the Dirac point. Nevertheless a shift in the Dirac point can be observed in Figures 3.19a and 3.19d.

This shift is most significant in the commercial devices with the observed Dirac point shifting from a gate bias of 38±1.0 V on the forward sweep to 47±1.0 V on the reverse sweep. Whilst the nature of the fabrication process for these devices is unknown it would suggest that there is significant moisture adsorption to the surface of the graphene film. This could additionally be attributed to the

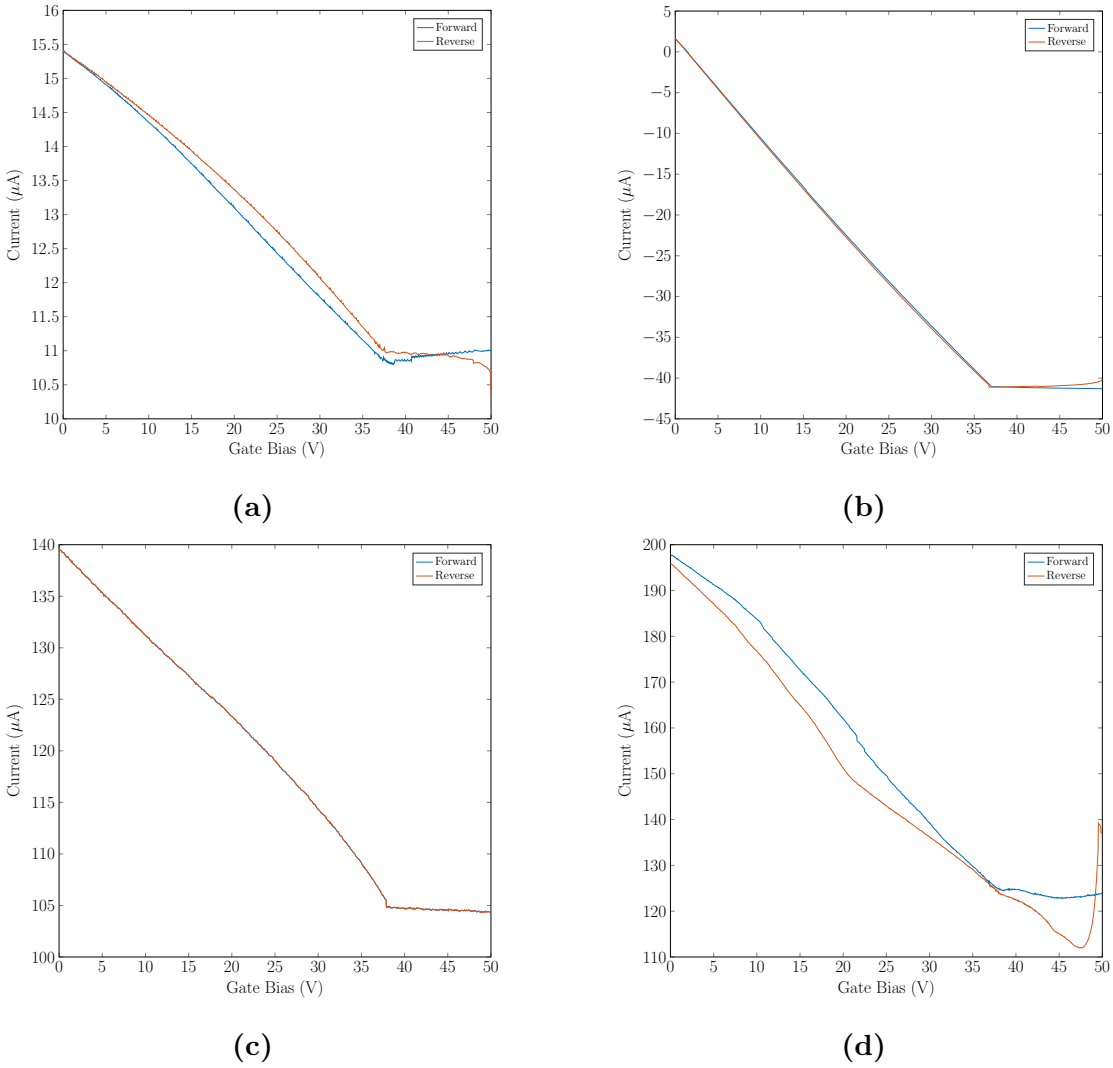


Figure 3.19: Hysteresis measurements of a) devices fabricated using no sacrificial layer, b) devices fabricated using an Al sacrificial layer, c) devices fabricated using a Cu sacrificial layer and d) commercial graphene devices.

method of storage of these devices with graphene die received in a gel pack. As the graphene die offered through this commercial supplier are unprotected and unpackaged this has the potential to introduce significant contamination to the graphene surface during storage. Gel packaging is a standard process in the semiconductor industry to allow for damage free transport of devices. The polymers present in this packaging however could potentially dope the graphene surface in devices where the surface is unprotected, as is the case for commercial devices used in this study.

There is also a small amount of hysteresis observed in devices fabricated using

no sacrificial layer (Figure 3.19a) however this is shown to be negligible in those fabricated using an Al sacrificial layer (Figure 3.19b) and removed completely when using a Cu sacrificial layer (Figure 3.19c). This strongly suggests that the surface quality of devices fabricated using a Cu sacrificial layer is significantly improved over those with no sacrificial layer and also offers improvements in comparison to an Al sacrificial layer. This corresponds with the outcomes of the surface analysis and electrical characterisation presented in previous sections which show that the use of a Cu sacrificial layer reduces surface doping by up to 60 % and exhibits improved electrical characteristics (with sheet carrier concentration reduced from $1.9\pm0.10\times10^{13}$ cm^{-2} when using no sacrificial layer to $3.8\pm0.11\times10^{12}$ cm^{-2} when using a Cu sacrificial layer).

Whilst extraction of the Dirac point is important for analysis of the surface quality of the graphene film it is also important to consider how knowledge of where this point lies can be utilised to optimise the electronic and transport properties of the graphene film. This will be considered in the following section with data analysed around the previously extracted Dirac points.

3.3.1 Gated Hall Measurements

Gated Hall measurements were performed by applying a range of external voltage bias to the back gate contact. Standard Hall measurements were then performed on devices at bias voltages around the Dirac voltage extracted from the data in Figure 3.17. A schematic diagram of the experimental setup is shown in Figure 3.20. Measurements were performed across commercially available graphene devices and those fabricated in this study using a Cu sacrificial layer. Gated Hall measurements were not possible on devices fabricated without a sacrificial layer or an Al sacrificial layer due to the low yield of functional devices, as described in Section 3.2.3. Nonetheless, the main focus of this section are the results of an investigation of the performance and electrical characteristics of devices fabricated using a Cu sacrificial layer as these will form the basis of the work demonstrated in subsequent chapters.

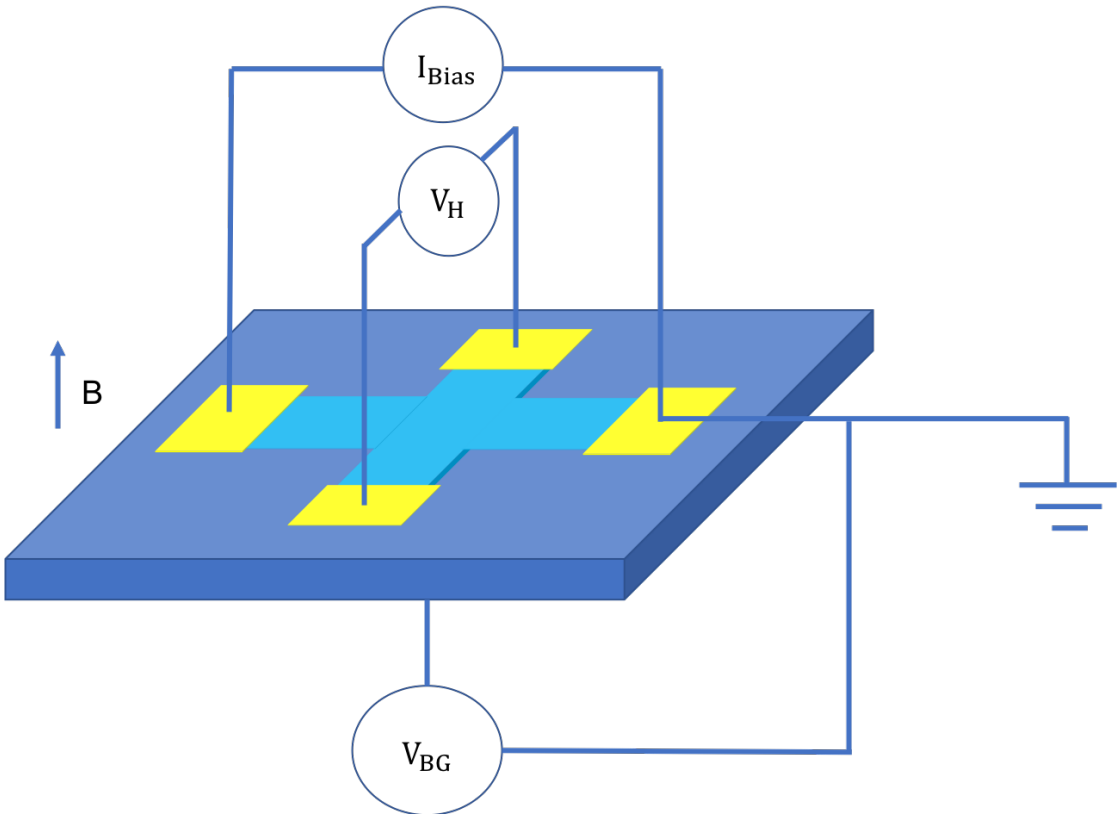


Figure 3.20: Schematic diagram of setup for gated hall measurements, showing the gate source bias (V_{BG}), the applied current bias (I_{BIAS}, the magnetic field (B) and the generated Hall voltage (V_H).

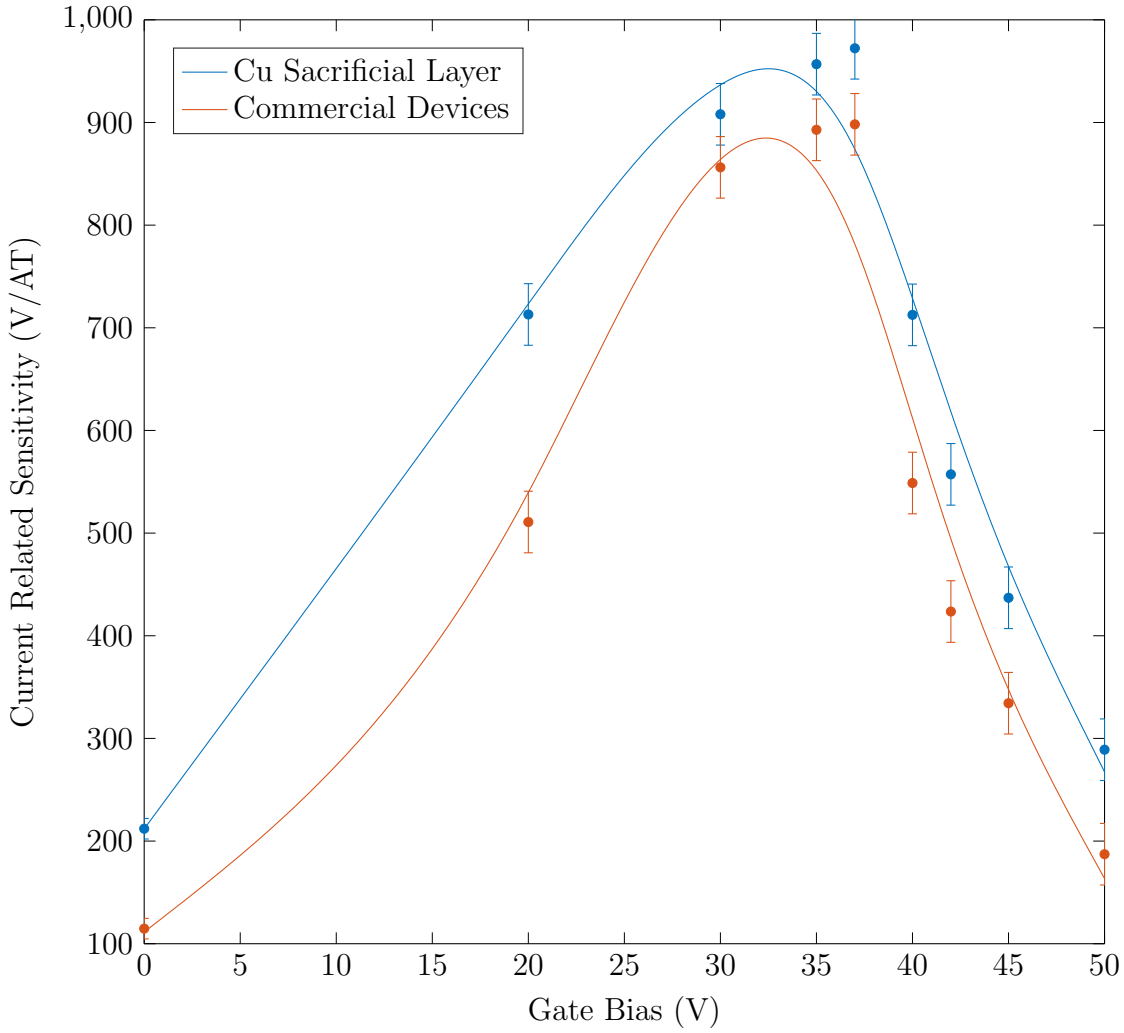


Figure 3.21: Current related sensitivity as a function of gate bias for devices fabricated using a Cu sacrificial layer and as received commercial devices. Polynomial curve fitting was applied for extraction of the Dirac point.

The data in Figure 3.21 show the current related sensitivity of commercial devices and those fabricated in this study using a Cu sacrificial layer as a function of gate bias. Initially considering the sensitivity of commercial devices, it is shown that the sensitivity increases up to a gate bias of 37±1.0 V, reaching a peak of 898±27.0 V/AT after which the sensitivity decreases, following a Gaussian trend. In devices fabricated using a Cu sacrificial layer in this study, the peak sensitivity is shown to correspond to a gate bias of 37±1.0 V with a magnitude of 972±19.0 V/AT. These trends correspond to the known behaviour of graphene around the Dirac point and also correspond to that of the Dirac voltage extracted from the two terminal measurements shown in Figure 3.17. It is notable that the

current related sensitivity for a gate bias of 0 V is higher than that extracted initially from standard Hall measurements in Figure 3.14 for both commercial devices and those fabricated using a Cu sacrificial layer. This usually indicates that there is a residual parasitic voltage present in the measurement setup to cause an increase in current related sensitivity compared to unbiased devices, potentially caused by grounding issues [160].

The current related sensitivity extracted at the Dirac point of Cu sacrificial layer devices (972±19.0 V/AT) brings the device sensitivity closer in line to that of CVD graphene Hall devices presented in literature [78,153] with maximum values in the region of 2000 V/AT typically seen. This is a vast improvement on the sensitivity extracted without gate biasing, with an increase of 9 times the un-gated value. This can potentially be optimised in future device iterations through fabrication of an Ohmic back contact for biasing and utilising higher quality graphene films through 'in house' CVD growth. Having the capability to grow CVD graphene films 'in house' would allow for controllability over the process parameters and chemicals used and additionally avoid the need for unnecessary transportation of graphene films outside of a controlled environment. Nevertheless this value is comparable to 2DEG Hall effect sensors in literature and significantly exceeds commonly used semiconducting Hall effect devices as can be seen from the data in Table 3.3.

Table 3.3: Current related sensitivity of commonly used Hall effect materials. [21,155].

Material	Current Related Sensitivity (V/AT)
2DEG	900-1200
InAs	10-100
GaAs	100-280

Critical electronic properties such as the sheet carrier density and carrier mobility can be extracted from the data in Figure 3.21 to determine the dependance on gate bias and investigate if the trends match those of the current related sensitivity. The resulting properties as a function of gate bias are shown in Figure 3.22 for commercial graphene devices. It can be seen that the sheet carrier density reaches a minimum of $7.0\pm0.2\times10^{11}$ cm^{-2} at a gate bias of 37±1.0 V, with carrier mobility also reaching a maximum of $3.1\pm0.10\times10^{3}$ $cm^2V^{-1}s^{-1}$ at the same point. This

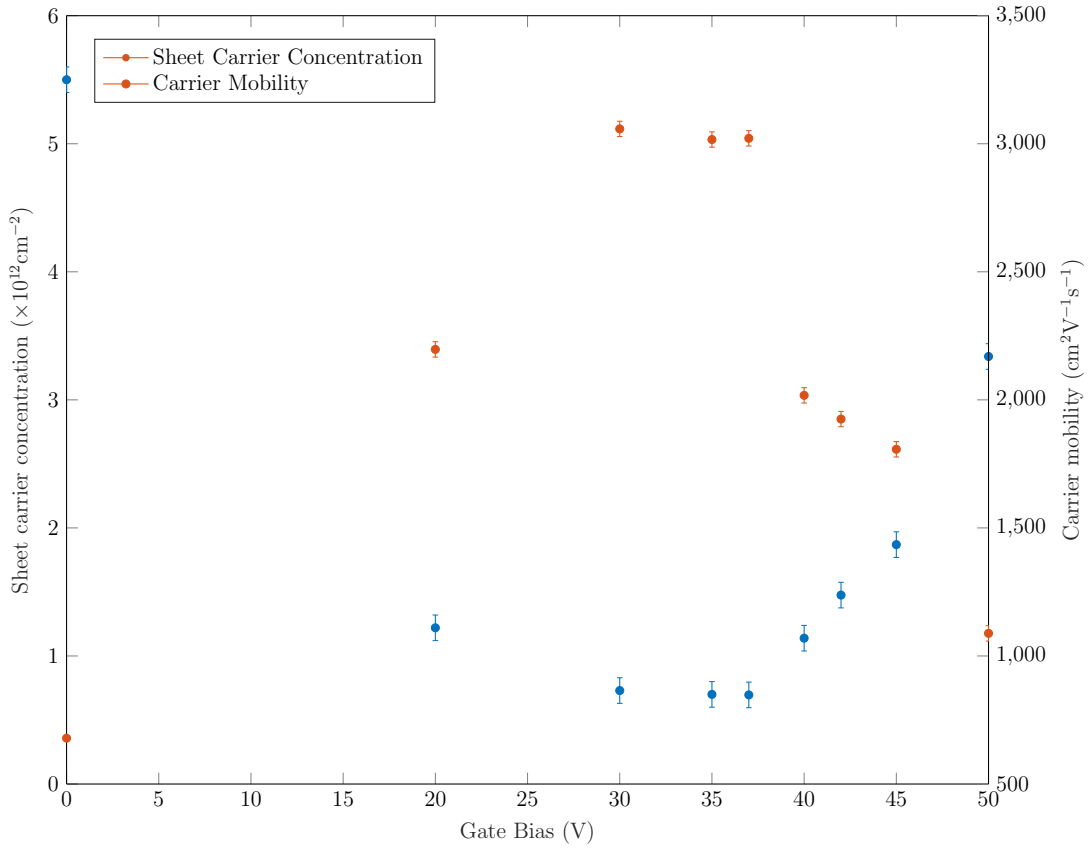


Figure 3.22: Sheet carrier density and carrier mobility as a function of gate bias for commercial devices.

corresponds to the peak current related sensitivity and is in good agreement with the known behaviour around the Dirac point.

The data in Figure 3.23 show these electronic properties as a function of gate bias for devices fabricated using a Cu sacrificial layer, similar to the commercial devices. These demonstrate a similar trend to that of the current related sensitivity, with the sheet carrier density reaching a minimum of $6.4\pm0.2\times10^{11}$ cm^{-2} at a gate bias of 37 ± 1.0 V and carrier mobility reaching a maximum of $3.7\pm0.11\times10^{3}$ cm^{2}V^{-1}s^{-1} at the same point. The properties extracted from devices using a Cu sacrificial layer are exhibiting a slight improvement of approximately 8.0 % in comparison to those quoted for commercially available devices from the same graphene manufacturer.

Considering the sheet carrier density, values extracted from CVD graphene in literature typically lie in the region of 10^{11}-10^{13} cm^{-2} [47]. The values extracted from the Dirac point of devices fabricated in this study are in the region of

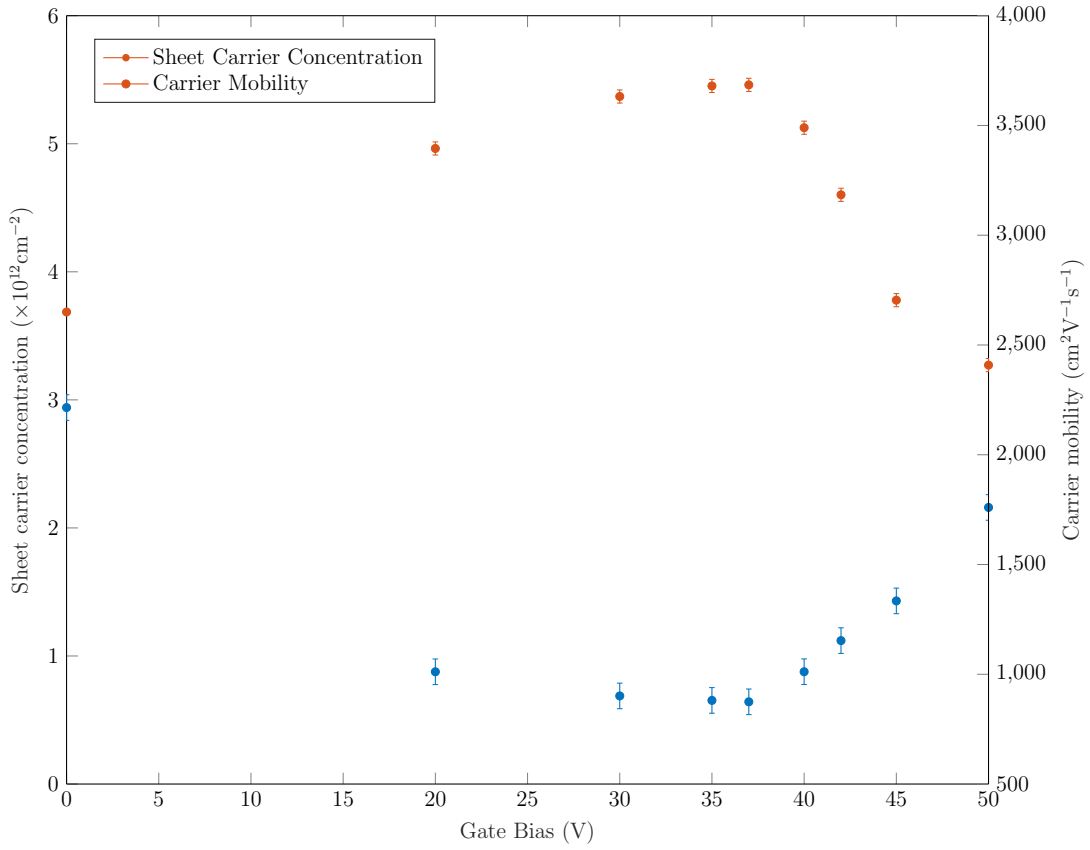


Figure 3.23: Sheet carrier density and carrier mobility as a function of gate bias for devices fabricated using a Cu sacrificial layer.

6.0×10^{11} cm^{-2} which corresponds with the lower end of values extracted from CVD graphene. Mobility values seen in high quality CVD graphene films also typically lie in the range of 3.0-4.0$\times10^3$ cm^{2}V^{-1}s^{-1} [161] with carrier mobility extracted from devices in this study around the Dirac point also falling within this range.

It is evident from the data in Figures 3.21 - 3.23 that even in devices where the Dirac point has been significantly shifted through doping and damage to the graphene surface, the electronic properties can be optimised significantly through external biasing to shift the Fermi level back towards this charge neutrality point. In order to implement this method into applications where long term stability of characteristics is required, the bias at which this occurs is also required to remain stable over time. This means the graphene surface of the active device needs to be sufficiently protected to prevent the introduction of further contaminants

and dopants to the surface which could result in further shifting of the Dirac point.

3.4 Packaging of Graphene Devices

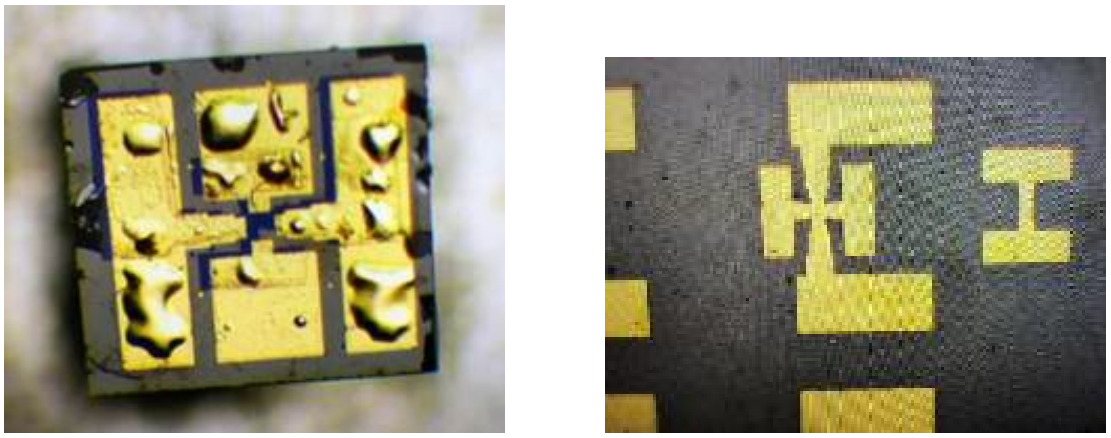
Appropriate packaging is critical when implementing devices into real world applications, presenting some additional challenges when considering the packaging of graphene devices. It is important that the packaging design prevents moisture adsorption to avoid contamination of the graphene surface and ensure that the device characteristics remain stable over time with negligible deterioration. This is particularly important in aerospace applications where low failure rates and long lifetimes are required for certification [162].

There are two key elements that need to be considered during the processing of graphene devices: the die attach and wire bonding to the metal contacts. The die attach process in particular can introduce contaminants onto the graphene surface due to outgassing so the method used needs to be carefully considered. Wire bonding presents difficulties due to the low adhesion of the graphene to the substrate. In addition to this the contact thickness on graphene devices is typically thinner ($\approx$500 nm) than those used in standard wire bonding processes ($\approx$1.0 μm) due to the graphene detaching during metal lift off process when using thicker contact layers.

The graphene Hall effect sensors described throughout chapter 3 were packaged by one of the project partners (TT Electronics) for implementation into a power module. The process and issues encountered are outlined in the following section.

3.4.1 Die Attach

Eutectic die attach was performed under mixed gas at a temperature of 425°C with the Au contacts showing evidence of blistering and some detachment. This is evident in Figure 3.24a which shows an example die after eutectic die attach.



(a) **(b)**

Figure 3.24: Optical images of metal contacts after die attach for a) devices fabricated on a Si/SiO_2 substrate and b) devices fabricated on a SiC substrate. (*Images provided by TT Electronics Semelab*).

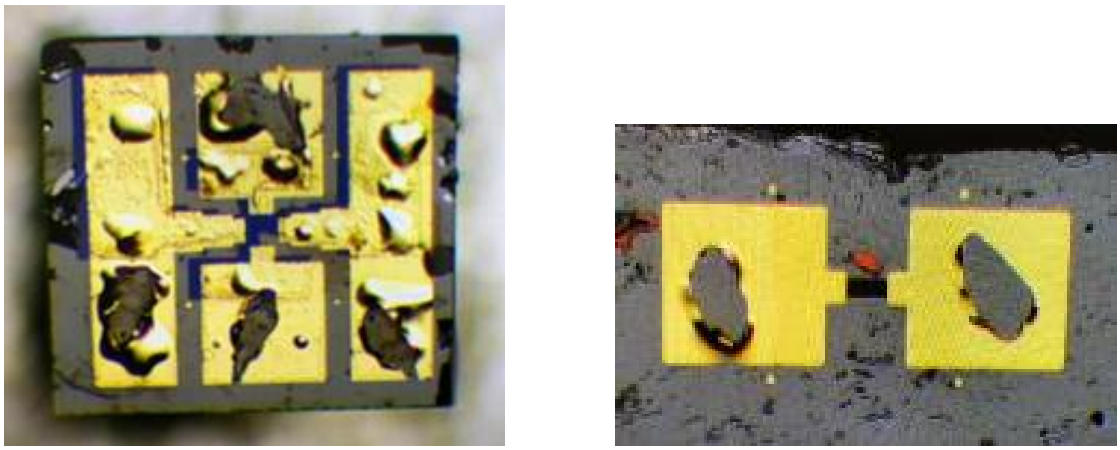
It is hypothesised that this bubbling occurs as a result of the weak bonding between the graphene film and the substrate exhibited in CVD grown and transferred films. The transfer process for CVD graphene may additionally result in moisture trapped between the film and substrate, resulting in the observed bubbling as the die is heated and any trapped moisture is evaporated from the surface. In order to reduce this bubbling, samples were fabricated using graphene on a SiC substrate. It is anticipated that as the graphene is epitaxially grown as opposed to transferred, the increased bond strength between the film and substrate will reduce detachment issues. Additionally, SiC can withstand higher temperatures than Si making it more robust to higher temperature processes.

The resulting die can be seen in the image in Figure 3.24b. It can be seen from Figure 3.24b that through the use of epitaxial graphene there is no bubbling of contacts or detachment observed.

3.4.2 Wire Bonding

The contact windows on the mask set used for this project were designed so that the metal contacts overlap the graphene layer. This is to allow for the wire bond to be attached to an area of the metal contact that is directly bonded to the substrate

in order to reduce issues with low adhesion of the graphene film. Wire bonding was carried out using a thermosonic wedge bond process with a 1.0 mil Au wire at 150°C.



(a) **(b)**

Figure 3.25: Optical images of metal contacts after wire bonding for a) devices fabricated on a Si/SiO_2 substrate and b) devices fabricated on a SiC substrate. (*Images provided by TT Electronics Semelab*).

Figure 3.25 shows optical images of graphene devices after attempting to wire bond to the metal contacts. Images of devices fabricated on a Si/SiO_2 layer are shown in Figure 3.25a with the wire bonding process shown to have removed the metal contact in the region of the bonding area. It can also be seen from Figure 3.25b that despite the eradication of contact bubbling when using a SiC substrate, the issue of metal detachment still remains when attempting the bonding process. In order to overcome this issue, further wire bonding trials are required. Steps include vacuum annealing of devices prior to wire bonding to remove any moisture that may be present and improve chances of adhesion. Additionally, the use of ball bonding as opposed to the ultrasonic wedge bonding initially used in order to reduce the force the metal contacts are subjected to during processing. Ball bonding is typically preferred in this case due to the lower pressure used during the bonding process.

The outcome of this study is currently pending however if successful it will allow for further optimisation of graphene devices and expand the environment in which they are capable of operating in. Whilst not having appropriate packaging limits

the lifetime of devices, initial stability measurements such as the high temperature and AC performance of graphene Hall effect sensors can be carried out with the results presented in the following chapter.

3.5 Summary

The challenges particular to fabricating functional, scaleable graphene devices are presented in this chapter. This is particularly notable when using CVD graphene due to the inherently weak bonding to the substrate, with van der Waals forces being the only bonding mechanism. Cu sacrificial layer method to reduce detachment of graphene from the surface during lithographic processing is presented and compared to comparative fabrication methods, namely standard lithographic processing (no sacrificial layer) and Al sacrificial layer method. AFM and Raman surface analysis techniques have demonstrated the improved cleanliness and uniformity of the graphene surface is demonstrated when using a Cu sacrificial layer. The defect ratios (D/G ratio) of devices fabricated using a Cu sacrificial layer is reduced to just 0.07±0.004 from 0.2±0.01 when using no sacrificial layer. Comparison of the 2D/G ratios with exhibited carrier concentration shifts in literature also suggests that the use of a Cu sacrificial layer reduces surface doping by up to 60 %. This correlates with AFM imaging which demonstrates improved surface quality and reduced roughness. Key electrical characteristics are also presented and compared to that of commercial graphene devices purchased from the manufacturer of the as received graphene films.

Cu sacrificial layer is shown to improve current related sensitivity up to approximately 165±16.5 V/AT from 32.4±6.40 V/AT when using no sacrificial layer. This improvement in electrical characteristics is universal, with carrier mobility and sheet carrier density also demonstrating an improvement. Use of a Cu sacrificial layer is also shown to increase yield up to 82 % and significantly reduces the variability of characteristics. Dirac point shifting is observed through external gate biasing, with the Dirac point shown to lie at a gate bias of approximately 37±1.0 V. Hysteresis of the Dirac point is also analysed and corresponds with surface analysis

and electrical data that Cu sacrificial layer method offers improved surface quality. The use of external gate biasing as a method of optimising electrical and transport characteristics is also presented with the current related sensitivity shown to increase to >900 V/AT around the Dirac point. Finally issues relating to wire bonding and packaging of graphene devices are presented.

Chapter 4

Stability of Graphene Devices

4.1 Introduction

Despite the success into the development of robust synthesis and fabrication techniques for graphene, relatively few studies have been undertaken into how graphene devices perform in real-world applications. Most crucially to this project, knowledge of how it performs in high temperature environments and the AC characteristics of devices at frequencies $>$ 120 kHz.

Numerous theoretical studies have shown that graphene has the capability to operate in high temperature environments based on the high thermal conductivity (5000 $Wm^{-1}K^{-1}$) and zero bandgap nature. Yin *et al.* [14] demonstrated that the intrinsic carrier density of graphene is an order of magnitude less sensitive to temperature than that of commonly used semiconductor materials such as Si and Ge up to a temperature of 2400 K. A graphene-metal composite sensor with a near zero temperature coefficient of resistance (TCR) was also demonstrated by Marin *et al.* [163] with devices exhibiting a $<$1.0 % increase in resistance at temperatures up to 333 K. Although initial work has been reported on the high temperature capabilities of graphene films, further investigation is required in order to understand the origins of any thermal stability in graphene devices and how this can be optimised further to enable viable long term use in real world applications.

The frequency operation of graphene devices presents a similar challenge. There

have been many studies demonstrating that graphene based devices, most commonly GFETs, are capable of operating in the THz region [164]. In the case of Hall sensors this far exceeds the maximum operating frequency of commercially available semiconducting devices (<120 kHz) [165, 166]. To date however there have been no published practical studies of graphene sensors operating at high frequency. It is evident from literature that the key to optimising both the frequency operation and high temperature characteristics of graphene devices is understanding how the degradation of the graphene surface from external contaminants impacts on these characteristics [167, 168]. The sensitivity and degradation of the graphene surface has been well documented and was clearly evidenced in the both chapter 2 and 3, as such it is critical to understand how the devices perform under comparable conditions to those of the intended applications. It is also crucial to understand how this performance can be enhanced further, particularly in the context of Hall effect sensing.

This chapter reports the electrical characteristics of graphene change at an operating temperature above ambient, as well as how it performs at current and field frequencies which is above those demonstrated for commercial Hall sensors. It will also explore how exposure to ambient air degrades the electronic properties over time and what methods can be implemented in future device iterations to overcome this. Measurements carried out for this section were performed on unpackaged devices due to the difficulties encountered in the reproducible packaging of graphene devices, as such results are influenced by the environment in which measurements were performed which has been taken into consideration when carrying out analysis of results.

4.2 High Temperature Characteristics of Graphene Devices

The ability to fabricate thermally stable current sensors is critical in areas such as power electronic converters, where the monitoring of current flow is essential for over-current protection and the closed loop monitoring. The origin of thermal

instability in conventional Hall devices stems from fluctuations in intrinsic carrier density and the contribution to overall device sensitivity. The main origin of fluctuation in intrinsic carrier density in these devices is due to bandgap narrowing with increasing temperature. The bandgap in a semiconductor as a function of temperature can be described by Equation 4.1 [150]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{4.1}$$

where $E_g(0)$ is the bandgap at 0 K in eV, α and β are material dependant constants and T the temperature in Kelvin.

A graphical representation of this equation for commonly used semiconductor materials; Si, InAs and InSb is shown in Figure 4.1. The bandgap is shown to decrease with increasing temperature in Kelvin.

This variation in bandgap has a direct impact on the intrinsic carrier density according to Equation 4.2:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \tag{4.2}$$

where N_C is the effective density of states in the conduction band in cm^{-3}, N_V the effective density of states in the valence band in cm^{-3}, k the Boltzmann's constant (1.38×10^{23} JK^{-1}) and T the temperature in Kelvin.

It can be seen from Equation 4.2 that this reduction in bandgap energy will cause a further increase to the exponential behaviour of the intrinsic carrier density. This often results in either additional circuitry being required to reduce the thermal instability or the use of larger active devices to reduce the impact of the external temperature. The superlative electronic properties of graphene at temperatures that range between room and cryogenic temperatures have been the subject of a significant number of reports in the literature. The low sheet carrier concentration, coupled with high carrier saturation velocity [39] that results from the linear dispersion relation and the thickness of a single atomic layer make graphene the leading candidate for the realisation of high sensitivity, high bandwidth Hall effect sensors. In addition to the superlative material properties, the potential to

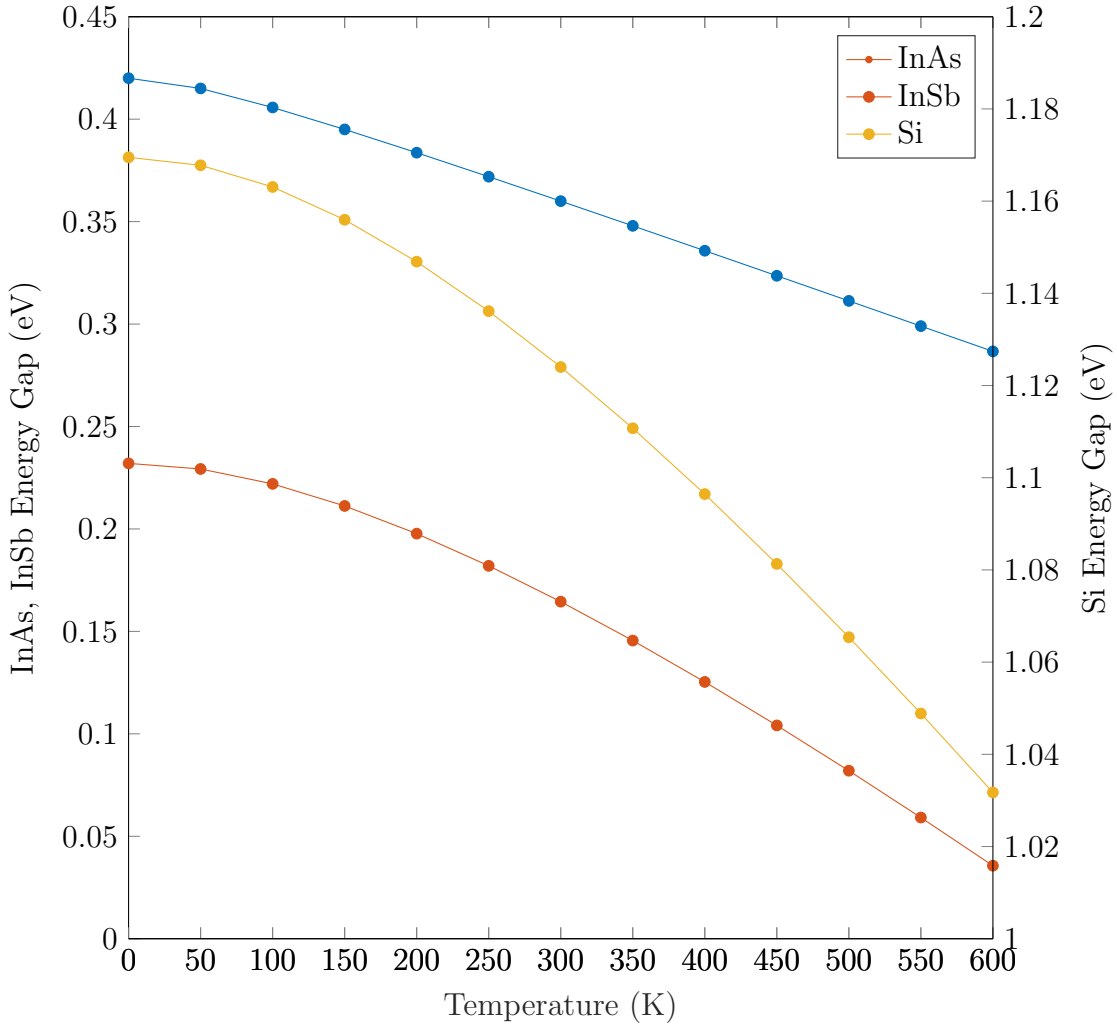


Figure 4.1: Temperature dependance of the bandgap in Si, InAs and InSb, calculated using material data from [150].

directly grow graphene on to the surface of a SiC wafer facilitates the monolithic integration of the Hall device with SiC based signal conditioning circuitry, which is typically required due to the low-level output of Hall devices.

4.2.1 Electrical Characteristics up to 473 K

Hall effect measurements were performed on un-gated sensors up to a temperature of 473 K - this represents the maximum temperature the sensors would be subjected to in the desired engine zone as described in Section 2.1. Devices were initially biased and measured at a temperature of 300 K. The temperature was then increased in steps of 50 K at a rate of 5 K/S. The temperature was then

stabilised for a period of 5 minutes before carrying out each measurement. High temperature measurements were carried out on 20 devices across the three wafers fabricated using a Cu sacrificial layer, with five measurements taken per device. Errors were calculated according to the standard deviation method described in Chapter 2. The Hall resistance for a typical sensor as a function of magnetic field is shown in Figure 4.2 with temperatures ranging from 300 K to 473 K. The data are shown to be linearly dependant on magnetic flux density for all five data sets with R^2 values exceeding 0.99 obtained. It can be seen that as temperature increases the zero field resistance decreases monotonically. This value likely originates from the misalignment of the current flow in the active region of the sensor, often arising from the misalignment of the arms in the Hall structure [157]. This value can be correlated with the sheet resistivity of the graphene and is expected to result in a quadratic Hall voltage component at fields significantly higher than those used in this study.

From the data in Figure 4.2 sheet carrier concentration and carrier mobility can be extracted as a function of temperature. The resulting trend is shown in Figure 4.3. Sheet carrier concentration is shown to go through a maximum of $1.9\pm0.040\times10^{13}$ cm^{-2} at 373 K with carrier mobility conversely shown to go through a minimum of $1.3\pm0.060\times10^{3}$ $cm^2V^{-1}s^{-1}$ at the same temperature. This corresponds with the known behaviour of graphene due to Fermi level shifting [169,170]. In gated devices the Fermi level can be tuned to operate at the Dirac point, however as these devices are not gated, as the temperature increases there is a build up of charge carriers causing the Fermi level to shift. This Fermi level shift could additionally be attributed to moisture adsorption to the graphene surface. The boiling point of water is known to be 373 K, suggesting that moisture present on the graphene surface is evaporated from the surface as the device is heated. This means that the graphene is now exhibiting annealing type behaviour with the electronic and transport properties improving beyond this point.

The data in Figure 4.4 show the experimental sensitivity extracted from the gradient of the sensor data shown in Figure 4.2. The data show that the sensitivity goes through a minimum at 373 K, the same temperature as the sheet carrier concentration shows a maximum value. The underlying mechanism behind the sensitivity

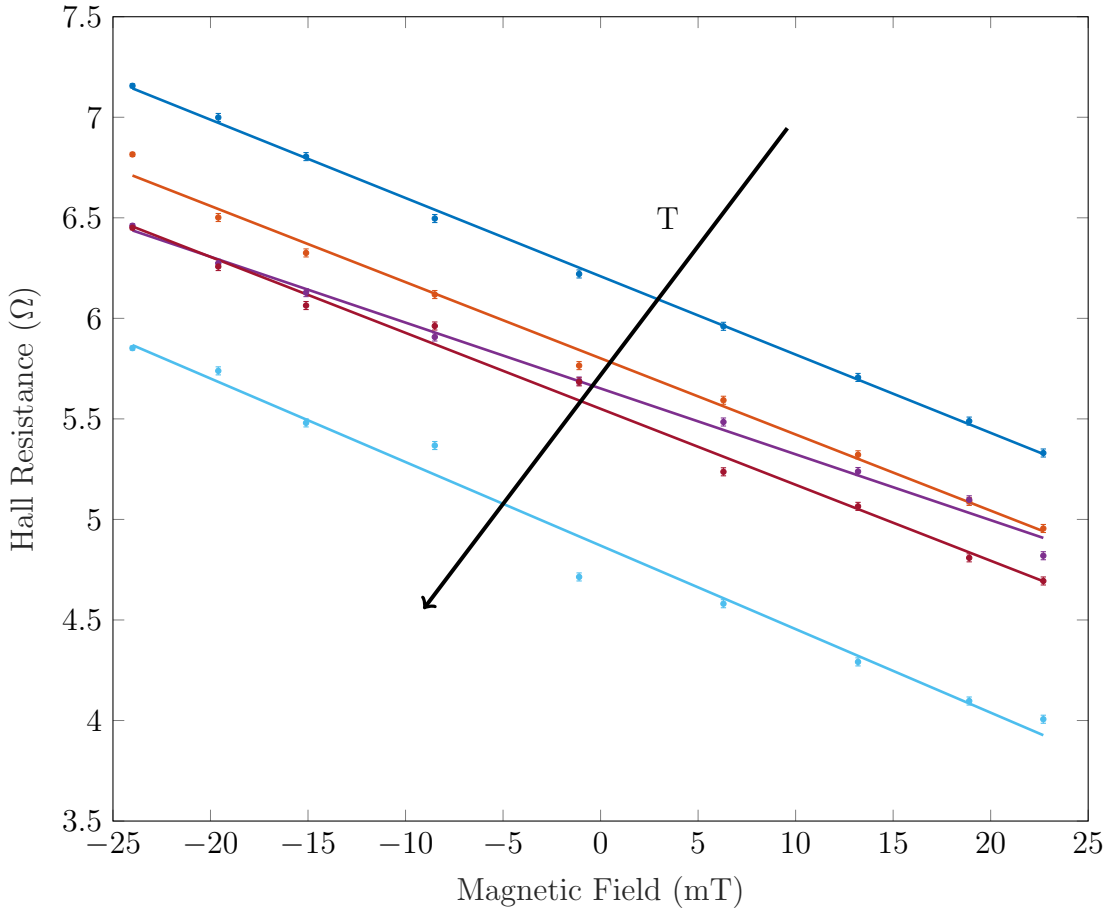


Figure 4.2: Hall resistance as a function of magnetic field with a fixed current bias of 3 mA for temperatures of 300 K, 323 K, 373 K, 423 K and 473 K.

in graphene Hall sensors that show non-monotonic characteristics was identified by normalising the experimental sensitivity with the carrier mobility and sheet resistance of the graphene. This resulted in a consistent value of $\frac{S_{(T)}}{\mu R_{SH}}$=1.0×10^{-4}, indicating that the sensitivity of the sensor is directly related to the carrier mobility and the sheet carrier concentration. This linear behaviour can be seen from the functional fit of current related sensitivity against μR_{SH} in Figure 4.5. The Hall geometry factor at low field can be extracted with a value of 3.3±0.010×10^{-2}, which is consistent with the requirements that 0≤G$_{H0}$≤1 [171].

The thermal coefficient of sensitivity as a function of temperature can be extracted from the data in Figure 4.4 according to Equation 4.3:

$$\frac{S_T}{S_{(T_0)}} = 1 + \alpha\,(T - T_0) \tag{4.3}$$

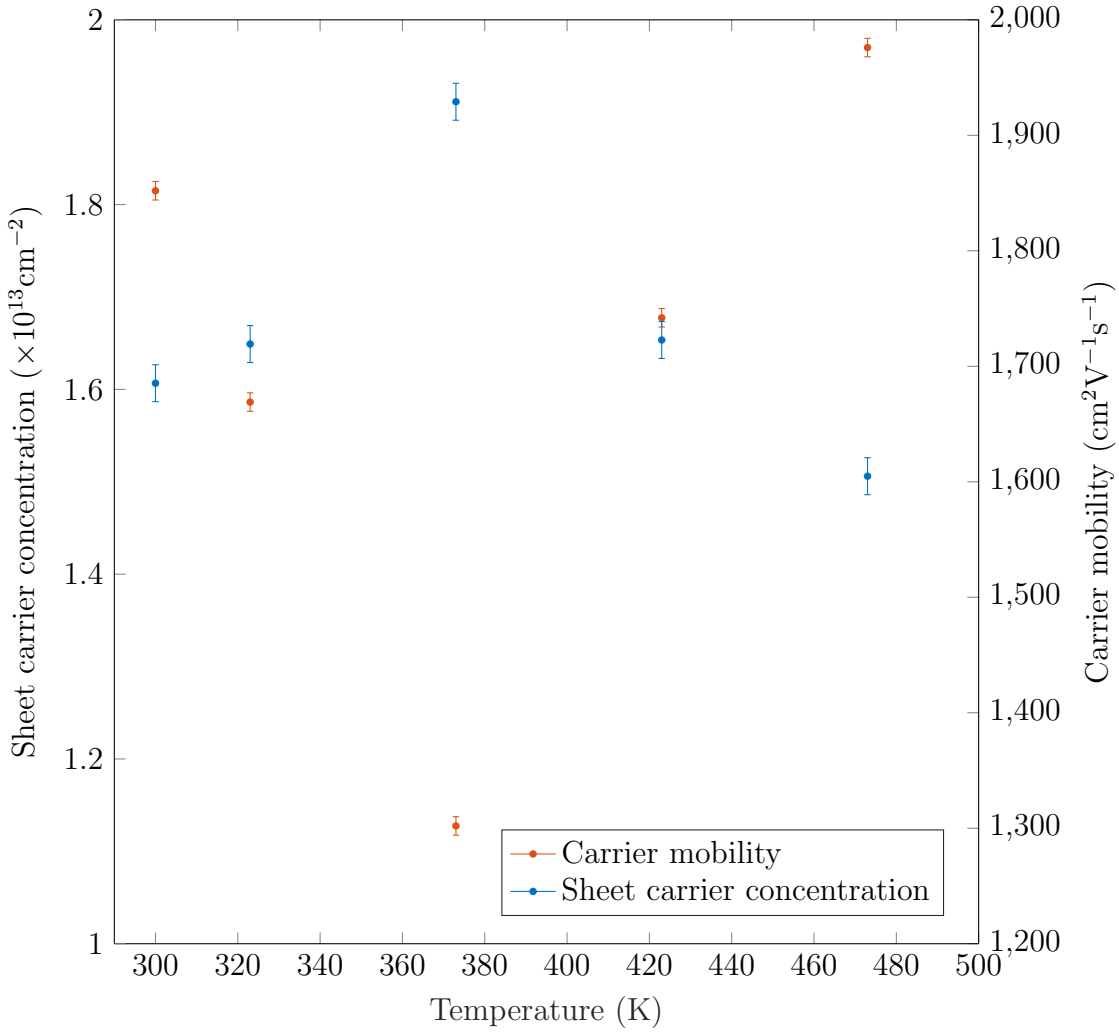


Figure 4.3: Experimental sheet carrier concentration and carrier mobility of graphene hall sensors as a function of temperature.

where $S_{(T)}$ is device sensitivity at measured temperature in V/AT, $S_{(T_0)}$ the device sensitivity at room temperature (T_0) in V/AT, and α the thermal coefficient in ppm/K.

The thermal coefficient for temperatures below the Dirac point can be extracted, yielding a value of -2.2±0.088×10^3 ppm/K, whereas for higher temperatures this becomes 2.7±0.14×10^3 ppm/K. Because the sensitivity close to 373 K is dominated by the shift in the carrier concentration arising from the influence of the Dirac point, the true temperature sensitivity of the graphene Hall sensor can be estimated by looking at the data points for 300 K and 473 K, resulting in a temperature coefficient of 0.92±0.023×10^3 ppm/K. The solid line in Figure 4.4 is a prediction

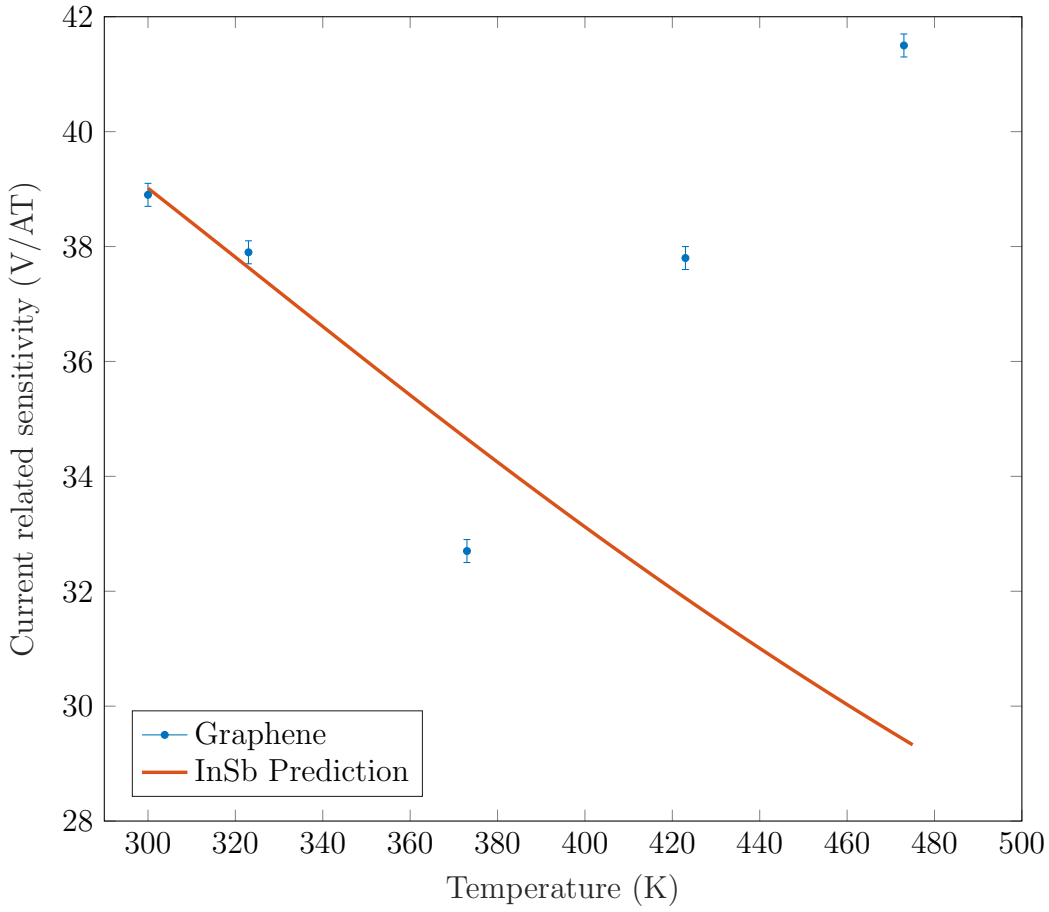


Figure 4.4: Current related sensitivity of graphene hall sensors as a function of temperature alongside InSb predicted performance.

of the sensitivity of an InSb Hall sensor, which can be calculated using Equation 4.4 [172].

$$S_I = \frac{1}{q} \frac{p\mu_h^2 - n\mu_e^2}{(p\mu_h + n\mu_e)^2} \tag{4.4}$$

where μ_e is the electron mobility, taken to be 7.7×10^4 $\mathrm{cm^2V^{-1}s^{-1}}$, μ_h the hole mobility, taken to be 850 $\mathrm{cm^2V^{-1}s^{-1}}$ [173] and n and p the electron and hole concentrations respectively [150].

InSb is one of the most commonly used semiconductors for room temperature Hall sensing due to its high sensitivity [21] however it suffers from large thermal drift due to the narrow bandgap which is exacerbated by the bandgap narrowing with increasing temperature, causing a large shift in intrinsic carrier density. The data show a similar temperature behaviour below 373 K to that of the graphene de-

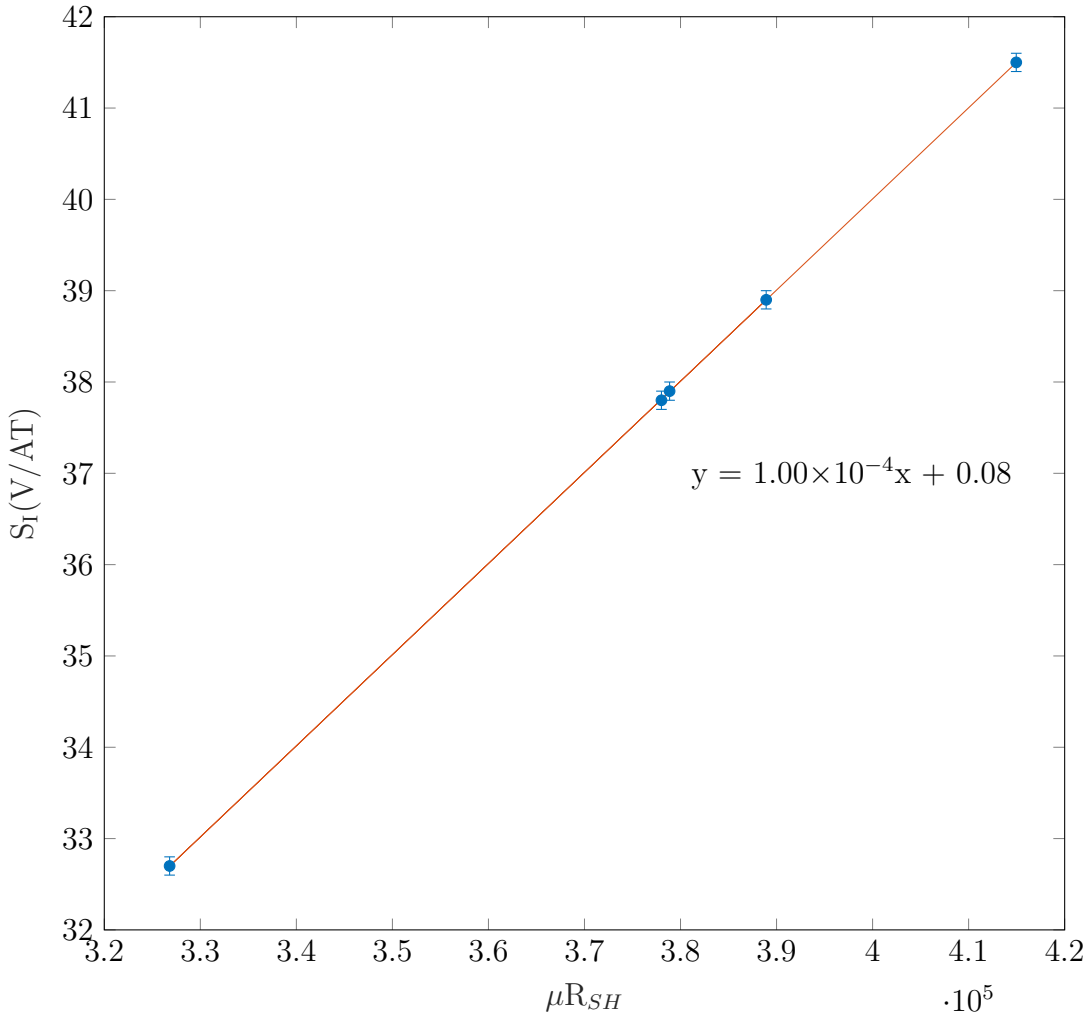


Figure 4.5: Current related sensitivity of graphene Hall sensors as a function of μR_{SH}.

vice. This indicates that in the region of the Dirac point, where the sheet carrier concentration changes rapidly, the temperature variation in the graphene sensor is too high for application in power electronic modules. In order to investigate the influence of the Dirac point on the temperature range of interest, the Hall sensors can be gated, controlling the sheet carrier concentration in the graphene [174] or the surface of the sensor can be oxygen functionalised using a low energy plasma process to suppress the carrier concentration, whilst maintaining the carrier mobility [175]. Both of these techniques will enable the realisation of high performance Hall sensors that are suitable for real-time current monitoring in power electronics modules in aerospace applications.

Oxygen functionalisation to suppress carrier concentration has been well documented in previous studies, most notably by Hernandez *et al.* [175]. The appli-

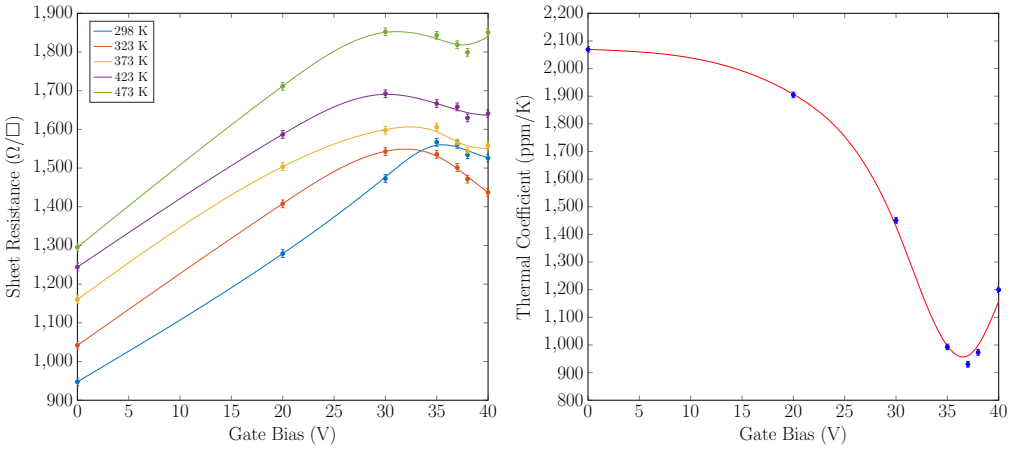
cation of an external gate bias to explicitly reduce the thermal drift of graphene devices has thus far not been demonstrated however the effect was observed by Banadaki *et al.* [98] in their characterisation of a graphene temperature sensor.

4.2.2 Electrical Characteristics of Gated Devices

To investigate the influence of the Dirac point on the thermal stability of graphene devices, high temperature measurements were repeated with an external gate bias applied. The gate bias was varied from 0 V to 40 V at temperatures up to 473 K. Newly fabricated devices were utilised for gated measurements, with devices initially biased and measured at a temperature of 300 K. The temperature was then increased in steps of 50 K at a rate of 5 K/S. The temperature was then stabilised for a period of 5 minutes before carrying out each measurement. Gated high temperature measurements were carried out on 20 devices across the three wafers fabricated using a Cu sacrificial layer, with five measurements taken per device. Errors were calculated according to the standard deviation method described in Chapter 2.

From these measurements critical electrical parameters such as current related sensitivity, carrier mobility and sheet carrier density were extracted. Initially the sheet resistance of graphene devices was extracted under these conditions with the data in Figure 4.6 showing this sheet resistance as a function of gate bias and the resulting thermal coefficient of the sheet resistance as a function of gate bias.

It can be seen that the thermal coefficient of the sheet resistance decreases with increasing bias, with the lowest thermal coefficient ($0.93\pm0.037\times10^3$ ppm/K) occurring at a gate bias of 37 ± 1.0 V. This corresponds to the analysis of the Dirac point in Section 3.3. This initially appears to differ from the data presented by Banadaki *et al.* [98] which indicates that the point of lowest thermal drift occurs beyond the Dirac point (where $V_g > V_{DIRAC}$). It is noted however that the Dirac point appears to shift with increasing temperature, a point which can be evidenced by extrapolating the Dirac point observed in Figure 4.6a. The resulting data can be seen in Figure 4.7. From this it can be seen that the Dirac point appears to occur around a gate bias of 35 ± 1.1 V initially and is shifted towards 30 V as the



(a) **(b)**

Figure 4.6: Gated sheet resistance variation with temperature showing a) extracted sheet resistance as a function of gate bias with increasing temperature and b) thermal coefficient of sheet resistance as a function of gate bias. Polynomial curve fitting was applied for extraction of the point of maximum sheet resistance and minimum thermal coefficient.

temperature increases. The annealing type behaviour previously discussed is likely the main source of this shifting, with the removal of contaminants and moisture from the surface shifting the Fermi level towards the charge neutrality point. The large FWHM of the Dirac point evidenced in the hysteresis measurements presented in Section 3.3 could additionally be responsible for the erroneous values extracted for the Dirac point during temperature measurements with the charge neutrality point occurring over a wide range of bias values.

Despite the exact point at which the Fermi level sits being unclear, it is evident from the data in Figure 4.6b that the thermal coefficient of the sheet resistance has a strong dependance on the external gate bias. The mechanism behind this reduced thermal coefficient is however undetermined so it is difficult to fully analyse this difference in behaviour from the devices presented in literature. It is evident however that in addition to the controllability of electrical characteristics it is also possible to control the thermal stability of devices to a some extent through external gate biasing.

Whilst the devices presented in the literature are also exposed to environmental conditions with no protective layer on the graphene film [98], the Dirac point is

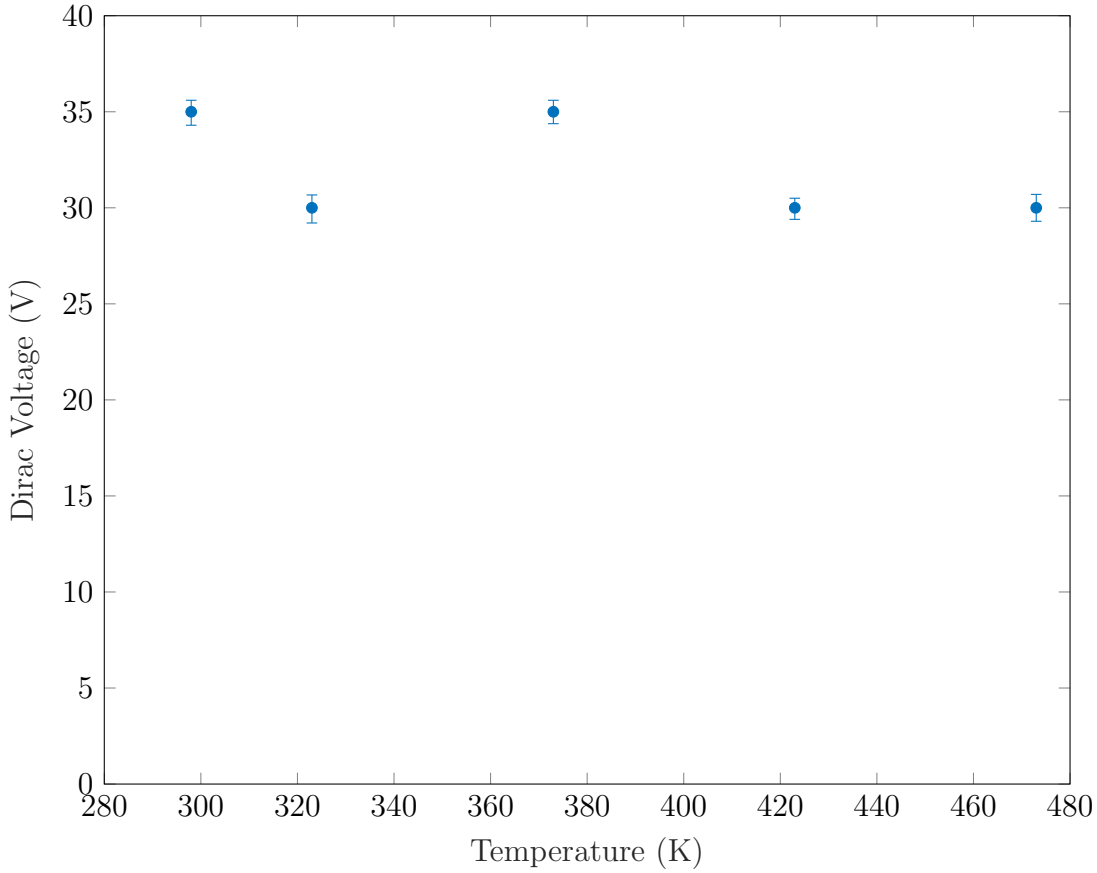


Figure 4.7: Dirac voltage extracted from Figure 4.6a as a function of temperature.

shown to occur between a gate bias of 0–1.0 V suggesting there are fewer contaminants present on the graphene surface. One suggestion for the difference in behaviour between the devices in literature (which typically exhibit a linear dependance on temperature) and those fabricated in this study is that the larger amount of contamination and moisture on the surface of the graphene film is resulting in the annealing type behaviour described in the previous section occurring despite external gate biasing. This effect can be observed further when considering additional electrical characteristics extracted such as current related sensitivity, carrier mobility and sheet carrier density.

The data in Figure 4.8 show the current related sensitivity extracted from graphene devices as a function of gate bias at temperatures ranging from 298 K to 473 K. The current related sensitivity is shown to reach a maximum point at a gate bias of 30±0.90 V, with the exception of data extracted at 323 K. This corresponds to the data extracted for sheet resistance in Figure 4.6 and again suggests that the

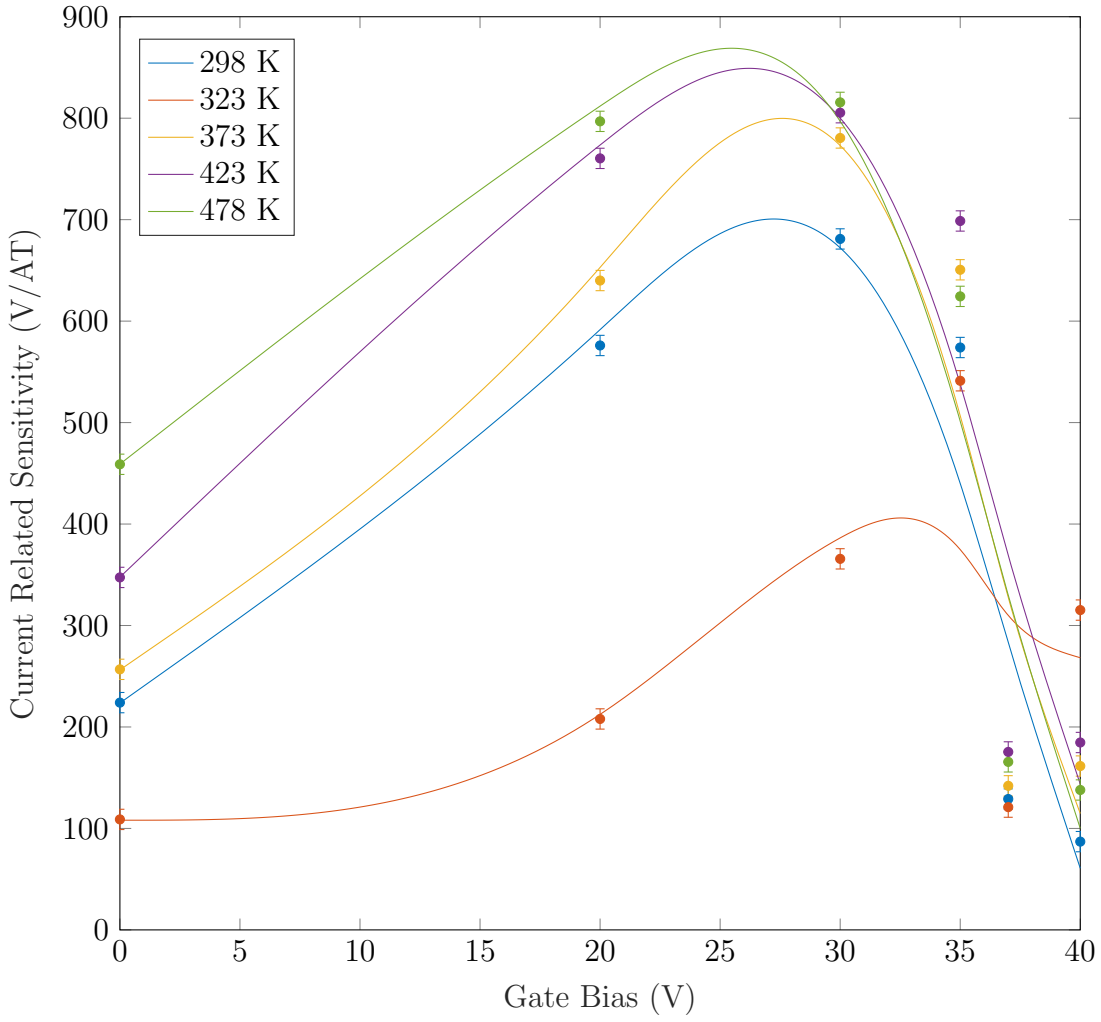


Figure 4.8: Current related sensitivity as a function of gate bias for temperatures ranging from 298 K to 473 K. Polynomial curve fitting was applied for extraction of the point of maximum current related sensitivity.

Dirac point has been shifted from the room temperature measurements reported in Section 3.2.3. Initial observation shows that the drift in temperature is reduced around gate biases of 35–37 V, which occurs at a higher gate bias than the Dirac voltage. From these data the thermal coefficient was extracted using Equation 4.3 as in the previous section. These data are shown in Figure 4.9 as a function of gate bias. The lowest thermal coefficient occurs at a gate bias of 35±1.1 V, with a value of just $0.50 \pm 0.025 \times 10^3$ ppm/K. The current related sensitivity is however reduced from its maximum at this point, resulting in a trade off between the point of maximum current related sensitivity and the point of minimum thermal sensitivity.

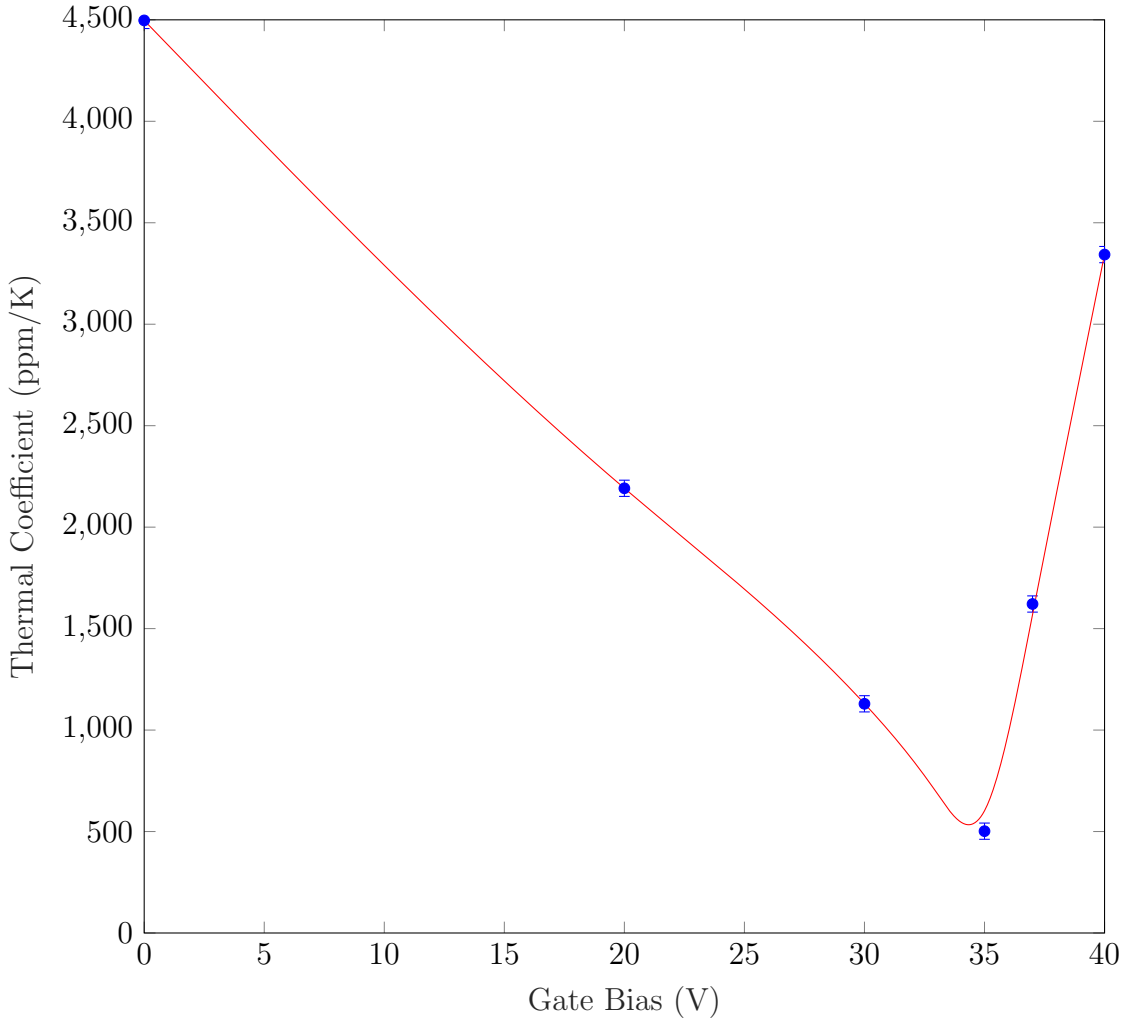


Figure 4.9: Thermal coefficient of the current related sensitivity as a function of gate bias. Polynomial curve fitting was applied for extraction of the point of minimum thermal coefficient.

The Gaussian trend of the sensitivity as a function of temperature is however still evident in Figure 4.8 as in the previous section where no external gate biasing was applied to devices. This suggests that this behaviour is likely due to the removal of contaminants from the graphene surface as the temperature is increased. This is also evident in the apparent shifting of the point at which the transport properties of the graphene begin to improve (from a temperature of 373 K to 323 K). This effect can be observed further when the current related sensitivity is shown as a function of temperature, as can be seen from the data in Figure 4.10. The data show that the current related sensitivity is reduced up to a temperature of 323 K before increasing beyond this point for gate biases up to 37±1.0 V. The data

extracted at a bias of 40±1.0 V is shown to be anomalous to this trend. However the data presented by Banadaki *et al.* does begin to exhibit an increase in thermal coefficient where $V_g >> V_{DIRAC}$ suggesting the lowest thermal coefficient occurs just beyond the Dirac point. Operation at a gate bias of 35±1.1 V and 37±1.0 V show the sensitivity to be almost independent of temperature, although the current related sensitivity is significantly reduced at 37±1.0 V.

It is additionally observed from the data in Figure 4.8 that the Dirac point is shifted beyond a temperature of 323 K. This also suggests an annealing type behaviour with heating of the devices which could contribute to the reduced thermal coefficient observed in Figure 4.9. The shift in Dirac point could also be due to the large FWHM of the Dirac point extracted from the hysteresis measurements in Chapter 3.

Both the sheet carrier density and carrier mobility can be extracted from the data in Figures 4.8 and 4.6 with the resulting data shown in Figure 4.11. The sheet carrier density and carrier mobility are shown as a function of gate bias with increasing temperature. The resulting thermal coefficient is also extracted and shown as a function of gate bias. As expected, these characteristics are shown to follow a similar trend to that of the current related sensitivity, with the lowest thermal coefficient occurring at a gate bias of 35±1.1 V. This follows the known behaviour of Hall effect sensors, with the current related sensitivity being inversely proportional to carrier density. The data extracted for the carrier mobility at a gate bias of 40±1.0 V exhibit a weaker temperature dependance than the data extracted for both the sheet carrier density and current related sensitivity. This is likely due to the fact that whilst the current related sensitivity is inversely proportional to the sheet carrier concentration, the mobility is additionally influenced by the current flow through the film and subsequently so is the resistance.

4.2.3 Origins of Non-Linear Thermal Behaviour

The non-linear behaviour of the electronic properties of graphene with temperature has previously been exhibited when determining the effects of ambient anneal on the sheet resistance. The data in Figure 4.12 show the sheet resistance of graphene

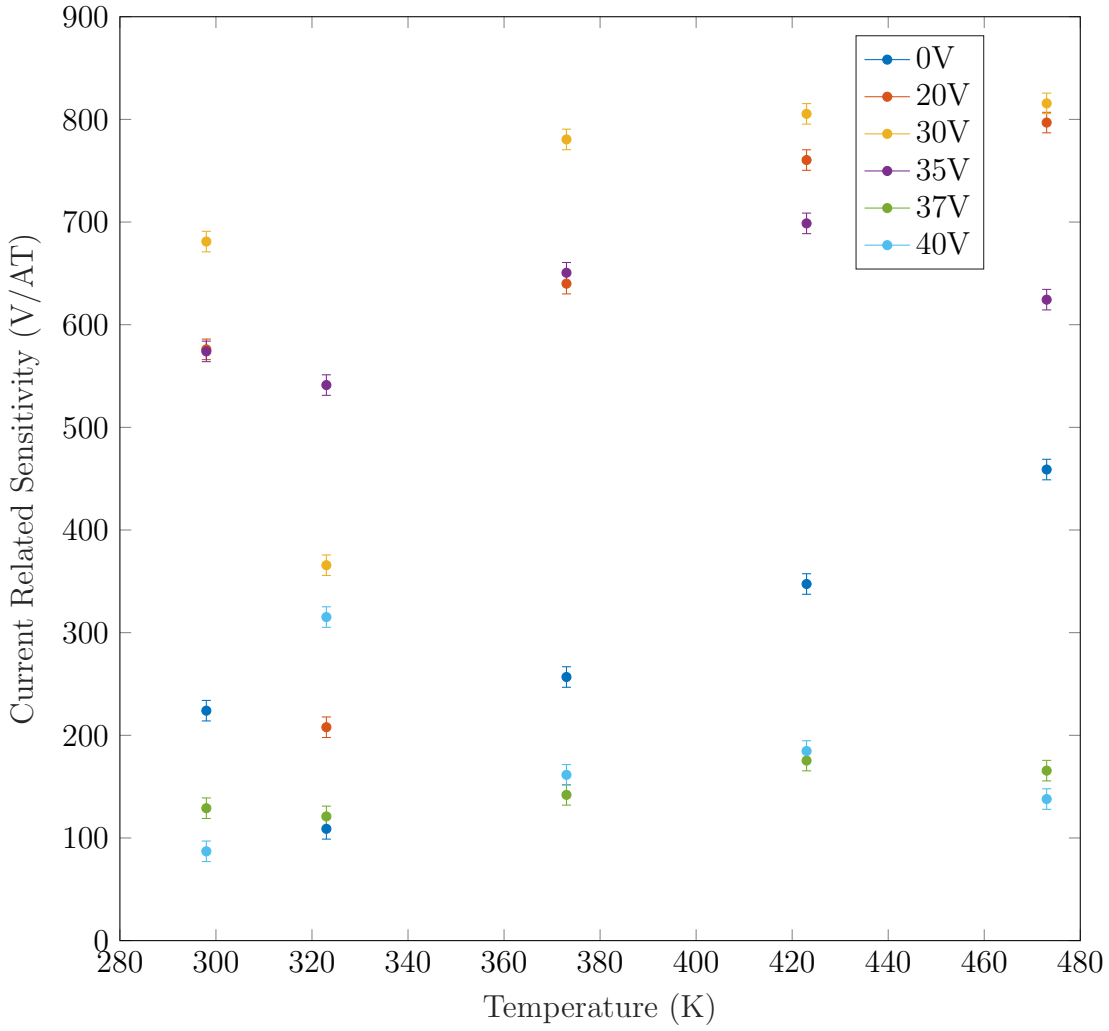


Figure 4.10: Current related sensitivity as a function of temperature for gate biases ranging from 0 V to 40 V.

devices as a function of temperature both during and after ambient anneal. It can be seen from these data that during initial ambient anneal the sheet resistance increases, similar to the expected degradation in electronic properties observed with increasing temperature [176]. This behaviour is however only exhibited up to a temperature of 373 K, beyond which the sheet resistance reduces. When temperature measurements are repeated post anneal this effect is diminished with sheet resistance having a thermal coefficient of just $0.27 \pm 0.014 \times 10^3$ ppm/K post anneal. This is ten times lower than the thermal coefficient extracted prior to annealing of $-2.7 \pm 0.14 \times 10^3$ ppm/K.

This is reflected in the subsequent Raman spectra taken from devices pre and post ambient anneal. The resulting data are shown in Figure 4.13. From the spectra

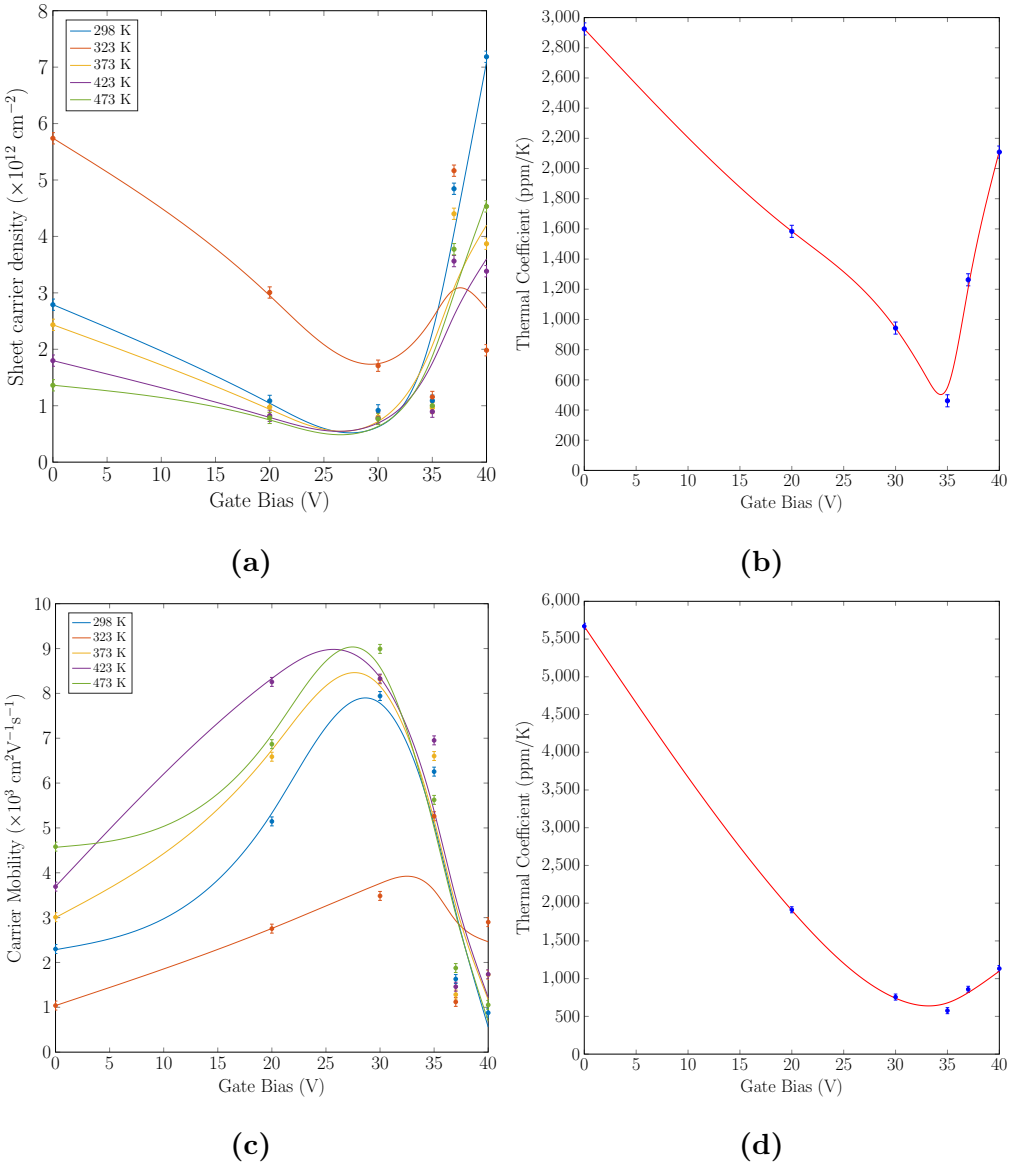


Figure 4.11: Gated electrical characteristics as a function of temperature showing a) extracted carrier density as a function of gate bias with increasing temperature, b) thermal coefficient of carrier density as a function of gate bias, c) extracted carrier mobility as a function of gate bias with increasing temperature and d) thermal coefficient of carrier mobility as a function of gate bias. Polynomial curve fitting was applied for extraction of the point of minimum sheet carrier density and thermal coefficient in addition to maximum carrier mobility.

taken prior to ambient annealing it can be seen that the 2D peak occurs at a wavelength of 2691 cm^{-1} and the G peak occurs at a wavelength of 1588 cm^{-1}. There are also additional D and D' peaks present in the spectra at 1351 cm^{-1} and 1627 cm^{-1} respectively. The 2D/G ratio and D/G ratio can also be extracted

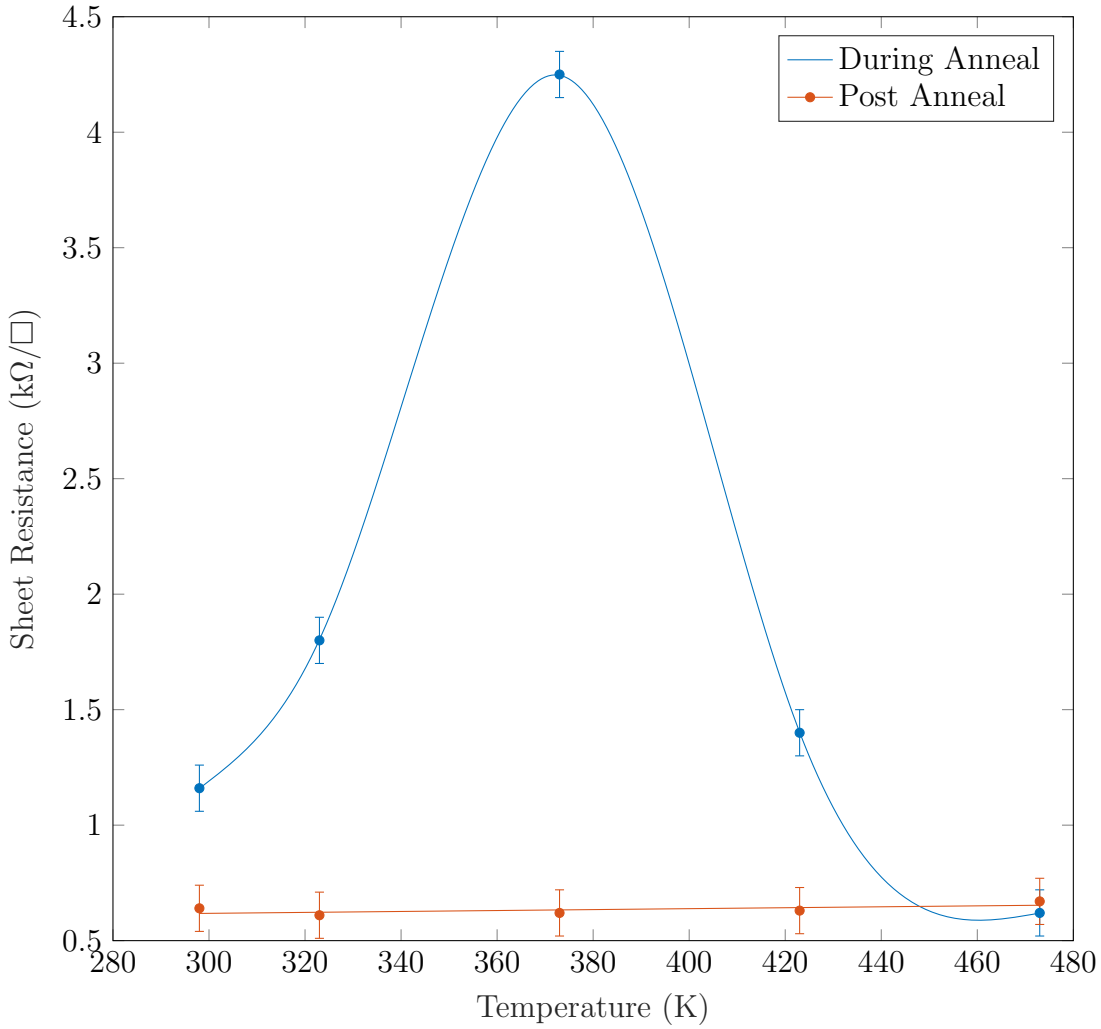


Figure 4.12: Sheet resistance of devices as a function of temperature during and after an ambient anneal. Polynomial curve fitting was applied to data extracted during anneal in order to extract the point at which annealing occurs. Linear fitting was subsequently applied to data extracted post anneal to demonstrate the linear behaviour exhibited by devices under these conditions.

from these spectra with values of 1.5±0.2 and 0.14±0.018 extracted respectively. The D/G ratio is of particular interest as this is an indicator of the defect density in the graphene film and can be used as a comparison point to determine if ambient annealing has reduced the level of defects present. Post anneal the 2D peak is shifted to 2697 cm^{-1} and the G peak is shifted to 1599 cm^{-1}. It can be seen however that the D and D' peaks associated with disordered graphene are not present in this spectra. The 2D/G ratio and D/G ratio were extracted as 1.0±0.12 and 0.020±0.0030 respectively. Comparison of the D/G ratio with a re-

duction from 0.14±0.018 prior to annealing to 0.020±0.0030 post anneal strongly suggests that ambient annealed has removed contaminants or defects present on the graphene surface. The 2D/G ratio reduction from 1.5±0.2 prior to annealing to 1.0±0.12 post anneal may be interpreted as a shift in electron concentration of almost 2.0×10^{13} cm^{-2} according to the data presented by Das *et al.*, seen in Section 3.2.2 [123].

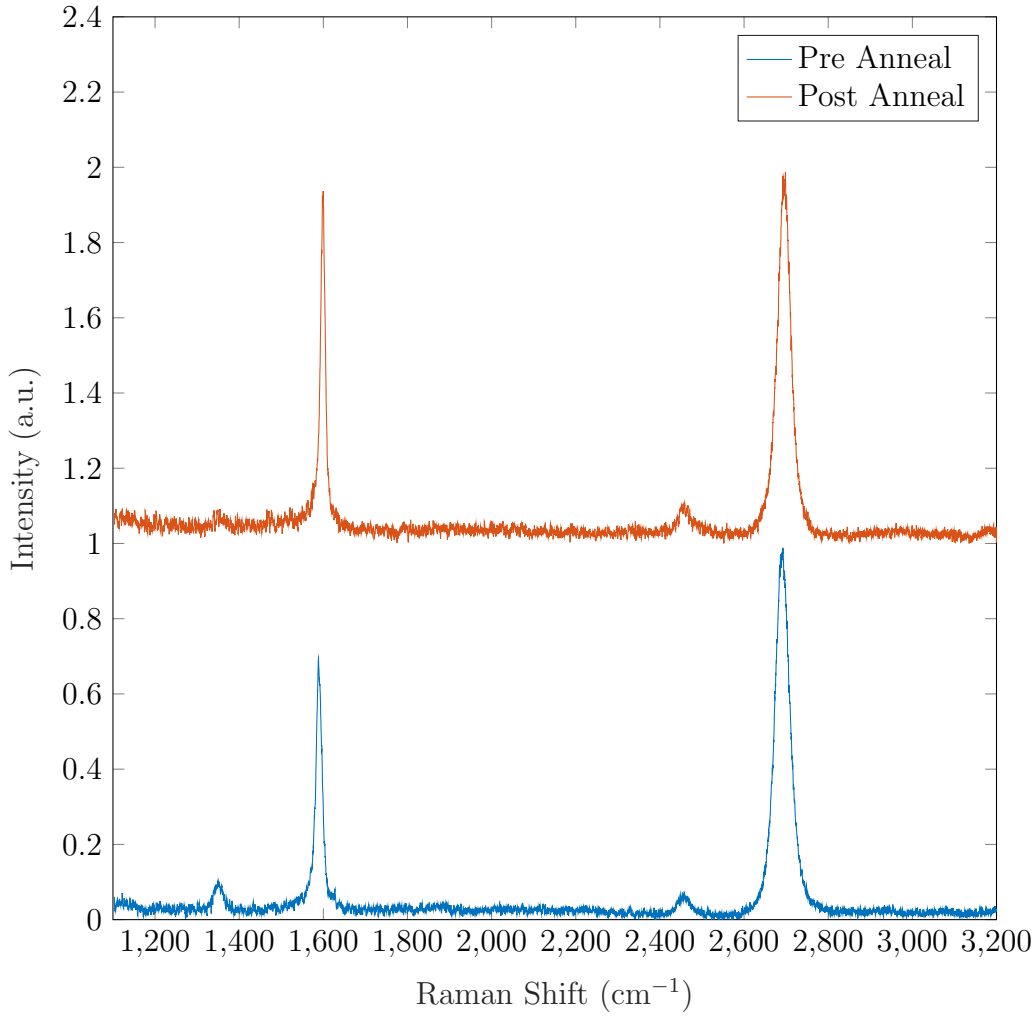


Figure 4.13: Raman spectra of graphene devices prior to and post anneal at 473 K.

Both the ambient anneal and Raman data shown in Figures 4.12 and 4.13 respectively strongly suggest the non-linear behaviour of the electronic properties of graphene with temperature to be a result of removal of contaminants from the graphene surface. The dominant source of this contamination is likely to be moisture absorption due to the temperature at which this annealing type behaviour occurs (373 K) corresponding to the known boiling point of water. A schematic

representation of the removal of contaminants from the graphene surface during the annealing process can be seen in Figure 4.14.

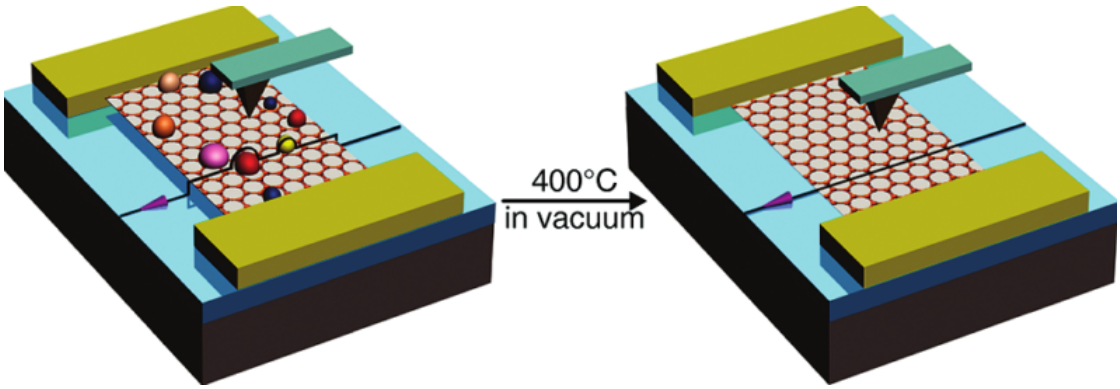


Figure 4.14: Schematic diagram of contaminants being removed from graphene surface during high temperature anneal process. *Image taken from [96].*

Extracting the temperature coefficient of resistance from the post anneal data in Figure 4.12 yields a value of $0.27\pm0.014\times10^3$ ppm/K which is both lower than the value extracted from gated sensors in Section 4.2.2 at $0.50\pm0.025\times10^3$ ppm/K and is additionally significantly lower than that of common semiconductor material based Hall sensors demonstrated in literature with InSb having a thermal coefficient in the region of 20×10^3 ppm/K [177] and GaAs in the region of 3.0×10^3 ppm/K [178]. The dependance of the Hall coefficient and carrier density in GaAs based Hall sensors on temperature can be seen in Figure 4.15. The temperature dependance in these devices exhibits a linearity which is not seen in the graphene devices. However it is clear they have a significantly stronger temperature dependance. Whilst the thermal coefficient is significantly reduced in GaAs over InSb they typically exhibit a small current related sensitivity meaning there is often a trade off in Hall sensors between the thermal coefficient and current related sensitivity. Whilst the trade off is also apparent in graphene sensors, the external gate biasing will allow for a highly sensitive Hall element with reduced thermal coefficient.

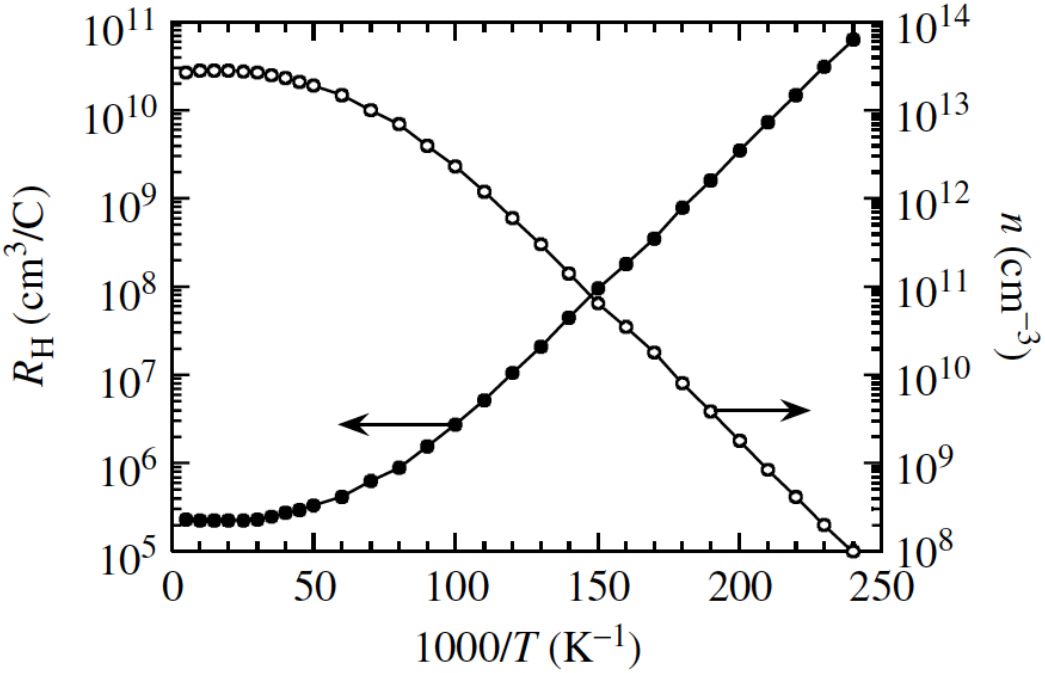


Figure 4.15: Hall coefficient and carrier density variation with temperature in GaAs. *Image taken from [179].*

4.2.4 Future Optimisation of Thermal Stability

It is evident from the results presented in this section that the application of an external bias does allow some level of control over the thermal coefficient of graphene devices. The removal of contaminants from the surface as the device is heated however still results in a gaussian type dependance on temperature. This can be reduced by annealing devices prior to operation. However where devices are unprotected, as is the case in this study, the re-introduction of contaminants to the surface from the surrounding environment results in a similar effect. It is clear that in order to reduce this effect some level of device protection or encapsulation is required. However this too may present with similar difficulties if the encapsulation layer is not carefully selected. If the encapsulation layer itself introduces dopants onto the graphene surface then a similar effect may be observed.

There exists an additional limitation on the operating temperature of the devices fabricated in this study in the substrate material. As these devices were fabricated on Si/SiO_2 the upper temperature limit for measurements was 473 K. Whilst

this exceeds the temperature requirements for the intended application (453 K), graphene has a theoretical temperature operation far exceeding this range and as such the fabrication of devices on a SiC substrate would allow for operation at temperatures up to 673 K and perhaps beyond.

4.3 AC Characteristics of Graphene Devices

The application of the graphene Hall sensors for closed loop monitoring of power electronics circuits requires detection of PWM signals at switching speeds in the region of 100-600 kHz. Present semiconducting Hall sensors marketed as high frequency are limited to operation at <120 kHz and are typically limited to a maximum operating temperature of 150°C. Theoretical studies have shown the switching speed advantages in graphene based devices, with predicted operating frequencies in the THz region [164, 180] which far exceeds the limit of present semiconducting materials such as Si and GaAs [181].

High frequency GFETs have been demonstrated with cut off frequencies of over 300 GHz based on CVD grown graphene and epitaxial graphene on SiC technology [182]. The data in Figure 4.16 show the peak cut off frequency extracted from GFET's demonstrated in literature as a function of gate length for epitaxial graphene, CVD graphene and mechanically exfoliated graphene.

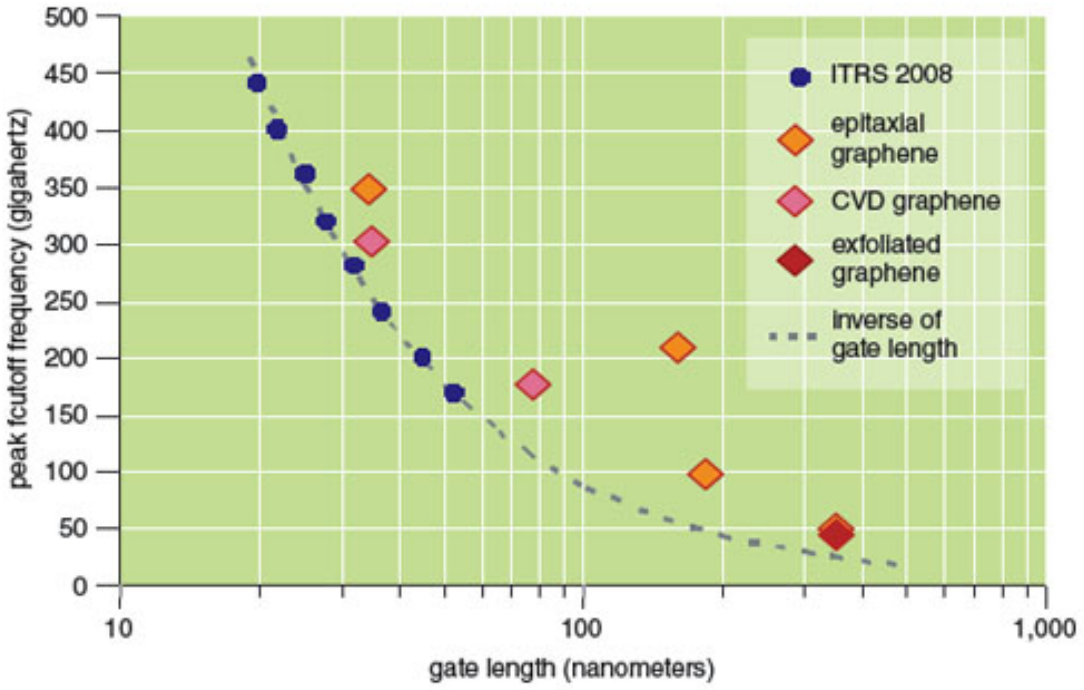


Figure 4.16: Cutoff frequency as a function of gate length for varying graphene synthesis methods. *Image taken from [183].*

In FET technology switching speed is increased through reduction in channel

length however beyond that the choice of semiconducting material is also critical to increasing the switching speed. Materials that conduct electric signals more rapidly are suited to higher frequency operation and as such carrier mobility is an important parameter to consider.

4.3.1 Test Setup

A bench top test setup allowed for measurements utilising an AC magnetic field up to 5.0 kHz and an alternating current bias up to 250 kHz. This test setup is shown in Figure 4.17. The current was driven by a Stanford voltage controlled current source (CS580), whilst the magnetic field was generated using a Kepco bipolar power supply to drive a copper wound coil. The AC signals were generated using a Keithley 3390 signal generator and a 7265 DSP lock-in amplifier to extract the signal.

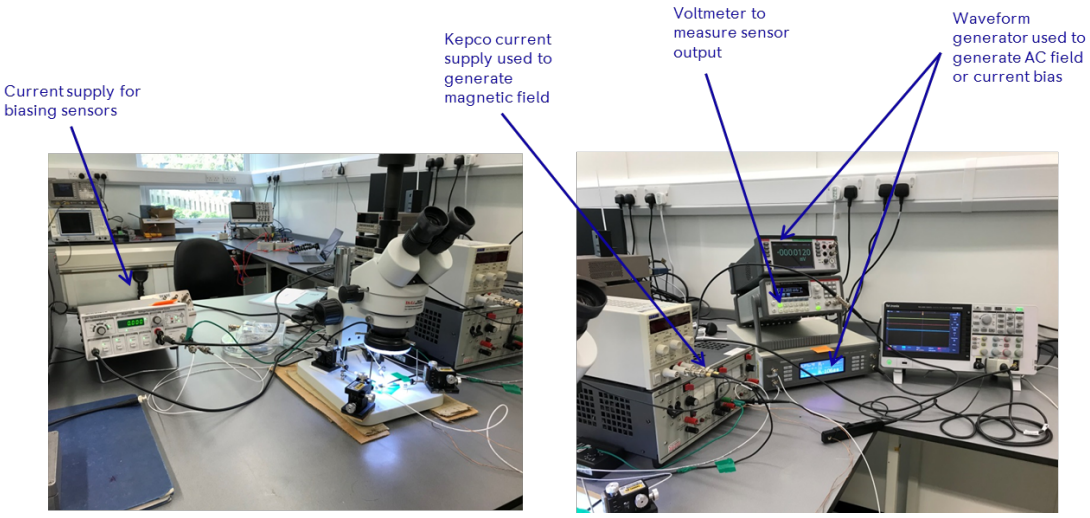


Figure 4.17: Test setup used to extract AC characteristics of the graphene Hall sensors.

There are a number of contributing factors that limit the frequency which can be driven through the system, making analysis of any extracted data particularly difficult. These factors need to be evaluated before analysing any data extracted from the test setup.

Initially considering the cables used in the test setup, these can suffer from signal loss (attenuation) originating from the following [184]:

- Radiation due to imperfect shielding
- Resistive losses in the cable conductor
- Signal absorption in the cable dielectric
- Signal reflection due to mismatches between the cable and terminations or along the cable due to non uniform impedance

Even in cables where the above are mitigated, some residual cable loss exists which can be described by Equation 4.5:

$$\alpha = 4.344 \left(\frac{R}{Z_0} \right) + 2.744 F_p \sqrt{\epsilon} f \tag{4.5}$$

where α is attenuation coefficient in dB/km, R the Ohmic resistance of the sum of the centre and outer conductors per 1.0 km of cable length at f, Z_0 the characteristic impedance in Ω, F_p the power factor of the dielectric used, ϵ the absolute permittivity of the dielectric in Fm^{-1}, and f the frequency in MHz.

The cables used in this test setup have an Ohmic resistance of 41 Ω/km and a characteristic impedance of 50 Ω. They have a polyethylene dielectric which has a power factor of 0.0002, calculated according to Equation 4.6 [185]. As the dissipation factor is <10 % then the difference with the power factor is negligible and they can be assumed to be the same. Polyethylene has a dielectric constant of 2.25 which is multiplied by the permittivity of free space (8.854×10^{-12} Fm^{-1}) to gain the absolute permittivity.

$$F_p = \frac{\tan(\delta)}{\sqrt{1 + \tan^2(\delta)}} \tag{4.6}$$

where $\tan(\delta)$ is the dissipation factor.

By combining Equations 4.5 and 4.6 the attenuation factor is calculated as a function of frequency up to 1.0 MHz with the resultant data shown in Figure 4.18. It can be seen from this data that the attenuation coefficient remains constant at 3.5 dB/km in the range of 0-1.0 MHz which far exceeds the maximum operating frequency of 250 kHz at which data were extracted for presentation in this section.

The cables used in the test setup have a length of 1.0 metre which equates to attenuation losses in the cable of 0.004 dB, at a signal level in the range of 10 mV. This amounts to a voltage loss of approximately 4.0 μV per cable. This level of loss should not have a significant impact on the data extracted during frequency measurements.

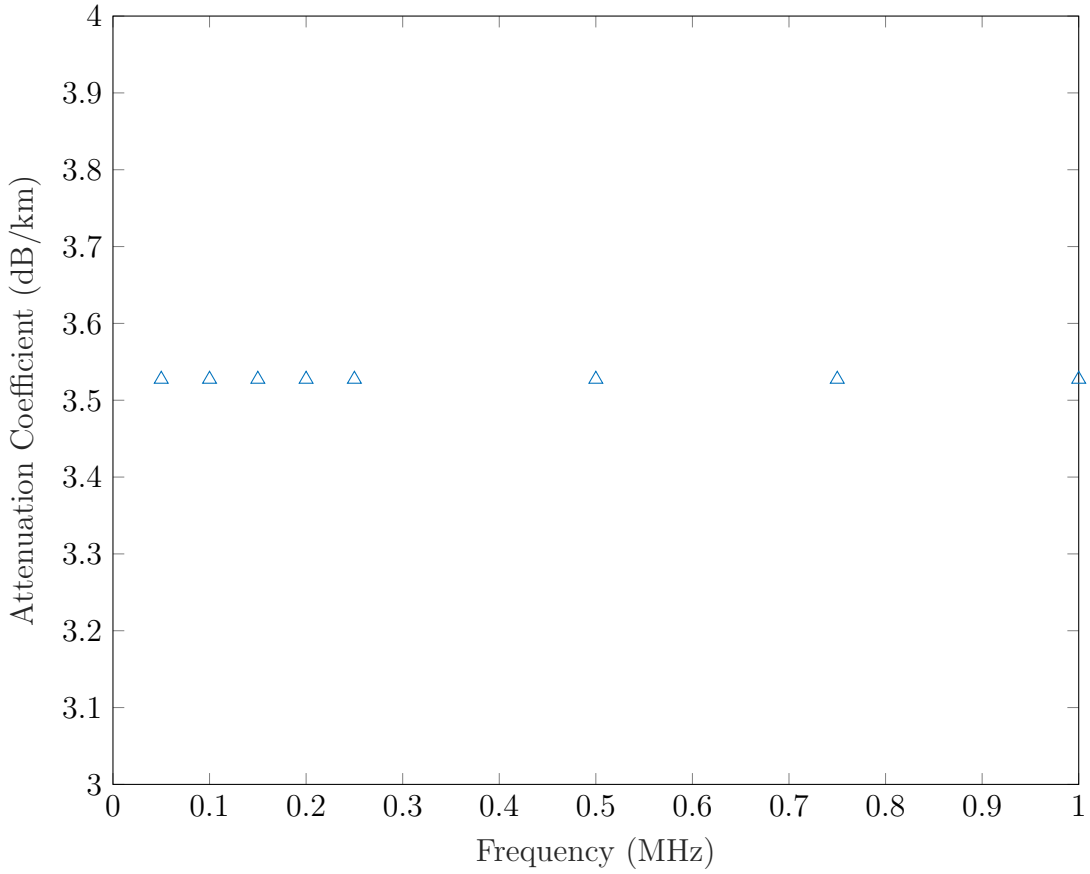


Figure 4.18: Cable attenuation coefficient as a function of frequency.

The main limitation in terms of the maximum frequency capability of the test setup should therefore be the lock-in amplifier which has a maximum operating frequency of 220 kHz and the coil used to generate the magnetic field. The limitations of the field coil will be described further in the following section. AC measurements described in the following sections were carried out on 20 devices across the three wafers fabricated using a Cu sacrificial layer, with five measurements taken per device. Errors were calculated according to the standard deviation method described in Chapter 2.

4.3.2 Alternating Magnetic Field

AC characteristics of graphene devices were initially extracted using an alternating magnetic field as this is comparable to the intended application which will see the Hall sensor detect the current flow through an inverter by detecting the magnetic field induced through a flux concentrator placed around the bus bar. The test setup used in this study however limits the generation of an alternating magnetic field with the dominating factor stemming from the current supply used to generate a field through the coil. The manual for the Kepco bipolar power supply stipulates that the output of the current channel is limited to a frequency response of just 5.0 kHz [186].

There exists an additional limitation stemming from the coil used to generate the magnetic field. The magnetic field at the centre of the coil in air can be described by Equation 4.7:

$$B = \mu_0 N I \tag{4.7}$$

where μ_0 is the field constant (1.26×10^{-6} Hm^{-1}), N the number of turns and I the current through the wire in Amps.

When driving the magnetic field with DC or at low frequency AC, the impedance of the coil remains low with the impedance typically being dominated by the parasitic resistance of the coil. However at high frequencies, this impedance is increased proportional to the frequency as can be seen from Equation 4.8:

$$|Z| = \sqrt{R^2 + (\omega L)^2} \tag{4.8}$$

where R is the resistance in Ω, ω the angular frequency in rad/s and L the inductance in Henrys.

At higher frequencies this impedance can be significantly higher than the resistance making it difficult to obtain a high current through the coil. The current through the coil is inversely proportional to the frequency and can be described by Equation 4.9:

$$I = \frac{V}{|Z|} = \frac{V}{\sqrt{R^2 + (\omega L)^2}} \tag{4.9}$$

Therefore in order to drive a high current through the coil, a high voltage driver is required. Due to this limitation, alternating magnetic field measurements were carried out at a lower frequency and device response to higher frequencies was analysed using an alternating current bias.

Devices were biased with a DC current of 2.0 mA and placed in the presence of an alternating magnetic field up to 5 kHz with a magnitude varying from 10-25 mT. The resulting frequency response of devices is shown in Figure 4.19.

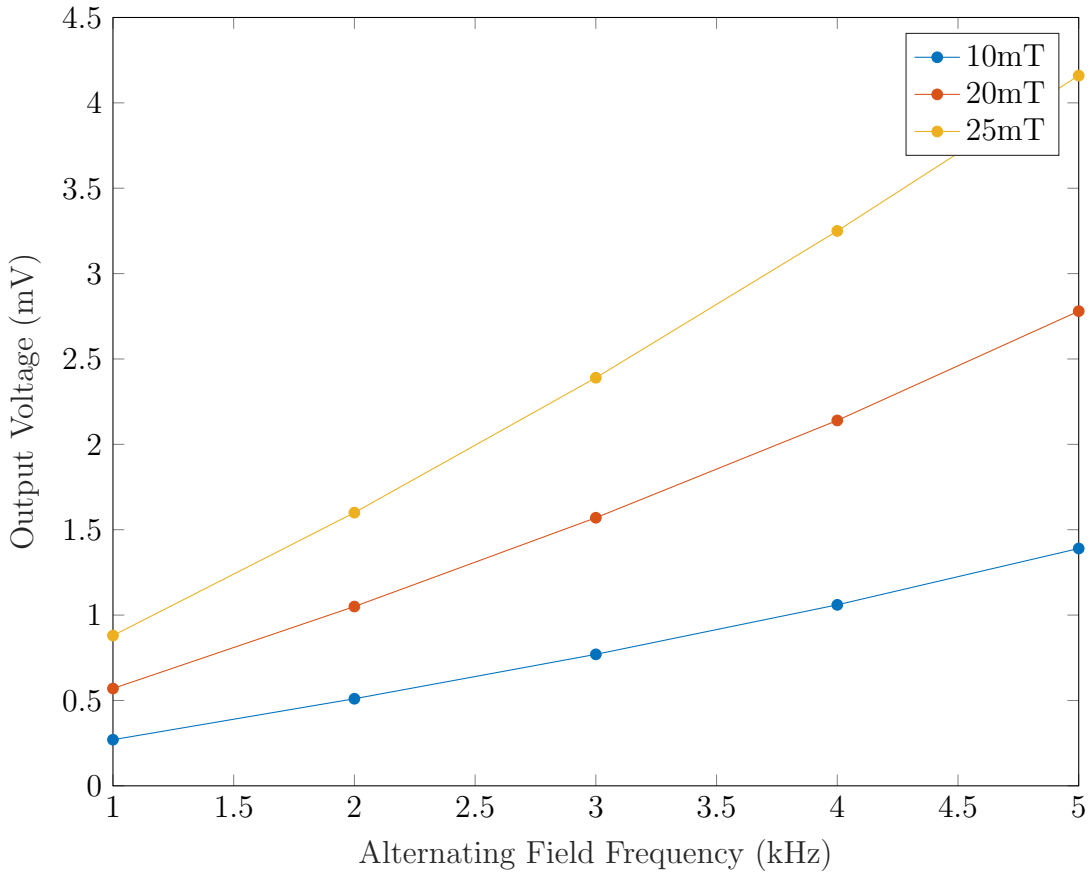


Figure 4.19: Frequency response of graphene Hall devices to an alternating magnetic field of magnitude 10 mT, 20 mT and 25 mT with a DC current bias of 2.0 mA.

Contrary to a typical frequency response, the magnitude of the output is shown to increase with increasing frequency. This is likely both due to the generation of parasitic inductances in the coil coupled with the proportional increase in impedance

with frequency. This effect can be reduced through the use of a Helmholtz coil pair [187] with the two coils placed in parallel. By placing the coils in parallel the impedance through the coils is halved and allows for generation of higher frequency magnetic fields at a cost to the magnitude of the flux density. This method was however not practical due to the sensors being unpackaged and thus requiring contact probing. As such, in order to investigate device response to higher frequencies it was deemed more practical to drive an alternating current bias whilst the magnetic field remained static.

4.3.3 Alternating Current Bias

In order to investigate the response of graphene devices at higher frequencies, the devices were tested using an alternating current bias. This allows for testing of frequencies up to 250 kHz and also reduces interference caused through driving an alternating current through the field coil which inhibited the previous test data. The test setup shown in Figure 4.17 allows a current bias to be driven at frequencies of up to 250 kHz. The alternating current bias driven at a frequency of 250 kHz is shown in Figure 4.20.

The data in Figure 4.21 show the frequency response of the Hall voltage measured on the graphene Hall sensors fabricated in this study when driven by an alternating current bias. It can be seen initially that the devices have a bandwidth of 200 kHz. This bandwidth significantly exceeds that of commercial Si devices, however is still significantly lower than the theoretical operation of graphene devices and even that of practical devices demonstrated in the literature. This limitation however is likely a limitation imposed by the test setup used for this study, with the lock-in amplifier having a maximum operating frequency of 250 kHz [188]. When comparing this to the data, it can be seen that the magnitude of the output shows the most dramatic reduction at this point suggesting this is the case.

It is evident from these data that the use of graphene sensors leads to increased bandwidth capability over that of commercially available semiconducting Hall sensors. The maximum operating frequency of the sensors reported in this section were limited by the test setup however it is expected that improved measurement

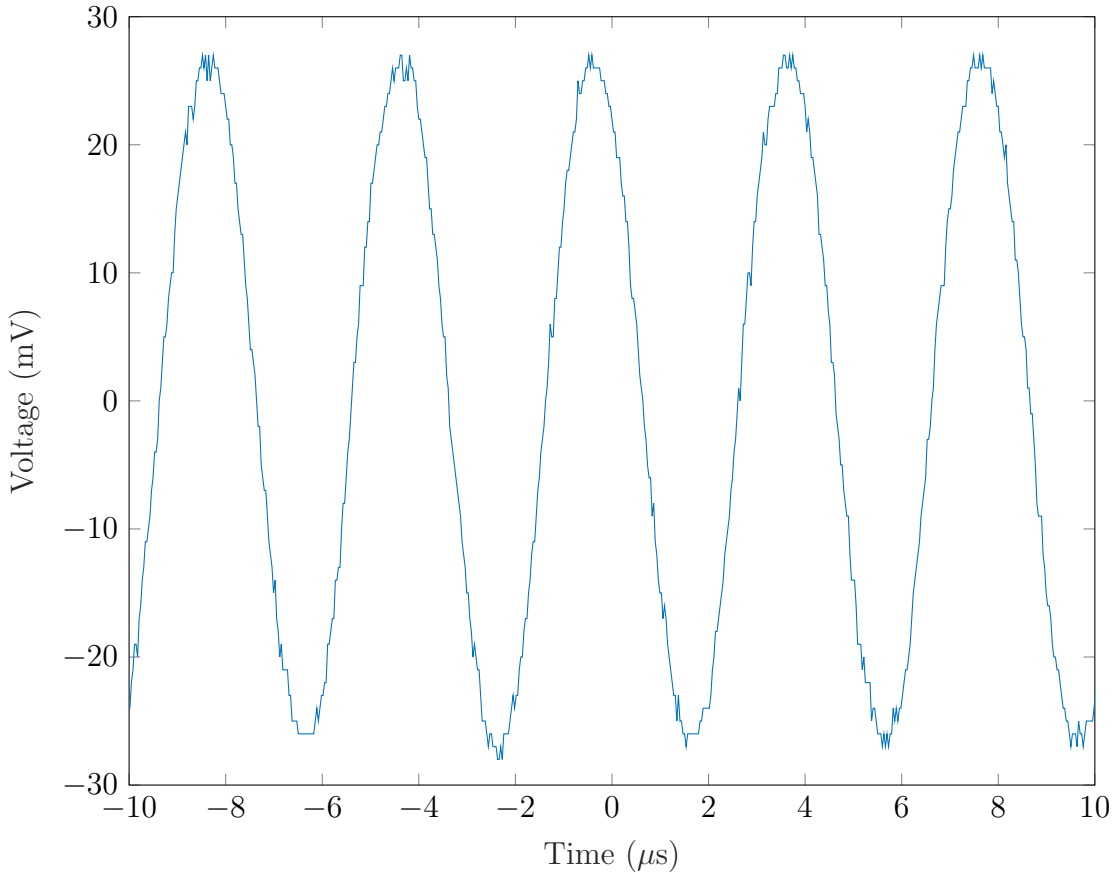


Figure 4.20: Input signal for 250 kHz alternating current bias.

capabilities would allow for a significantly increased bandwidth, potentially into the region of GHz [182]. As with the temperature capability of the devices, an appropriate packaging solution could potentially allow for additional enhancement with the reduction of parasitics in the system due to a minimised test setup.

4.4 Summary

This chapter has demonstrated the high temperature capability of graphene Hall sensors, with measurements taken up to temperatures of 473 K. High temperature characteristics of unprotected graphene devices are presented with a Gaussian trend exhibited in the thermal coefficient. Reduction of this effect and the thermal coefficient through external gate biasing is demonstrated with the thermal coefficient reduced to as low as $0.50 \pm 0.025 \times 10^3$ ppm/K. Analysis as to the root cause of this Gaussian trend is carried out with the influence of contaminants

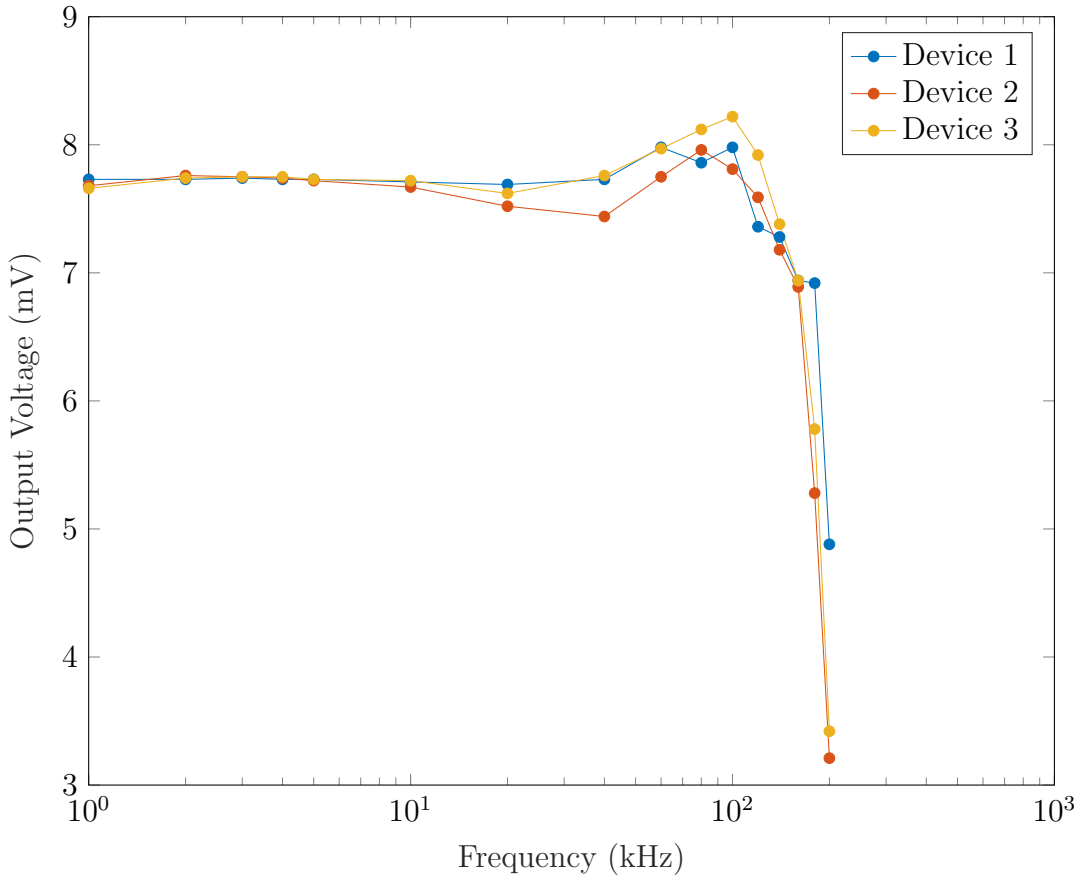


Figure 4.21: Hall sensor output as a function of frequency when subject to an alternating current bias.

and moisture on the graphene surface on the thermal stability of graphene devices demonstrated through electrical characterisation and Raman spectroscopy. It is concluded that the most likely cause of the Gaussian behaviour is moisture absorption to the graphene surface with the temperature coefficient reduced to $0.27 \pm 0.014 \times 10^3$ ppm/K post anneal. Recommendations as to how to reduce this effect in future device iterations are presented as a result of this information. AC characteristics of unprotected graphene devices up to 200 kHz are also demonstrated. Devices show stable output characteristics up to this point with drop off in output due to limitations of test setup. 200 kHz exceeds the limit on present commercial devices and the intended application for this project however results suggest graphene is capable of operating far beyond this limit. Finally, the limitations of the long term stability of these characteristics without appropriate encapsulation and packaging of graphene devices are demonstrated with suggestions as to how to optimise this for future device iterations/projects.

Chapter 5

Integration of Devices with SiC Technology

5.1 Introduction

The main intended application of the Hall sensing devices is to monitor the current flow through an inverter power module. A representative schematic of this is shown in Figure 5.1, with the Hall sensor shown to detect the magnetic flux density generated by the current flow through the inductor allowing the determination of current flow. A current source is required for the bias stage of the sensor whilst the output is shown to go through an amplification stage. The actual design of the inverter in this power module is not a focus of the research presented in this thesis however it is important to consider this input when designing the signal conditioning of the sensor output signal. This output signal requires a significant level of conditioning including offset level shifting, amplification and filtering to reduce the risk of signal attenuation and reduce any noise present in the system.

The low-level output voltage generated by Hall sensors typically requires amplification in order to provide a useable signal for processing and transmission. In addition to this a constant current source is also required in practical applications in order to allow for generation of a voltage at the output which is proportional

to that of the magnetic field the sensor is to detect. As such additional electronic circuit development is required in order to provide a functional Hall sensor package. This however does not come without challenges as these circuits are also subject to the same conditions, namely the high temperatures and high switching speeds.

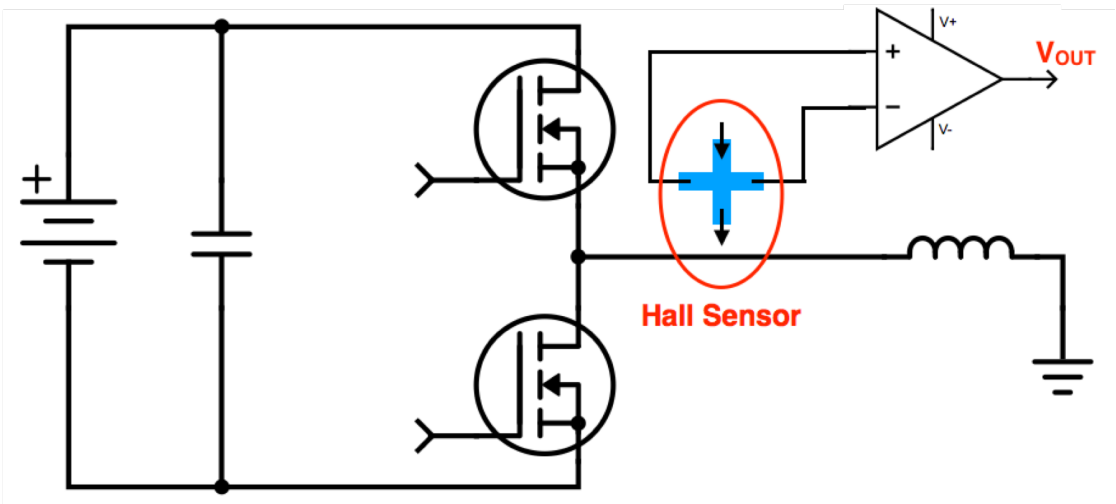


Figure 5.1: Schematic of Hall sensor detecting the flux generated by the current flow through a switched mode inverter inductor and subsequent amplification stage.

The environmental implications described in Chapter 2 mean that electronic devices designed for implementation within zone 2 of aircraft engines are likely to be SiC based. Developing circuitry utilising SiC based devices presents additional challenges. SiC based MOSFETs suffer from a number of intrinsic limitations as previously discussed in Chapter 2, namely an unstable threshold voltage due to poor gate oxide quality, restricting maximum operating temperatures to below 300°C. As such, JFETs were chosen for the realisation of these circuit designs due to the increased threshold voltage stability and reduction of intrinsic noise. The depletion mode nature of these devices however required an additional gate driver circuit to be implemented in the inverter design.

This chapter presents the analysis of the characteristics of SiC based JFETs for implementation into a representative LTSpice model. This model was then implemented into electronic circuit designs for analysis of a fully integrated Hall effect system.

5.2 SiC JFET Development

A significant amount of work has been carried out previously between initially the Emerging Technologies and Materials (ETM) research group at Newcastle University and Rolls-Royce Control Systems (RRCS). Whilst future iterations of this work has moved to Durham University, the JFETs that are to be analysed in the following sections were developed at Newcastle.

Rupert Stevens [189] designed and fabricated the n-channel SiC JFETs which will form the basis of the circuit simulations in this chapter with Chan *et al.* carrying out device characterisation [190]. The devices were fabricated with the intention of development for high temperature differential amplifiers for harsh environment applications. This work was further developed into compact modelling for development of SiC JFET integrated circuits [191]. A cross-sectional schematic of this JFET design is shown in Figure 5.2, comprising of three epitaxial layers; p-, n and p+. RIE was employed to define the isolation cell between devices with a second etch step forming the lateral extent of the gate region. Nitrogen implantation was carried out in the n epitaxy to form the n+ source and drain region, followed by activation anneal with graphite cap protection to prevent step bunching and dopant-out diffusion from the implanted region. This enables the formation of low-resistivity Ohmic contacts to the source and drain region. A SiO_2 layer was then grown under dry oxygen for surface passivation and contact windows were opened by buffered oxide (BHF) etching. Rapid thermal annealing process was performed on the subsequent contact metal deposition to form an Ohmic alloy on the source, drain, and gate regions respectively. Finally, Au was deposited on the surface and patterned using a lift off process to facilitate wire bonding.

Electrical characterisation of these devices was performed using a Keithley 4200 parameter analyser in order to extract the output characteristics of the JFETs as well as the C-V characteristics.

It is important to note that whilst extracting key JFET device characteristics for implementation into LTSpice modelling, fixed material parameters for 4H-SiC were assumed. The anisotropy of mobility often seen in SiC is not taken into

account which in turn may have an impact on the accuracy of simulations as the mobility of just a single direction is taken into account. It is also noted that whilst the frequency dependance of devices overall is taken into account, the frequency dependance of the dielectric constant is not and as such these may have an impact on high frequency operation of circuits in practice as opposed to the simulations outlined in this section. Nevertheless the simulation of JFET characteristics are deemed to have high enough accuracy for demonstration of the Hall system as a whole. Future experimental work may allow for tuning of these simulations to a higher degree of accuracy.

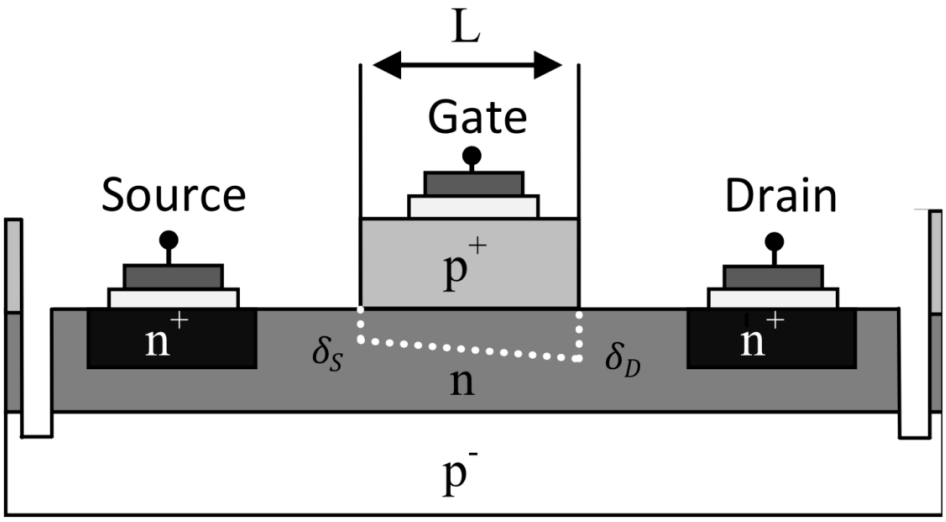


Figure 5.2: Cross-sectional schematic of SiC JFET, showing channel length and gate, source, drain contacts. *Image taken from [190].*

5.2.1 Transfer Characteristics

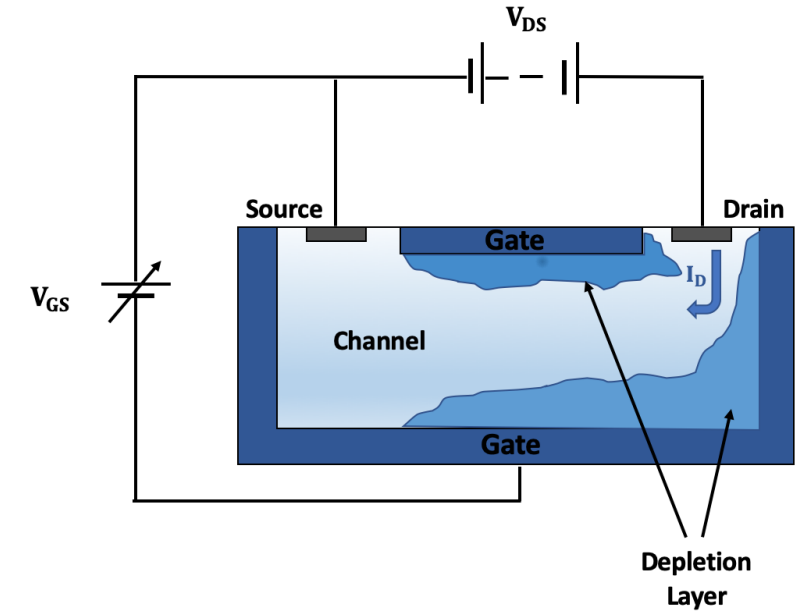
In order to analyse the transfer characteristics it is important to consider the fundamental operation of a JFET. A JFET is essentially a narrow piece of resistive semiconductor material which is either n or p type doped to form the channel region. This channel region has two electrical connections; the drain and the source. By applying a bias between these drain and source connections a current (I_D) flows between the drain and source channels, the magnitude of which can be controlled by applying a bias to the gate. This drain-source bias results in

a depletion layer forming due to the drain terminal having a higher reverse bias (V_{GD}) than at the source terminal (V_{GS}). This is demonstrated in the schematic shown in Figure 5.3a which shows the formation of this depletion region and the biasing conditions it results from.

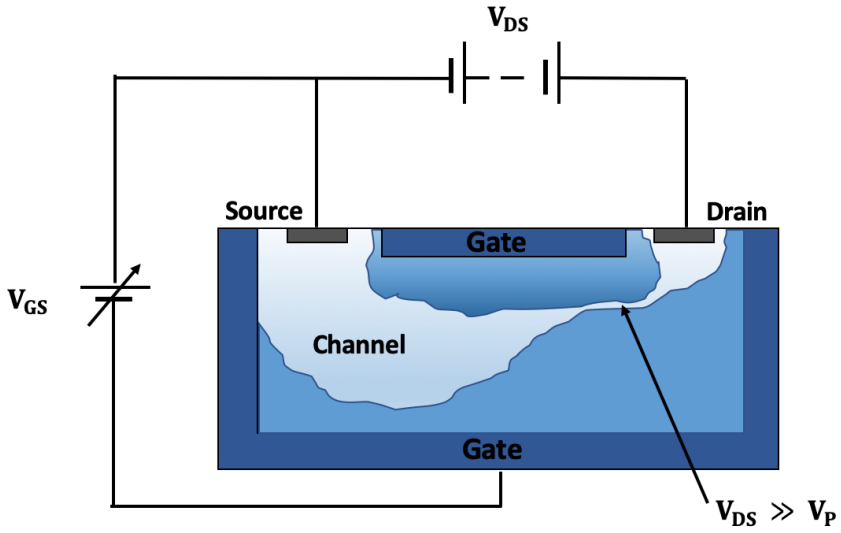
With no external gate biasing (i.e. when V_{GS}=0 V) and a low drain-source bias applied, this depletion region remains minimal and maximum current flows through the channel which is also known as the saturation current (I_{DSS}). If a negative voltage is applied to the gate the volume of the depletion region increases reducing the volume of the channel through which current can flow. The width of this depletion region is increased as the reverse bias at the gate is increased (i.e. V_{GS} becomes more negative) until the channel is 'pinched-off' and no more current can flow through this region. The gate bias at which this occurs is known as the pinch-off voltage (V_P). A schematic representation of this channel pinch-off is shown in Figure 5.3b.

Both the saturation and pinch-off regions can be seen in the typical transfer characteristics of a JFET shown in Figure 5.4. This shows the drain current as a function of both gate bias and drain-source voltage. These transfer characteristics can be split into three distinct regions of operation: the linear region where drain voltage remains low and $I_D \propto V_{DS}$, the non-linear region where $V_{DS}<V_{DSSat}$ and the saturation region where the drain current is constant and independent of the drain voltage. As the gate bias is reduced and becomes more negative there is a corresponding reduction in both the saturation current and voltage (V_{DSSat}), with a negative gate bias required to turn off the JFET.

Analysis of the transfer characteristics of the SiC JFET devices extracted by Chan *et al.* [190] allows the implementation of critical device parameters into SPICE modelling. This will allow for accurate circuit design of SiC JFET based functional primitives for integration with the graphene Hall effect sensors fabricated in this project. The parameters required for this modelling can be seen in Table 5.1.



(a)



(b)

Figure 5.3: Schematic of a lateral JFET structure showing a) the formation of the depletion region and b) channel pinch off. Gate, source, drain, channel and depletion layer regions are shown with drain-source voltage (V_{DS}), gate-source voltage (V_{GS}), pinch-off voltage (V_p) and drain current (I_D) also denoted.

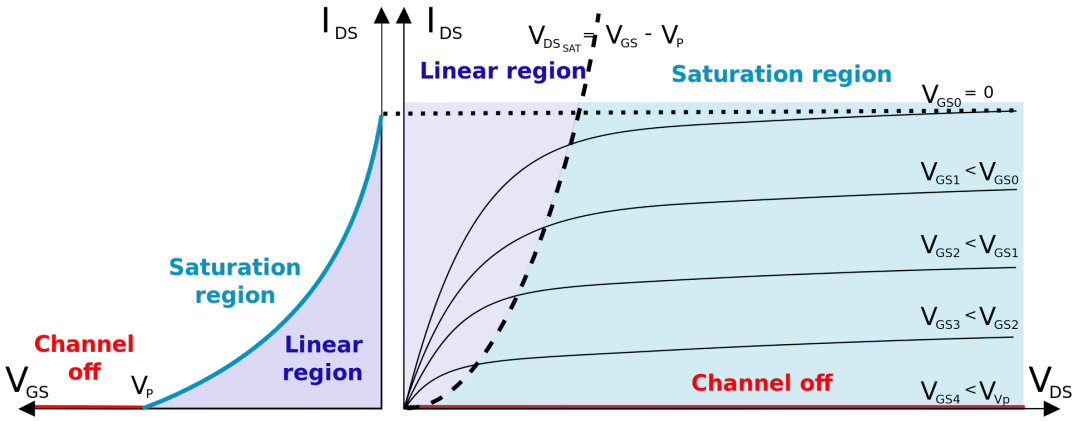


Figure 5.4: Typical JFET transfer characteristics.

Table 5.1: Default parameters for SPICE JFET model. [192].

Symbol	Parameter Name	Default Value	Unit
V_{TO}	Threshold voltage	-2.0	V
β	Transconductance parameter	10^{-4}	AV^{-2}
λ	Channel-length modulation	0	V^{-1}
r_D	Drain resistance	0	Ω
r_s	Source resistance	0	Ω
C_{GS}	Gate-source junction capacitance	0	F
C_{GD}	Gate-drain junction capacitance	0	F
ϕ_0	Gate-junction potential	1.0	V
I_s	Gate-junction saturation current	10^{-14}	A
k_f	Flicker noise coefficient	0	
a_f	Flicker noise exponent	1.0	
T	Nominal temperature	27	°C

The pinch off voltage and saturation current can be extracted from the output characteristics according to Shockley's equation which describes the drain current in the saturation region [193]:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{5.1}$$

where I_{DSS} is saturation current in Amps, V_{GS} the gate bias Volts and V_P the pinch-off voltage in Volts.

The drain current in the linear region can further be described by Equation 5.2:

$$I_D = \frac{aW}{L} q N_d \mu_n \left(1 - \sqrt{\frac{V_{GS}}{V_P}}\right) \tag{5.2}$$

where a is the channel thickness for a given V_{GS} in cm, W the channel width in cm, L the channel length in cm, q the charge of a proton ($1.6{\times}10^{-19}$ C), N_d the channel doping in cm^{-3} and μ_n the electron mobility in cm^{2}V^{-1}s^{-1}.

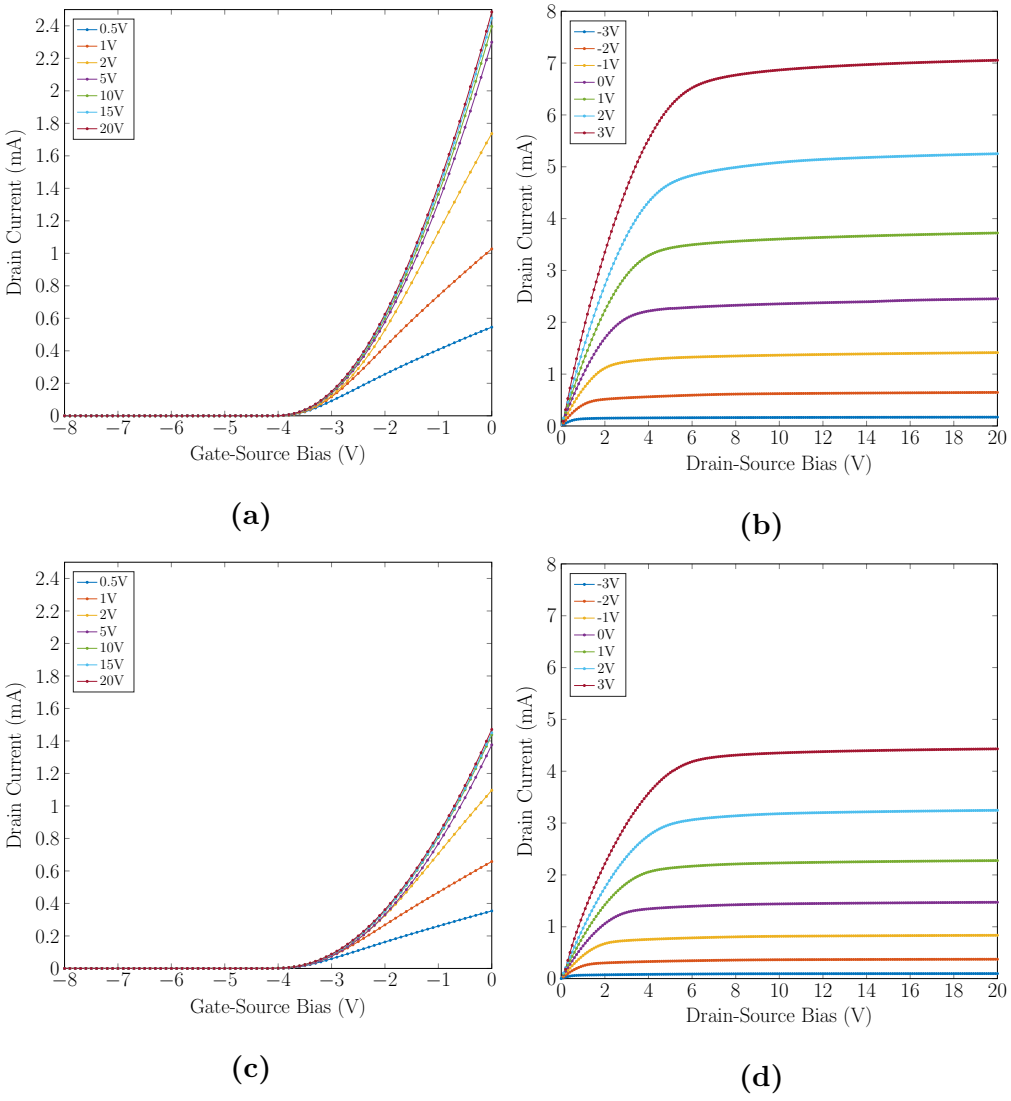


Figure 5.5: Drain current of SiC n-channel JFET's as a function of a) gate-source bias (9.0 μm channel length), b) drain-source bias (9.0 μm channel length), c) gate-source bias (15 μm channel length) and d) drain-source bias (15 μm channel length).

The data in Figure 5.5 show the output characteristics of SiC JFETs with channel lengths of 9.0 μm and 15 μm. The pinch off voltage of these devices can be observed

where fit lines cross the x-axis in Figures 5.5a and 5.5c with a value of -4.1 V extracted for both device types. However, devices with a shorter channel length exhibit a higher saturation current, which is in good agreement with Equation 5.2. The comparable pinch off voltage is however unexpected, with a negative shift in pinch off voltage typically observed in devices with a shorter gate length, attributed to reduced area of the channel region [194]. The dependance of the pinch-off voltage on the properties of the channel region can be described by Equation 5.3:

$$V_P = qN_d \frac{A^2}{2\epsilon_0 \epsilon_r} \tag{5.3}$$

where N_d is the channel doping concentration in cm^{-3}, A the area of the channel region in cm^2, ϵ_0 the permittivity of free space in Fm^{-1} and ϵ_r the material dielectric constant (9.76 in 4H-SiC) [150]. Dielectric constant is assumed to be isotropic and static for the purpose of these simulations which may need to be taken into consideration when developing circuits for higher frequency applications.

In order to investigate this further the pinch-off voltage is additionally extracted from Figures 5.5b and 5.5d. This can be done by extrapolating an exponential curve through the knee point (i.e. the point where the curve visibly bends) of the saturation region and equating the value at this point to $V_{DSsat} = V_{GS} - V_p$. This yields a value of -2.9 V for the 9.0 μm channel length devices and -3.3 V for the 15 μm channel length devices. These values are the true gate pinch-off voltage of the device with the values extracted previously more commonly referred to as the threshold voltage. This can be described by Equation 5.4 and is shown to be additionally influenced by the gate-junction potential.

$$V_{TO} = V_p - \phi_0 \tag{5.4}$$

where ϕ_0 is the gate-junction potential.

It is clear that the gate junction potential has an influence on the threshold voltage observed at this point leading to the comparable values seen previously, yielding an extracted gate junction potential of 1.2 V for devices with a 9.0 μm channel length and 0.80 V for devices with a 15 μm channel length. Both extracted values are significantly lower than the value typically observed in 4H-SiC p-n junctions

of 2.8 V [195], likely due to the variation in channel doping in order to achieve the desired pinch-off voltage.

In addition to the gate junction potential, threshold and pinch-off voltages the transconductance can also be extracted from the JFET transfer characteristics. Transconductance is the ratio of the change in drain current to the change in gate source bias with a constant drain voltage and effectively expresses the effectiveness of the control of the drain current by the gate voltage. This parameter can be described by can be Equation 5.5 with the parameter able to be extracted from the gradients of the linear region in Figures 5.5a and 5.5c.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{5.5}$$

The transconductance parameter maxima occur at V_{GS}=0 V in JFETs and is the value which is denoted in JFET datasheets and device modelling and is the value which will be implemented into the JFET SPICE modelling in this case. These maxima can be described by Equation 5.6:

$$g_{mo} = \frac{2I_{DSS}}{V_P} \tag{5.6}$$

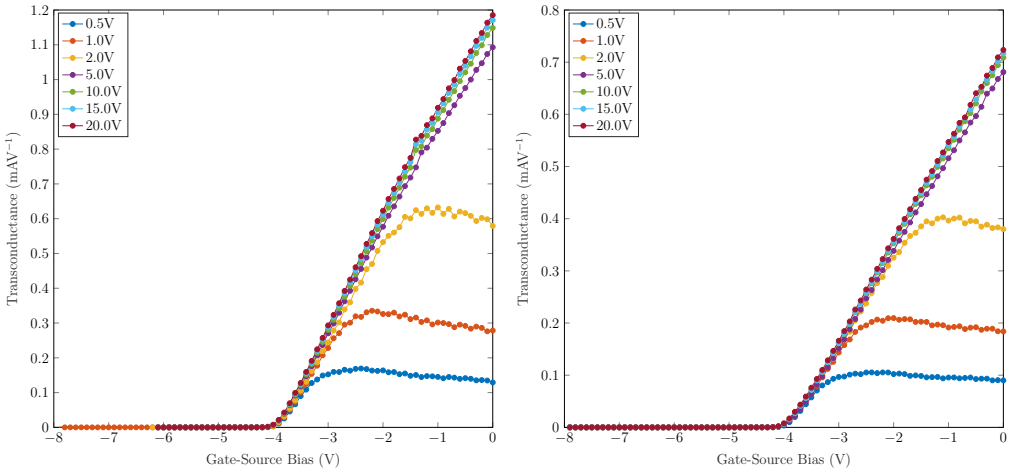


Figure 5.6: Transconductance as a function of gate-source bias with increasing drain-source bias for a) JFETs with a 9.0 μm channel length and b) JFETs with a 15 μm channel length.

The transconductance as a function of gate-source bias can be seen in Figure 5.6. It can be seen that for both 9.0 μm and 15 μm the transconductance parameter

increases with drain bias. The spread between values however begins to saturate at drain biases of above 5.0 V. As the circuit designs outlined in this chapter will be designed to run from a 12 V power source, the transconductance to be implemented into the SPICE simulations will be taken where their is a constant drain-source bias of 10 V.

This gives a transconductance of 1.2 mAV^{-1} for devices with a 9.0 μm channel length and 0.71 mAV^{-1} for devices with a 15 μm channel length. This transconductance gain however is not the same as the transconductance coefficient which can be extracted by plotting the square root of the drain current as a function of gate-source bias. The gradient of the linear region in this case is equivalent to the square root of the transconductance coefficient.

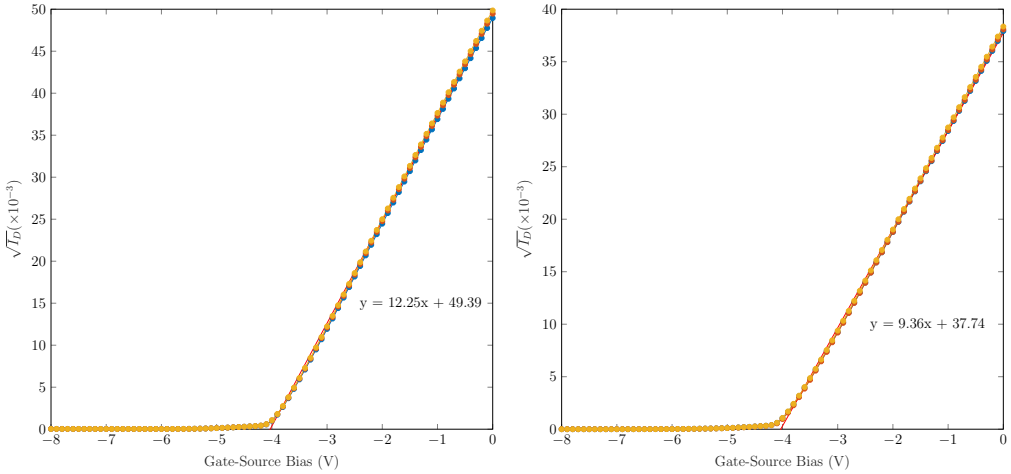


Figure 5.7: Square of drain current as a function of gate source bias for a) JFETs with a 9.0 μm channel length and b) JFETs with a 15 μm channel length for extraction of transconductance coefficient.

The data in Figure 5.7 show the square root of the drain current as a function of gate-source bias. From this the transconductance coefficient, saturation current and pinch-off voltage can be extracted. Initially considering the transconductance coefficient, this yields a value of 1.5×10^{-4} AV^{-2} for devices with a 9.0 μm channel length and 8.8×10^{-5} AV^{-2} for devices with a 15 μm channel length. The saturation current is extracted as 2.4 mA and 1.4 mA respectively. The pinch-off voltage is found to be -4.1 V for both devices. Both the drain saturation current and

pinch-off voltage can additionally be related to the transconductance coefficient, β, according to Equation 5.7:

$$\beta = \frac{I_{DSS}}{{V_p}^2} \tag{5.7}$$

Conversely the dynamic output resistance, r_d, can be described as the ratio of the change in drain-source bias to the change in drain current with a constant gate-source bias. Equation 5.8 describes this output resistance.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \tag{5.8}$$

The source resistance can in turn be described by Equation 5.9:

$$r_s = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{1}{g_m} \tag{5.9}$$

Extrapolating from the data in Figure 5.6 yields a source resistance of 0.87 kΩ for devices with a 9.0 μm channel length and 1.4 kΩ for devices with a 15 μm channel length. The dynamic output resistance can additionally be extracted from the linear region in Figures 5.5b and 5.5d yielding values of 0.45 kΩ for devices with a 9.0 μm channel length and 0.53 kΩ for devices with a 15 μm channel length. As expected devices with a shorter channel length have reduced resistance due to the fact that $R \propto L$, as can be seen from Equation 5.2.

In order to estimate the channel length modulation parameter, λ, the drain current in the pinch-off region needs to be considered. The relationship between the drain current and the channel length modulation parameter can be described by Equation 5.10 [192]:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS}) \qquad V_{DS} \geq V_{GS} - V_P \geq 0. \tag{5.10}$$

This is an extension to Equation 5.1 and describes how the impact of channel length modulation on the current in the saturation region. This parameter was extracted for drain currents in the drain region at a drain-source bias of 10 V. This yielded a value of 1.0×10^{-3} V^{-1} for devices with a 9.0 μm channel length and 5.0×10^{-2} V^{-1} for devices with a 15 μm channel length.

5.2.2 Capacitance Characteristics

The capacitance of devices at the gate-source junction were extracted as a function of gate-source bias for frequencies of 1.00 MHz, 100 kHz and 10.0 kHz. The resultant data can be used to extract the zero bias gate junction capacitance for implementation into SPICE modelling. The data in Figure 5.8 show the capacitance at the gate-source junction for devices with a 9.0 μm and 15 μm channel length respectively as a function of gate-source bias.

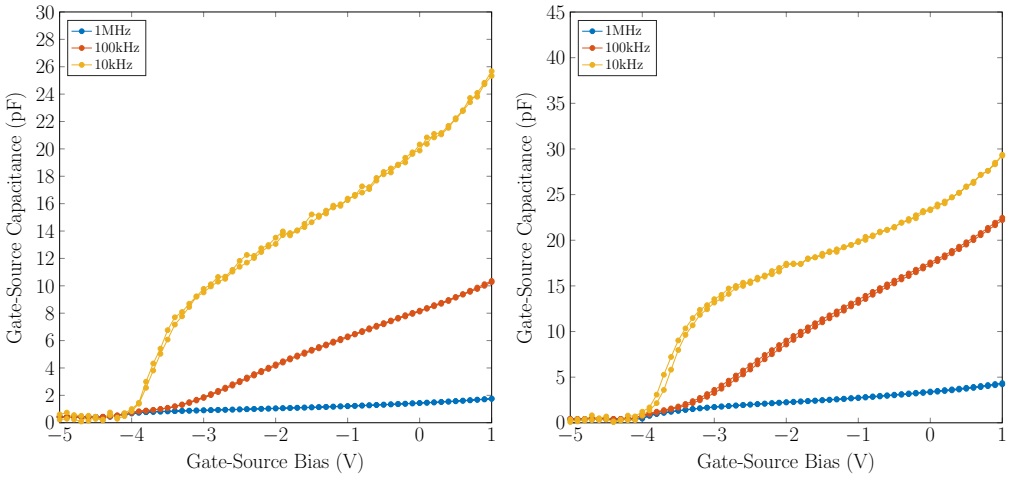


Figure 5.8: Capacitance characteristics of the gate-source junction with a) 9.0 μm channel length and b) 15 μm channel length.

The zero bias gate-source junction capacitance can be extracted from these data from the point where the gate-source bias is zero, yielding a value of 1.4 pF for devices with a 9.0 μm channel length and 3.3 pF for devices with a 15 μm channel length. As there are no data available for the capacitance at the gate-drain junction, it is assumed to be equal to that at the gate-source junction for simulation purposes.

5.2.3 Noise Characteristics

Flicker noise is a type of electronic noise which exhibits a 1/f spectral density, it is therefore also commonly referred to as 1/f noise. When present in devices it can affect the circuits ability to operate effectively, particularly when used in

power electronics and RF applications. It is caused by fluctuations in conductance, the origins of which is thought to be due to either carrier density or mobility fluctuations. Noise characteristics of individual JFET structures were extracted with further work required in the analysis of 1/f noise in differential amplifier circuits. Typically this is more difficult to determine with external biasing resulting in additional noise in the system. The spectral density of 1/f noise can be described by Equation 5.11:

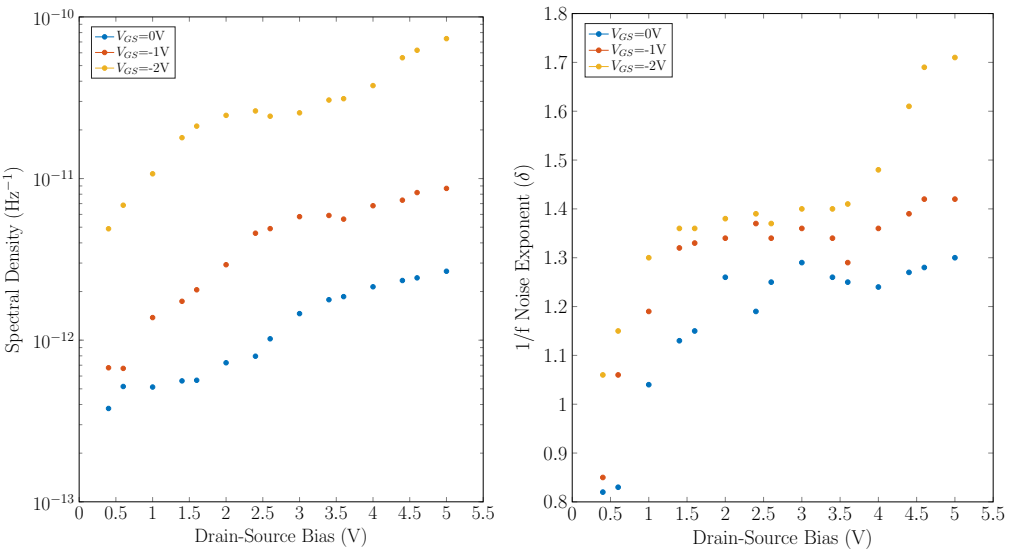
$$\frac{S_I}{I^2} = \frac{\alpha}{Nf^2} \tag{5.11}$$

where N is the number of charge carriers in cm^{-3}, f the frequency in Hz and α the Hooge parameter.

The number of charge carriers can subsequently be defined by Equation 5.12:

$$N = N_d W L \delta \tag{5.12}$$

where N_d is the doping concentration in cm^{-3}, W the width of the gate region in cm, L the length of the gate region in cm and δ the 1/f exponent.



(a) **(b)**

Figure 5.9: Noise characteristics extracted from devices with a 9.0 μm channel length over a bandwidth of 10.0 kHz showing a) spectral density as a function of drain-source bias with decreasing gate-source bias and b) noise exponent as a function of drain-source bias with decreasing gate-source bias.

The data in Figure 5.9 show both the spectral density and 1/f noise exponent of JFET devices with a 9.0 μm channel length as a function of gate-source bias. Devices additionally had a channel width of 250 μm and a doping concentration of 10^{17} cm^{-3} with measurements carried out at 10.0 kHz. It can be seen from the data in Figure 5.9 that both the spectral density and noise exponent exhibit an increase with increasing drain-source bias. It can also be observed that these values are reduced with decreasing gate-source bias. For the purposes of SPICE modelling the noise exponent that occurs at zero gate junction potential when the JFET is in the saturation region (i.e. $V_{DS} > 4.0$ V) is the value utilised. This corresponds to a value of approximately 1.3.

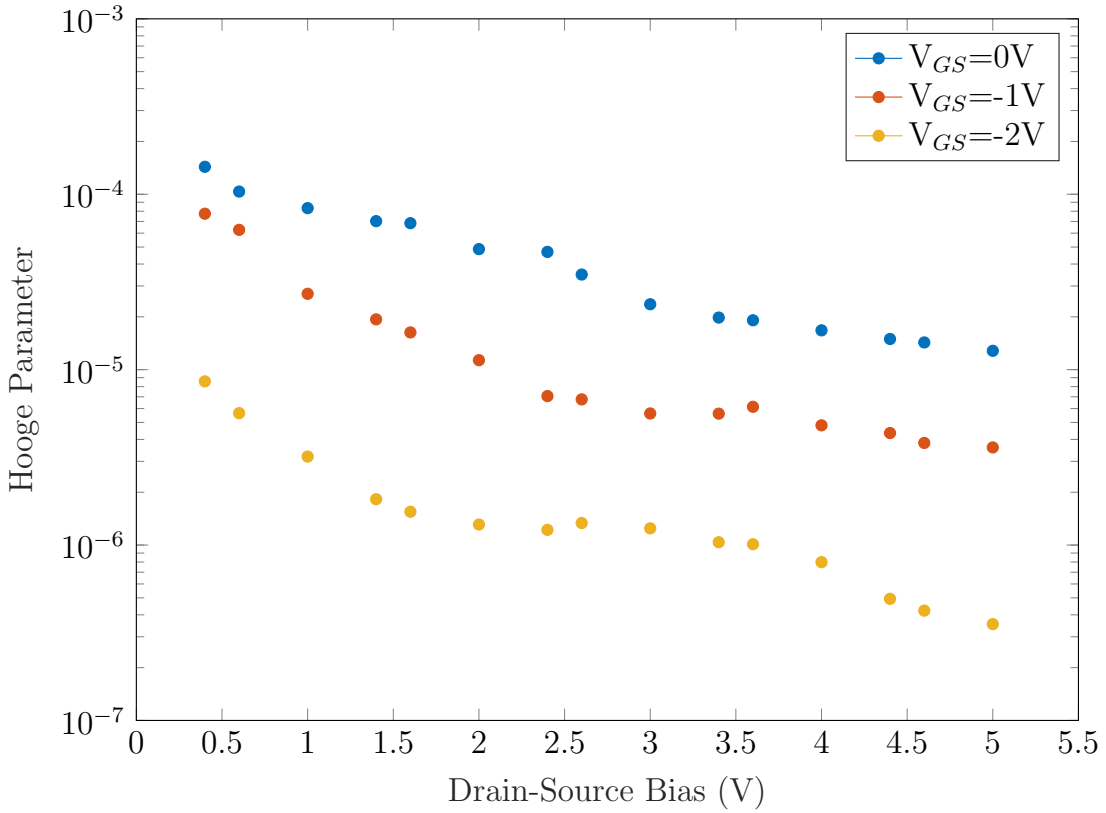


Figure 5.10: Hooge parameter as a function of drain-source bias with decreasing gate-source bias extracted from the data in Figure 5.9a.

The Hooge parameter (also commonly referred to as the noise coefficient) can be extracted from Equations 5.11 and 5.12 yielding a value of 1.4×10^{-4} increasing to 1.5×10^{-4} as drain-source bias is increased, with 0 V applied gate bias. The Hooge parameter as a function of drain source-bias with decreasing applied gate bias is shown in Figure 5.10. It can be seen from this data that as the gate-

source bias is decreased, the Hooge parameter also decreases with values as low as 10^{-7} exhibited where V_{GS}=-2.0 V. This is close to values of Si based JFETs described in literature with values of 2.0×10^{-8} observed [196]. As previously, for implementation to SPICE modelling the parameter that occurs at zero gate junction potential when $V_{DS} > 4.0$ V is the value utilised (1.3×10^{-5}).

5.3 JFET SPICE Modelling

The device parameters extracted in the previous section can be implemented into an appropriate SPICE model to provide accurate circuit designs that utilise the SIC JFET's. Key figures of merit when extracting critical device parameters from JFETs are that of the transfer and output characteristics. From this a static model can be developed and implemented into SPICE in order to provide accurate simulations of circuit designs. A typical large-signal model that can be implemented into SPICE is shown in Figure 5.11, including modelling of the charge storage that typically occurs in the two gate junctions. The parameters implemented in the LTSpice model are shown in Table 5.2 for both 9.0 μm and 15 μm channel length devices.

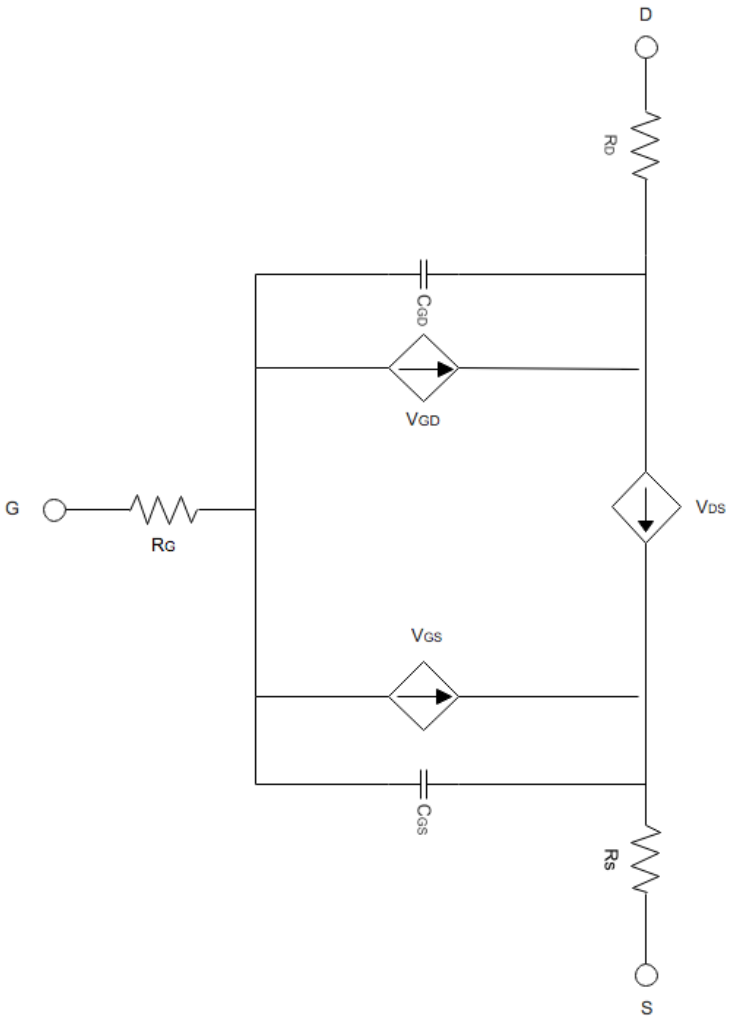


Figure 5.11: Large signal model of a n-channel JFET.

Table 5.2: Default and extracted parameters for LTSpice JFET model. [192].

Symbol	Parameter Name	Default Value	Extracted Value 9μm	Extracted Value 15μm	Unit
V_{TO}	Threshold voltage	-2.0	-4.1	-4.1	V
β	Transconductance parameter	10^{-4}	1.5×10^{-4}	8.8×10^{-5}	AV^{-2}
λ	Channel-length modulation	0	1.0×10^{-3}	5.0×10^{-2}	V^{-1}
r_D	Drain resistance	0	0.45×10^{3}	0.53×10^{3}	Ω
r_s	Source resistance	0	0.87×10^{3}	1.4×10^{3}	Ω
C_{GS}	Zero Bias Gate-source junction capacitance	0	1.4	3.3	pF
C_{GD}	Zero Bias Gate-drain junction capacitance	0	1.4	3.3	pF
ϕ_0	Gate-junction potential	1	1.2	0.8	V
$_s$	Gate-junction saturation current	10^{-14}	1.4×10^{-9}	1.1×10^{-12}	A
k_f	Flicker noise coefficient	0	1.3×10^{-5}	1.3×10^{-5}	
a_f	Flicker noise exponent	1	1.3	1.3	
T	Nominal temperature	27	27	27	°C

These parameters were input into a LTSpice model based on the large signal model seen in Figure 5.11. Transfer characteristics were subsequently simulated with drain-source bias varied from 0 to 20 V and gate-source bias varied from -8.0 to 0 V, comparable to transfer characteristics extracted from devices in Figure 5.5. The resultant data can be seen in Figure 5.12. The model in this case is specific to the JFETs used in this project for the purpose of accurate circuit simulations only and can not be applied to alternative JFET designs.

The simulated output characteristics seen in Figure 5.12 are shown to be within a 9.0 % accuracy to that of the extracted characteristics seen in Figure 5.5. This variation is however comparable to that of the variability in characteristics seen across devices ($\sim$ 10 %) [197–199] and as such it is not necessary to improve the modelling accuracy until the device process technology is further developed. For simulation purposes it is decided that devices with a 9.0 μm channel length are to be utilised in the majority of circuit designs due to the increased output current

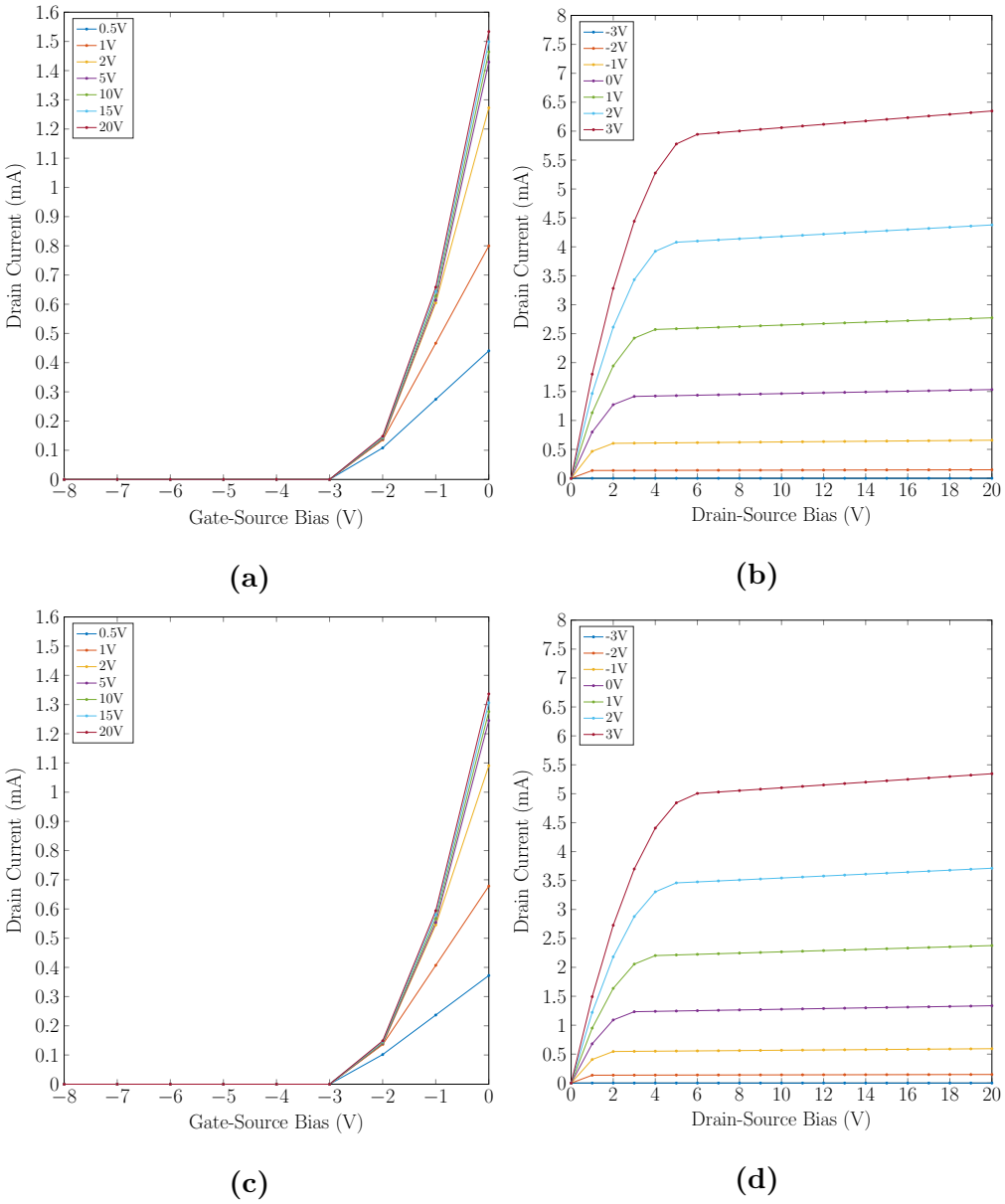


Figure 5.12: SPICE simulation of the drain current of SiC n-channel JFET's as a function of a) gate-source bias (9.0 μm channel length), b) drain-source bias (9.0 μm channel length), c) gate-source bias (15 μm channel length) and d) drain-source bias (15 μm channel length).

and transconductance. Devices with a 15 μm channel length are however utilised in current source biasing of active load differential amplifiers.

5.4 System Integration

The overall Hall sensor system is made up of two input stages (the current bias and the magnetic field) and a series of signal conditioning at the output of the Hall effect sensor. A system level block diagram is shown in Figure 5.13.

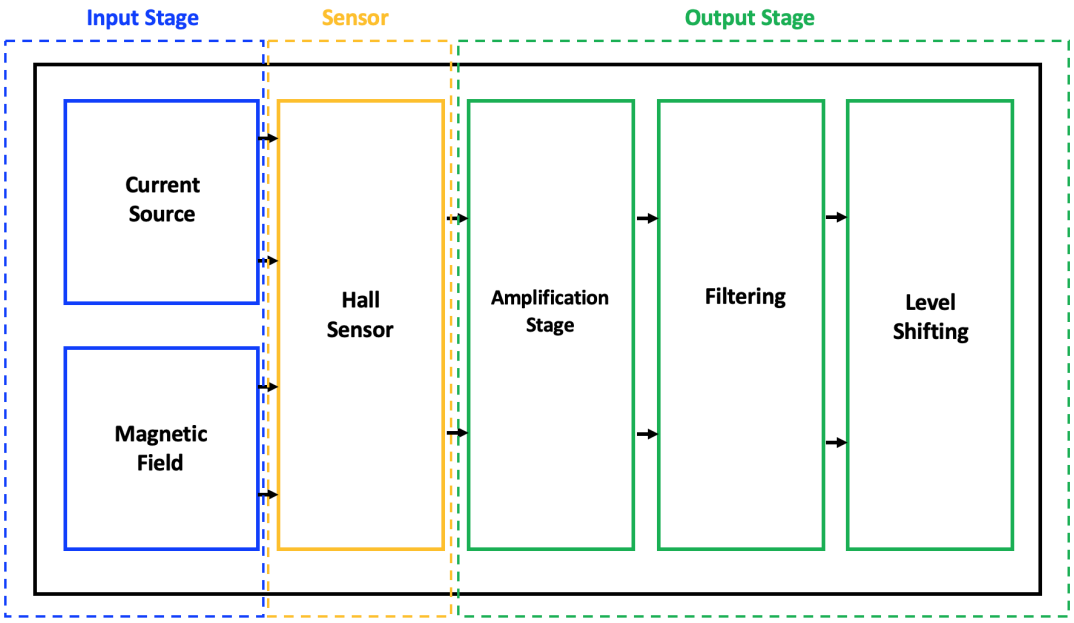


Figure 5.13: Block diagram of final integrated system showing the input stage, sensor component and output stage.

Circuit designs for this system are based on the n-channel SiC JFETs described in Section 5.3 with the simulations carried out in LTSpice utilising the previously developed JFET model. Output signal conditioning consists of an amplification stage which is necessary due to the low level signal produced at the output of the Hall sensor. Appropriate amplification can reduce the chance of signal attenuation often seen when extracting low level signals through long cables [200], this could be particularly prevalent in aerospace applications where signals will often be bundled together in a single cable harness. Amplification may also include a buffer stage due to the high output impedance of the Hall effect output signal. Level shifting is often required due to the zero field offset voltage exhibited in the output characteristics of the Hall sensors however will not be considered in this section for simulation purposes. Finally appropriate filtering, typically in the form of a low pass filter is required in order to reduce signal noise.

5.4.1 Current Source

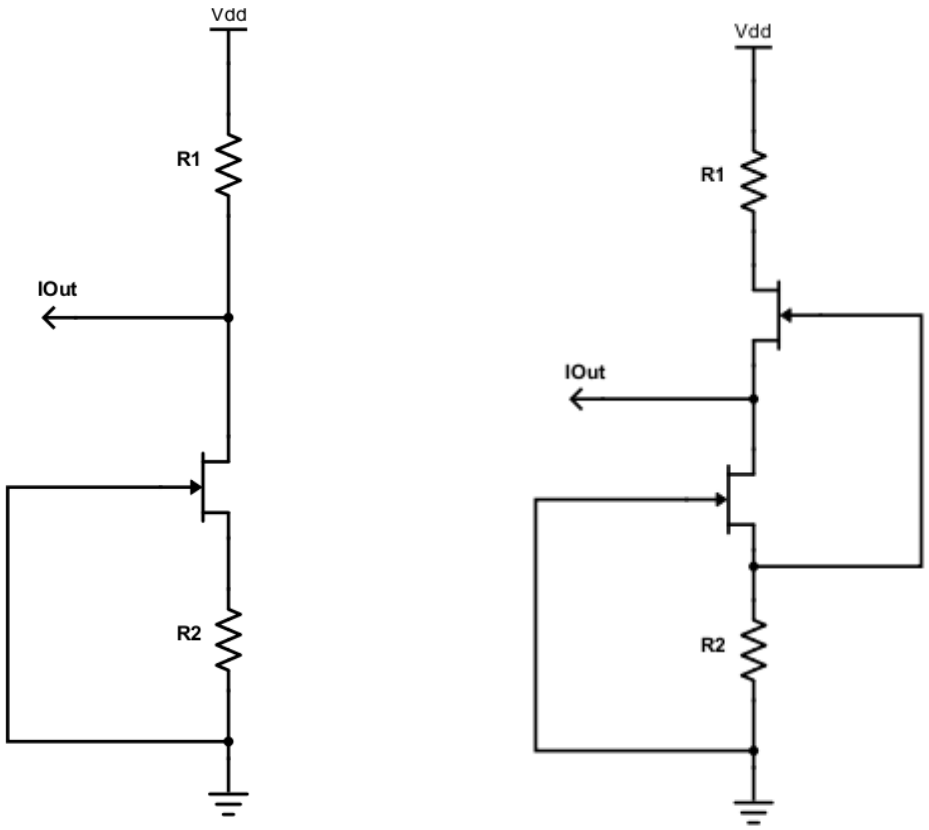
For applications that require magnetic field sensing, such as proximity sensors, a constant current source is required as part of the overall sensor system. In order for this to be fully integratable with both the Hall sensor and amplification circuitry it is necessary to use SiC JFETs for this design. JFETs can be used as a voltage controlled current source through reverse biasing of the gate-source junction, in the case of the n-channel JFET used in these simulations a negative gate-source bias is required. This can be achieved through the addition of a source resistor to self bias this junction. The voltage drop across this resistor is used to set the gate-source bias and subsequent channel current. A low value drain resistor is additionally utilised in order to limit the maximum current flow through the JFET and allow for a stable output. Figure 5.14a shows a schematic of a JFET current source in this configuration.

The source resistance value required to obtain a desired drain current can be determined by Equations 5.13 and 5.14:

$$V_{GS} = -V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \tag{5.13}$$

$$R_S = \frac{V_{GS}}{I_D} \tag{5.14}$$

The JFET devices have a pinch off voltage of -2.9 V and a drain saturation current of 2.4 mA. In order to achieve the desired drain current of 1.0 mA, a 1.0 kΩ source resistor is required. The output of the basic JFET current source as a function of gate bias with increasing source resistance can be seen in Figure 5.15a. It can be seen that the current-voltage characteristics exhibit an increase in output current after the saturation point with output current only remaining constant when a high source resistance is applied - this is expected due to the channel length modulation effects seen in short channel FETs as described in section 5.2.1. This effect is less prominent as the source resistance is increased allowing for a potentially suitable current source where R_S is in the region of 8.0 to 10 kΩ however the increased resistance results in a reduced drain current magnitude. Due to the low level output



(a) **(b)**

Figure 5.14: Schematic diagram of a) basic current source using SiC JFET and b) cascaded current source using SiC JFETs.

exhibited in Hall effect sensors it is preferred to have a higher current bias in order to maximise the Hall sensor output and reduce any potential signal attenuation associated with extracting low level signals in high noise environments [201].

A proposed solution to reduce the channel length modulation effects without significantly impacting the drain current magnitude is seen in 5.14b in the form of a cascaded current source design. The circuit utilises two JFETs in cascade configuration in order to increase the small-signal output resistance, resulting in a more constant output current due to greater saturation. The output current in the saturation region can again be controlled through self biasing the gate-source junction with a source resistor.

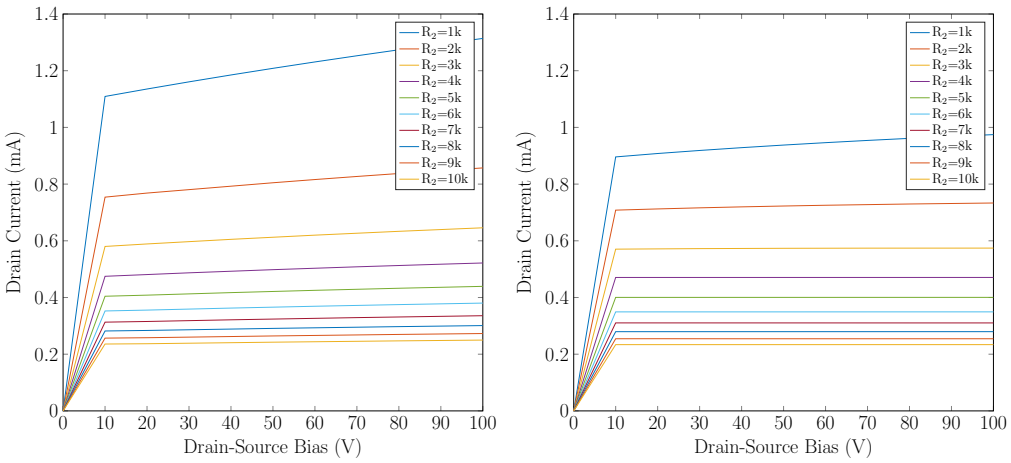


Figure 5.15: SPICE simulation of SiC current source in a) basic configuration and b) cascaded configuration for source resistances of 1.0-10 kΩ.

The drain current of the cascaded current source as a function of drain bias with increasing source resistance can be seen in Figure 5.15b. It can be seen that whilst the magnitude of the drain current exhibits a small reduction (approximately 18 % lower) likely due to the added resistance of a second JFET, the modulation is significantly reduced with a continuous current obtained in the saturation region for source resistances > 3.0 kΩ. Additionally the spread in output current increase from 10.0 to 100 V for a source resistance of 1.0 kΩ is reduced from 0.16 mA exhibited when using a basic JFET current source to 0.050 mA when using a cascaded current source.

In order to allow for a stable output with a practical magnitude for current bias, a cascaded current source configuration utilising a 2.0 kΩ source resistance is selected for simulations. This gives a stable output current bias of approximately 0.70 mA. Whilst the stability of this output could be improved through the use of a higher value source resistance, it is preferred to have a higher magnitude current bias due to allow for generation of a higher magnitude Hall voltage at the sensor output.

5.4.2 Input Signal

The input signal of which the Hall sensors are designed to monitor also need to be considered in the simulations in order to gain an accurate representation of the final output signal. The graphene Hall sensors developed in this project are designed to offer over current protection to inverters used in aerospace applications. This inverter signal will operate with a minimum switching speed in the region of 10.0 kHz, requiring the Hall sensor to be capable of sampling frequencies of at least 100 kHz in order to accurately detect the signal. The AC measurements demonstrated in Section 4.2 have shown that the Hall sensor fabricated in this study have a minimum bandwidth of 200 kHz, confirming their suitability for this application.

The inverter output signal was represented in LTSpice by generating a PWM wave with a 10.0 kHz switching frequency and amplitude of ±270 V. This amplitude was selected as this is the most common supply voltage used in medium power inverters for the desired application. In order to generate a magnetic field for the sensor to detect, a flux concentrator is to be placed around the bus bar which is represented by flowing the current through an inductor in simulations. The subsequent circuit schematic of the simulated PWM signal and flux concentrator is shown in Figure 5.16 with the subsequent output signal shown in Figure 5.17.

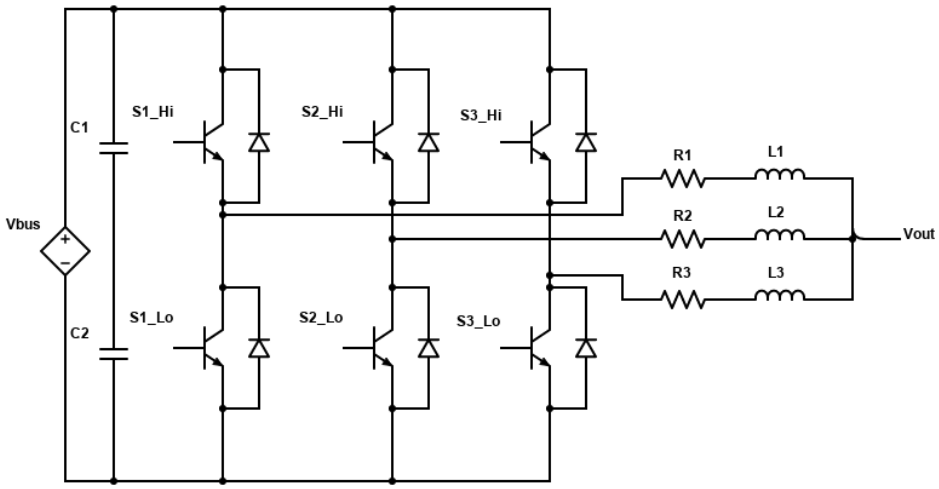


Figure 5.16: Circuit schematic of three-phase input inverter.

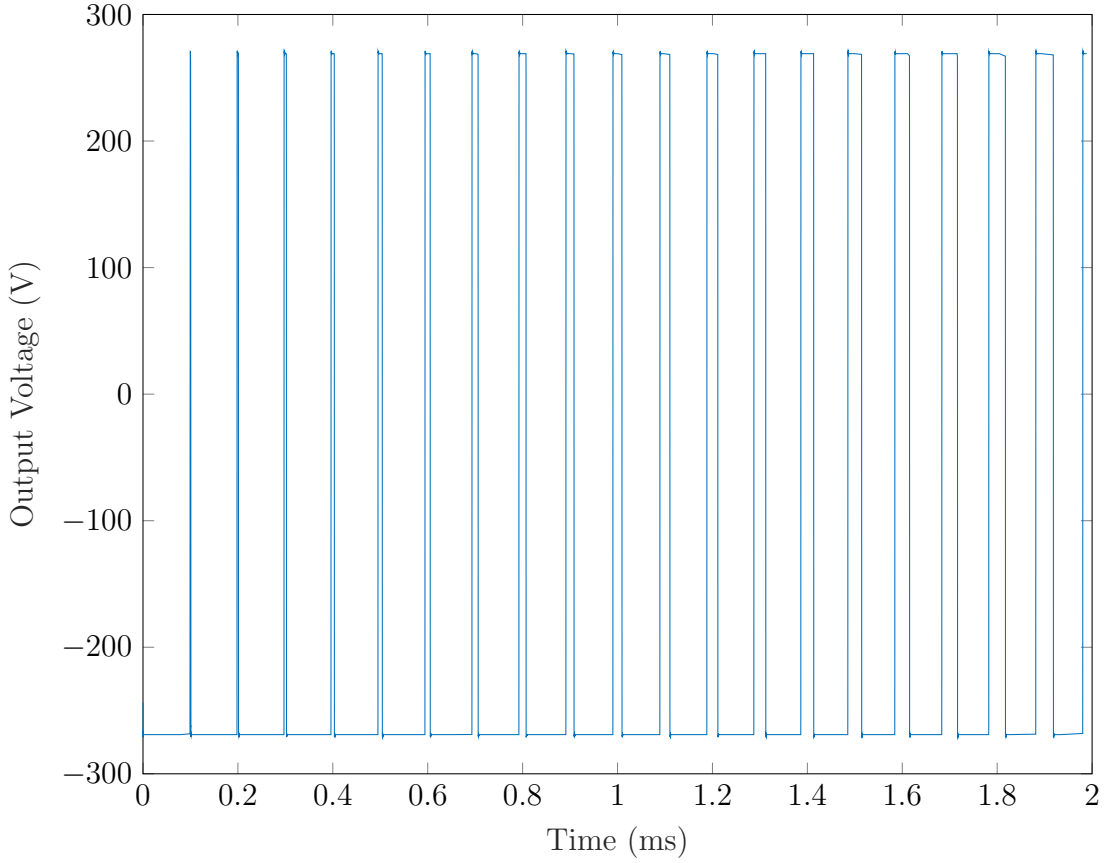


Figure 5.17: Simulated output waveform of three-phase input inverter.

5.4.3 Hall Effect Sensor

Both the current source and PWM signal models can be used to develop an accurate equivalent circuit model of the Hall effect sensors developed in this study. The circuit model is to be developed based on an input current bias of 0.70 mA and a 15 mT magnetic field for a sensor with current related sensitivity of 165±16.5 V/AT. The value of sensitivity was based on that extracted from room temperature devices in Chapter 3. Figure 5.18 shows a schematic of the model that was used to represent the Hall sensor in LTSpice. As the Hall effect sensor is essentially a resistive piece of material, it can be represented as such with the input resistance initially selected to represent that of the sheet resistance values extracted in Section 3.2.3 of 0.80±0.10 kΩ/□. The output of the Hall sensor is calculated on the basis $V \propto BI$. For an unbiased sensor with sensitivity of 165±16.5 V/AT this would result in a DC output of 1.7 mV. The input resistance in the model was then calibrated accordingly to correlate with the anticipated

output. The high output impedance of the sensors is represented by R_{Out1} and R_{Out2} with values of 0.50 MΩ utilised in both cases.

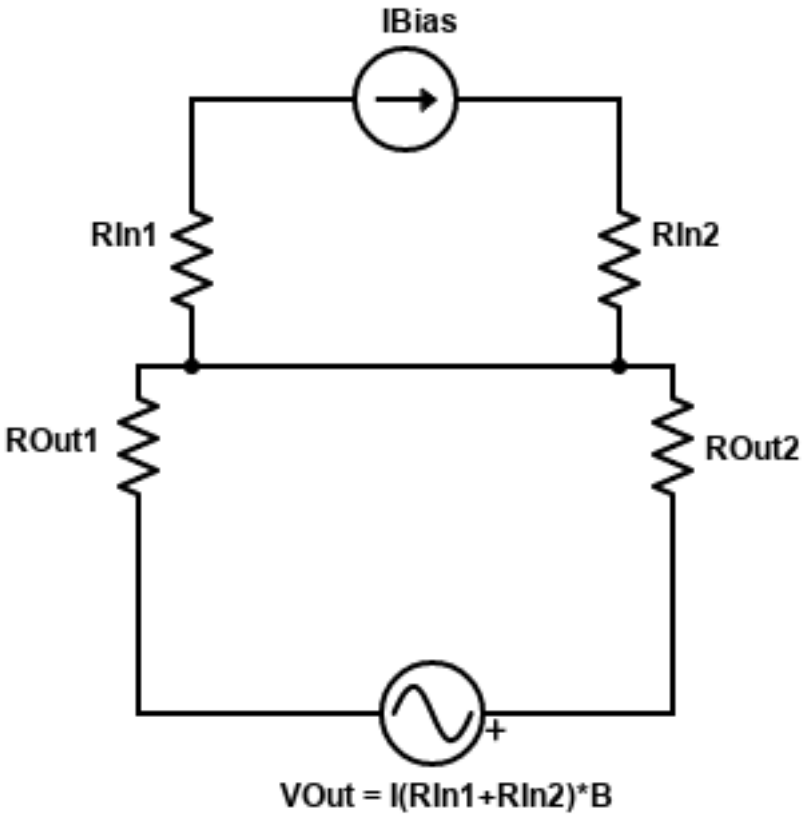


Figure 5.18: Hall sensor LTSpice schematic showing input resistors and high impedance output resistors.

For back gated sensors operating at the Dirac point a sensitivity of 972±19.0 V/AT is achievable. With a flux of 15 mT and current bias of 0.70 mA this would result in a DC Output of 10 mV. The input resistors were adjusted accordingly to a value of 0.39 kΩ. Both the DC and AC output signals for un-gated sensors and those biased at the Dirac point can be observed in Figure 5.19. It can be seen that operation at the Dirac point gives a Hall sensor output which is almost six times greater than that of un-gated sensors.

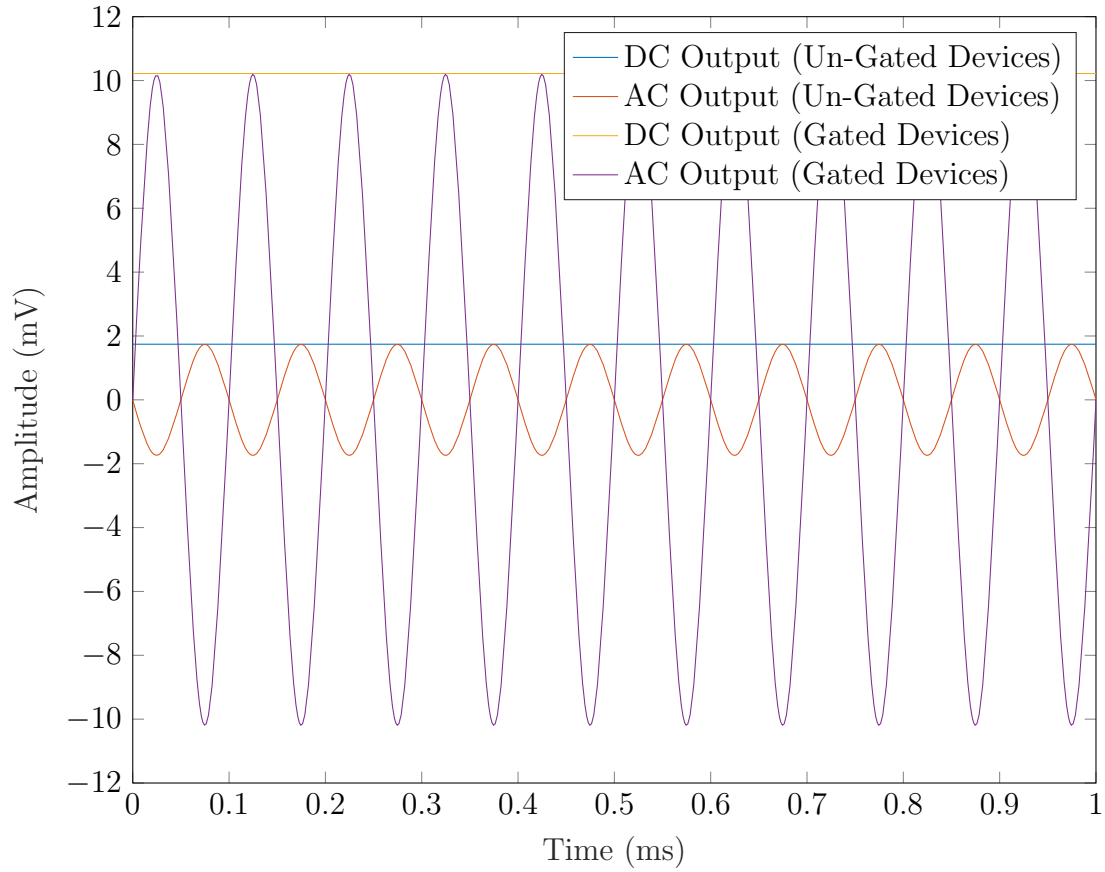


Figure 5.19: AC and DC outputs of Hall sensor model based on un-gated sensor with 0.70 mA current bias and 165 V/AT sensitivity (blue and red traces) alongside that of gated sensors with 0.70 mA current bias and 972 V/AT sensitivity (yellow and purple traces).

5.4.4 Amplifier Designs

Amplification of the output signal is required in order to reduce the risk of signal attenuation, particularly in applications which may require transferral of the signal through long cables mixed with additional signals. Hall effect sensors additionally exhibit a high output impedance which often requires buffering in order to sample the signal. As such design of amplifiers for the Hall effect system will focus on two stages; an initial unity gain buffer amplifier and a secondary differential gain stage.

Buffer Amplifier

The output of the Hall effect sensor has a high input impedance which requires buffering in order to provide a useable signal. This initial amplification stage can also be used to provide some initial gain to the output signal with the option of adding a secondary amplification stage to boost the signal further. The common drain buffer amplifier used in simulations is shown in Figure 5.20. This takes a high impedance input and provides a low impedance output with a voltage gain close to unity. The input impedance is determined by Rin_Hi and Rin_Lo with the output impedance determined by the source resistors, Rs_Hi and Rs_Lo.

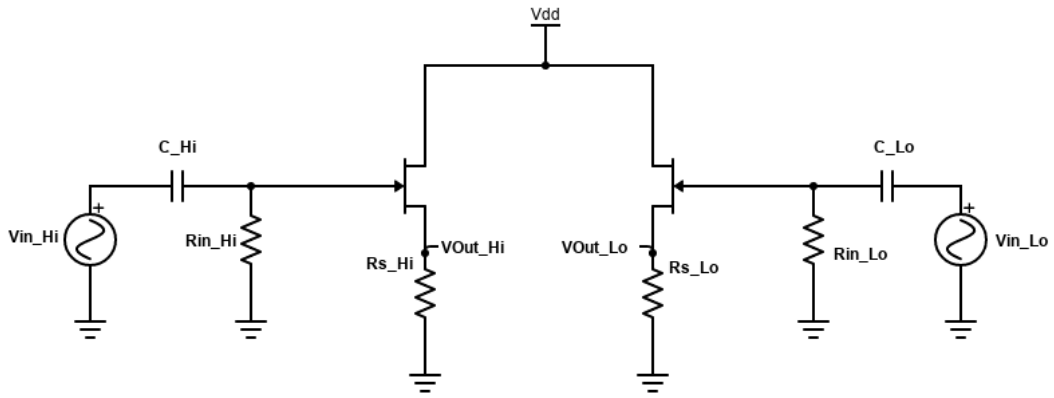


Figure 5.20: Buffer amplifier circuit schematic.

The voltage gain of this amplifier is defined by Equation 5.15:

$$A_v = \frac{v_{out}}{v_{in}} \approx 1 \tag{5.15}$$

This equation is valid when $g_m R_s \gg 1$. In the case of the SiC JFETs which these simulations are based on, the transconductance value is 1.2 mAV^{-1} and as such it is recommended to use a source resistance of at least 10 kΩ.

The data in Figure 5.21 show the output signal magnitude of the buffer amplifier as a function of source resistance. It can be seen that increasing this source resistance brings the gain closer to unity but at a cost to the output impedance with unity gain achieved for source resistances >0.20 MΩ. As the main aim of this stage is to reduce the impedance of the signal, a 30 kΩ source resistor was utilised to keep

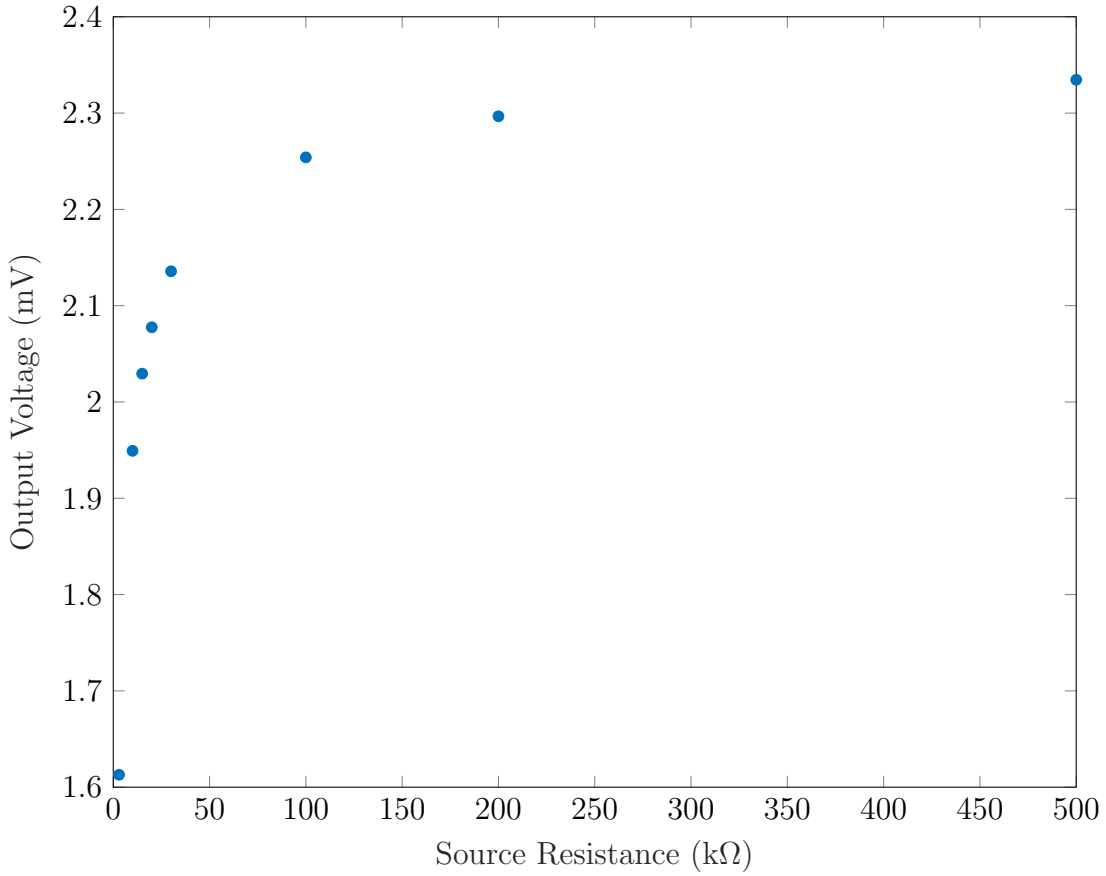


Figure 5.21: DC output voltage of buffer amplifier with increasing source resistance for a DC input of 2.4 mV.

the output impedance low with this output then fed into a secondary amplifier stage to boost the signal.

The data in Figure 5.22 show the AC output signal in response to a 2.4 mV, 10.0 kHz waveform with this amplification stage shown to have a gain <1.0 ($\sim$ 0.9) giving a signal with output amplitude of approximately 2.2 mV. Signal impedance has however been reduced from the region of MΩ down to 30 kΩ. As the main aim of the buffer stage is to reduce the signal impedance it is preferred to have this small reduction in signal amplitude at this stage with the preceding differential gain stage utilised to boost the amplitude of the final output signal that is to be used for sampling.

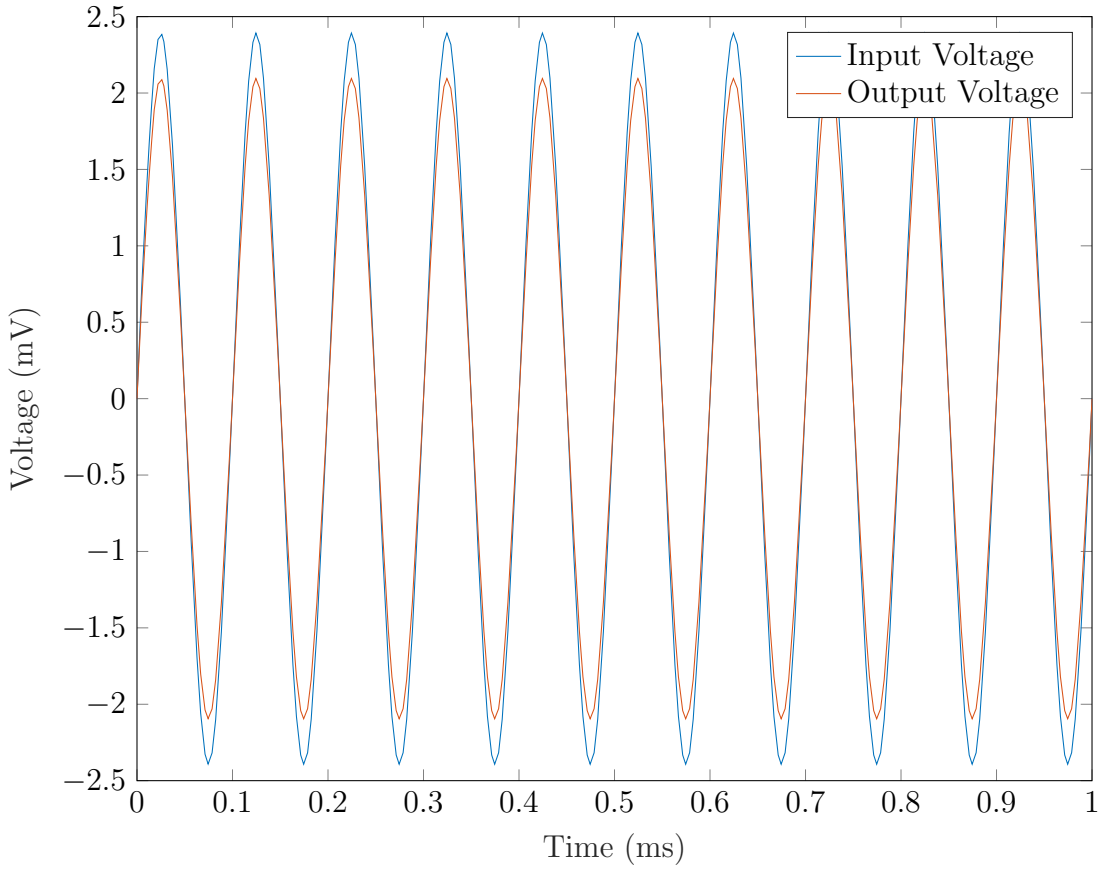
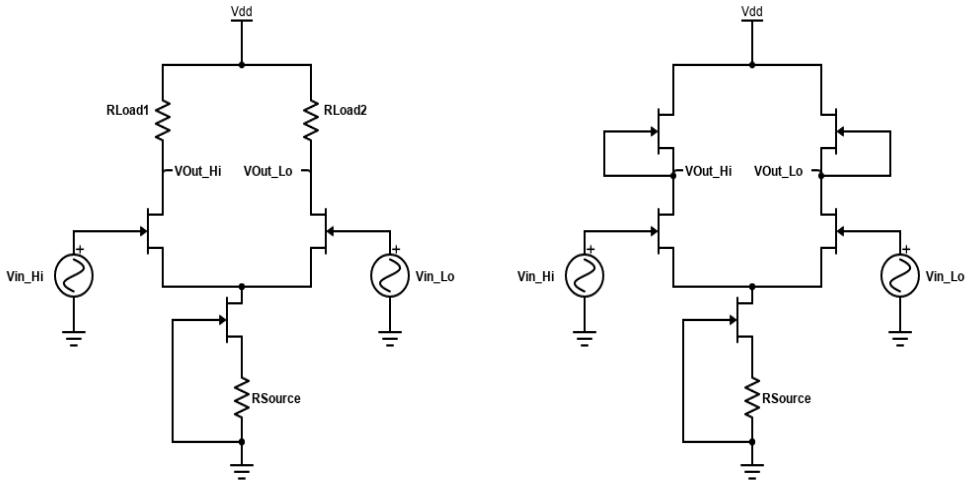


Figure 5.22: AC input and output voltage of buffer amplifier with a source resistance of 30 kΩ

Differential Amplifier

The differential pair is an ever present technology in analogue circuits. They are used to amplify the difference between two electrical input signals. Two main configurations of this circuit exist; passive load and active load. The schematics in Figure 5.23 show a differential, long-tailed pair amplifier with optional passive or active load. Typically, an active load design is used to achieve a high small-signal impedance and increase the AC gain of the single stage amplifier whereas a passive load is more often used in multiple stage amplifiers due to reduced mismatching [202–204].

The gain of a differential pair in passive load configuration can be described by Equation 5.16 whilst active load configuration is described by Equation 5.17.



(a) **(b)**

Figure 5.23: Circuit schematic of JFET differential pair showing a) passive load configuration and b) active load configuration.

$$A_V = g_m \left(R_{Load} \| \frac{1}{g_D} \right) \tag{5.16}$$

$$A_V = g_m \left(\frac{1}{g_{d-upper}} \| \frac{1}{g_{d-lower}} \right) \tag{5.17}$$

where g_m is transconductance, R_{Load} the load resistance in Ω and g_d the drain conductance.

In order to compare the two configurations, both a passive load and active load JFET differential pair were simulated in LTSpice. A 12 V supply bias was used, with a 2.0 mV, 10.0 kHz input signal. For both passive and active load configurations current sourcing was utilised through the use of a JFET current source to achieve a bias of 30 μA. This current source works with the load devices (the resistors in the case of passive and the JFETs in the case of active) to set the operating point of the differential amplifier. This allows for the amplifier output to remain constant across the whole voltage range and not respond to any changes in the common mode voltage between the differential pair.

In practical systems the voltage generated at the output of a differential pair is

the sum of both the differential gain and the common mode gain, as can be seen by Equation 5.18:

$$V_{Out} = A_{vd}v_{id} + A_{vc}v_{ic} \tag{5.18}$$

where A_{vd} is the differential voltage gain, v_{id} the difference in input voltage in Volts, A_{vc} the common mode voltage gain and v_{ic} the difference between the common mode voltage in Volts.

In order to minimise this it is important to consider the Common Mode Rejection Ratio (CMRR) which is defined as the ratio of the differential voltage gain to common voltage gain, as described by Equation 5.19:

$$\text{CMRR} = \frac{A_{vd}}{A_{vc}} \tag{5.19}$$

An ideal system would have a common-mode voltage gain of zero [205] and is ultimately the case when simulations are carried out in LTSpice. Nevertheless it is important to include the current biasing critical to minimising this factor in a practical solution when carrying out simulations.

In the case of passive load configuration the gain is the achieved through selection of an appropriate source resistance to bias the differential pair in the saturation region. For passive load differential pair with a current source bias of 30 μA, the optimum differential gain was found to occur at a load resistance of 0.50 MΩ. Biasing of active load configuration differs in that is often required to utilise a negative supply voltage in order to achieve the required biasing points. For operation in the saturation region it is required that V_{DD}=2V_{SS}. In order to achieve this without a negative supply voltage, a 15 μm transistor is used to obtain higher current source biasing ($\sim$ 0.90 mA).

The subsequent input and output voltage signals of simulated passive and active load amplifiers are shown in Figure 5.24. The data show that passive load configuration offers the highest differential gain of 35 dB. The gain of active load amplifiers is shown to be significantly lower when using a 12 V supply voltage at just 1.5 dB which is increased to 29 dB when using a 30 V supply voltage. The

differential gain achieved for the single stage passive load amplifier is comparable to those described by Patil *et al.* in literature which exhibit a single stage passive load differential gain of 40 dB [203]. As the active load configuration is shown to require a supply voltage in excess of 30 V to achieve comparable differential gain, it is decided to use a passive load configuration going forward as this is more suitable for the intended application.

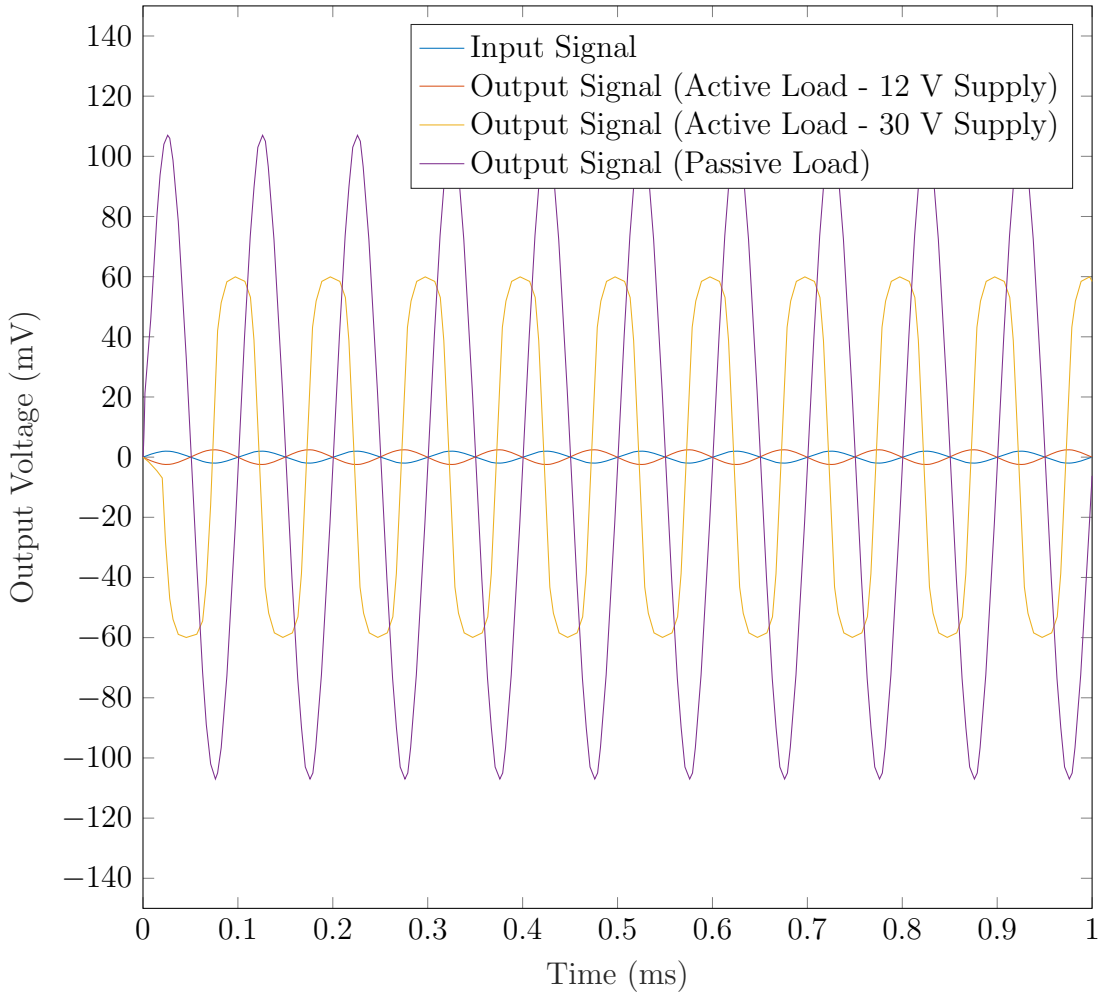


Figure 5.24: Amplitude of differential amplifier input signal (blue trace), output signal in active load configuration for a 12 V voltage supply (red trace), output signal in active load configuration for a 30 V voltage supply (yellow trace) and output signal in passive load configuration (purple trace).

Whilst the differential amplifier schematics described have a differential output, in some applications it may be more practical to convert this to single ended. In order to achieve this a current mirror load is employed as can be seen from the schematic in Figure 5.25. This current mirror effectively replicates the current seen in one

active load to control the current flow through the other. This is often employed when constructing multi stage amplifiers and may be suitable in this case for use as a comparative signal for level shifting. It however results in additional shifting of the output signal as can be seen from the data in Figure 5.26. The gain is additionally reduced to 28 dB in this case and as such a passive load configuration with differential output is employed for use in the final integrated system.

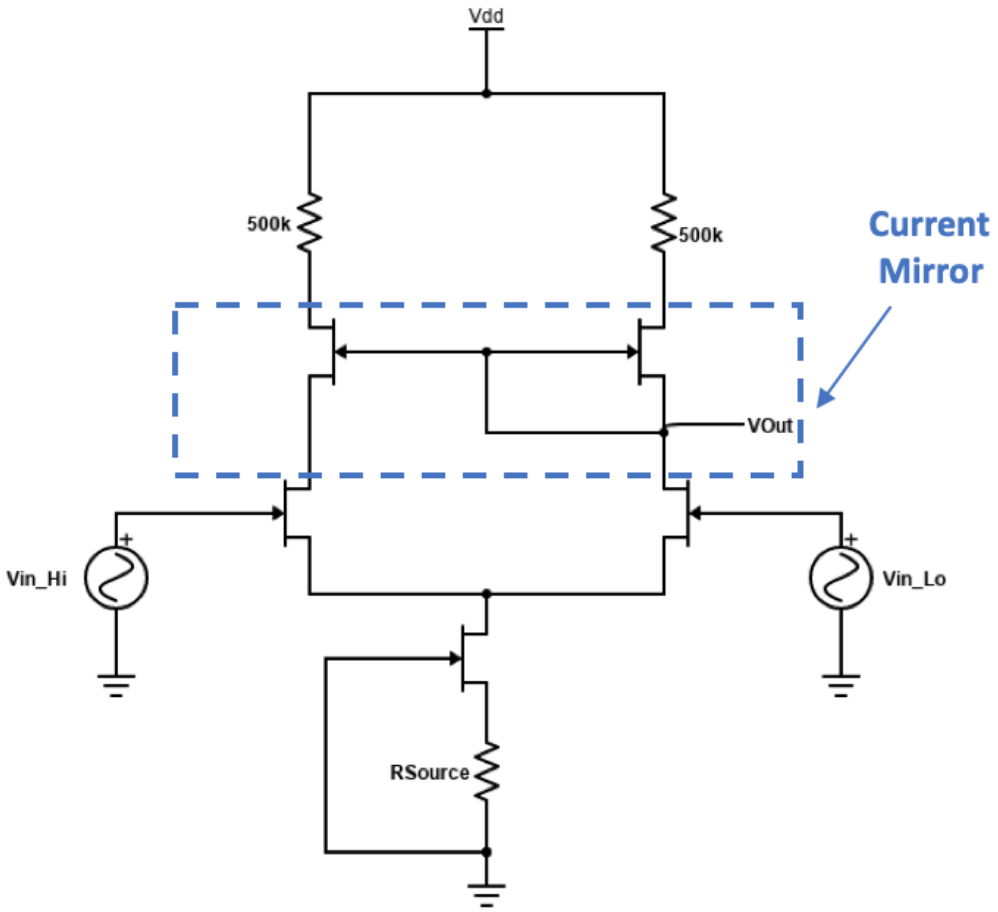


Figure 5.25: Circuit schematic of secondary gain stage with current mirror used to convert output from differential to single ended.

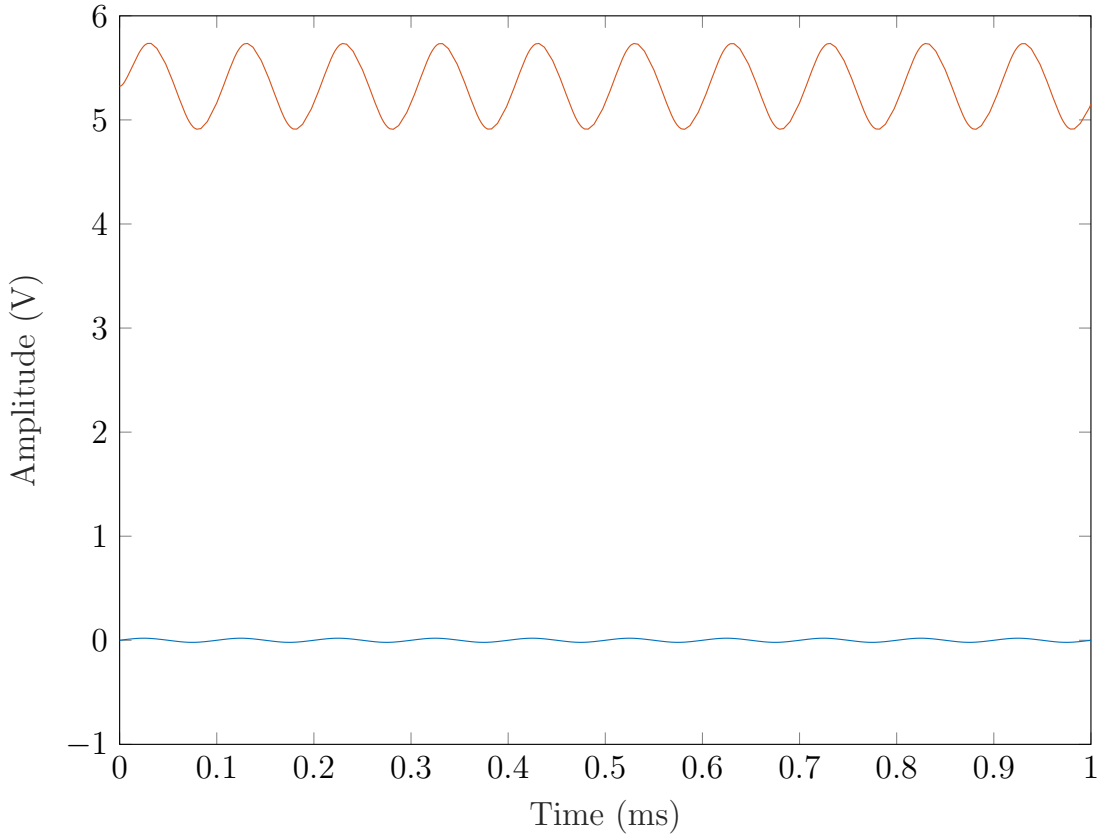


Figure 5.26: Amplitude of passive load differential amplifier with current mirror input signal (blue trace) and output signal (red trace).

5.4.5 Filtering

Filtering at the output of the Hall system is often used to remove any noise present in the system with this most commonly occurring in the form of a Low-Pass Filter (LPF). A circuit schematic of the standard RC LPF is shown in Figure 5.27.

The cut off frequency of the low-pass filter seen in Figure 5.27 can be described by Equation 5.20:

$$f_c = \frac{1}{2\pi RC} \tag{5.20}$$

where R is the resistance in Ω and C the capacitance in Farads.

The switched mode inverters at present operate at 10.0 kHz requiring a cut off frequency of 100 kHz. To achieve this requirement a resistance of 1.0 kΩ and capacitance of 1.6 nF is used with the resulting simulated frequency response

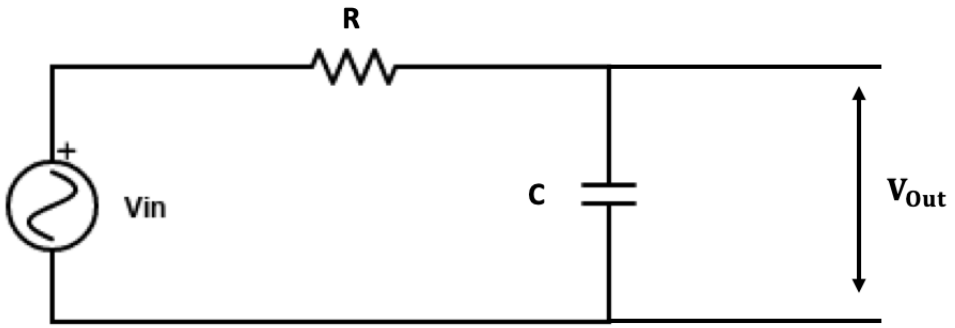


Figure 5.27: Schematic diagram of RC based Low-Pass Filter showing voltage input and output.

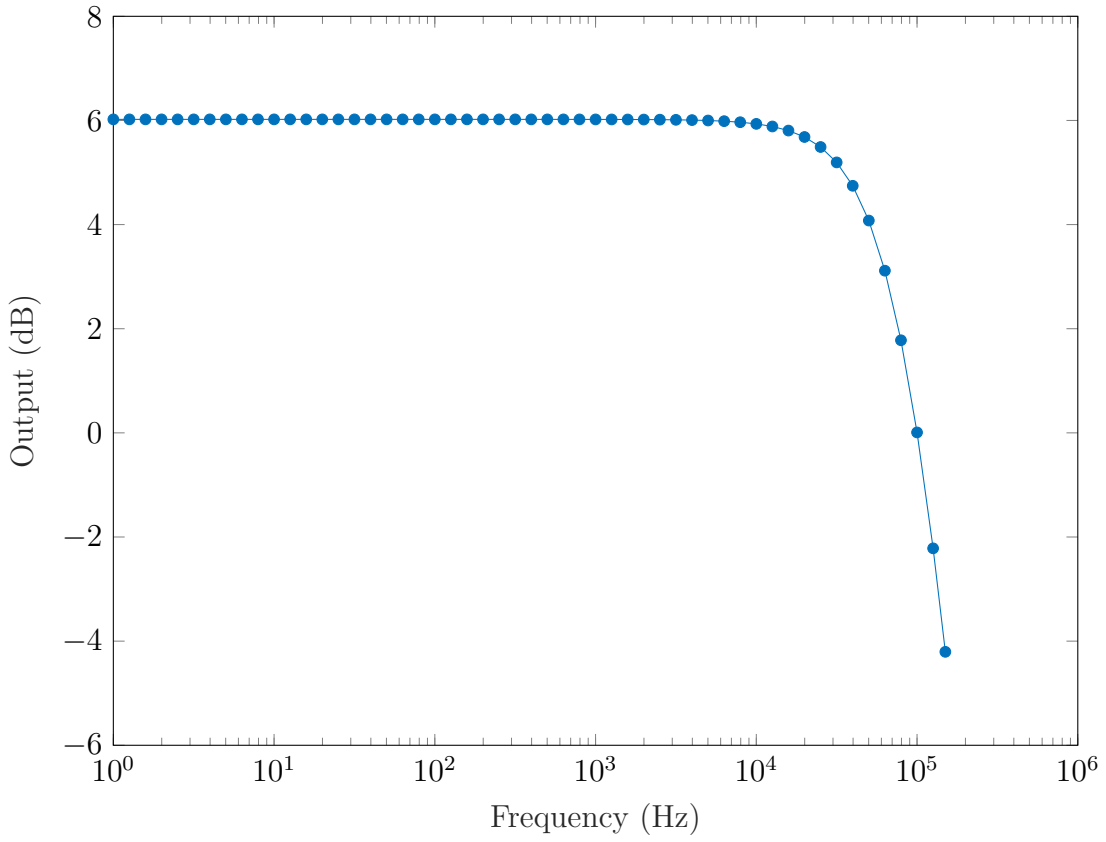


Figure 5.28: Frequency response of the low-pass filter shown in Figure 5.27 with R=1.0 kΩ and C=1.6 nF.

shown in Figure 5.28. This filtering is implemented at the input to the differential gain stage in the final system.

5.4.6 Final Integrated System

The circuit schematics developed in LTSpice were integrated into a final Hall effect system design, with the PWM wave generated in the input signal section utilised to generate the magnetic flux of which the sensor will detect. A circuit schematic of this system is shown in Figure 5.29 showing the input current bias, Hall effect sensor, buffer amplifier, filtering and differential gain stage.

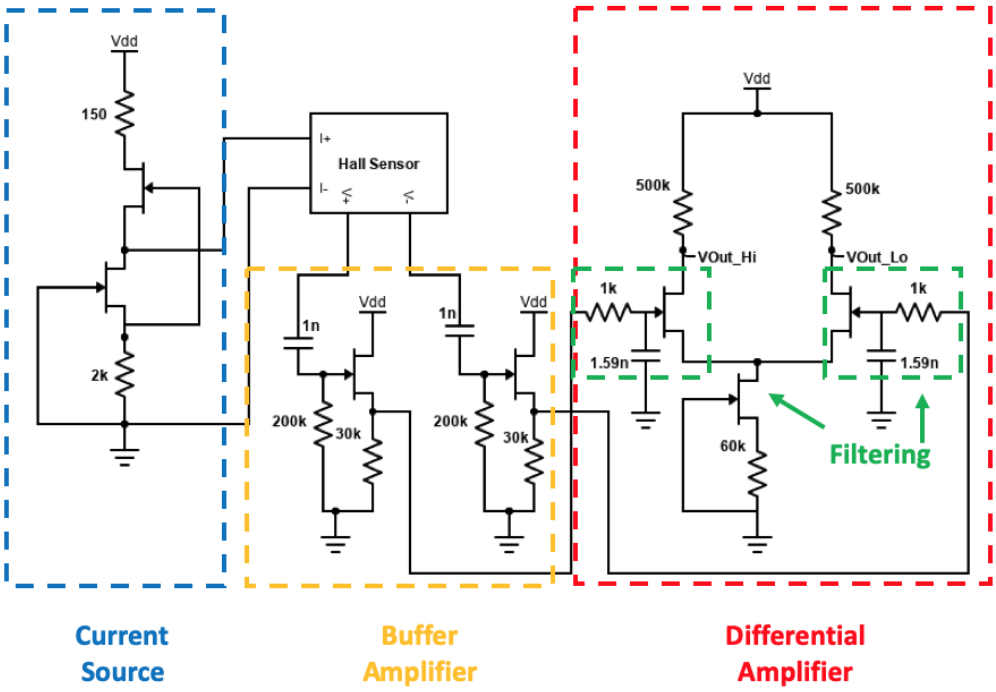


Figure 5.29: Schematic diagram of final integrated system showing input current source, Hall sensor, buffer amplifier, filtering and differential gain stage.

The full system was simulated with a DC bus voltage of ±270 V and supply voltage of 12 V. The voltage signals at the Hall sensor and buffer amplifier stages for ungated sensors and those operated at the Dirac point are shown in Figures 5.30 and 5.31 respectively.

As expected, the output at the buffer amplifier stage exhibits a slightly reduced amplitude in comparison to the signal seen at the Hall sensor output due to the less than unity gain. The voltage signals at the output to the differential gain

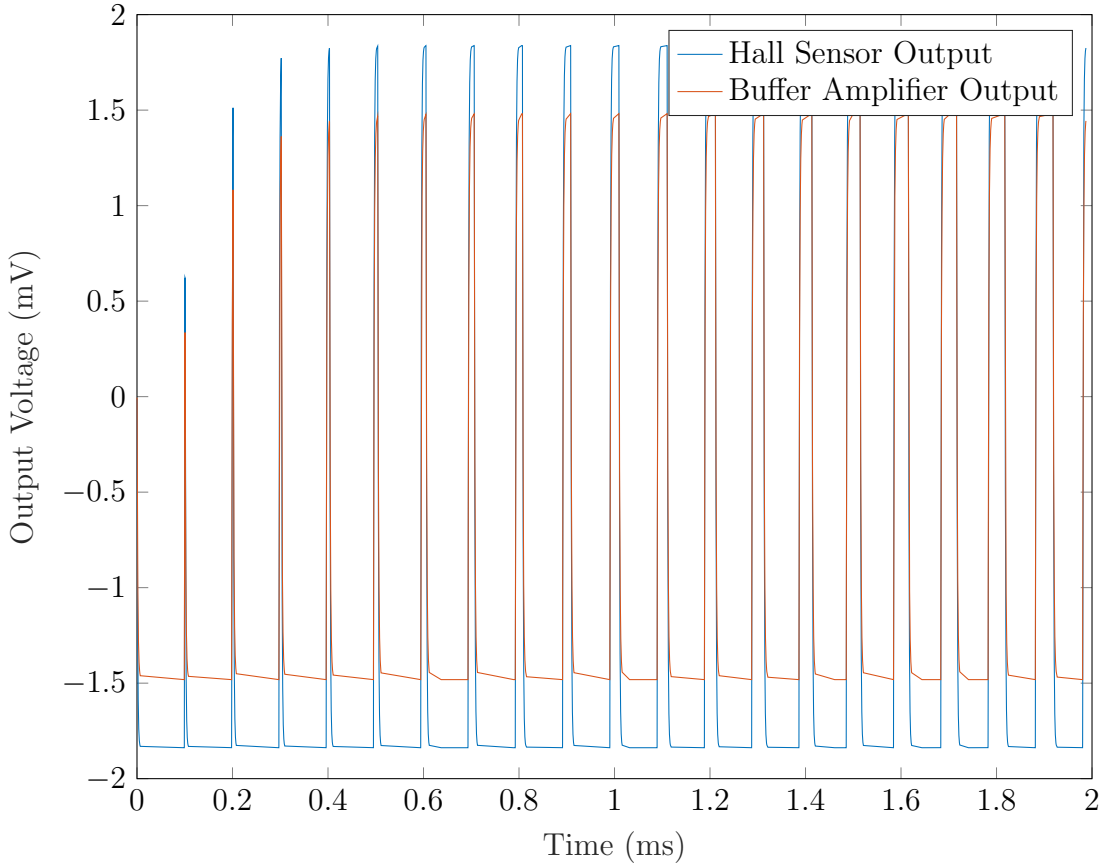


Figure 5.30: Output signals of the Hall sensor (blue trace) and buffer amplifier (red trace) in the final integrated Hall effect system for un-gated sensor simulations.

stage for both un-gated sensors and those operated at the Dirac point can be seen in Figure 5.32. It is observed that the output signal at the differential stage has an amplitude of ±70 mV for un-gated sensor systems and ±0.38 V for those operated at the Dirac point. This represents an overall system gain of 32 dB in both cases. If the application required an output signal of larger amplitude, an additional differential gain stage could be added to the output in the future.

It is observed that this simulation does not utilise level shifting which may be required for where sensors exhibit and offset voltage at zero field. This can be achieved by comparing the signal obtained at the differential gain stage output with a voltage reference signal biased to the same value as that of the offset. This will result in shifting of the output signal to be centred around 0 V.

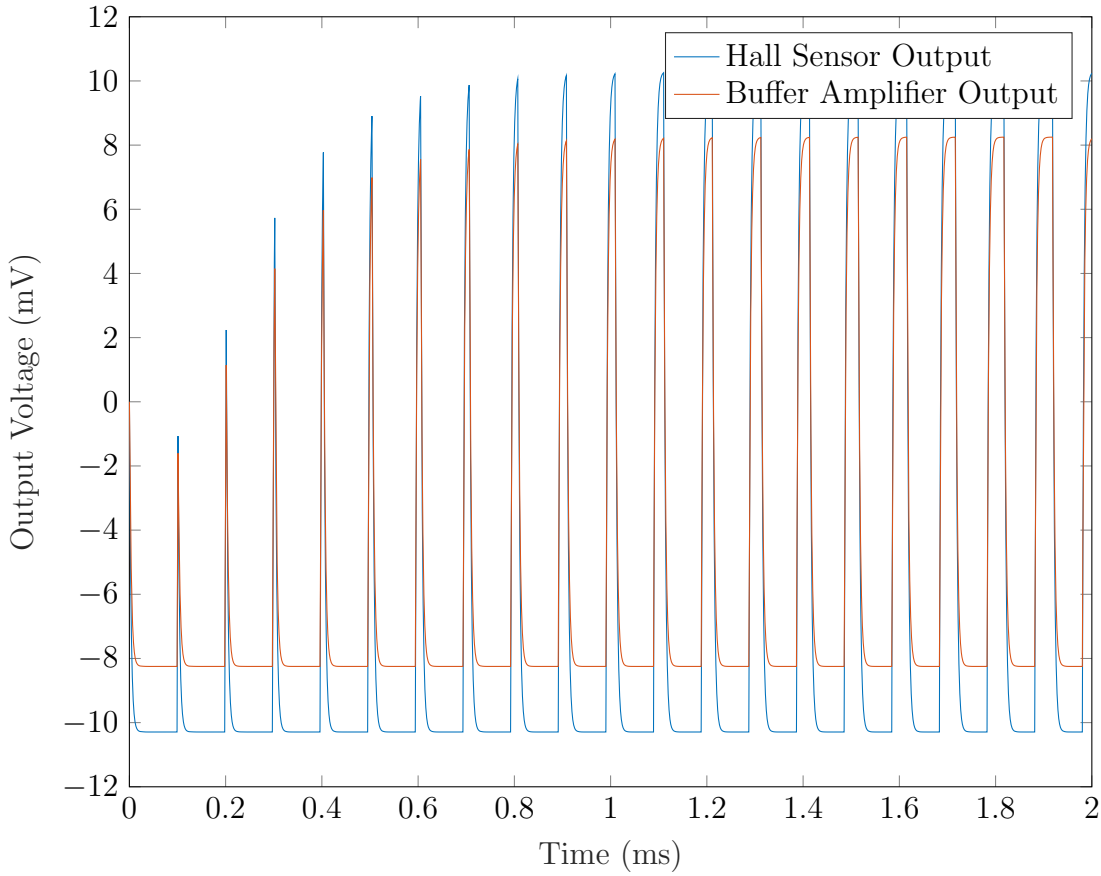


Figure 5.31: Output signals of the Hall sensor (blue trace) and buffer amplifier (red trace) in the final integrated Hall effect system for sensors biased at the Dirac point.

5.5 Summary

This chapter has demonstrated the use of n-channel SiC JFETs for development of high temperature interface circuitry required for integration with graphene Hall effect sensors. The analysis of both 9.0 μm and 15 μm channel length JFET characteristics is presented with critical electrical, capacitance and noise characteristics extracted for implementation into an LTSpice model. The JFET SPICE modelling is shown with the simulated output characteristics shown to be within 9.0 % of those extracted from functional devices. LTSpice modelling is used to develop both the input and output circuitry that forms the final Hall sensor system made up of the input current bias, the PWM signal of which the Hall sensor will detect, buffering and differential amplification of the output signal and finally level shifting and filtering. Current biasing is developed in the form of a JFET cascaded current source, providing a constant current of 0.70 mA to the sensor input. The

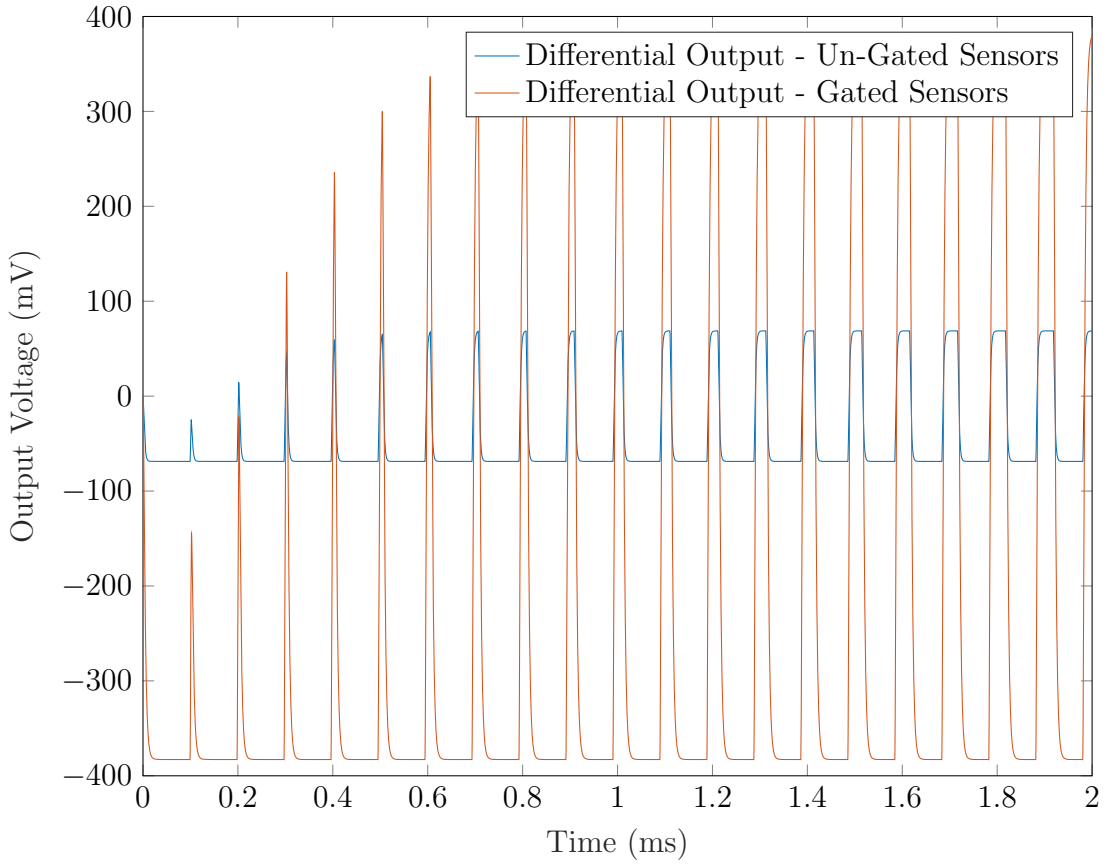


Figure 5.32: Output signals of the differential amplifier in the final integrated Hall effect system for un-gated sensor (blue trace) and sensors biased at the Dirac point (red trace).

PWM signal is simulated using a ±270 V bus voltage with the signal fed through an RL circuit to represent the flux concentrator that is to be placed around the bus bar in the physical system. Both input signals are used to develop a Hall sensor model for both unbiased sensors and sensors biased at the Dirac point based on a 0.70 mA input current bias and a 15 mT flux.

Amplification of output signals based on a two-stage approach is demonstrated with an initial unity-gain buffer amplifier and a secondary differential gain stage utilised. The source resistance selected for use with the buffer amplifier (30 kΩ) yields a gain slightly lower than unity ($\sim$ 0.90) however represents an output impedance reduced by over 6.0 times that of the input impedance. A passive load amplifier with a gain of 35 dB is demonstrated, showing to offer a significantly improved gain over that of active load configuration (1.5 dB) at the desired supply voltage. The design of a basic low pass filter is also described for removal of

unwanted noise present in the system. Finally, the overall integrated system is shown with an observed overall gain of 32 dB over the input signal representing an output of magnitude ±70 mV for un-gated Hall sensor systems and ±0.38 V when operated at the Dirac point.

Chapter 6

Conclusions

The use of graphene as a Hall effect sensor for current sensing in power electronics modules has been investigated. Firstly, the optimisation of device processing techniques to reduce surface contamination through the use of a Cu sacrificial layer is considered. Raman spectroscopy and AFM surface analysis techniques were employed to investigate the impact of varying lithographic processing methods on the graphene film quality. Devices were fabricated using no sacrificial layer (comparable to optical lithography processing for bulk semiconductor materials, Al sacrificial layer and Cu sacrificial layer. It was found that the use of a Cu sacrificial layer significantly reduces defect density over that of both no sacrificial and Al sacrificial layers with a reduction in surface doping of 60 % observed. Height profiles obtained from AFM imaging additionally observe a reduction in surface roughness from 16±0.60 nm and 17±0.40 nm for devices fabricated using no sacrificial layer and Al sacrificial layer respectively to 8.8±0.20 nm when using a Cu sacrificial layer.

Comparatively, surface analysis of as received graphene films prior to lithographic processing was also observed with surface roughness exhibiting 250 % increase when using Cu sacrificial layer suggesting that whilst this method improves the surface quality over comparative fabrication methods, residue is still introduced to the surface during processing. Defect density of Cu sacrificial layer devices was however found to be comparable to that of as received films albeit exhibiting a small increase from 0.03±0.002 to 0.07±0.004. Whilst it is evident that the

use of a Cu sacrificial layer offers improved surface quality over that of alternative lithographic processing methods it is clear that the graphene surface remains highly sensitive to external contamination and alternative methods may need to be utilised post processing in order to optimise device characteristics.

Electrical characterisation was employed on devices in order to compare the extracted transport properties and determine whether the use of a Cu sacrificial layer offers optimised characteristics. It is observed that devices fabricated using an Al sacrificial layer results in the weakest device electronic properties with current related sensitivities as low as 17.0±5.90 V/AT and carrier mobilities of $1.0\pm0.36\times10^3$ $cm^2V^{-1}s^{-1}$. Conversely when using a Cu sacrificial layer this is optimised with current related sensitivities as high as 165±16.5 V/AT observed, exceeding that of commercial bulk semiconducting devices and carrier mobilities as high as $2.1\pm0.23\times10^3$ $cm^2V^{-1}s^{-1}$. It is additionally noted that device yield is optimised to 82 % and the spread in device characteristics reduced to as low as 10 %. This variability is comparable to that observed in commercially processed devices and is an key parameter in the aerospace industry where reliability is critical.

Device characteristics were optimised further through external gate biasing to shift the Fermi level towards the charge neutrality point (Dirac point). Analysis of device behaviour around this point also allow for observations to be made as to the graphene film quality. It is determined that the use of a Cu sacrificial layer reduces hysteresis around the Dirac point, consolidating the results seen previously that this method offers higher quality graphene films with optimised device characteristics. The characteristics are extracted around the Dirac point, observed at a gate bias of 37±1.0 V, with current related sensitivity increased as high as 972±19.0 V/AT at this point which is comparable to that of CVD graphene and 2DEG Hall devices demonstrated in literature.

Testing of devices was employed under conditions representative to which the graphene devices are expected to operate. Firstly, characteristics of devices were extracted up to a temperature of 473 K. A non-linear, gaussian trend was observed with temperature attributed to evaporation of moisture trapped on the surface of

the graphene film during heating. External gate biasing is shown to reduce the effects of this non-linearity with the lowest value of thermal coefficient obtained at $V_G > V_{DIRAC}$. Thermal coefficient of current related sensitivity is found to be reduced to $0.50 \pm 0.025 \times 10^3$ ppm/K at this point, a marked improvement on both devices in literature and that of commercial devices. InSb devices typically exhibit a thermal coefficient in the region of 20×10^3 ppm/K and GaAs 3.0×10^3 ppm/K. Device characteristics at this point however still show signs of non-linear behaviour, this is found to be reduced when employing a vacuum anneal with thermal coefficient reduced to $0.27 \pm 0.014 \times 10^3$ ppm/K post anneal. It is concluded that for development of highly sensitive devices with low thermal coefficient an appropriate packaging solution is required to be developed to reduce moisture adsorption to the surface alongside external gate biasing for Dirac point operation.

AC characteristics of graphene devices up to 200 kHz are also demonstrated. Devices show stable output characteristics up to this point, exceeding that of the 120 kHz limit imposed on bulk semiconducting Hall sensors. The limitation observed in the graphene Hall sensors in this study is attributed to an inherent limitation with the test setup, namely the maximum operating frequency of the lock-in amplifier.

The graphene Hall sensors developed in Chapter 3 were modelled in LTSpice alongside SiC based JFETs originally developed at Newcastle University for simulation of a fully integrated Hall effect system. JFET characteristics were analysed for development of a representative LTSpice model with simulated results exhibiting a 9.0 % variation in characteristics over those extracted from devices. This is comparable to the variability in device characteristics seen across a wafer currently of 10 %. This JFET model is used to develop functional input and output circuitry namely an input current source and output amplification. Current biasing is developed in the form of a cascaded JFET current source, providing an input current bias of 0.70 mA. Amplification of the Hall effect signal is split into two stages; buffering to shift the signal from high impedance to low impedance and a differential gain stage in order to maximise the amplitude of the output signal. The final differential gain stage used is based on passive load configuration in order to observe the required supply voltage of 12 V, yielding a differential gain of

35 dB. These systems are integrated together alongside the Hall effect sensor and input inverter signal in order to produce simulated output characteristics of a full Hall effect system for un-gated Hall sensors and those biased at the Dirac point. This ultimately results in a final output signal of ±70 mV for un-gated sensors and ±0.38 V for those biased at the Dirac point.

The results demonstrated here show the potential for graphene Hall devices to be implemented in applications use of Hall effect sensing was previously precluded. The fabrication methods and subsequent optimisation of device characteristics show devices with significantly increased resolution and sensitivity over that of commercial Hall effect devices. High temperature characteristics up to 473 K additionally observe a thermal coefficient of $0.27 \pm 0.014 \times 10^3$ ppm/K allowing for deployment in harsher environment systems. The system modelling will allow for development of future integrated graphene and SiC Hall effect sensors with the fabrication work acting as a crucial stepping stone towards the realisation of reproducible, wafer scale fabrication of graphene based devices for real world applications.

6.1 Future Work

It is evident throughout this work that development of a suitable packaging solution is critical for implementation of devices to real world applications. There are several streams of work required for the realisation of such a solution. Firstly, development of a repeatable, damage free wire bonding process that will ultimately allow for devices to be implemented into packaging. This may involve the modification of the metal stack used for contacts potentially with a trade off as to optimal graphene-metal contact for device performance and that of suitability for adhesion during the bond process. Secondly, the development of an encapsulation layer to protect the surface of the graphene film from moisture adsorption and potential contamination.

Fabrication of devices on a SiC substrate will allow for analysis of characteristics at temperatures beyond those seen up to 473 K in this work, potentially push-

ing the operating limit up to 673 K and above. The development of a suitable packaging solution as described previously will also allow for analysis for thermal behaviour without the influence of moisture and contaminants adsorbed to the surface in order to determine if this results in a truly linear temperature dependance. Extension of AC characterisation of devices can also be obtained through optimisation of test setup to allow for measurement of device characteristics at frequencies > 200 kHz.

Finally, development of a thermal model for SiC based JFETs in order to investigate the influence additional circuitry will have on the overall system thermal drift and suitability for application in higher temperature environments. As well as the simulation of higher temperature systems, development and build of a fully integrated Hall effect system using both the graphene Hall effect sensors developed in this study and the SiC based JFETs for implementation into practical applications. This will allow for future testing of devices in both power electronics modules and could potentially be extended to positional and speed control of electrical machines.

Whilst these areas of work remain to be explored, it has been shown that graphene based devices offer great potential in overcoming the limitations seen in present day current sensing methods with highly sensitive devices capable of operating up to 473 K and 200 kHz presented.

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